Genesis HIGH SPEED

User Manual

English

Desktop and Rack Mount Tethered Data Acquisition System

GEN17tA

HBM

A04377_03_E00_00 HBK: UNRESTRICTED

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References made to the Perception software are for version 7.40 or higher

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Legal statement
This product uses GNU General Public Licensed (GPL) software, the source code is available at:
www.hbm.com/highspeed

For more information please refer to the following website:
www.gnu.org

This product includes software developed by the OpenSSL Project for use in the OpenSSL Toolkit.
www.openssl.org/

Table of Contents

1 About this manual

1.1 Symbols used in this manual

The following symbols are used throughout this manual to indicate warnings and cautions.

WARNING

Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.

WARNING

Indicates an electrical shock hazard which, if not avoided, could result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation which, if not avoided, could result in minor or moderate injury; or alerts against unsafe practices; or alerts against actions which could damage the product or result in a loss of data.

CAUTION

The ESD susceptibility symbol indicates that handling or use of an item may result in damage from ESD if proper precautions are not taken.

HINT/TIP

The info icon indicates sections which provide additional information about the product. This information is not essential for correct operation of the instrument, but provides knowledge to make better use of the instrument.

1.2 Manual conventions

When the wording “Click Start ...” is used, this refers to the Windows® Start button. Compared to Windows® XP, Windows® Vista, Windows® 7 and Windows® 10, the Start Menu has undergone some significant changes. The taskbar icon is no longer labeled "Start" and is now simply the pearl icon (of the window-frame in an orb).

For clarity and convenience, these conventions are used throughout this manual:

- **Menu names** from the display appear in bold, blue lettering.
- **Settings** within a menu appear in bold, red lettering.
- **Front panel controls** and **control names** appear in bold, black lettering.

2 Safety Messages

2.1 Introduction

IMPORTANT

Read this section before using this product!

This instrument is mains powered and protective ground connections are required (unless otherwise specified for certain parts).

This manual contains information and warnings that must be observed to keep the instrument safe. The instrument should not be used when environmental conditions exceed the instrument's specifications (e.g. damp, high humidity) or if the unit is damaged.

For the correct and safe use of this instrument, it is essential that both operating and service personnel follow generally accepted safety procedures in addition to the safety precautions specified in this manual.

Whenever it is likely that safety protection has been impaired, the instrument must be made inoperative and secured against any unintended operation. Qualified maintenance or repair personnel should be informed. Safety protection is likely to be impaired if, for example, the instrument shows visible damage or fails to operate normally.

Appropriate use
This instrument and the connected transducers may be used only for measurement and directly related control tasks. Any other use is not appropriate. To ensure safe operation, the instrument may only be used as specified in this user manual.

- The covers protect the user from live parts and should only be removed by suitably qualified personnel for maintenance and repair purposes.
- The instrument must not be operated with the covers removed.
- This instrument must not be used in life support roles.
- There are no user serviceable parts inside the instrument.

It is also essential to follow the respective legal and safety regulations for specific applications during use. The same applies to the use of accessories. Additional safety precautions must be taken in setups where malfunctions could cause major damage, loss of data or even personal injury.
Some examples of precautions are: mechanical interlocking, error signaling, limit value switches, etc.

Maintenance and cleaning
The instrument is a maintenance-free product. However, please note the following information about cleaning the housing:

- Before cleaning, disconnect the instrument completely.
- Clean the housing with a soft, slightly damp (not wet!) cloth. Never use solvents, since these could damage the housing or the labeling on the front panel.
- When cleaning, ensure that no liquid gets into the housing or connections.

General dangers, failing to follow the safety instructions
This instrument is a state-of-the-art device and as such is fail-safe. Using this instrument may be hazardous if it has been installed incorrectly and is operated by untrained personnel. Any person assigned to install, maintain or repair the unit or to put the unit into operation must have first read and understood the user manual, particularly the technical safety instructions.

Residual risks
This instrument's scope of supply and performance covers only a small area of measurement technology. In addition, equipment planners, installers and operators should plan, implement and respond to the safety engineering considerations of measurement technology in such a way as to minimize any residual risks. Prevailing regulations must be complied with at all times. The residual risks of the measurement technology must be referenced.

Conversions and modifications
Neither the design nor the safety features of this instrument may be modified without our express prior written agreement. Any modification shall exclude all liability on our part for any resultant damage. In particular, any repair or soldering work on cards (replacement of components) is prohibited. When exchanging complete units, use only original parts from HBM. The unit is delivered from the factory with a fixed hardware and/or software configuration. Changes should only be made within the possibilities documented in this manual.

Qualified personnel

People entrusted with the installation, fitting, operation of the instrument and putting the unit into service must have the appropriate qualifications. The instrument may only be installed and used by qualified personnel, in strict accordance with the specifications and the safety rules and regulations. This includes people who meet at least one of the three following qualification levels:

- Project personnel: Have a working knowledge of the safety concepts of automation and test and measurement technology.
- Automation plant or test and measurement operating personnel: Have been instructed on how to handle the equipment and are familiar with the operation of the cards and technologies described in this documentation.
- Commissioning engineers or service engineers: Have successfully completed the training on how to repair the automation systems. They are also authorized to activate, to ground and to label circuits and equipment in accordance with engineering safety standards. It is essential that the legal and safety requirements for the product and any accessories are complied with during use.

2.2 Grounding

The instrument must be used with a protective ground connection via the protective ground conductor of the supply cable. The protective ground conductor is connected to the instrument before the line and neutral connections are made when the supply connection is made. If the final connection to the supply is made elsewhere, ensure that the ground connection is made before line and neutral connections are made.

WARNING

Any interruption of the ground connection, inside or outside the instrument, is likely to make the instrument dangerous. Intentional interruption is prohibited.

For protection against electric shock, all external circuits or equipment need a safe insulation. Therefore, peripheral equipment must not be connected to the system with a power supply without the SELV (Separated Extra Low Voltage) rating unless explicitly mentioned.

Signal connections to the instrument should be connected after the ground connection is made and disconnected before the ground connection is removed, i.e. the supply lead must be connected whenever signal leads are connected.

WARNING

For safety, it is essential that the protective ground connector of the instrument is used whenever voltages greater than 33 V RMS, 46.7 V PEAK or 70 V DC (IEC 61010-1:2010) are connected. This is to prevent the instrument's case becoming live in the event of a protective ground interruption, which could occur if the supply connector is accidentally disconnected from the instrument.

The primary purpose of protective grounding is to provide adequate protection against electric shock that could cause death or injury to personnel while working on de-energized equipment. This is accomplished by grounding and bonding to limit the body contact or exposure to voltages at the work-site to a safe value if the equipment were to be accidentally energized from any source of hazardous energy. The greatest source of hazardous energy in most cases is direct energizing of the equipment from a power-system or source.

WARNING

If connection to a protective ground is not possible for any reason, then please refer to the international safety standard EN 50191:2000

2.2.1 Mains power cord

WARNING

Do not use the equipment with damaged cords and/or cables. Replace a damaged cord and/or cable immediately.

2.3 Instrument symbols

A variety of symbols can be found in the system. Below is a list of symbols and their meaning.

This symbol is used to denote the measurement ground connection. This point is not a protective ground connection.

This symbol is used to denote a protective ground connection.

This symbol is used to denote a frame or chassis ground connection. This point is not a protective ground connection.

Where caution is required, this symbol refers to the user manual for further information.

This symbol warns that high voltages are present close to this symbol.

This symbol shows that the switch is a power switch. When pressed, the instrument state toggles between the operating and power-off mode. When the system is in power-off mode, all electronics are disconnected from the power, except for a small circuit used to detect the switch state.

2.4 Protection and isolation

2.4.1 Measurement categories

- The international standards for test equipment safety are IEC 61010-1 and the IEC 61010-2-030.
- IEC 61010-1 defines three overvoltage categories (CAT II, CAT III, and CAT IV) for the power supply of an instrument.
- IEC 61010-2-030 defines three measurement categories (CAT II, CAT III, and CAT IV) for an instrument's input measurements which can be directly connected to mains supply.
- All measurement inputs which are not specified to be connected to the mains power have no CAT rating and are referred to as O (like Others).

Categories in accordance with IEC 61010-2-030:2010
Electrical equipment, specifically measurement tools, can be assigned into four categories in accordance with IEC 61010-2-030:2010. These measurement categories are indicated by the terms O (previously CAT I), CAT II, CAT III and CAT IV. Originally, these categories were used to indicate the overvoltage or surge voltage that was likely to occur and could be sustained by the equipment. Currently, the category indicates the amount of energy that can be released if a short circuit occurs. A higher category number indicates a higher energy level that can occur and can be sustained by the equipment.

O (Other) (previously referred to as **CAT I**): This category is for measurements not directly connected to a mains supply. Measurements for this category are signal levels, regulated low voltage circuits or protected secondary circuits. For this category, there are no defined standard overvoltage or surge impulse levels.

CAT II: This category is for measurements directly connected to a low voltage mains supply. Measurements for this category are mains sockets in household applications or portable tools. This category expects a minimum of three levels of overcurrent protection between the transformer and connection point of the measurement. (See Figure 2.1).

CAT III: This category is for measurements directly connected to the distribution part of a low voltage mains installation. Measurements for this category are circuit breakers, wiring, junction boxes, etc. This category expects a minimum of two levels of overcurrent protection between the transformer and connection point of the measurement. (See Figure 2.1).

CAT IV: This category is for measurements directly connected to the source of a low voltage mains installation. Measurements for this category are overcurrent protection devices, ripple control units, etc. This category expects that there is a minimum of one level of overcurrent protection between the transformer and connection point of the measurement circuit. (See Figure 2.1).

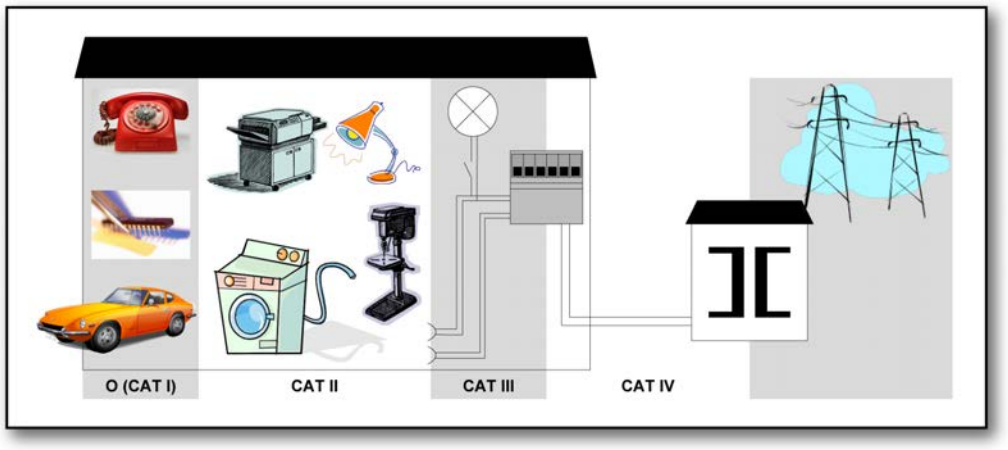


Figure 2.1: Category indication in accordance with IEC 61010-2-030:2010

Example: A measurement device is specified as 600 V CAT II, maximum input voltage 1000 V DC.

Table 2.1: Insulation test voltages in accordance with IEC 61010-2-030:2010

Nominal Voltage (V RMS or V DC)	IEC 61010-2-030:2010					
	5 sec. AC test (V RMS)			Impulse test (V)		
	CAT II	CAT III	CAT IV	CAT II	CAT III	CAT IV
≤ 150	840	1390	2210	1550	2500	4000
> 150 ≤ 300	1390	2210	3310	2500	4000	6000
> 300 ≤ 600	2210	3310	4260	4000	6000	8000
> 600 ≤ 1 000	3310	4260	6600	6000	8000	12000

Using the table above, it can be concluded that this specification informs the user that the device passed the insulation tests; 5 sec at 2210 V RMS and impulse 4000 V. The maximum operating input voltage is 1000 V DC. This device is to be used to measure CAT II circuitry up to 600 V.

WARNING

Measurement inputs of this instrument should not be used to measure high-energy signals of measurement categories CAT II, CAT III or CAT IV (IEC 61010-2-030:2010) (e.g. mains measurements) , unless specifically stated for the specific input.

2.4.2 Basic insulation versus reinforced

For reference, the basic insulation and supplementary insulation and the reinforced insulation test values for CAT II can be found below.

Table 2.2: Test voltages for the testing electric strength of solid insulation in measuring circuits in measurement category II (IEC 61010-2-030:2010)

Nominal voltage line to neutral AC RMS or DC of MAINS being measured. [V]	Test voltage			
	5 s AC test [V RMS]		Impulse test [V peak]	
	Basic insulation and supplementary insulation	Reinforced insulation	Basic insulation and supplementary insulation	Reinforced insulation
≤ 150	840	1390	1550	2500
> 150 ≤ 300	1390	2210	2500	4000
> 300 ≤ 600	2210	3510	4000	6400
> 600 ≤ 1000	3310	5400	6000	9600

Several means of protection can be used to protect a user from hazardous voltages. As can be seen below, basic insulation and supplementary insulation is one mean of protection, but reinforced insulation is also a means of protection.
The test voltages are different for each mean of protection, as can be found in the table above.

Additional means of protection for single fault conditions
Accessible parts shall be prevented from becoming HAZARDOUS LIVE IN SINGLE FAULT CONDITION. The primary means of protection (see Figure 2.2) shall be supplemented by one of **A**, **B**, **C** or **D**. Alternatively, one of the single means of protection **E** or **F** shall be used. See Figure 2.2.

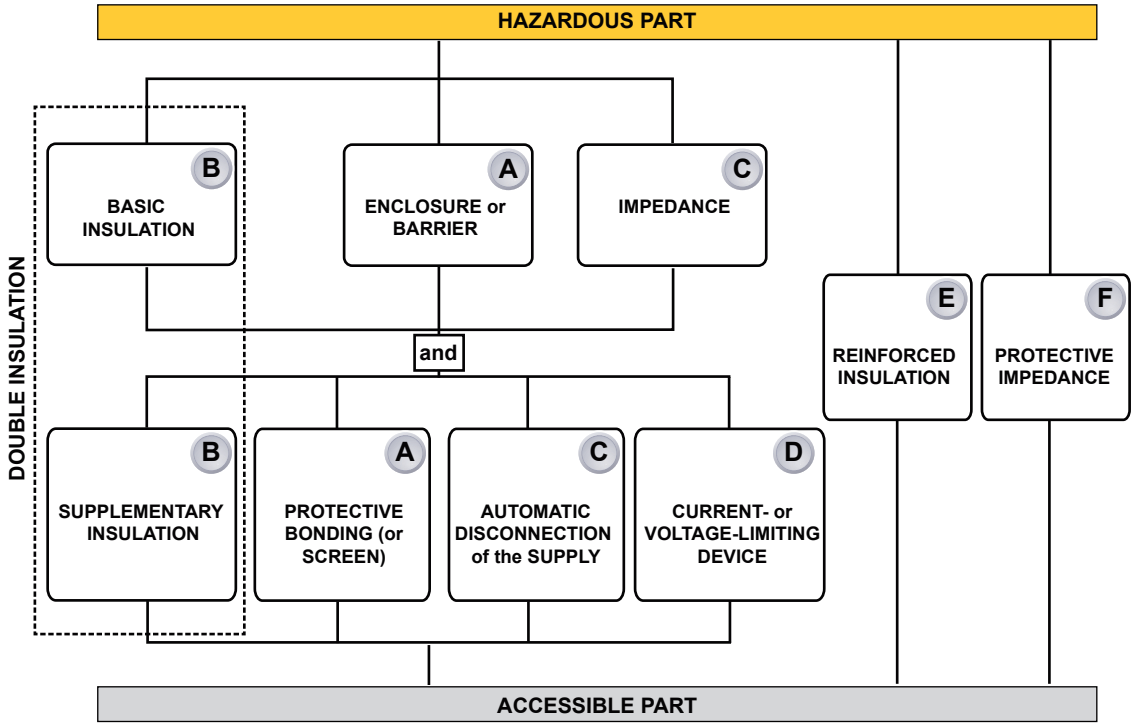


Figure 2.2: Acceptable arrangement of protective means against electric shock

Example: A measurement device is specified as 600 V CAT II reinforced insulation, with a maximum input voltage 1000 V DC.
Using the information above, it can be concluded that this specification informs the user that the measurement device is tested on input to chassis ground for five seconds at 3510 V RMS and impulse 6400 V. The maximum operating input voltage is 1000 V DC. This device is to be used to measure CAT II circuitry up to 600 V.

2.4.3 Protection

WARNING

ELECTRICAL SHOCK HAZARD!
Any interruption of the protective conductor inside or outside the apparatus is likely to make the apparatus dangerous. Intentional interruption is prohibited.
When the apparatus is connected to its supply, terminals may be live, and the opening of covers for removal of parts is likely to expose live parts.

Whenever it is likely that the protection has been impaired, the apparatus must be made inoperative and be secured against any unintended operation.

The protection is likely to be impaired if, for example, the apparatus shows visible damage or has been subjected to severe transport stresses.

It is the responsibility of the user to ensure the safety of any accessories used with the equipment, such as probes.

Proper use of this device depends on careful reading of all instructions and labels.

If the instrument is used in a manner not specified by HBM, the protection provided by the instrument can be impaired.

WARNING

This instrument must not be operated in explosive atmospheres.

WARNING

This instrument and related accessories are not designed for biomedical experimentation on humans or animals and should not be directly connected to human or animal subjects or used for patient monitoring.

2.4.4 Overvoltage/current protection

All signal inputs are protected against overloads and transients. Exceeding the limits stated in the specifications, particularly when connected to potentially high-energy sources, can cause severe damage that is not covered by the manufacturer's warranty.

WARNING

Do not remove covers. Refer to qualified individuals for servicing.

The covers protect the user from live parts and should only be removed by suitably qualified personnel for maintenance and repair purposes.

The instrument must not be operated with the covers removed.

There are no user serviceable parts inside.

2.4.5 Isolation

CAUTION

For input channels with plastic BNCs (galvanically isolated from the chassis), the input conductors including the BNC shell may carry hazardous voltages. Only appropriate insulated BNC connectors should be used.

It is the responsibility of the user to ensure the safety of any accessories used with the instrument, such as probes.

CAUTION

Even low voltage inputs may contain high voltage fast transients (spikes), which could damage the input. For this reason it is not safe, for instance, to make direct connections to an AC line supply, unless specifically stated otherwise for the specific input.

2.5 Environment

The instrument should be operated in a clean, dry environment with an ambient temperature as specified in the data sheets.

The instrument is specified for use in a Pollution Degree II environment, which is normally non-conductive with temporary light condensation, but it must not be operated while condensation is present. It should not be used in more hostile, dusty or wet conditions, as specified in the Pollution Degree II environment.

Humidity should be between 0% and 80%. When moving the device from a cold to a warm environment, the device has to be left off for a period of 30 minutes to avoid short circuits as a result of condensation.

Note *Direct sunlight, radiators and other heat sources should be taken into account when assessing the ambient temperature.*

If the instrument has a fan installed, leave space around the equipment for unrestricted ventilation.

Do not store the equipment in hot areas. High temperatures can shorten the life of electronic devices and damage batteries.

Do not store the equipment in cold areas. Before the equipment warms up to its normal operating temperature, moisture can form inside the equipment, which may damage the equipment's electronic circuits.

Do not drop, knock or shake the equipment. Rough handling can break internal electronics and/or PCBs.

Do not use harsh chemicals, cleaning solvents or strong detergents to clean the instrument. To clean the instrument, disconnect all power sources and clean the housing with a soft, slightly damped (not wet!) cloth.

It is the responsibility of the user to ensure the safety of any accessories used with the instrument, such as probes.

2.6 Laser Safety

Some of the GEN series cards or systems use lasers. All laser products used are classified as a **Class 1 laser product**. The lasers do not emit hazardous light but it is recommended to avoid direct exposure to the beam.

WARNING

Intrabeam viewing of the laser product may produce dazzling visual effects, particularly in low ambient light. Lasers of any wavelength with sufficient output power can cause injury.

The built-in laser complies with laser product standards set by government agencies for Class 1 laser products:

The GEN series products are certified as Class 1 Laser Products and comply with US FDA regulations. These are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950. The devices are for use only under the specifications and ratings specified in the manual and data sheets.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

2.7 Manual handling of loads

The Manual Handling of Loads Directive 90/269/EEC from the European Community lays down the minimum health and safety requirements for the manual handling of loads where there is a risk particularly of back injury to workers.

CAUTION

The weight of the instrument may exceed 17.5 kg when fully loaded. Please take appropriate actions before lifting the instrument.

Before lifting or carrying a heavy object, the following questions should be asked:

- Can one person lift this load safely, or do two people need to lift the load?
- How far will the load have to be carried?
- Is the path clear of clutter, cords, slippery areas, overhangs, stairs, curbs or uneven surfaces?
- Will closed doors that need to be opened be encountered?
- Once the load is lifted, will it block the carrier's view?
- Can the load be broken down into smaller parts?
- Should the carrier wear gloves to get a better grip and to protect hands?

Contact the "Occupational Health and Safety" organization, or equivalent, in your country for more information.

The GEN17tA weighs approximately 35.9 kg with 17 acquisition cards plugged in (18.9 kg without acquisition cards)

2.8 International safety warnings

Dansk

SIKKERHEDSADVARSEL
Dette instrument skal anvendes med en sikkerhedsjordforbindelse, som er tilsluttet via lysnetkablets beskyttelsesjordledning eller via en sikkerhedsjordklemme, hvis instrumentet er forsynet hermed. Hvis sikkerhedsjordforbindelsen afbrydes, inden i eller uden for instrumentet, kan instrumentet udgøre en farekilde. Sikkerhedsjordforbindelsen må ikke afbrydes. Der skal desuden tilsluttet en signaljordforbindelse, hvis et indgangssignal overstiger 33 V RMS, 46,7 V PEAK eller 70 V DC (IEC 61010-1:2010).

Dækslerne må ikke fjernes.

Afbryd dette instrument eller dets strømforsyning fra lysnettet ved at fjerne IEC-stikket. Instrumentets vekselstrømsafbryder er kun beregnet til funktionelle formål. Den er ikke beregnet eller egnet til at afbryde instrumentet fra lysnettet.

Hvis målingerne et omfattet af EN 50110-1 og EN 50110-2, skal alle kort med en driftsspænding på mere end 50 V AC RMS eller 120 V DC tilsluttes af en kvalificeret tekniker eller en elektriker, og arbejdet skal kontrolleres af en kvalificeret tekniker. (En kvalificeret tekniker er en person, som i kraft af sin specialuddannelse, sin viden og erfaring samt sit kendskab til relevante bestemmelser kan vurdere omfanget af det arbejde, de skal udføre, og afdække de potentielle risici, og som er blevet udpeget som kvalificeret tekniker af deres arbejdsgiver).

Nederlands

VEILIGHEIDSWAARSCHUWING
Dit instrument mag uitsluitend worden gebruikt als een beschermde massa (aarde) is aangesloten via de beschermde massageleider van de voedingskabel, of indien het instrument daarvan is voorzien via de veiligheids-massa-aansluiting. Als de beschermde massa, binnen of buiten het instrument, wordt onderbroken, dan kan dat hierdoor uitermate gevaarlijk worden. Het opzettelijk onderbreken van de massa is verboden. Indien er een signaal wordt aangeboden van meer dan 33 V RMS, 46.7 Vpeak of 70 V DC (IEC 61010-1:2010) dient eveneens een signaalaarding aangesloten te zijn.

De deksels mogen nooit worden verwijderd.

Om dit instrument los te koppelen of van het stroom af te halen, dient de IEC-aansluiting er uit te worden getrokken. De wisselstroom-voedingsschakelaar op dit instrument is uitsluitend bestemd voor functionele doeleinden. Het is niet bedoeld of geschikt als een ontkoppelingsapparaat.

Voor metingen die binnen de EN 50110-1 en EN 50110-2 vallen: let op dat alle panelen met bedrijfsspanningen van meer dan 50 V AC RMS of 120 V DC alleen door een gekwalificeerde technicus mogen worden aangesloten of door een persoon die is opgeleid in de elektrotechniek en onder toezicht van een gekwalificeerde technicus staat. (Gekwalificeerde technici zijn personen, die op basis van hun specialistische opleiding, kennis en ervaring als ook hun kennis van de betreffende voorzieningen, in staat zijn om het werk dat aan hen is toevertrouwd te beoordelen en mogelijke gevaren te ontdekken en door hun werkgever zijn aangewezen als gekwalificeerde technici.)

Suomi

TURVAOHJEITA

Tätä laitetta käytettäessä sen tulee olla suojamaadoitettu joko verkkojohdon suojajohtimen tai erillisen suojamaadoitusliitännän kautta, mikäli laitteeseen on sellainen asennettu. Suojamaadoituksen katkaiseminen laitteen sisä- tai ulkopuolelta tekevät siitä vaarallisen. Tahallinen katkaisu on kiellettyä. Lisäksi signaalimaa on oltava kytkettynä, jos jokin tulosignaali ylittää tehollisarvon 33 V, huippuarvon 46,7 V tai 70 V DC (IEC 61010-1:2010).

Älä poista suojakansia.

Katkaise laitteen tai sen virtalähteen käyttöjännite irrottamalla IEC-liitin. Laitteen verkkokytkimellä on ainoastaan toiminnallinen tarkoitus. Sitä ei ole tarkoitettu, eikä se sovellu laitteen erottamiseen käyttöjännitteestä.

Mittauksissa, jotka kuuluvat EN 50110-1- ja EN 50110-2-standardien soveltamisalaan, huomaa, että kortit, jotka toimivat tehollisarvojännitteellä yli 50 V AC tai 120 V DC, saa kytkeä vain pätevä asentaja tai sähköteknisen koulutuksen saanut henkilö pätevän asentajan valvonnassa. (Pätevät asentajat ovat henkilöitä, jotka erikoiskoulutuksensa, tietojensa ja kokemuksensa sekä asiaan kuuluvien määräysten tuntemuksensa ansiosta pystyvät arvioimaan heille annettuja töitä ja havaitsemaan mahdolliset vaarat ja jotka heidän työnantajansa on nimennyt ammattitaitoisiksi asentajiksi).

Français

ATTENTION - DANGER!
Lorsqu'il est en fonctionnement, cet instrument doit impérativement être mis à la masse par le conducteur de terre du câble d'alimentation ou, si l'instrument en comporte une, par la borne de terre. Il peut être dangereux en cas de coupure du circuit de terre, que ce soit à l'intérieur ou à l'extérieur de l'instrument. Il est formellement interdit de couper intentionnellement le circuit de terre. De plus, une masse signal doit être connectée si l'un des signaux d'entrée, quel qu'il soit, dépasse 33 V RMS (valeur efficace), 46,7 V PEAK (valeur de crête) ou 70 V DC (courant continu) (CEI 61010-1:2010).

Ne pas déposer les panneaux de protection.

Pour déconnecter cet instrument ou son alimentation de l'alimentation secteur, débrancher le cordon d'alimentation (CEI). L'interrupteur d'alimentation secteur sur cet instrument est purement fonctionnel. Il ne s'agit pas d'un dispositif de coupure du courant, et n'est pas conçu pour cette fonction.

Pour les mesures entrant dans le champ d'application des normes EN 50110-1 et EN 50110-2, veuillez noter que tous les panneaux avec des tensions de service supérieures à 50 V AC RMS (tension efficace) ou 120 V DC (courant continu) ne peuvent être connectés que par un technicien qualifié ou une personne formée en ingénierie électrique et supervisée par un technicien qualifié. (Les techniciens qualifiés sont des personnes qui, du fait de leur formation, leurs connaissances et leur expérience spécialisées ainsi que leur connaissance des dispositions réglementaires appropriées, sont capables d'évaluer le travail qui leur est confié et détecter les risques possibles, et qui ont été désignées comme techniciens qualifiés par leur employeur).

Deutsch

WARNHINWEIS!
Dieses Gerät muss mit einer Schutzerde betrieben werden, die über den Schutzleiter des Speisekabels oder über die Erdungsklemme des Gerätes (falls vorhanden) anzuschließen ist. Bei einer Unterbrechung der Schutzerde außerhalb oder innerhalb des Gerätes kann eine Gefahr am Gerät entstehen. Eine beabsichtigte Unterbrechung ist nicht zulässig. Achtung! Bei Signalspannungen über 33 V Effektivwert, 46,7 V Spitzenwert oder 70 V Gleichspannung (IEC 61010-1:2010) muss die Signalmasse angeschlossen sein.

Die Schutzabdeckungen nicht entfernen.

Zum Trennen des Gerätes oder seiner Spannungsversorgung von der Wechselstromversorgung den IEC-Stecker abziehen. Der Wechselstromversorgungs-Schalter dient bei diesem Gerät nur für Funktionszwecke. Er ist nicht als Trennvorrichtung bestimmt bzw. geeignet.

Für Messungen gemäß EN 50110-1 und EN 50110-2 bitte berücksichtigen, dass alle Platinen mit Betriebsspannungen über 50 V AC RMS oder 120 V DC nur durch einen qualifizierten Elektriker oder einer elektrotechnisch unterwiesenen Person unter Aufsicht eines qualifizierten Technikers durchgeführt werden dürfen. (Qualifizierte Techniker sind aufgrund ihrer fachlichen Ausbildung, Kenntnisse und Erfahrungen sowie Kenntnis der einschlägigen Bestimmungen in der Lage, die ihnen anvertrauten Arbeiten zu beurteilen und mögliche Risiken zu erkennen, sowie Personen, die durch ihren Arbeitgeber zu qualifizierten Technikern ernannt worden sind).

Italiano

AVVISO DI SICUREZZA
Questo strumento deve esser utilizzato con un collegamento protettivo di messa a terra tramite il filo di messa a terra del cavo di alimentazione o tramite il terminale di messa a terra in sicurezza, nel caso in cui lo strumento ne sia dotato. Qualsiasi interruzione della messa a terra di protezione, sia all'interno che all'esterno dello strumento, lo renderà pericoloso. È vietata qualsiasi interruzione causata intenzionalmente. Inoltre, la connessione di terra deve essere collegata se ad uno qualsiasi degli ingressi viene applicato un segnale superiore a 33 V RMS, 46,7 V di picco o 70 V c.c. (IEC 61010-1:2010).

Non rimuovere le coperture.

Per disinnestare questo strumento o l'alimentazione dalla corrente alternata, scollegare il connettore IEC. L'interruttore dell'alimentazione a corrente alternata di questo strumento viene fornito esclusivamente per scopi operativi e non viene inteso, né è adatto, per essere utilizzato come dispositivo di disinnesto.

Si noti che per le misurazioni che rientrano nell'ambito di applicazione delle norme EN 50110-1 ed EN 50110-2, tutte le schede con tensioni di esercizio superiori a 50 V c.a. RMS o 120 V c.c. possono essere collegate esclusivamente da un tecnico qualificato o da una persona in possesso di una formazione specifica nel campo dell'ingegneria elettrica sotto la supervisione di un tecnico qualificato. (Per tecnico qualificato si intende una persona che, in virtù della propria formazione , preparazione ed esperienza specialistica, nonché conoscenza delle disposizioni di settore, è in grado di valutare il lavoro che gli viene assegnato e di individuare possibili rischi, oltre ad essere stato nominato tecnico qualificato dal proprio datore di lavoro).

Norsk

ADVARSEL!
Dette instrument må betjenes med beskyttelsesjord tilkoblet via beskyttelsesjordlederen til tilførselskabelen eller via beskyttelsesjordklemmen, hvis instrumentet er utstyrt med en slik. Ethvert brudd i beskyttelsesjorden inni eller utenpå instrumentet kan føre til at instrumentet blir farlig. Tiltenkt brudd er tillatt. I tillegg må en signaljord tilkobles hvis et inngangssignal overskrider 33 V RMS, 46,7 V PEAK eller 70 V DC (IEC 61010-1:2010).

Ikke fjern dekslene.

For å koble dette instrumentet eller dets strømforsyning fra AC-tilførselen, trekker du ut IEC-kontakten. AC-tilførselsbryteren på dette instrumentet er kun for funksjonelle formål. Den er ikke beregnet for, eller egnet til frakoblingsenhet.

For målinger som faller innenfor EN 50110-1 og EN 50110-2 må man være oppmerksom på at alle kort med arbeidsspenninger over 50 V AC RMS eller 120 V DC kun kan kobles til av en kvalifisert tekniker eller elektriker og overvåket av en kvalifisert tekniker. (Kvalifiserte teknikere er personer som på grunn av sin spesialistopplæring, kunnskap og erfaring, samt sin kunnskap om relevante bestemmelser, er i stand til å gå inn i arbeidet som de har fått i oppdrag å utføre og detektere mulige farer, og som er blitt utnevnt som kvalifiserte teknikere av sin arbeidsgiver.

Português

AVISO DE SEGURANÇA
Este instrumento deve funcionar com uma terra de proteção conectada através do condutor da terra de proteção do cabo de alimentação ou, caso o instrumento esteja equipado com um, através do terminal da terra de proteção. Qualquer interrupção da terra de proteção, no interior ou no exterior do instrumento, poderá tornar o instrumento perigoso. A interrupção intencional é proibida. Além disso, deve ser conectado um sinal de terra se qualquer sinal de entrada exceder 33 V RMS, 46,7 V PICO ou 70 V CC (IEC 61010-1:2010).

Não retirar as tampas.

Para desconectar este instrumento ou a respetiva fonte de alimentação da alimentação CA, retire o conector IEC da ficha. Neste instrumento, o interruptor de alimentação CA é fornecido apenas para fins funcionais. Não se destina a, nem é adequado para, ser utilizado como dispositivo de desconexão.

Para medições abrangidas pelas normas EN 50110-1 e EN 50110-2, tenha em atenção que todos os quadros com tensões de funcionamento superiores a 50 V CA RMS ou 120 V CC apenas poderão ser conectados por um técnico qualificado ou por alguém com formação em engenharia elétrica e supervisionados por um técnico qualificado. (Técnicos qualificados são pessoas que, devido à sua formação especializada, ao conhecimento e à experiência, bem como ao seu conhecimento das disposições relevantes, são capazes de avaliar o trabalho que lhes é confiado e detetar possíveis riscos e são pessoas que foram nomeadas técnicos qualificados pelo seu empregador.)

Português (Brasil)

AVISO DE SEGURANÇA
Este instrumento deve ser operado com um terra de proteção conectado por meio do condutor do terra de proteção do cabo de alimentação ou, se o instrumento estiver equipado com um, por meio do terminal de aterramento de segurança. Qualquer interrupção do terra de proteção, no interior ou no exterior do instrumento, poderá tornar o instrumento perigoso. A interrupção intencional é proibida. Além disso, deve ser conectado um sinal de terra se qualquer sinal de entrada exceder um máximo de 33 V RMS, 46,7 V PICO ou 70 V CC (IEC 61010-1:2010).

Não retirar as tampas.

Para desconectar este instrumento ou a fonte de alimentação dele da alimentação CA, desconecte o conector IEC. Neste instrumento, o interruptor de alimentação CA é fornecido somente para fins funcionais. Não se destina a, nem é adequado para, ser usado como dispositivo de desconexão.

Para medições no escopo das normas EN 50110-1 e EN 50110-2, note que todos os quadros com tensões de funcionamento superiores a 50 V CA RMS ou 120 V CC poderão somente ser conectados por um técnico qualificado ou por alguém com formação em engenharia elétrica e supervisionados por um técnico qualificado. (Os técnicos qualificados são pessoas que, devido à sua formação acadêmica, conhecimento e experiência, bem como ao seu conhecimento das provisões relevantes, são capazes de avaliar o trabalho que lhes é confiado e detectar possíveis riscos e são pessoas que foram nomeadas técnicos qualificados por seu empregador.)

Español

ADVERTENCIA SOBRE SEGURIDAD
Este instrumento debe utilizarse conectado a tierra a través del conductor de puesta a tierra del cable de alimentación o de la borna de seguridad, si dicho instrumento estuviera equipado con ella. Cualquier interrupción de esta puesta a tierra, dentro o fuera del instrumento, hará que el manejo del mismo resulte peligroso. Queda terminantemente prohibido dejar en circuito abierto dicha puesta a tierra. Además, debe conectarse una señal de tierra si cualquier señal de entrada sobrepasa los 33 V eficaces, los 46,7 V de PICO o los 70 V de CC (IEC 61010-1:2010).

No quite las tapas.

Para desconectar este instrumento o su fuente de alimentación de la CA, desenchufe el conector IEC. El interruptor de entrada de CA (encendido) se incluye solo para fines funcionales. No está pensado para utilizarse como medio de desconexión, ni tampoco es adecuado para ello.

En cuanto a las mediciones que se clasifiquen bajo el alcance de las normas EN 50110-1 y EN 50110-2, tenga en cuenta que los cuadros con tensión de funcionamiento por encima de los 50 V de CA eficaces o los 120 V de CC solo puede conectarlos un técnico cualificado o una persona con formación en ingeniería eléctrica y supervisada por un técnico cualificado. (Los técnicos cualificados son personas que, debido a su formación especializada, conocimientos y experiencia, así como por su conocimiento de los suministros pertinentes, son capaces de evaluar el trabajo encomendado y detectar posibles riesgos, al igual que personas nombradas como técnicos cualificados por la empresa contratadora).

Svenska

SÄKERHETSVARNING
Detta instrument måste användas med jordad anslutning via strömkabelns ledare eller, om sådan finns, via en isolerad jordterminal. Avbrott i den isolerande jordningen inuti eller utanför strömgivaren kan göra strömgivaren farlig. Avsiktligt avbrott är förbjudet. Dessutom måste en signaljordning anslutas om någon ingångssignal överskrider 33 V RMS, 46.7 V PEAK eller 70 V DC (IEC 61010-1:2010).

Ta inte bort skydden.

Dra ut IEC-kontakten för att koppla loss instrumentet eller dess strömkälla från strömförsörjningen. Brytaren för växelströmförsörjningen på detta instrument är endast avsedd för funktionella syften. Den är inte avsedd eller lämplig som frånkopplingsenhet.

För mått inom intervallen som anges i EN 50110-1 och EN 50110-2, observera att alla kort med arbetsspänning över 50 V AC RMS eller 120 V DC kan endast anslutas av en kvalificerad tekniker eller en person som är utbildad i elteknik och övervakas av en kvalificerad tekniker. (Kvalificerade tekniker är personer som på grund av sin specialistutbildning, kunskap och erfarenhet liksom sin kunskap om relevanta enheter kan utvärdera arbetet som tilldelas dem och göra kvalificerade riskbedömningar samt utses av sina arbetsgivare till kvalificerade tekniker).

English

SAFETY WARNING

This instrument must be operated with a protective ground (earth) connection via the protective ground conductor of the supply cable or, if the instrument is fitted with one, via the protective ground terminal. Any interruption of the protective ground, inside or outside the instrument, is likely to make the instrument dangerous. Intentional interruption is prohibited. In addition, a signal ground must be connected if any input signal exceeds 33 V RMS, 46.7 V PEAK or 70 V DC (IEC 61010-1:2010).

Do not remove the covers.

To disconnect this instrument or its power-supply from the AC supply, unplug the IEC connector. The AC supply switch on this instrument is provided for functional purposes only. It is not intended, or suitable, as a disconnecting device.

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that all cards with working voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience as well as their knowledge of the relevant provisions are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

日本語

安全上の警告
本機器の操作は、電源ケーブルの保護接地線で接地（アース）を施した上で行ってください。また、安全接地用端子が存在する場合は、これを経由して本機器を接地してください。機器の内部または外部にある保護接地線が遮断されると、機器が危険な状態に陥る可能性があります。故意に保護接地線を遮断することを禁止します。また、入力信号が33 V RMS、ピーク時に46.7 V RMS、または70V DCを超える場合は、信号接地線を接続してください（IEC 61010-1:2010）。

カバーを外さないでください。

本機器またはその電源供給をAC電源供給から遮断するには、IECコネクターを抜きます。本機器のAC電源スイッチは、機能上の目的のためだけに提供しています。したがって、機器の主電源遮断用として意図されていないか、適応していません。

EN 50110-1とEN 50110-2の適用範囲に該当する測定を行う際、使用電圧が50 V AC RMSまたは120 V DCを超えるすべての基板の接続作業は、適正な資格を持つ技術者が、または電気工学の訓練を受けた者が適正な資格を持つ技術者の監督の下、行わなければなりませんのでご注意ください。(適正な資格を有する技術者とは、専門技術者に向けた訓練を受け、知識と経験を有し、該当する規定についても熟知しているため、委託された作業の内容を評価し、存在する可能性のあるリスクを特定することができ、雇用主により適正な資格を有する技術者として任命されている者を指します。)

中文

安全警告

该仪器必须通过电源电缆的保护接地线连接到保护接地（接地），如果该仪器已配备了安全接地端子，则通过该端子接地。断开仪器内外的任何保护接地可能使设备存在危险。严禁有意断开。此外，若任何输入信号高于 33 V RMS, 46.7 V 峰或 70 V DC，则必须将信号接地 (IEC 61010-1:2010)。

不要取下保护盖。

要将此设备或其电源断开交流电源，请拔下 IEC 接头。仪器上的交流电源开关仅用于功能性目的。而不是用于或适用于断开设备。

对于 EN 50110-1 和 EN 50110-2 中的测量，请注意：所有工作电压高于 50 V AC RMS 或 120 V DC 的板卡只能由合格的技术人员或在由受过电气工程培训的人员在合格技术人员的监督下进行连接。（合格技术人员指的是其专业培训、知识和经验以及相关规定的指示能够胜任委托给他们的工作并能检查出可能风险的人，这些人会被其雇主指定为合格技术人员)。

РУССКИЙ

ПРЕДУПРЕЖДЕНИЕ
Для эксплуатации данного прибора необходимо использовать защитное заземление, подключенное через проводник заземления кабеля питания или через терминал защитного заземления, если прибор оснащен таковым. В случае прерывания защитного заземления (внутри или снаружи прибора) прибор может стать травмоопасным. Преднамеренное прерывание заземления запрещено. Кроме того, необходимо подключить сигнальное заземление, если напряжение входного сигнала превышает 33 В среднеквадр. знач., 46,7 В пиков. знач. или 70 В пост. тока (IEC 61010-1:2010).

Не демонтируйте крышки.

Для отключения данного прибора или его блока питания от сети переменного тока отсоедините разъем IEC. Переключатель питания переменного тока данного прибора предусмотрен только для функциональных целей и не должен использоваться в качестве устройства отключения.

Для проведения измерений в соответствии со стандартами EN 50110-1 и EN 50110-2 следует учесть, что подключение всех плат, рабочее напряжение которых превышает 50 В перемен. тока среднеквадр. знач. или 120 В пост. тока, может выполнять только квалифицированный технический персонал или сотрудники, прошедшие курс обучения по электротехнике, под наблюдением квалифицированного персонала. (Квалифицированным техническим персоналом считаются сотрудники, которые после специальной подготовки, получения требуемых знаний и опыта, а также знакомые с основными процедурами, способны оценить доверенную им работу, определив возможные риски. При этом назначение на должность квалифицированного технического работника осуществляет работодатель.)

안전 경고

안전 경고
본 장비는 반드시 보안용 접지(접지)가 전원 공급 장치 케이블의 보안용 접지 도체를 통해 연결된 상태에서 작동해야 하며, 접지가 장착된 경우에는 보안용 접지 터미널을 통해 작동해야 합니다. 장비 내부 혹은 외부적으로 접지 방해 요인이 있는 경우 사용자에게 위험할 수 있습니다. 고의적인 방해는 금지됩니다. 또한, 입력 신호가 **33 V RMS, 46.7 V** 피크 또는 **70 V DC (IEC 61010-1:2010)**를 초과하는 경우 신호 접지를 연결해야 합니다.

덮개를 제거하지 마십시오.

AC 공급 전원으로부터 이 기기 또는 전원 공급 장치를 분리하려면 **IEC** 커넥터를 뽑으십시오. 본 장비의 **AC** 전원 공급 스위치를 장비 작동 외에 다른 용도로 사용하지 마십시오. 본 스위치는 단절 용도로 설계되지 않았으며, 이에 적합하지도 않습니다.

EN 50110-1 및 **EN 50110-2** 범위에 속한 측정값의 경우, **50 V AC RMS** 또는 **120 V DC** 를 초과하는 작동 전압의 모든 보드는 검증된 전문 기사 또는 전기 공학 교육을 받고 검증된 전문 기사의 감독을 받는 사람만이 연결할 수 있습니다. (검증된 전문 기사는 전문가 교육, 지식 및 경험뿐만 아니라 관련 규정의 지식을 보유하고 있어 그들에게 위임된 작업을 수행하고 가능한 위험을 탐지할 수 있으며 고용주가 자격을 갖춘 기술자로 지명한 사람입니다.)

2.9 Operation of electrical installations

Working on, with, or near electrical installations implies certain dangers. These electrical installations are designed for the generation, transmission, conversion, distribution and use of electrical power. Some of these electrical installations are permanent and fixed, such as a distribution installation in a factory or office complex, others are temporary, such as on construction sites, and others are mobile or capable of being moved either while energized or while neither energized nor charged.

The European Standard EN 50110-1 sets out the requirements for the safe operation of and work activity on, with, or near these electrical installations. The requirements apply to all operational, working and maintenance procedures. The European Standard EN 50110-2 is a set of normative annexes (one per country) which specify either the present safety requirements or give the national supplements to these minimum requirements at the time when this European Standard was prepared.

WARNING

High voltage and qualified personnel

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that working with voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience, as well as their knowledge of the relevant provisions, are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

3 Normative Documents and Declarations

3.1 Electrical

3.1.1 Electrostatic Discharge (ESD)

When handling disconnected devices, electrostatic discharge (ESD) can cause damage if discharged into or near sensitive components on the device. Take steps to avoid such an occurrence.

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN17tA system, its connections or a plug-in card.

Description of ESD

Static electricity is an electrical charge caused by the buildup of excess electrons on the surface of a material. To most people, static electricity and ESD are nothing more than annoyances. For example, after walking over a carpet while scuffing your feet, building up electrons on your body, you may get a shock - the discharge event - when you touch a metal doorknob. This little shock discharges the built-up static electricity.

ESD-susceptible equipment

Even a small amount of ESD can harm circuitry, so when working with electronic devices, take measures to help protect the electronic devices, including the GEN17tA data acquisition system, from ESD harm. Although HBM has built protections against ESD into its products, ESD exists and, unless neutralized, could build up to levels that could harm the equipment. Any electronic device that contains an external entry point for plugging in anything from cables to acquisition cards is susceptible to entry of ESD.

Precautions against ESD

Any built-up static electricity should be discharged from the user and the electronic devices before touching an electronic device, before connecting one device to another, or replacing acquisition cards. This can be done in many ways, including the following:

- Grounding oneself by touching a metal surface that is at earth ground. For example, if the computer has a metal case and is plugged into a standard three-prong grounded outlet, touching the case should discharge the ESD on the body.
- Increasing the relative humidity of the environment.
- Installing ESD-specific prevention items, such as grounding mats and wrist straps.

While appropriate precautions to discharge static electricity should always be taken, the user may want to take extra precautions to protect the electronic equipment against ESD if ESD events are observed in the present environment.

The use of wrist straps
Use an ESD wrist strap whenever you open a chassis, particularly when you will be handling circuit cards and components. In order to work properly, the wrist strap must make good contact at both ends (with the user's skin at one end, and with the chassis at the other).

WARNING

The wrist strap is intended for static control only. It will not reduce or increase your risk of receiving an electric shock from electrical equipment. Follow the same precautions you would use without a wrist strap.

WARNING

Wrist straps should only ever be used in situations where no direct power is connected to the circuit or system being handled.

3.1.2 Electromagnetic Compatibility (EMC)

EMC stands for Electromagnetic Compatibility. The overall intention is that electronic equipment must be able to co-exist with other electronic equipment in its immediate vicinity and that the electronic equipment does not emit large amounts of electromagnetic energy. Thus, there are two distinct requirements for electromagnetic compatibility: emission and immunity.

This instrument generates, accepts and can radiate radio frequency energy and, if not installed and used in accordance with the operator manual, may cause harmful interference to other equipment. However, there is no guarantee that interference will not occur in a particular installation.

Immunity test: All immunity tests are done with the failure criterion being a change of the instrument's control settings. Any of these tests may produce a spurious trigger. Measurements are not valid during and immediately after the immunity tests.

Whether the instrument causes interference to other equipment can be determined by turning the instrument on and off. If this instrument does cause minor harmful interference to other equipment, the user is encouraged to try reducing the interference by one or more of the following measures:

- Re-orient or relocate the affected equipment.
- Increase the distance between the instrument and the affected equipment.
- Re-orient or relocate interface cables.
- Connect the instrument to an outlet on a different supply circuit to the affected equipment.

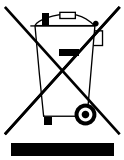
Electrical supply cables, interface cables and probes should be kept as short as practical, preferably a maximum of 1 m. Interface cables should be screened and interface cables longer than 3 m are not acceptable in terms of interference port immunity.

3.2 Environment

3.2.1 RoHS and WEEE - Waste Electrical and Electronic Equipment

Since February 2003, European Union legislation stating that EU members now restrict the use of hazardous substances in electrical and electric equipment (Directive 2011/65/EU and amendment 2015/863) and promotes the collection and recycling of such electrical equipment (Directive 2012/19/EU) has been in force.

Statutory waste disposal mark



The electrical and electronic devices that bear this symbol are subject to the European waste electrical and electronic equipment directive 2012/19/EU. The symbol indicates that the device must not be disposed of as household garbage.

In accordance with national and local environmental protection and material recovery and recycling regulations, old devices that can no longer be used must be disposed of separately and not with normal household garbage. For more information about waste disposal, please contact local authorities or the dealer from whom the product was purchased. As waste disposal regulations may differ from country to country within the EU, please contact the supplier about waste disposal regulations if necessary.

Packaging

The original packaging of HBM devices is made from recyclable material and can be sent for recycling. For ecological reasons, empty packaging should not be returned to us.

3.2.2 China RoHS

The product will comply with general hazardous substances limits for at least 10 years, and will be ecologically safe to use during this period, as well as recyclable. This is documented by the 10 years symbol on the system as statutory mark of compliance with emission limits in electronic equipment supplied to China.

Table 3.1: Hazardous substances

Part Name 部件名称	Hazardous Substances 有害物质					
	Lead 铅 (Pb)	Mercury 汞 (Hg)	Cadmium 镉 (Cd)	Hexavalent Chromium 六价铬 (Cr (VI))	Polybrominated biphenyls 多溴联苯 (PBB)	Polybrominated diphenyl ethers 多溴二苯醚 (PBDE)
Main PCB	X	O	O	O	O	O
PSU-module	X	O	X	O	O	O
CPU-module	O	O	O	O	O	O
Metal Parts	O	O	O	O	O	O
Plastic Parts	O	O	O	O	O	O
Cables	O	O	O	O	O	O
This table is prepared in accordance with the provisions of SJ/T 11364. 本表格依照SJ/T 11364规定的规定编制。						

O Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.
表示该有毒有害物质在该部件所有均质材料中的含量均在GB/T 26572规定的限量要求以下。

X Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.
表示该有毒有害物质至少在该部件的某一均质材料中的含量超出GB/T 26572规定的限量要求。

3.3 CE Declaration of conformity

For information about the CE Declaration of conformity, please refer to www.hbm.com/en/1254/downloads/.

3.4 FCC Class A Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1 This device may not cause harmful interference.
2 This device must accept any interference received, including interference that may cause undesired operation.

Note *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if it is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.*

IMPORTANT

Any modifications made to this device that are not approved by HBM may void the authority granted to the user by the FCC to operate this equipment.

4 Batteries

4.1 General

The GEN17tA has internal batteries.

Battery lifetime

A battery's lifetime depends on how it is handled. High temperature, super-fast charging and harsh discharges are conditions that harm batteries. Repeated full discharge cycles also stress the battery.

Precautions and warnings when using batteries

- Use the battery only for its intended purpose.
- Do not take batteries apart or modify them. The batteries must not be damaged, crushed, pierced or exposed to high temperatures. If a battery is handled inappropriately, it could be a risk of combustion or explosion.
- Do not leave the batteries in hot or cold places, as you will reduce the capacity and lifetime of the batteries. Always try to keep batteries at room temperature. A system with hot or cold batteries may not work temporarily, even if the batteries are fully charged.
- Do not short-circuit the battery. Accidental short-circuit can occur when a metallic object causes a direct connection between the + (plus) and - (minus) terminals of the battery, for example when a spare battery is carried in a pocket or bag. Short-circuiting the terminals may damage the battery or the object that causes the short-circuiting.

WARNING

If leaked battery fluid comes into contact with your eyes, immediately flush out your eyes with water and consult a doctor, as it may result in blindness or other injury. If leaked battery fluid comes in contact with your body or hands, wash thoroughly with water.
If leaked battery fluid comes into contact with the instrument, carefully wipe the instrument, avoiding direct contact with your hands.

4.2 Removal and replacement

WARNING

ELECTRICAL SHOCK HAZARD! Remove all cables before proceeding.

There is one CR2032 battery located inside in a GEN17tA in the Battery CPU section (see Figure 4.1).

To access the CPU section battery for removal or replacement, the mainframe PC section cover needs to be removed from the GEN17tA. For instructions on how access the CPU section, please refer to chapter "Accessing the CPU section" on page 107.

CAUTION

Use HBM approved batteries only.
CR2032 batteries from VARTA® and Panasonic® are approved by HBM.

CAUTION

All GEN series mainframes are factory-calibrated as delivered to the customer. Swapping, replacing or removing cards may result in minor deviations to the original calibration. Make sure that the input cards are reinstalled in the exact same slot that they were removed from to avoid changes to the calibration results.

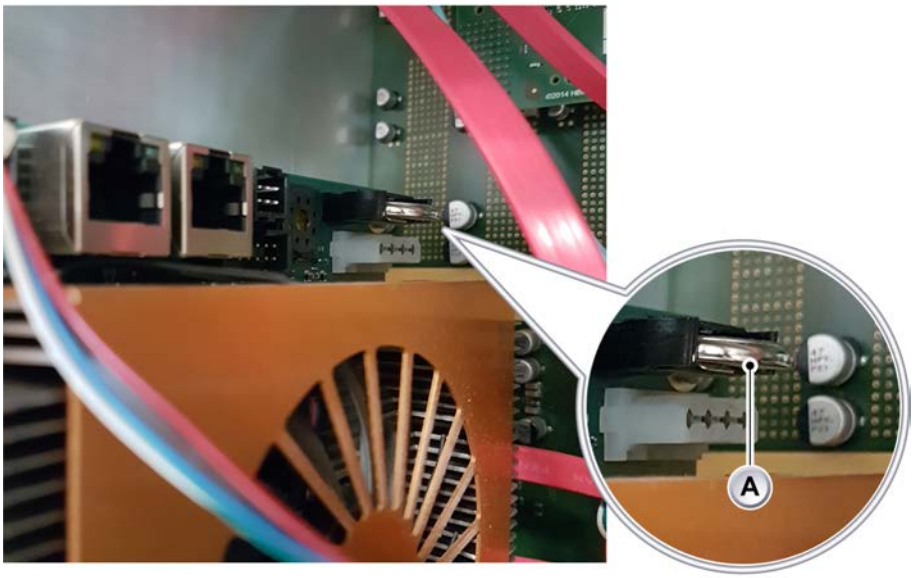


Figure 4.1: Battery - CPU section

A Battery in the CPU section

Remove/replace the battery from the CPU section

1 Power off the GEN17tA system and remove the power input cable.

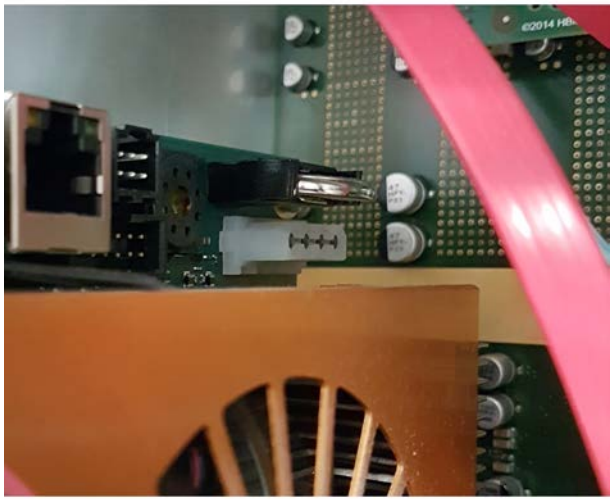


Figure 4.2: Battery - CPU section

2 Disconnect all cables to the acquisition cards.

3 To obtain access to the GEN17tA CPU section, please refer to chapter "Accessing the CPU section" on page 107.

4 To remove the battery, pull the battery out of the holder.

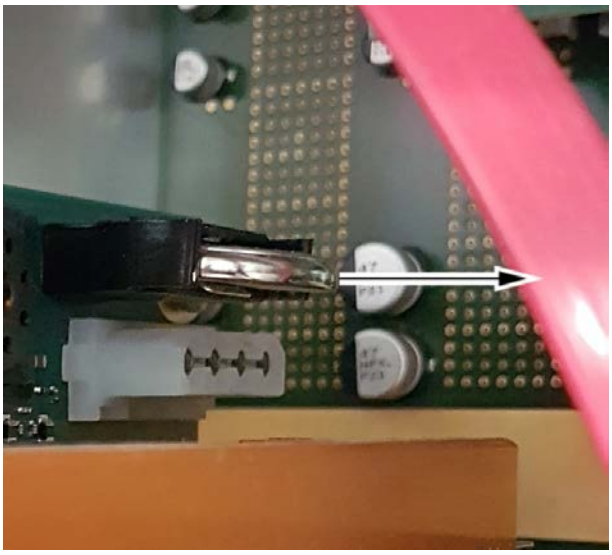


Figure 4.3: Remove battery (CPU section)

Note *Place the new battery in the same direction as the original battery was placed.*

5 Push the battery into position.

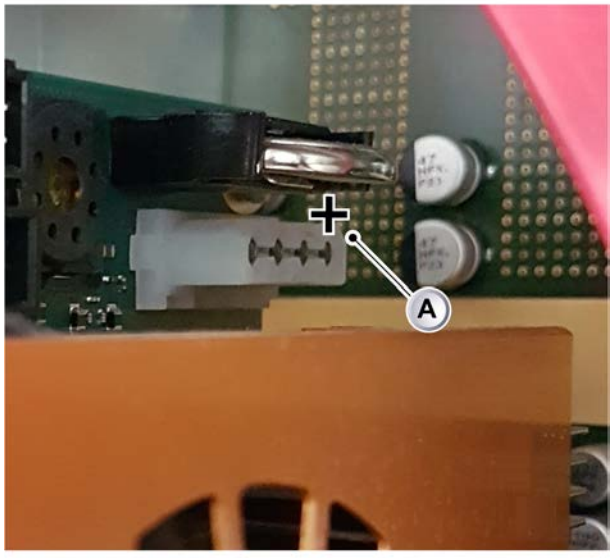


Figure 4.4: Battery in final position (CPU section)

A Make sure the battery is inserted with the “+” sign towards the fan.

6 Close the GEN17tA CPU section (in reverse order) as described in this chapter "Accessing the CPU section" on page 107.

4.3 Recharging

The GEN17tA does not use rechargeable batteries. When batteries are depleted, dispose of the batteries.

4.4 Disposal

Dispose of used batteries only in accordance with local chemical waste regulations. Always recycle.

WARNING

Do not dispose of batteries in a fire.

For more information about waste disposal, please contact the local authorities or the dealer from whom the product was purchased.
As waste disposal regulations may differ from country to country within the EU, please contact the supplier about waste disposal regulations if necessary.

5 Mains Power

5.1 Power and frequency requirements

To connect or disconnect the instrument from the AC supply, plug or unplug the IEC connector from the instrument or external power supply. The instrument should be positioned to allow access to the AC connector. The front power switch on the instrument is not a disconnecting device. When the instrument is connected and the rear switch is in the ON position, some power will be consumed.
For more information, please refer to chapter "Connecting power" on page 64.

The GEN17tA uses up to 1200 VA and operates from line voltages between 100 V AC and 240 V AC at 47-63 Hz. The power connection of the GEN17tA is a standard IEC 320 EN 60320 C20, 2-pole, 3-wire (male) appliance inlet, designed for 250 V at 16 A. The power inlet has an automatic thermal circuit breaker for overload protection. For more information, please refer to chapter "Fuse requirements and protection" on page 66.

CAUTION

Do not position the GEN17tA in a way that makes it difficult to remove the power input cable.

The GEN17tA must be connected to ground by the conductor of the supply cable. This is to ensure that all electromagnetic Compatibility (EMC) requirements are met.

5.2 Connecting power

The power inlet and the protective ground connection are located at the rear of the GEN17tA system. A mains power cord that is in accordance with the destination country's standards is shipped with the unit. For more information on power consumption, please refer to chapter "Mains Power" on page 63.

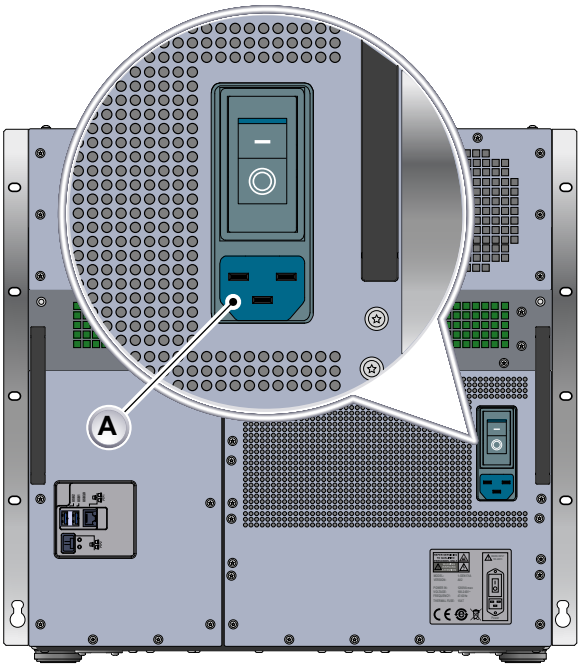
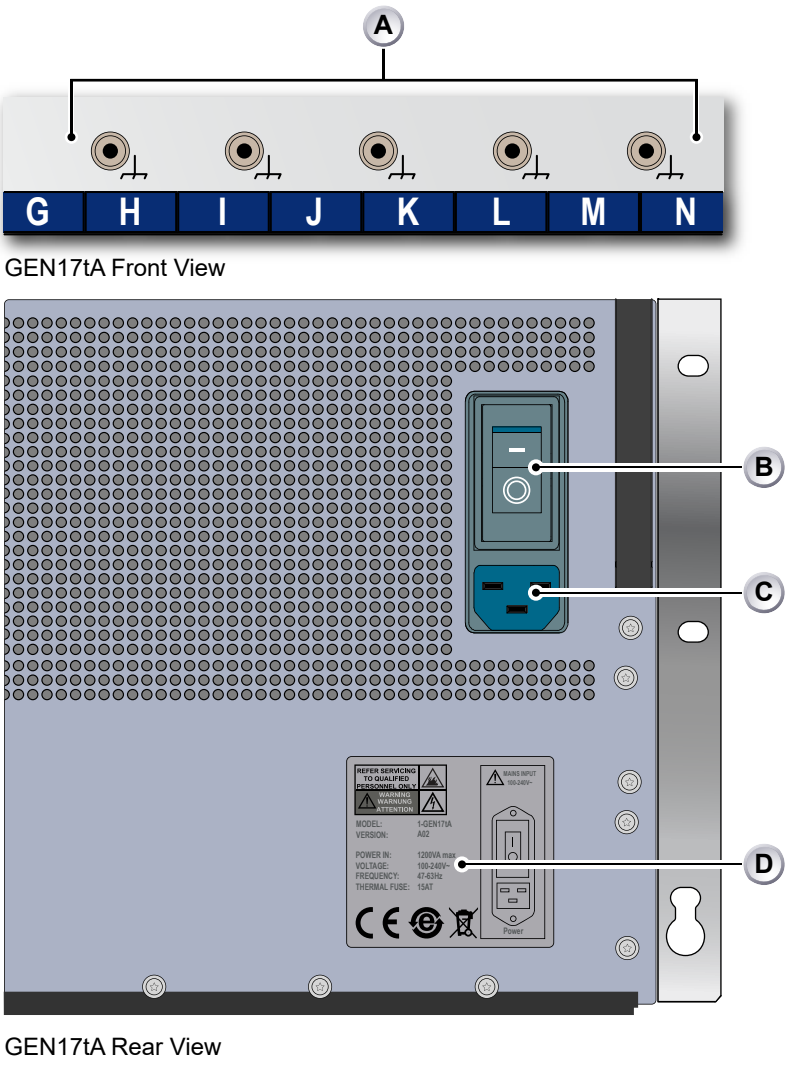


Figure 5.1: GEN17tA Desktop and Rack Mount Tethered Data Acquisition System

A Power inlet

The power inlet and inlet switch connects/disconnects the main power from the GEN17tA. To disconnect the GEN17tA from the AC supply completely, unplug the IEC connector from the instrument.
Plugging in the unit will not switch on the GEN17tA instrument. Make sure the rear mains switch is ON first. Then use the standby button on the front panel to power on the unit; see "GEN17tA control" on page 114.



GEN17tA Front View

GEN17tA Rear View

Figure 5.2: Power inlet

A Chassis ground
B Power on-off switch
C Power inlet
D Voltage rating

HINT/TIP

After an unexpected power loss the instrument will automatically return to the last power state when power is restored.

5.3 Fuse requirements and protection

GEN17tA is equipped with an automatic thermal circuit breaker type TA45.
Additionally for the UK, a fuse should be fitted in the line supply plug.

WARNING

Any interruption of the protective conductor inside or outside the apparatus is likely to make the apparatus dangerous. Intentional interruption is prohibited.

When the apparatus is connected to its supply, terminals may be live, and opening covers to remove parts is likely to expose live parts.

Whenever it is likely that the protection has been impaired, make the apparatus inoperative and secure it against any unintended operation.
For example, if the apparatus shows visible damage or has been subjected to severe transport stresses, the protection is likely to be impaired.

It is the responsibility of the user to ensure the safety of any accessories used with the equipment, such as probes.

WARNING

Connect a protective ground wire as an additional safety measure to prevent electric shock or damage to GEN17tA.

Using this device properly depends on the user reading all instructions and labels carefully.

If the instrument is used in a manner not specified by HBM, the protection provided by the instrument can be impaired.

5.4 Fuse replacement

The GEN17tA is equipped with a 2-pole, rocker actuated circuit breaker type TA 45 (16 A) and has no additional fuses.

6 Introduction

6.1 Introducing GEN17tA

Figure 6.1: Using GEN17tA

Some of the main features include:

- Combines a data recorder and transient recorder system
- Transient RAM up to 250 MegaSamples per channel in parallel
- Isolated and non-isolated channels with high-fidelity signal conditioning
- Unlimited recording size and duration
- A variety of data storage capabilities
- 19" rack form factor
- Tethered device for remote use via Ethernet

Data archiving is a challenging task when doing data acquisition. GEN17tA offers a variety of storage and archiving options. Using the built-in removable drive bay, GEN17tA can be equipped with a 960 GB RAID 0 Solid State Drive (SSD). The instrument can be connected to a network using built-in wired interfaces.

6.2 Mainframe overview

There are several different GEN series mainframes available:

Model	Slots	Design	Comments
GEN2tB	2	Portable	Tethered, portable data recording solution, best suited for low channel count applications. Option for 19" rack mount available.
GEN3i/ GEN3iA	3	Portable	An integrated all-in-one portable data recording solution suitable for field use. Best suited for lower channel count or medium computing power applications.
GEN4tB	4	Portable/Rack	Tethered, portable data recording solution, best suited for lower channel count applications. Option for 19" rack mount included.
GEN7i/ GEN7iA	7	Mobile	An integrated all-in-one mobile data recording solution suitable for field use. Best suited for medium channel count or high computing power applications. Option for 19" rack mount available.
GEN7tA	7	Mobile/Rack	Tethered mobile data recording solution, best suited for medium channel count applications. Option for 19" rack mount available.
GEN17tA	17	Rack	Tethered 19" rack mounted mainframe. Best suited for higher channel count applications.

All mainframes share many of the GEN series features. Besides the listed differences in the table above, other differences are: mechanical form factor, power consumption, integrated PC or tethered PC use, etc. For technical details, please refer to the individual mainframe data sheets.

6.2.1 Mainframe feature comparison

Mainframe	Standard streaming (cPCI backplane)	Fast Streaming (PCI-e backplane)	Option carrier card	EtherCAT® support
1-GEN3I, 1-GEN3IA, 1-GEN7I and GEN7IA	Yes	Yes	Yes	No
1-GEN2TB	No	Yes	Yes	No
1-GEN4TB	No	Yes	Yes	Yes
1-GEN7TA and 1-GEN17TA	Yes	Yes	Yes	Yes

IRIG/GPS and Ethernet PTP synchronization	IRIG and IRIG/GPS synchronization	1 Gbit Ethernet (RJ45, electrical) PTP synchronization	1 Gbit Ethernet (SFP, optical) PTP synchronization	10 Gbit Ethernet (RJ45, electrical) without PTP synchronization	10 Gbit Ethernet (SFP, optical) without PTP synchronization
1-GEN3I, 1-GEN3IA, 1-GEN7I, GEN7IA, 1-GEN2TB, 1-GEN4TB, 1-GEN7TA and 1-GEN17TA	Yes	Yes	Yes	No	No

6.3 Hardware

The acquisition section of the GEN17tA is based on the successful and proven GEN series Data Acquisition System.

In GEN17tA the same concepts are used.

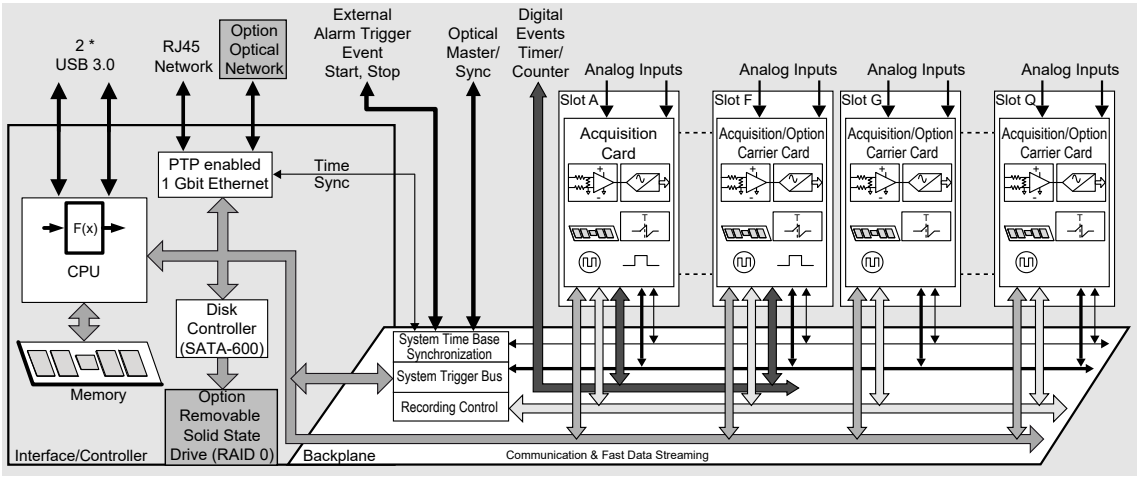


Figure 6.2: Block Diagram GEN17tA

6.3.1 PCI-e/CPCI backplane

GEN17tA uses a combined PCI-e/CPCI backplane. The PCI-e (Peripheral Component Interconnect Express) backplane can transfer data at very high speeds to ensure the highest system throughput. The CPCI (Compact Peripheral Component Interconnect) backplane can transfer data at high speeds to ensure a high system throughput. The combined backplane supports backward compatibility to support any GEN series acquisition cards and allows new acquisition cards to use the faster PCI-e transfer speeds.

HINT/TIP

The CPCI backplane is the standard data storage bus. All acquisition cards introduced to market before 2014 support only this backplane. The maximum aggregate streaming rate for these acquisition cards is 200 MB/s.

Check the detailed specifications of the individual acquisition cards to see whether it uses the fast data storage bus of the GEN17tA if aggregate streaming rates above 200 MB/s are required.

6.3.2 Input cards

GEN17tA can accept up to 17 input cards. Each input card includes one or more digitizers, a powerful CPU or DSP for filtering, intelligent triggering, and acquisition management. For more information on the various cards, please refer to chapter "Available input cards" on page 213.

Note *Before changing or removing input cards, always check the warranty information. Changing input cards will void the tight calibration of the input card. Wider tolerances have to be considered when exchanging input cards.*

6.3.3 Master/Sync support

The GEN17tA system has a built-in Master/Sync connector. This connector supports the GEN series Master/Sync extended synchronization protocols and is fully backward compatible with the basic synchronization protocols. The single synchronization connector allows for the direct connection of one Sync mainframe to the GEN17tA or the GEN17tA to be a Sync mainframe within any Master/Sync multi mainframe setup.

6.3.4 Thermal protection

Every GEN series mainframe supports a feature called Thermal Shutdown. For this, the mainframe and acquisition cards have built-in digital thermal sensors to measure local temperatures. The GEN series embedded software reads these values every minute and monitors the system's internal temperature for overheating.

Automatic user warnings are initiated using the following diagram (see Figure 6.3).

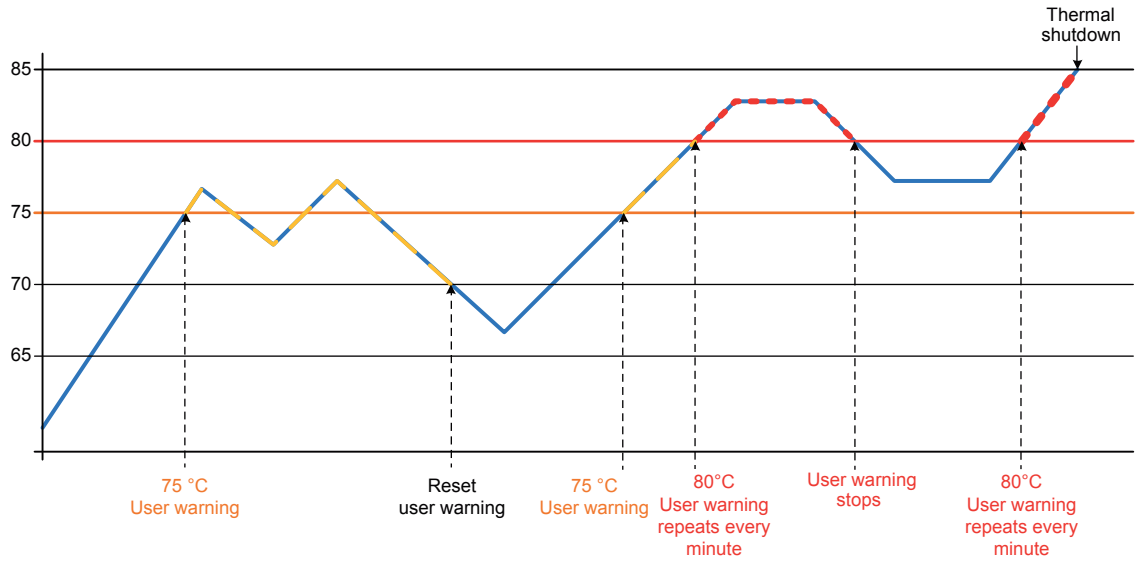


Figure 6.3: Thermal protection - Automatic user warnings

- As soon as one of the internal thermocouples measures a temperature above +75 °C for the first time, a single user warning is initiated. As long as the highest temperature measured is above +70 °C and below +80 °C, no additional user warnings are initiated.
- If the internal temperature drops below +70 °C after reaching +75 °C, the system assumes that the user has performed an action, to reduce internal temperatures. If the internal temperature reaches +75 °C again, the system assumes that there is a new thermal problem and a new user warning is initiated.
- If the internal temperature keeps rising and reaches +80 °C, the system assumes that a critical zone has been reached. User warnings will be sent every minute for as long as the measured temperatures are above +80 °C. If the temperature drops below +80 °C, the warnings sent at minute intervals stop. If the temperature rises above +80 °C again, user warnings are initiated every minute again.
- If the internal temperature were to keep rising and then reaches +85 °C, an automatic thermal system shutdown user warning is initiated, the automatic thermal shutdown event is logged in the systems error log and the system will shut down.

At next power-on of the GEN series system, the automatic thermal shutdown event will be presented to the user again and can be found in the error diagnostics of the mainframe.

6.4 Acquisition

GEN17tA is a multi-channel modular Data Acquisition System. It provides real-time data for waveform and meter displays. It allows unlimited recording duration and file size at a high streaming rate. Statistics are performed in real-time. Its extreme performance signal conditioning includes both Bessel and Butterworth anti-alias filters to provide excellent response.

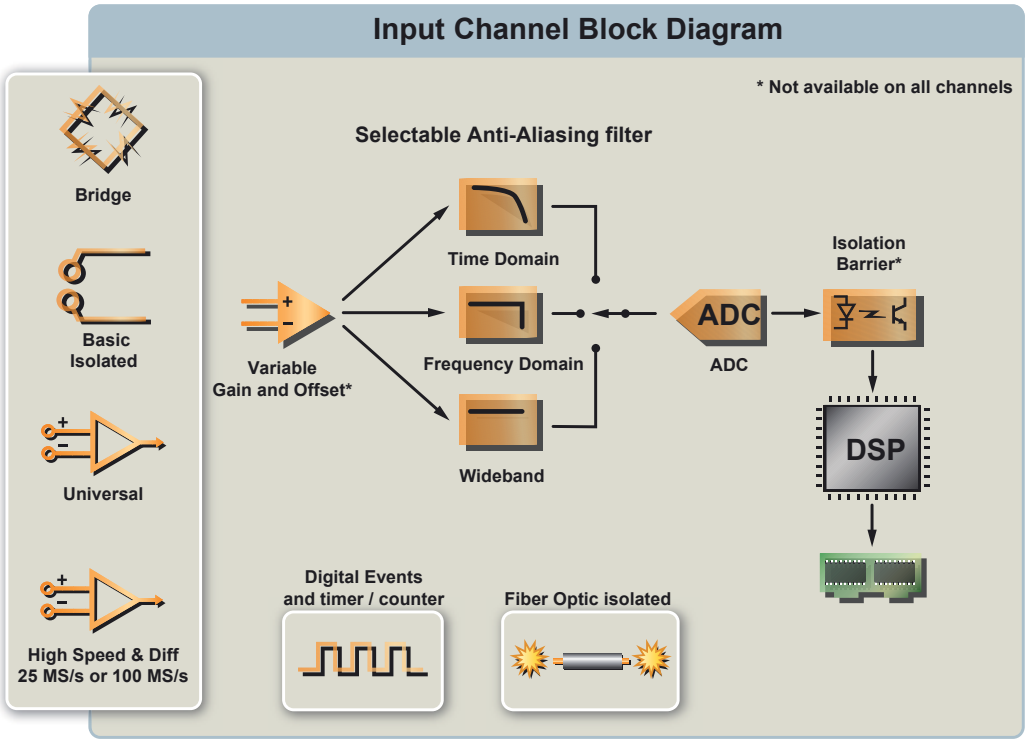


Figure 6.4: Input channel block diagram

It also functions as a transient recorder with a hardware trigger on all channels with hysteresis, delay and logic features. Transient memory is huge and can capture minutes of data on all channels. Segmented sweeps are displayed with no dead time and the recorder has a wide analog bandwidth.

6.4.1 StatStream®

Most PC-based DAQ systems can easily acquire megabytes of data. But even the most powerful PC is poorly equipped to display and process files of megabytes or gigabytes. In fact, most DAQ systems fail to display over 99% of live data! The exclusive StatStream® technology accelerates all aspects of a measurement task with dedicated hardware and firmware.

While recording, StatStream® pre-processes a display summary at the full resolution of a PC monitor. Even a single transient point on any channel is accurately displayed.

In addition, StatStream® continuously calculates parameter values on blocks of data. Vital statistics are available at every moment, including warnings if any channel goes off scale. The Perception software offers a variety of meters to display these on-line parameters.

When reviewing stored files, the embedded StatStream® data enables an accurate, detailed overview of any size file in seconds. Unlike competitive systems, the GEN17tA has no need to inspect gigabytes of information just to display the last kilobyte. While zooming in, more detail is displayed while always maintaining the highest visible resolution.

6.5 Signal conditioning

GEN17tA supports common analog sensors with the highest performance signal conditioning available. All inputs are sampled simultaneously for exact time correlation.

Plug-and-play hardware discovery with scalability to any number of channels. Perception software can group and outline similar amplifiers for one-click settings. Extensive diagnostics gives the confidence of correctly wired and working sensors before any test.

6.6 Data storage

In addition to mega samples of on-board RAM, record data directly to the GEN17tA optional SSD, or to a network attached storage over the Gigabit Ethernet. GEN17tA always stores to on-board high-speed RAM. Recorded data is then automatically stored at the GEN17tA defined storage location at maximum speed.
Storing data to the optional removable built-in GEN17tA SSD allows data storage at 350 MB/s. In continuous mode, a full drive recording can be made at 350 MB/s. In circular recording, the GEN17tA can monitor signals at 350 MB/s forever and will stop only when triggered by a user pre-defined event. The entire optional SSD can then be used as pre-trigger recording.

HINT/TIP

The optional SSD RAID system of GEN17tA can reach 350 MB/s continuous storage. To reach this speed, GEN17tA has a fast data storage bus added to the backplane. Only acquisition cards designed to work with this fast data storage bus can achieve the maximum streaming rates of the GEN17tA SSD.

Recorded files are standard Perception files with the PNRF extension (Perception Native Recording File).

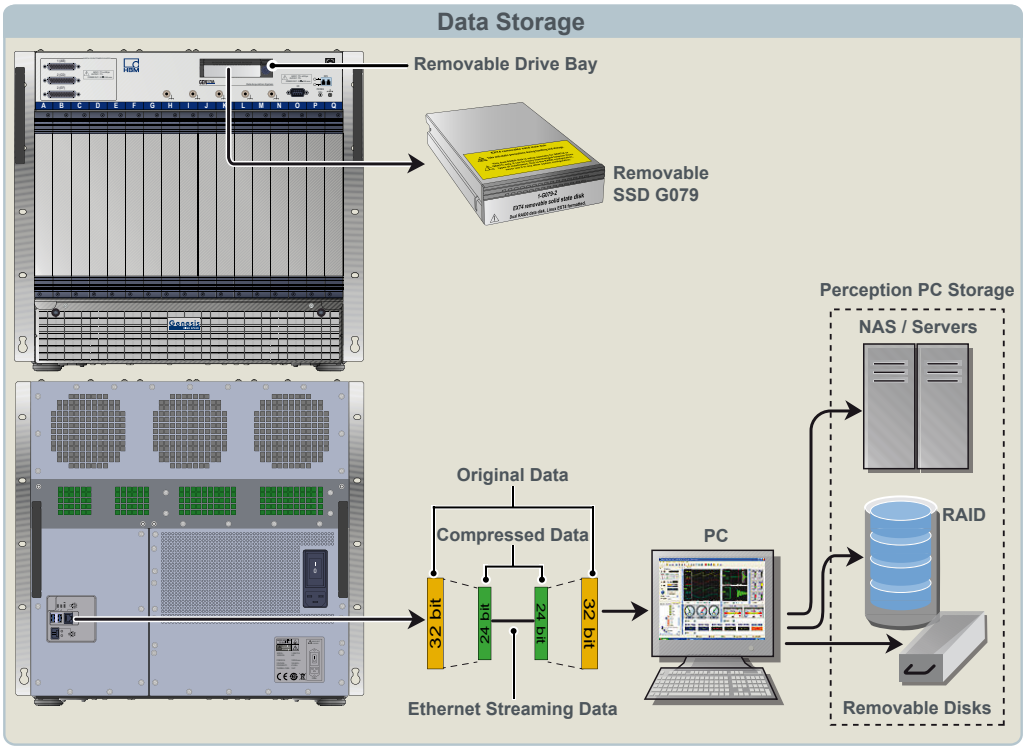


Figure 6.5: Data storage options

6.6.1 RAID 0 technology

The GEN17tA optional removable drive supports RAID functionality. RAID is an abbreviation for **R**edundant **A**rray of **I**ndependent **D**isks. RAID technology exists in many different forms, each with its own specific use case. Within this manual, only the GEN17tA RAID mode will be explained. More RAID knowledge can be found on Wikipedia (www.en.wikipedia.org/wiki/Standard_RAID_levels).

The GEN17tA optional drive uses a 2-disk RAID 0 setup to increase the overall continuous storage speed. RAID 0 does not offer any enhanced data security. If one of the drives has a read error, the entire recorded data is lost.

WARNING

Make regular backup copies of all recorded data to prevent data loss due to drive errors.

HINT/TIP

Regular predictive replacement of drives is recommended to minimize the risk of losing data. For more information, please refer to appendix "Preventive maintenance" on page 386.

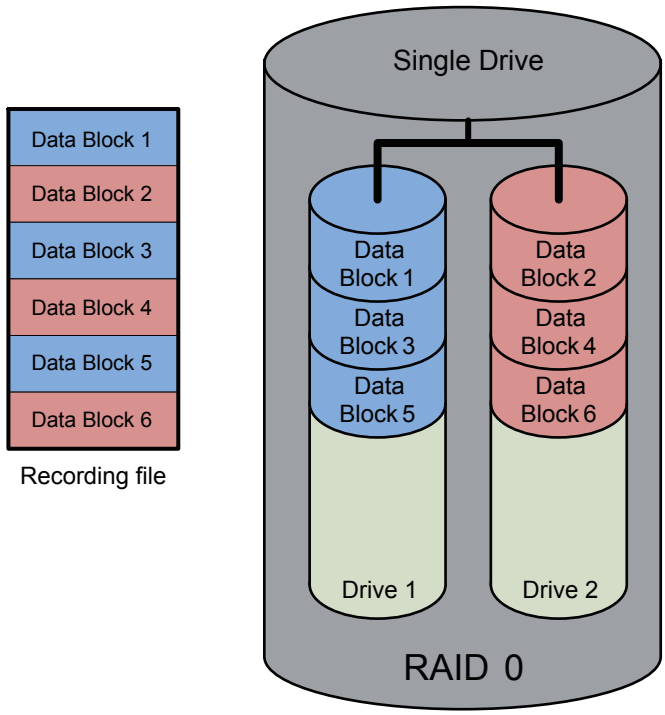


Figure 6.6: RAID 0 data storage

When two drives are set up in a RAID 0 mode, the operating system will only see a single drive. Only the RAID controller has the knowledge of the two drives.

Any (recording) file written to a drive is always stored using multiple smaller blocks of data. Each block of data is written sequentially to the drive. As the data is written to the RAID controller, it spreads the sequential written data blocks across the drives of the RAID array. As GEN17tA uses two drives, all odd data blocks are written to Drive 1 all even data blocks are written to Drive 2.

The net effect is a data read and write speed that is almost double the speed when using a single hard drive. However, if one of the drives experiences data read errors, the entire recording is lost as no redundancy is available.

WARNING

Linux will not recognize the removable drive option as a removable drive. To prevent loss of data and drive integrity, power off the GEN17tA before removing or replacing your drive.

6.6.2 Solid State Drive (SSD) technology

GEN17tA uses state-of-the-art Solid State Drives.

A Solid State Drive has no moving parts and creates a reliable data storage medium in environments with higher shock and vibrations. The absence of the moving disk head also avoids the standard hard disk seek times. Solid State Drives therefore offer a higher continuous streaming rate.

WARNING

Solid State Drives require predictive replacement to minimize the risk of down time or loss of data. For more information, please refer to "Preventive maintenance" on page 386.

6.7 Interface/Controller section

GEN17tA has a built-in industrial PC. This PC channels the tethered communication with the remote PC.

Features include:

- Intel Core™ i3 processor 6th generation(1)
- Linux (3.x or newer) operating system
- 1 wired (RJ45) and 1 optical (SFP) gigabit Ethernet connector, PTP support for timing synchronization
- Optional removable 960 GB SSD in RAID 0 setup (Solid State Drive)

(1) Intel® and Intel® Core™ are trademarks of Intel Corporation in the U.S. and/or other countries.

Refer to the GEN17tA datasheet for full details.

7 Setting up the GEN17tA

7.1 GEN17tA connections

The GEN17tA has several connections with different functions.

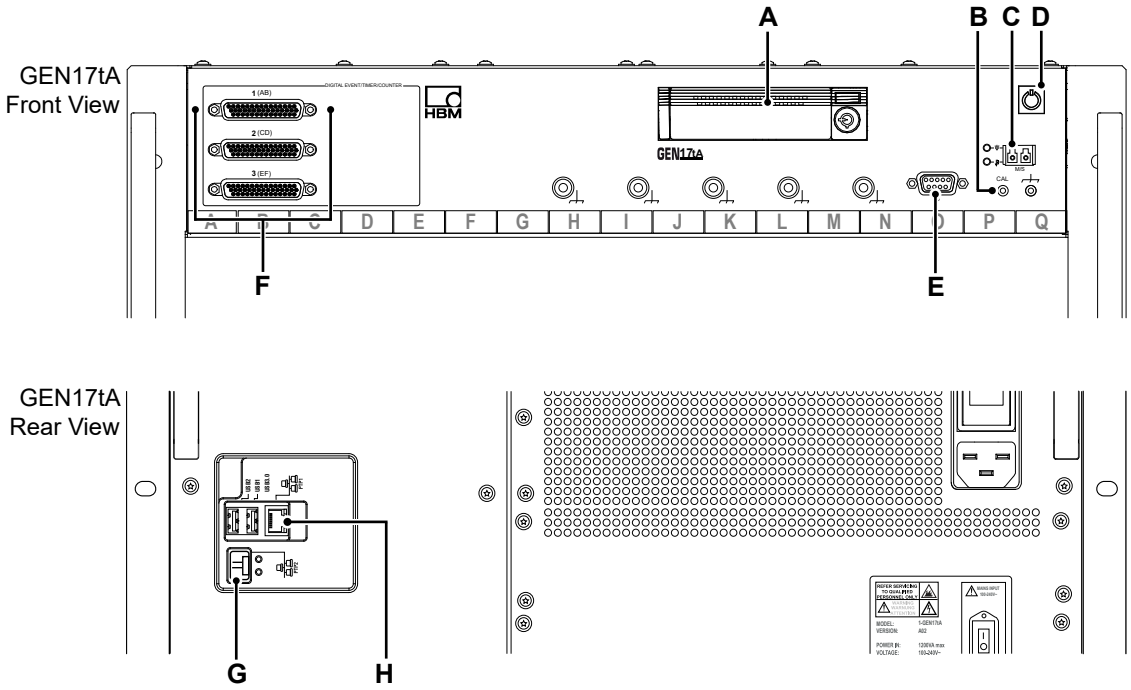


Figure 7.1: PC connections - Front view (top) and rear view (bottom)

A **Removable drive bay**
See chapter "Removable drive bay" on page 83 for more details.

B **Probe calibration**
See chapter "Probe calibration" on page 98 for more details.

C **Master/Sync connector** (optical)
See chapter "Master/Sync connector" on page 145 for more details.

D **Standby switch**

E **I/O connector** (trigger in/out, clock in, event in/out, start/stop)
See chapter "I/O connector" on page 154 for more details.

F **Digital Event/Timer/Counter**
See chapter "Digital Event/Timer/Counter" on page 100 for more details.

G **PTP enabled network optical SFP slot (SFP module is optional)**
See chapter "Connecting the GEN series to a network" on page 86 for more details.

H **PTP enabled network RJ45**
See chapter "Connecting the GEN series to a network" on page 86 for more details.

7.1.1 Removable drive bay

The GEN17tA drive bay supports removable solid state data disk (1-G079).

The removable system Solid State Drive (G074) is a factory installed option. This option consists of two Solid State Drives configured in a RAID 0 volume. RAID volumes require a match between the systems BIOS settings and the configuration of the disk volumes. Any mismatch between these settings will make the RAID volume unreadable.

The removable data disk option is a standard EXT4 (Linux file system) formatted disk. EXT4 disks can only be used to transfer data to PCs that support the EXT4 file format. For example, the Windows® operating system does not support the EXT4 file format. However, commercial tools are available for Windows® to enable the use of EXT4 formatted disks.

WARNING

The removable Solid State Drive option (G079) is configured as a RAID 0 volume of two disks. This configuration is custom made for GEN17tA and should not be used in any other system. When connecting this RAID configuration to other computers, the drives will not be recognized and data access is not possible. Do not use disk repair software tools to try and get access to the data stored on this RAID volume. Any attempt to access the data with wrong bios RAID settings will result in complete loss of all data stored on the RAID volume.

Figure 7.2: GEN17tA removable drive bay

A Drive bay
B Drive carrier
C Keylock
D Eject button

Inserting a drive carrier:

1. Power off GEN17tA.
2. If the drive bay eject button is released, push it to lock the eject button inside the bay.
3. Slide the drive carrier into the frame, then push the carrier in until it clicks.
4. Insert the key included in delivery into the keylock and turn it 90 degrees clockwise to secure the carrier to the frame.
5. Power on GEN17tA.

HINT/TIP

The first time that any drive is used with the removable drive bay, it appears as a blank, unallocated drive. The drive inside the enclosure needs to be formatted before use.

WARNING

Formatting a drive will erase all data on the drive, so be sure to back up all data before beginning this operation.

A Drive carrier

Safe drive carrier removal:

1. Power off GEN17tA.
2. Insert the key included in delivery into the keylock and turn it 90 degrees counter-clockwise to unlock the drive carrier.
3. Push the eject button below the keylock once to release the button.
4. Push the eject button again to eject the carrier.

WARNING

Never remove a removable disk without powering down GEN17tA. The operating system uses the disk continuously while GEN17tA is powered ON. Removing the drive without powering it down can result in a system crash and possible loss of data.

7.2 Connecting the GEN series to a network

The GEN series uses standard TCP/IP protocol over Ethernet to communicate with the controlling PC. The Interface/Controller provides access to the Ethernet network.

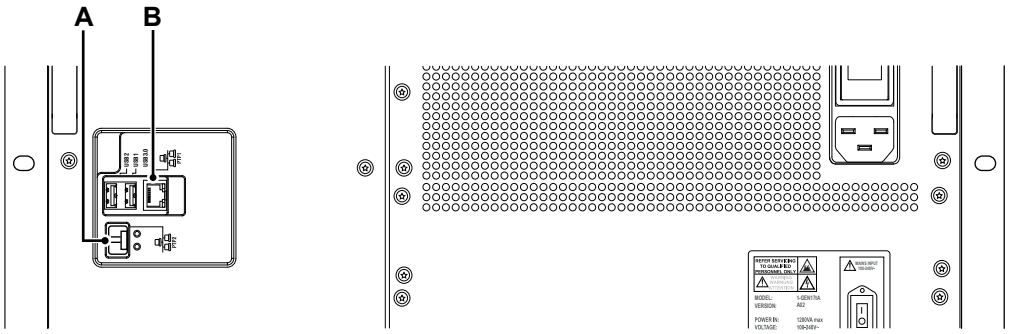


Figure 7.3: Interface/Controller connections (GEN17tA rear view)

The Interface/Controller has connections that can be used to connect other devices to the GEN17tA system.

A PTP enabled network optical SFP slot (SFP module is optional)

B PTP enabled network RJ45

The GEN series can be connected in one of two ways:

- Directly to a PC, or
- To a company network

The GEN series is an extremely high-performance acquisition system that is capable of transferring Megabytes of data at high speed to the controlling PC. For the best performance and fastest throughput, HBM strongly recommends the GEN series be connected directly to an Intel© Core i5 or i7 based PC, or better, with the CPU operating at a clock frequency of 2.5 GHz or greater and a 1 Gigabit Ethernet adapter.

If the controlling PC also connects to a company network, a second hardware Ethernet adapter in the PC is recommended for this purpose. A second adapter preserves the Gigabit connection for the fastest possible data transfer while preventing GEN series network traffic from potentially interfering with the company network performance.

7.2.1 Default network settings

By default, all network interfaces are configured to use DHCP. If no DHCP response is received within six seconds, the network interfaces will assign themselves network IP addresses in the range of 169.254.xxx.xxx with a subnet mask of 255.255.0.0. This is called "Automatic Private IP Addressing" and is also built into Microsoft Windows®.
The default Mainframe password is **"genesis"** (lowercase, without the double quotation marks).

7.2.2 Connecting the GEN series directly to a PC

The GEN series can be connected directly to a PC. At the same time, the PC can be connected to a corporate network. For this you will need a PC with two Ethernet NICs (Network Interface Cards.) The one for the GEN series must be at least 1 Gbit for the best performance. You will require either a CAT5e Ethernet cable or an optical cable from your PC to the GEN series, depending on the options installed.

Figure 7.4: Direct connection to PC

Since NIC #1 in the illustration is not on the company network, the PC and the GEN series cannot automatically obtain network IP addresses from a DHCP server as they normally would. After the DHCP time-out period, both the PC and Genesis mainframe fall back to Automatic Private IP Addressing. Therefore, it is not necessary to make any network settings on the GEN series or the PC. **However, communication is only possible a minute or two after powering up the GEN series.** To avoid the one minute wait, a fixed IP address and subnet mask may be manually assigned in both the PC and the GEN series.

7.2.3 Connecting the GEN series to a company network

To avoid using a PC with two Ethernet cards, the GEN series can be connected to an Ethernet port on the local network. HBM recommends adding a 1 Gigabit autosensing Ethernet switch for this purpose. Low-cost compact switches that have four to eight ports and that are sufficient for connecting a number of instruments to a PC are readily available at any computer store. A switch allows the PC to communicate locally with instrument(s) with a dedicated high-speed connection, without burdening the company network with potentially high data rates. It simply plugs in and requires no network configuration.

The network could look like Figure 7.5.

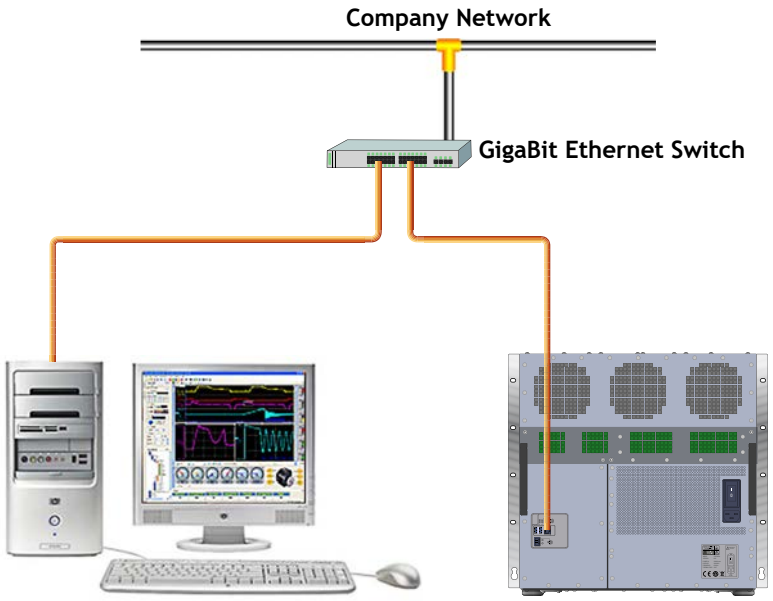


Figure 7.5: Connection to corporate network

The GEN series is pre-set for DHCP to automatically obtain a network IP address from the company server, just as the PC does. There is no need to make any network settings on the GEN series or PC.

7.2.4 Note on IP address and DHCP

An IP address is like a telephone number or a home address -- each one is entirely unique. Every computer on the Internet or a local network has its own IP address. The standard format is four groups of numbers separated by periods, and each number is an integer between 0 and 255.

192.168.178.111

Along with, the IP address, the computer uses a network mask. The network mask is used to identify the size of the local address range. To address a computer outside this address range, a network router is required to transfer the network messages to another address circle. This could be compared to a telephone long distance call. A netmask standard format is four groups of numbers separated by periods, and each number is an integer between 0 and 255. Left to right each group should be either 255 or any of the values 254, 252, 248, 240, 224, 192, 128 or 0. As soon as a group is not set to 255, the remaining groups must be 0. E.g. 255.128.0.0.

255.255.255.0

With this example and the IP address above, the range of addresses for this mainframe would be:

192.168.178.0 to **192.168.178.255**

WARNING

Within the addressable range of any system, the lowest and highest address are each assigned with special network features. These addresses (Example 192.168.178.0 and 192.168.178.255) should not be assigned to any mainframe.

IP addresses can be divided into two groups: static and dynamic. Computers that run important tasks all day, every day, such as servers and mail servers, have static IP addresses; their addresses never change.

DHCP operates like any other client-server relationship. When the PC or GEN series connects to a DHCP server, the server leases the machine a private IP address. The machine lives at that address until the lease expires, at which point a new IP address is assigned to the machine. When the DHCP server is configured, the lease duration can be set at different intervals. The most common lease duration among ISPs and other large networks is three days. DHCP servers can be located within a PC or a network router.

To use static IP addresses, set the GEN series network setting **Use DHCP** to **False**.
When there is a DHCP server, set the GEN series network setting **Use DHCP** to **True**.

WARNING

When Use DHCP is set to False and when multiple mainframes are used, a different IP address must be set for each mainframe.

7.2.5 Network testing and troubleshooting

1. If the GEN series is connected to the Ethernet correctly, the LINK LED in the Ethernet connector will illuminate within a few seconds to indicate that a hardware interface has been detected. If the LINK LED does not illuminate, the Ethernet cable is not connected or is wired incorrectly.
2. If the LINK LED is illuminated but the Perception software cannot find the GEN series system, check the TCP/IP network settings on the GEN series and on the PC. On the Windows® PC, select Start in the task bar, click Run… and type "CMD" (without quotation marks). This opens a command window. In the command window type, IPCONFIG or IPCONFIG /ALL to view settings. Some of the most common problems are:
   - IP addresses that are not in the same range. Normally, the first three octets are the same and the fourth one varies, such as 169.254.10.252 and 169.254.10.200.
   - Identical IP addresses. The PC and the GEN series must have at least one different digit in the fourth octet.
   - IP addresses that use the reserved numbers 0 or 255. All digits should be between 1 and 254.
   - The subnet masks are not completely identical.

7.3 Restore default network settings

To restore a mainframe to its default network settings, take the following steps:

1. Turn the mainframe off and wait for five seconds.
2. Turn the mainframe on.
3. Wait for the three-tone sound indicating the system has started.
4. Within one minute after that sound has stopped. Press the stand by button for short periods (approximately 0.5 seconds) five times. A four-tone sound is played to confirm that the default network settings will be applied.

Note *The default network settings will be applied to all network interfaces (please refer to paragraph "Connecting the GEN series directly to a PC" on page 87)*

Note *To power down normally within that period, keep the power button pressed for at least four seconds.*

7.4 Removing and installing input cards

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN17tA system, its connections or a plug-in card.

CAUTION

The GEN17tA Data recorder is factory-calibrated as delivered to the customer. Swapping, replacing or removing of cards may result in minor deviations to the original calibration. The GEN17tA system should be tested and, if necessary calibrated, at one-year intervals or after any major event that may affect calibration. When in doubt, consult the local supplier.

7.4.1 Removing cards

CAUTION

Heatsink and other parts may be hot when removed just after switch-off.

To remove a card:

1 Power off the GEN17tA system and remove the power input cable.
2 Disconnect all cables from the acquisition cards.

3 Loosen the small set screw on both ejectors on the card.

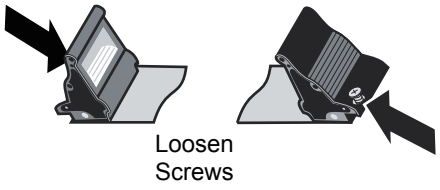


Figure 7.6: Removing card (Part 1)

4 Press the inner grey button on each ejector to release the catch.

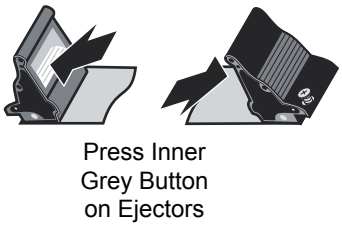


Figure 7.7: Removing card (Part 2)

5 Press both ejectors outward to release the card. They act as levers to gently pull the card from its backplane sockets.
6 Slide the card out of the GEN17tA unit.

7.4.2 Installing cards

To install a card:

1 Power off the GEN17tA system and remove the power input cable.
2 Ensure that the ejector levers are in the farthest outermost position, tilting away from the card.
3 Slide the card into its guide rails until the ejectors contact the perforated metal strips on the left and right.
4 Press both ejectors inward to seat the card. They act as levers to gently pull the card into its backplane sockets. The grey button should snap to its default position and lock the ejectors.
5 Tighten the small set screw on both ejectors on the card:

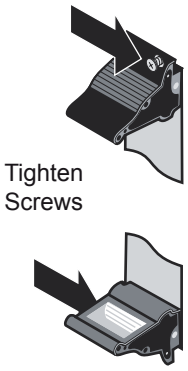


Figure 7.8: Card ejectors with screws

WARNING

Screws must be locked to meet CE emissions.

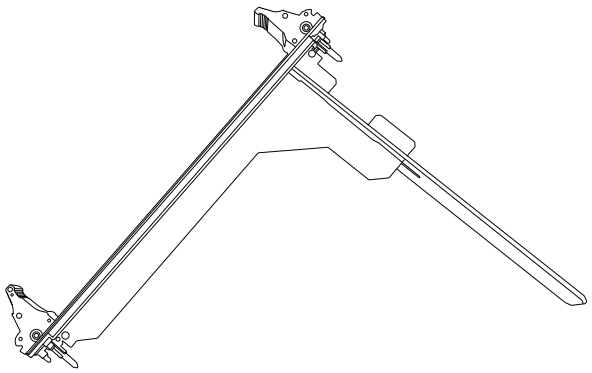


Figure 7.9: Blind panel (1-G009)

WARNING

Any empty slots must be covered with a blind panel on the back to meet the cooling requirements of the mainframe.

7.5 Handles

The handles are used to carry the GEN17tA system.

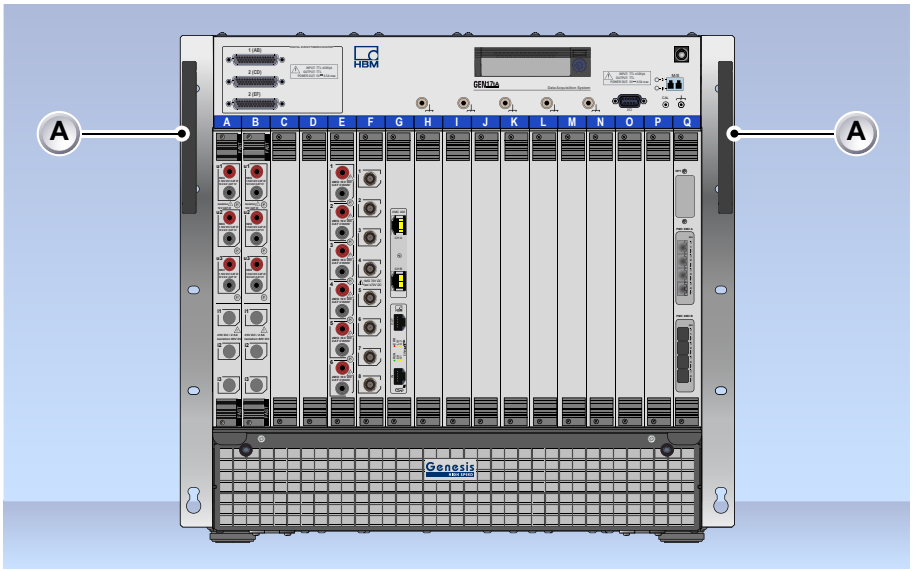


Figure 7.10: Front side handles

A Front side handles

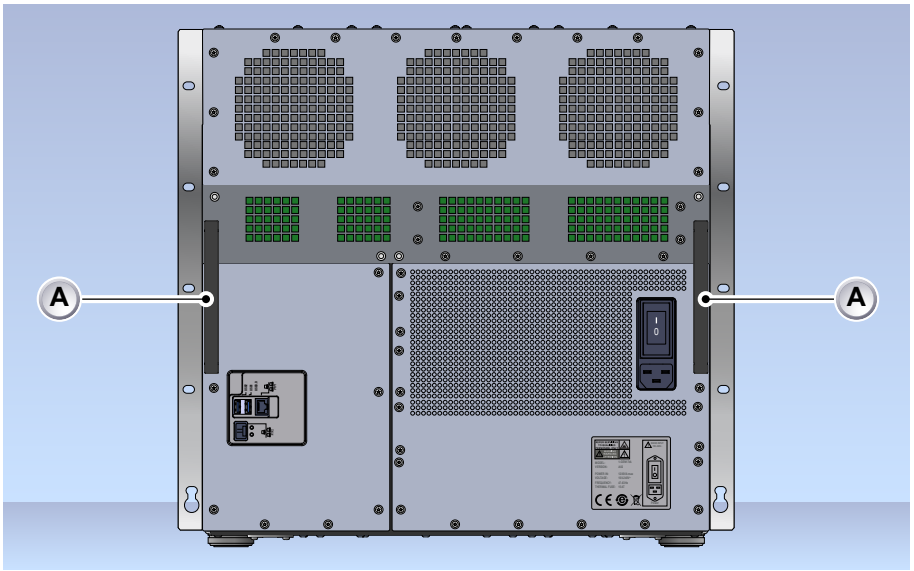


Figure 7.11: Rear side handles

A Rear side handles

7.6 Feet

GEN17tA stands on four rubber feet in normal operation position. Two feet are positioned at the rear and two are at the front of the instrument, the feet are user removable (can be screwed off the unit).

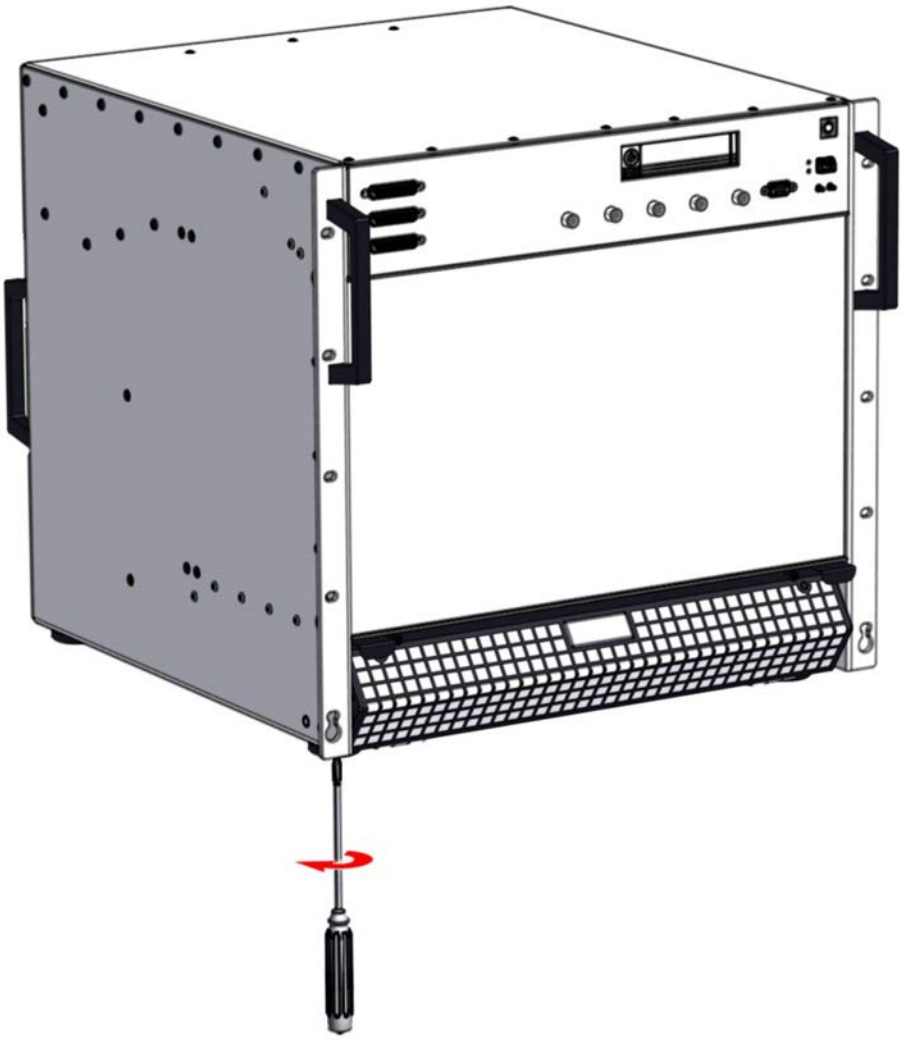


Figure 7.12: Removable feet on each bottom corner (1)

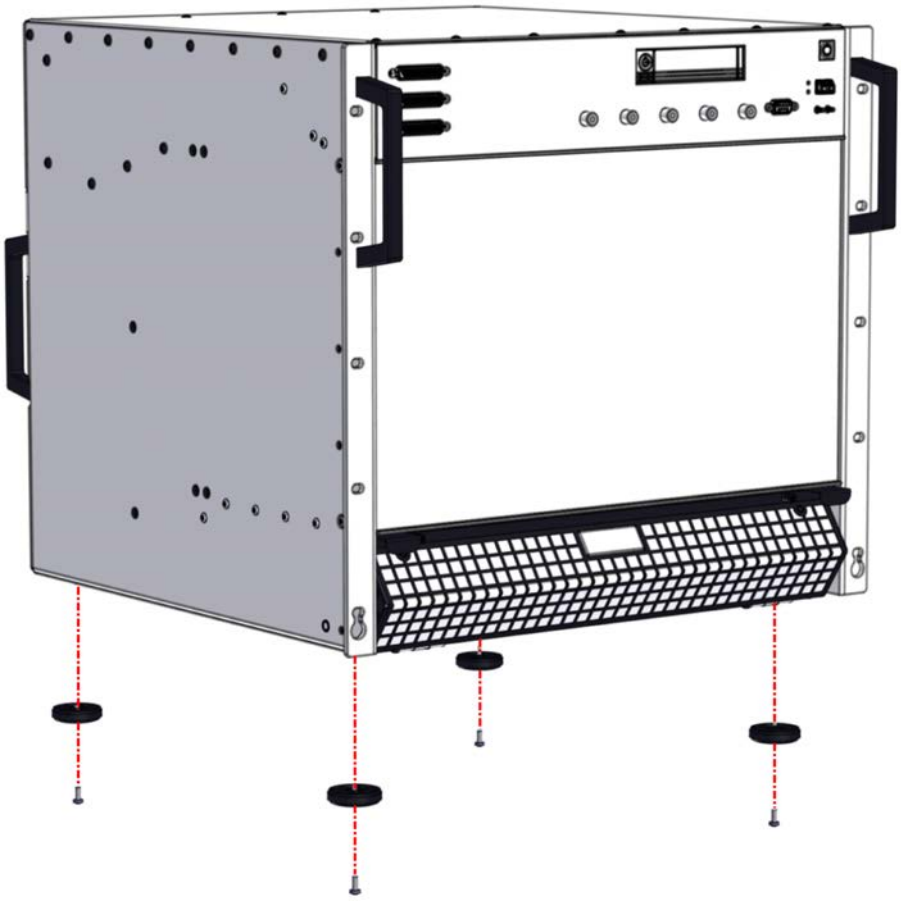


Figure 7.13: Removable feet on each bottom corner (2)

7.7 Probe calibration

The GEN17tA mainframe is provided with a probe calibration output. This output can be used to calibrate probes used in combination with the Genesis High-speed measurement system.

The probe calibration output drives a calibration signal with the following characteristics:

- ~1 kHz square wave
- 0 V to 2 V amplitude when using a 1 MΩ load
- 0 V to 1 V amplitude when using a 50 Ω load

In order to calibrate a probe, connect the probe output to an acquisition card and set up the acquisition channel in accordance with the probe calibration signals as described above.

Connect the probe ground wire to the probe calibration ground output pin and the probe input to the probe calibration signal output pin. See Figure 7.14.

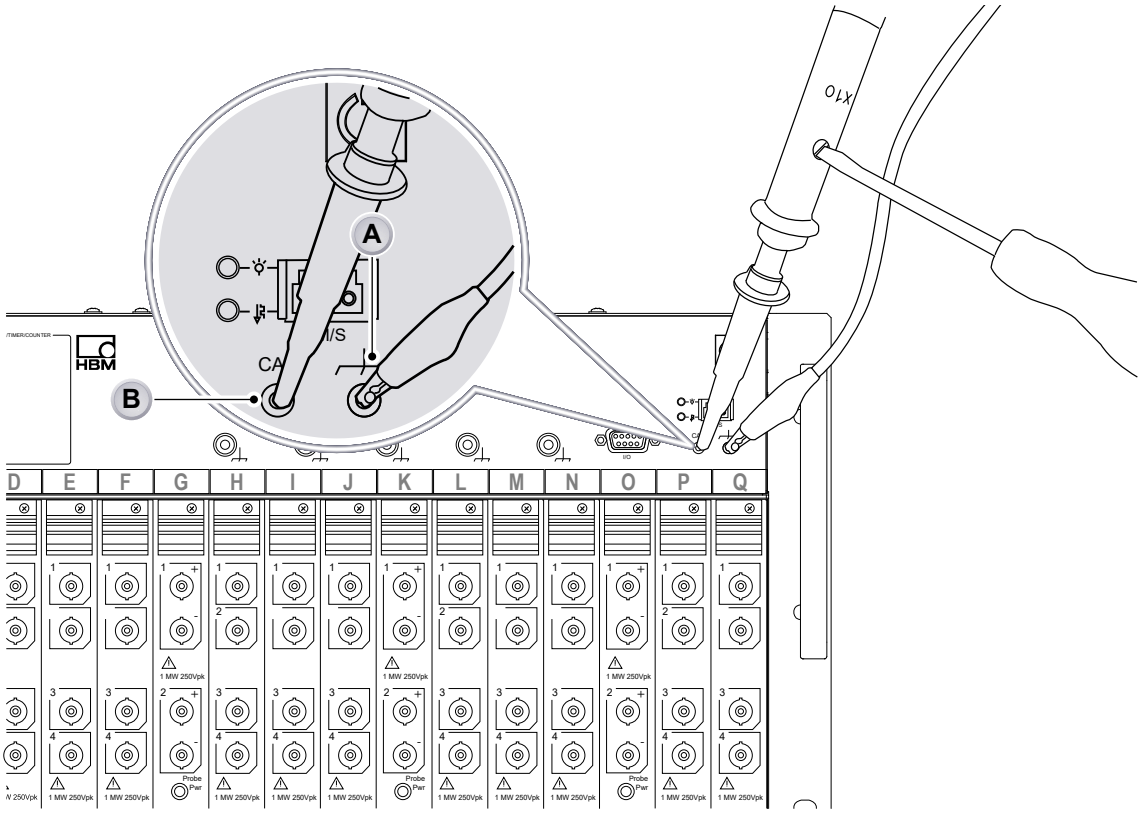


Figure 7.14: Probe calibration

A Probe GND

B Probe input

Set the trimmer of the probe so that the signal in Perception resembles the input signal.
Figure 7.15 below shows how the signal should look. When the trimmer is positioned incorrectly, undershoot or overshoot is seen in the signal.

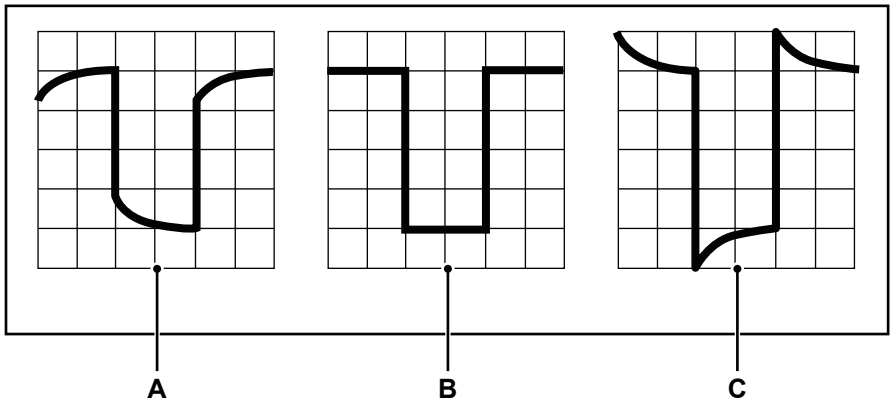


Figure 7.15: Trimming of response - Incorrect and correct waveform responses

A Incorrect - Undershoot

B Correct

C Incorrect - Overshoot

7.8 Digital Event/Timer/Counter

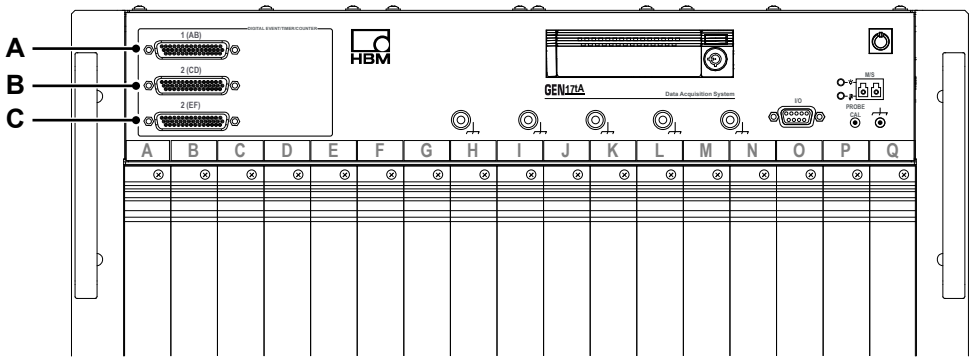


Figure 7.16: Digital Event/Timer/Counter

A Digital Event/Timer/Counter 1 (AB)

B Digital Event/Timer/Counter 2 (CD)

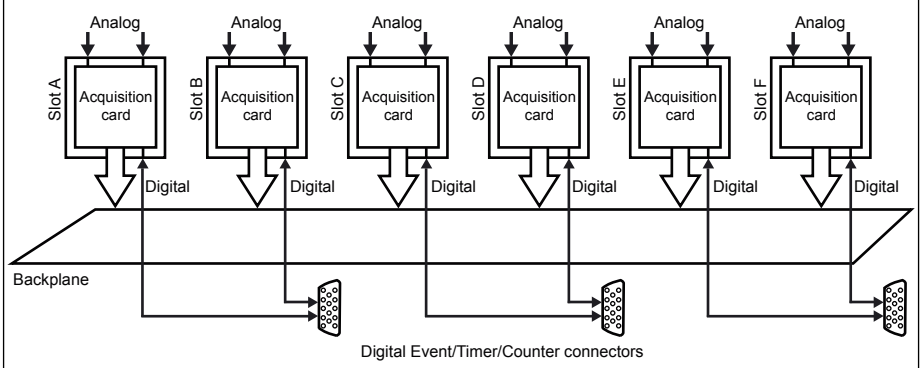
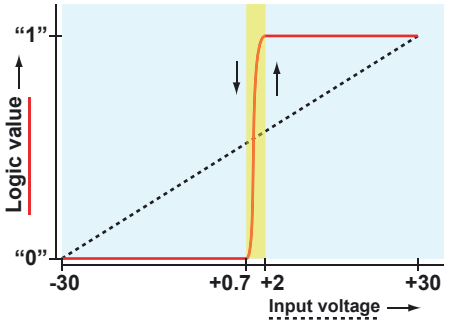
C Digital Event/Timer/Counter 3 (EF)

The GEN17tA mainframe comes with three Digital Event/Timer/Counter connectors. These connectors are internally connected to Slots **A** to **F** of the mainframe. Each Digital Event/Timer/Counter connector is wired to one pair of acquisition Slots; Connector 1 to Slots **A** and **B**, Connector 2 to Slots **C** and **D** and Connector 3 to Slots **E** and **F**.

- Acquisition card(s) installed in Slot **A** and/or **B** can use the inputs of the Digital Event/Timer/Counter Connector 1 (**AB**).
- Acquisition card(s) installed in Slot **C** and/or **D** can use the inputs of the Digital Event/Timer/Counter Connector 2 (**CD**).
- Acquisition card(s) installed in Slot **E** and/or **F** can use the inputs of the Digital Event/Timer/Counter Connector 3 (**EF**).

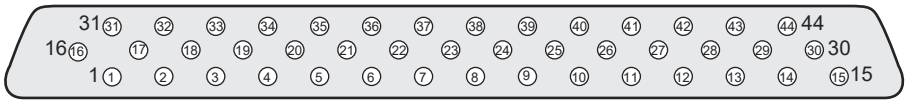
WARNING

Not all GEN series acquisition cards have support for the Digital Event/ Timer/Counter connector. Only the acquisition cards that have support listed in their specification sheet will be able to use this connector. (See "Model overview (Part 2)" on page 214 for more details).

Digital Event/Timer/Counter	
 **Figure 7.17:** Digital Event/Timer/Counter block diagram	
Number of connectors	3
Connector type	44 pin, female D-type connector, AMP HD-22 series (Tyco/TE connectivity: 5748482-5)
Cable connector type	44 pin, male D-type connector, HDP-22 series (Tyco/TE connectivity: 1658680-1)
Output power	
Voltage	5 ± 0.5 V DC
Maximum current	1 A to be shared by the three connectors: the sum of the currents on the connectors should not exceed 1 A
Event inputs	
Number of events	16 per card, two cards per connector
Levels	TTL Compatible, Low -30 V to 0.7 V, High 2 V to 30 V
 **Figure 7.18:** Logic threshold voltage levels	
Overvoltage protection	± 30 V DC

Digital Event/Timer/Counter	
Timer/Counter	
Number of channels	Two per card, two cards per connector
Functions	See specifications of acquisition cards that support these inputs in table "Model overview (Part 2)" on page 214
Outputs	
Number of outputs	Two per card, two cards per connector
Functions	See specifications of acquisition cards that support these outputs in table "Model overview (Part 2)" on page 214
Output levels	TTL compatible; 0 V < Low < 0.6V; 2 V < High < 5 V
Output resistance	49.9 Ω ± 1%
Maximum output current	50 mA, short circuit protected

Digital Event/Timer/Counter Connector Pin Assignment



PIN 1 - Event Input 1A & Reset Timer/Counter 2A
PIN 2 - Event Input 2A & Direction Timer/Counter 2A
PIN 3 - Event Input 3A & Clock Timer/Counter 2A
PIN 4 - Event Input 4A
PIN 5 - Event Input 5A
PIN 6 - Event Input 6A
PIN 7 - Event Input 7A
PIN 8 - Event Input 8A
PIN 9 - Event Input 9A
PIN 10 - Event Input 10A & Reset Timer/Counter 1A
PIN 11 - Event Input 11A & Direction Timer/Counter 1A
PIN 12 - Event Input 12A & Clock Timer/Counter 1A
PIN 13 - Event Input 1B & Reset Timer/Counter 2B
PIN 14 - Event Input 2B & Direction Timer/Counter 2B
PIN 15 - Event Input 3B & Clock Timer/Counter 2B
PIN 16 - Event Input 4B
PIN 17 - Event Input 5B
PIN 18 - Event Input 6B
PIN 19 - Event Input 7B
PIN 20 - Event Input 8B
PIN 21 - Event Input 9B
PIN 22 - Event Input 10B & Reset Timer/Counter 1B
PIN 23 - Event Input 11B & Direction Timer/Counter 1B
PIN 24 - Event Input 12B & Clock Timer/Counter 1B
PIN 25 - Event Input 13B
PIN 26 - Event Input 14B
PIN 27 - Ground
PIN 28 - Ground
PIN 29 - Ground
PIN 30 - Ground
PIN 31 - Event Input 15B
PIN 32 - Event Input 16B
PIN 33 - Event Input 13A
PIN 34 - Event Input 14A
PIN 35 - Event Input 15A
PIN 36 - Event Input 16A
PIN 37 - Event Output 2B
PIN 38 - Event Output 1B
PIN 39 - Event Output 2A
PIN 40 - Event Output 1A
PIN 41 - Ground
PIN 42 - Ground
PIN 43 - +5 V Power
PIN 44 - +5 V Power

For connectors supporting slot C/D and E/F replace A with C & E and B with D & F

Figure 7.19: Pin diagram for Digital Event/Timer/Counter connector

7.8.1 Isolated event adapter

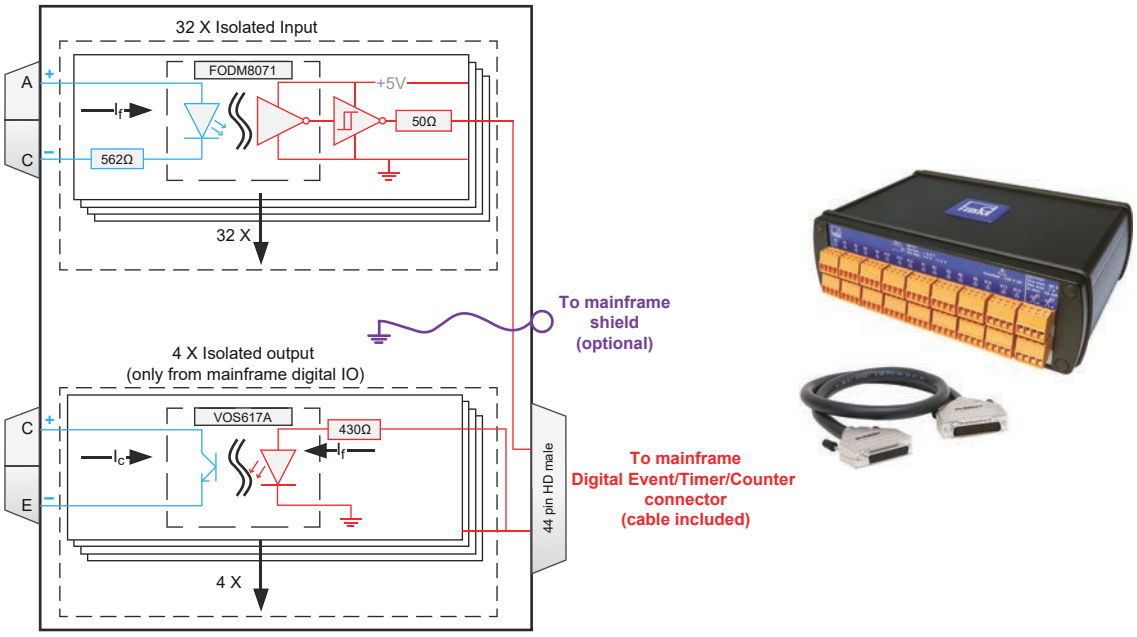


Figure 7.20: Block diagram and image

To isolate the Digital Event/Timer/Counter inputs a special adapter is available. It has a maximum 230 V RMS isolation spec and comes with a connection cable to directly connect the adapter to the mainframe.

The adapter isolates all input and output events and Timer/Counter pins.

See “G070A Torque/RPM adapter" and "G072 Isolated Digital Event Adapter" data sheets for detailed usages and specifications.

7.8.2 Torque/RPM adapter

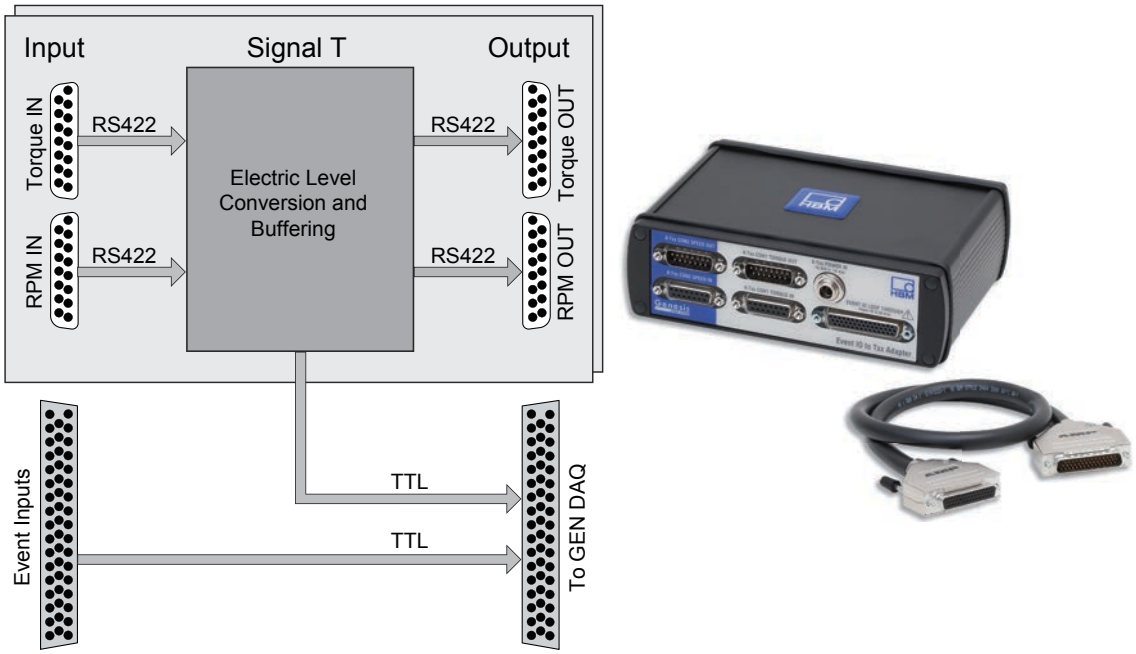


Figure 7.21: Block diagram and image

HBM's Torque and RPM sensors come standard with RS422 digital output signals. As the GEN series Digital Event/Timer/Counter inputs are TTL inputs, signal need to be converted to make both side able to work together.

The Torque/RPM adapter is designed to both perform the signal conversion as well as make sure the connectors used support standard Torque and RPM cables.

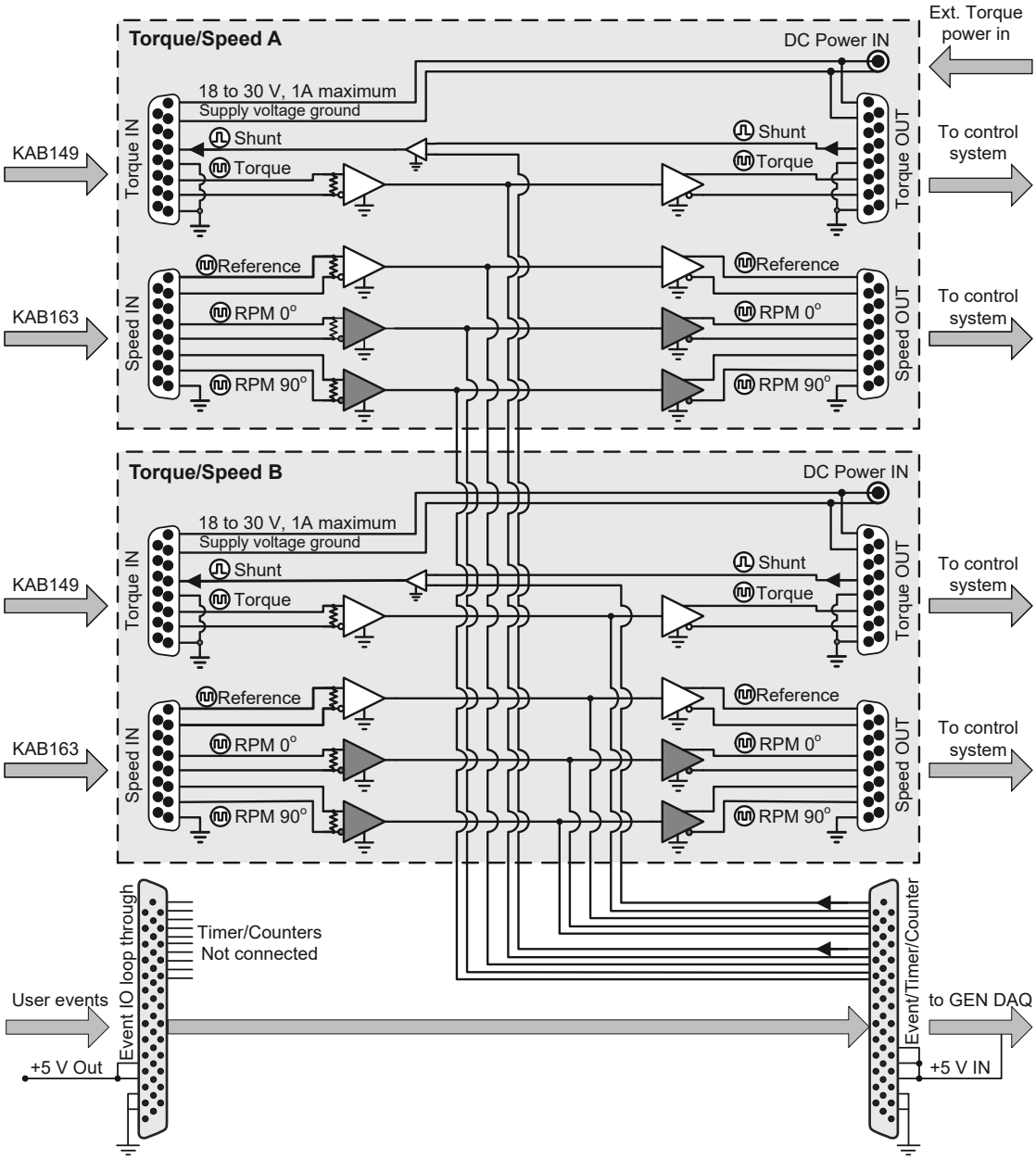


Figure 7.22: Block Diagram Torque/RPM Adapter

Using this adapter T12, T40 and alike torque transducer can be directly connected to the GEN series mainframe without additional need to build your own cables.

The adapter also supports a so called T-function. If the need exists to connect the output of the Torque/RPM sensor both to a GEN series mainframe and any other receiving system, the T-function output renews the original signal with an RS422 transmit buffer. This setup garantees a point to point connection required for proper RS422 usage.

7.9 Accessing the CPU section

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN17tA system, its connections or a plug-in card.

CAUTION

The GEN17tA Data recorder is factory-calibrated as delivered to the customer. Swapping, replacing or removing of cards may result in minor deviations to the original calibration. The GEN17tA system should be tested and, if necessary calibrated, at one-year intervals or after any major event that may affect calibration. When in doubt, consult the local supplier.

CAUTION

Heatsink and other parts may be hot when removed just after switch-off.

To remove a card:

1 Power off the GEN17tA system and remove the power input cable.
2 Disconnect all cables from the acquisition cards.

3 Using a torx screwdriver remove all screws from the rear cover plate.

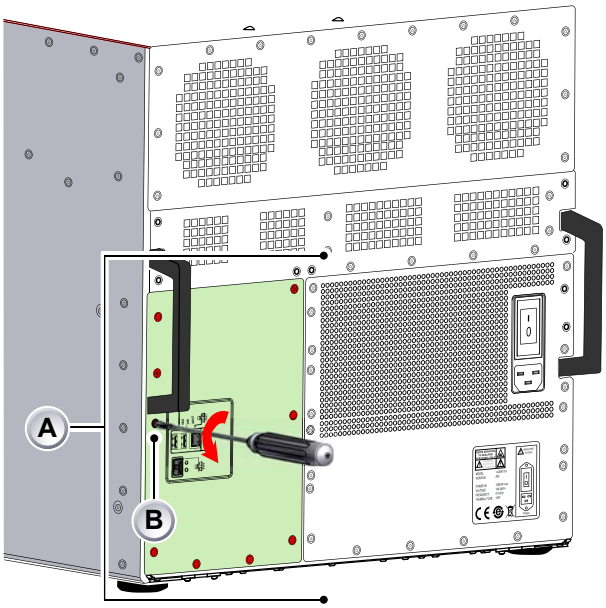


Figure 7.23: Remove rear cover plate screws

A Rear cover plate

B Screws

4 Remove all indicated screws from the GEN17tA.

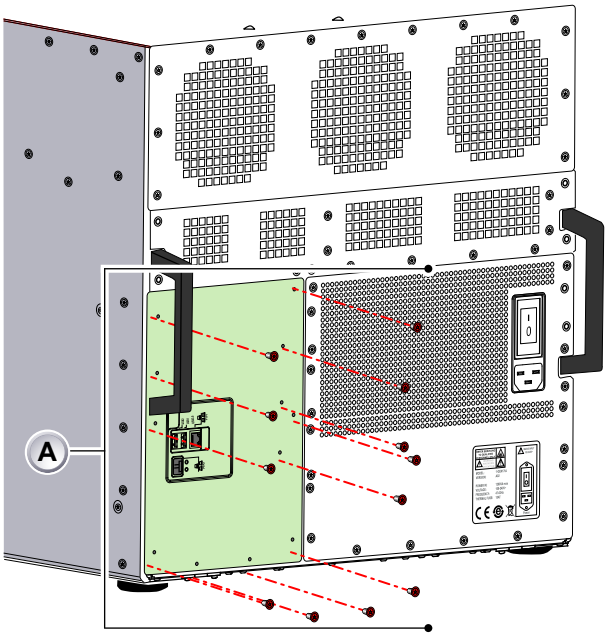


Figure 7.24: Remove all rear cover plate screws

A Rear cover plate

5 Remove the rear cover plate of the GEN17tA.

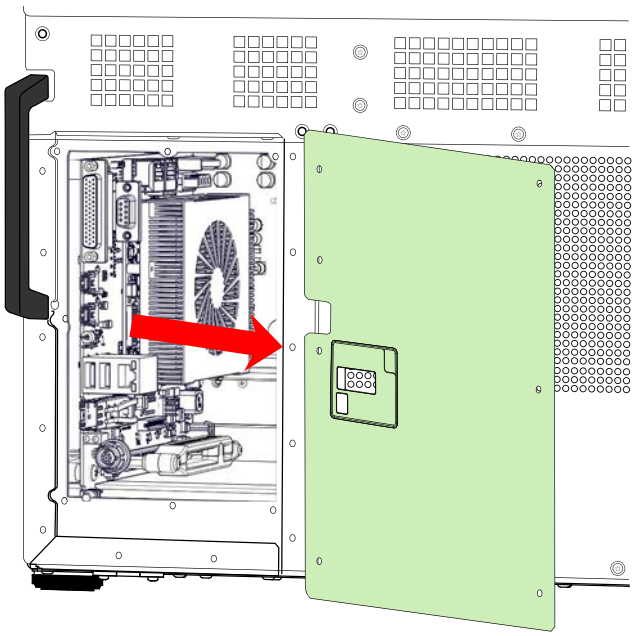


Figure 7.25: Remove cover plate

6 Close the GEN17tA CPU section in reversed order.

7.10 Air filter replacement

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN17tA system, its connections or a plug-in card.

To replace the air filter:

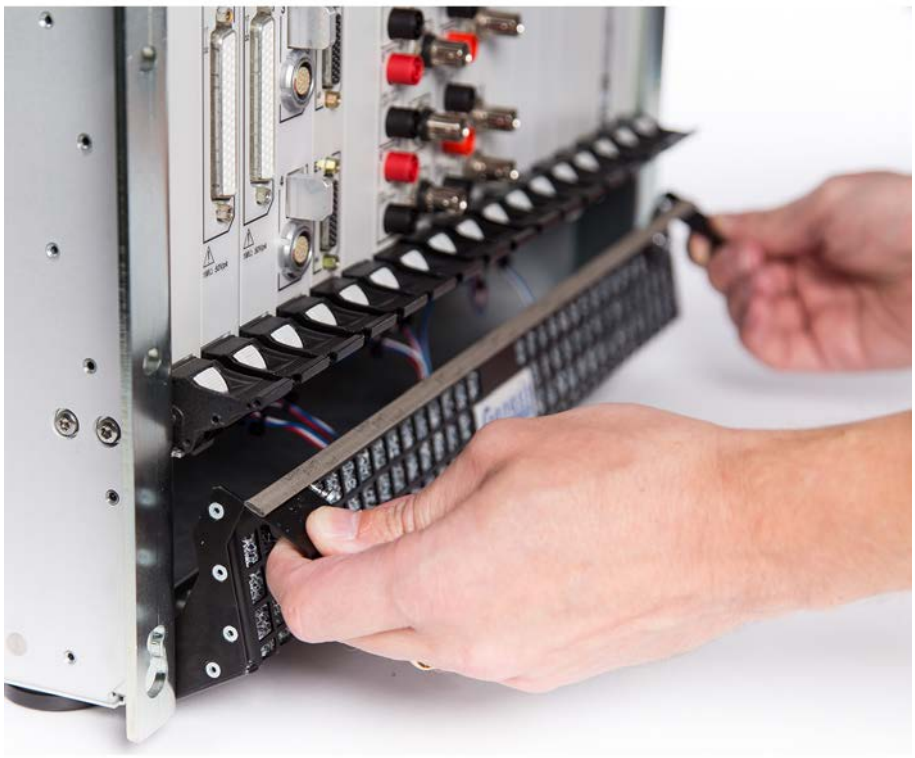
1. Power off the GEN17tA system and remove the power input cable.
2. Disconnect all cables from the acquisition cards.
3. Remove the screws from the air filter locking bracket.

Figure 7.26: Unlock screws on the air filter access panel

A Screw on filter access panel (left side)

B Screw on filter access panel (right side)

4 Pull down the levers on both sides of the bracket and pull the bracket outwards.



5 Remove the inside screws of the bracket that hold the filter down.

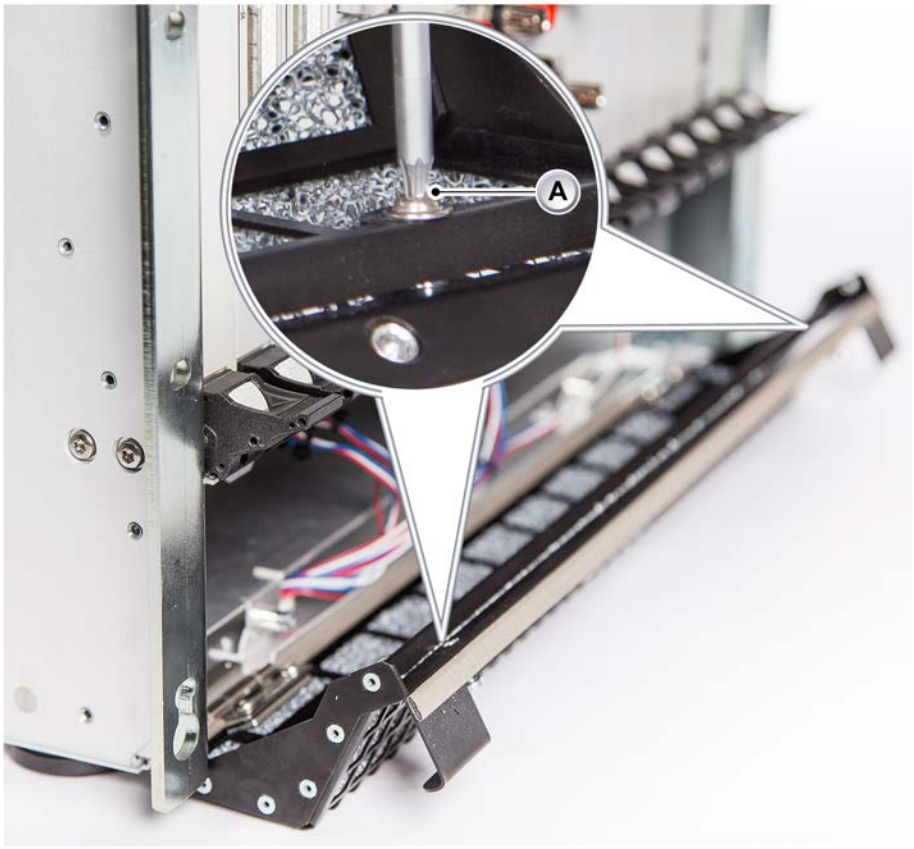


Figure 7.27: Screws inside the bracket

A Screws inside the bracket (left side/right side)

6 Lift the inside bracket and remove the air filter.

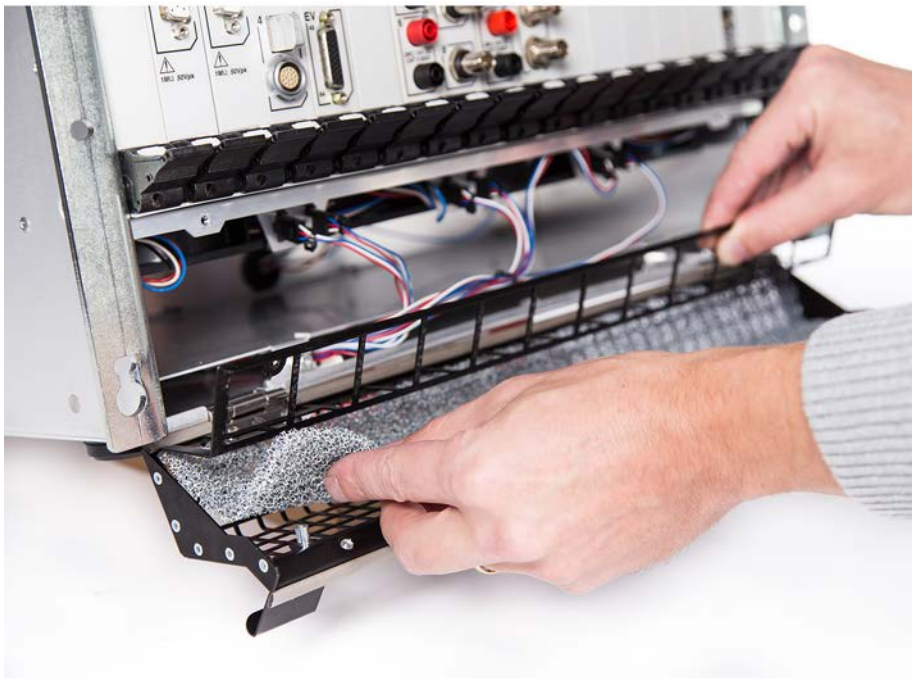


Figure 7.28: Removing the air filter

7 Insert the new air filter and close the GEN17tA in reverse order.

8 Getting Started

8.1 GEN17tA control

The GEN17tA can only be controlled by Perception V6.72 or higher.

Standby

On GEN17tA, the standby button is located on the front panel. When this button is pressed, the instrument state toggles between operating and standby mode. In standby mode, some power is consumed and the instrument is NOT disconnected from the AC supply. To switch off the instrument completely from the mains power, switch the ON/OFF switch at the rear to OFF position or disconnect the mains power cable from the instrument.

HINT/TIP

After power on, the GEN17tA typically plays a three-tone sound as soon as it is operational. During the first 100 seconds after power on, the system will not power off when the standby button is pressed again.

HINT/TIP

When the system does not power off when the standby button is pressed, keep the standby button pressed for four seconds to enforce a hard power off. If data recording to the system built-in disks is active, the last few seconds of recorded data might be lost. Only use this forced power-off method when data loss is acceptable or after waiting several minutes to allow the system to first save its recorded data to disk.

Figure 8.1: Power button

A Standby button - Press to power on or off, or hold for more than four seconds for a forced power off and integrated Power LED - is illuminated when power is on.

8.2 Connecting GEN17tA to Perception

To control, set up and use GEN17tA, Perception software needs to be connected to the GEN17tA.

1 Connect the GEN series system to the Perception PC and start Perception.

Note *Perception can be adapted to meet personal wishes. The Getting started sequence is described using the default installed selections.*

2 The user mode selection dialog appears (see Figure 8.2):

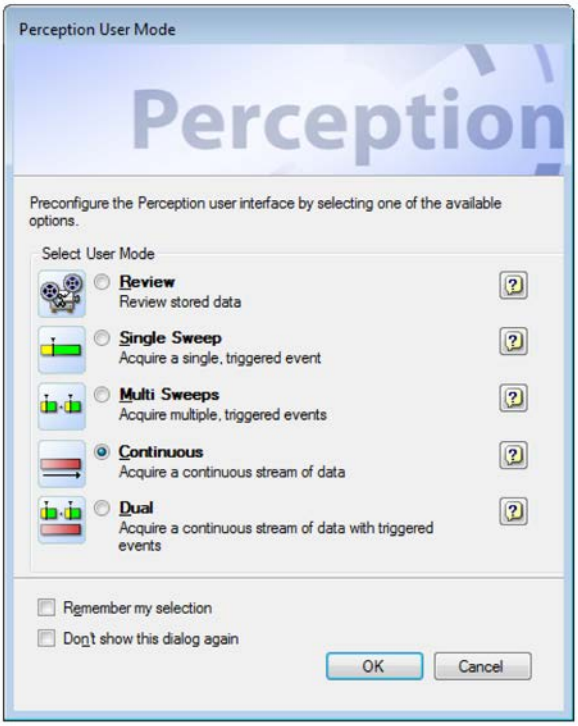


Figure 8.2: Perception User Mode dialog

User modes are explained in the Perception Data Acquisition Software manual. For this section about getting started, the system defaults are used.

Click **OK** to continue.

3 Perception will continue to start. To continue, Perception will ask which job it should perform (see Figure 8.3):

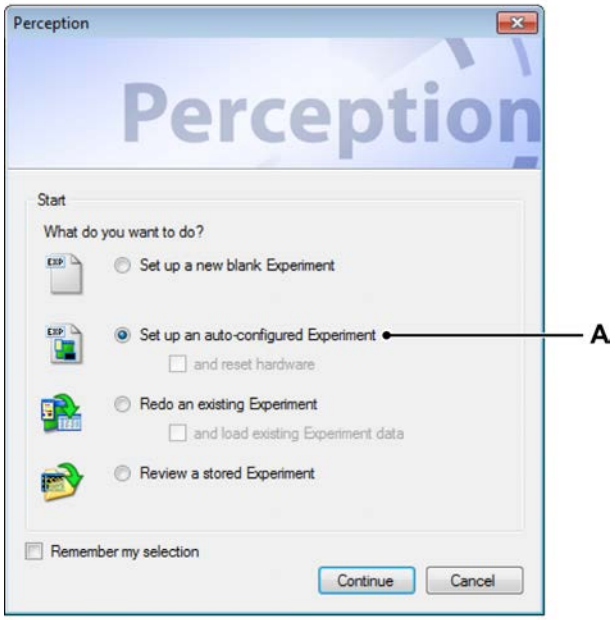


Figure 8.3: Perception job dialog

A Set up an auto-configured Experiment

In the dialog, select:
Set up an auto-configured Experiment Let Perception search for connected acquisition hardware and create a default layout. Optionally you can select **and reset hardware**. When this option is selected, Perception resets the hardware and restores the factory default settings in the mainframe.
Click **Continue**. This will show a selection of mainframes (see Figure 8.4) or automatically make a selection if only one mainframe is available.

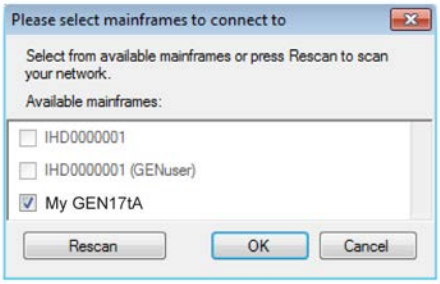


Figure 8.4: Mainframe selection

From the list of available mainframes, select the mainframe(s) required for the experiment. Click **OK** to continue.

When using the mainframe for the first time, the IP address should have been dynamically assigned. This ensures that the IP address matches the PC if the PC network settings are also configured dynamically. However, if the mainframe or PC is configured to a static IP-address, the two networks may not match. The list of available mainframes shows every HBM mainframe supported by Perception, even if network settings do not match.

Network conflict

If a network setting conflict is detected, this conflict must be resolved before the connection can continue. The Perception Connect dialog appears (see Figure 8.5).

Initially, the dialog appears with the settings currently used by this mainframe, i.e. the ones containing the conflict. Make the changes required to resolve the conflict and click **Continue** to complete the connection process.

Note *If the conflict has not been properly resolved, this is indicated in the diagnostics overview. The hardware is still shown in **Unused Hardware** in this case. By connecting to the hardware again, the Perception Connect dialog will appear again.*

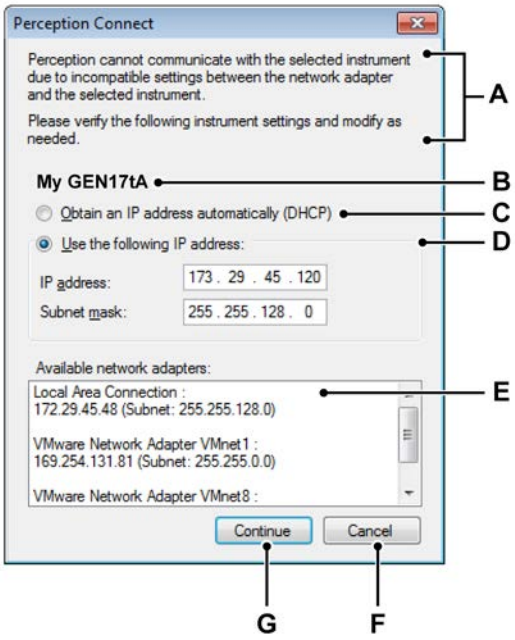


Figure 8.5: Perception Connect dialog

A **Description** of the connection and/or configuration problem encountered by Perception.

B **Mainframe name** The name of the mainframe on which the problem was encountered.

C **DHCP** To configure for dynamic addressing (recommended default), click for the mainframe to obtain an IP address automatically, and then click **Continue**.

D **Fixed IP address** To configure for static addressing, click **Use the following IP address**, and in **IP address** and **Subnet mask** type the IP address and subnet mask to match the settings of the network adapter installed in the PC running Perception

E **Network adapter information** List of available network connections of the PC running Perception. In Windows®, check the detailed settings of the network adapter. Make sure that the network adapter settings in the mainframe match the settings in the PC.

F Click **Cancel** to stop the connection process for this mainframe.

G Click **Continue** to apply the changes and to continue the connection.

If a reboot of the system is required to apply the new network settings, this will be done automatically. The progress window (see Figure 8.6) will close automatically when the mainframe has been rebooted.

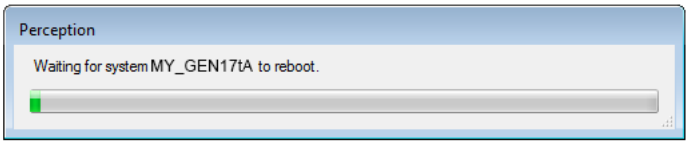


Figure 8.6: Perception progress indicator for mainframe reboot

9 Acquisition and Storage

9.1 Introduction

Data acquisition hardware within the GEN17tA is based on the concept of a **recorder**. A recorder consists of a number of acquisition **channels** that share the same basic recording parameters: sample rate, sweep length and pre- and post-trigger length. Usually, a single recorder is physically identical to a single acquisition card. Multiple recorders can be placed in a single **mainframe**. The mainframe is the housing for the recorders. The mainframe provides the power and includes the interface for the local area network. A mainframe has its own network address (IP address).

For the sake of simplicity, we will consider a single channel in this section.

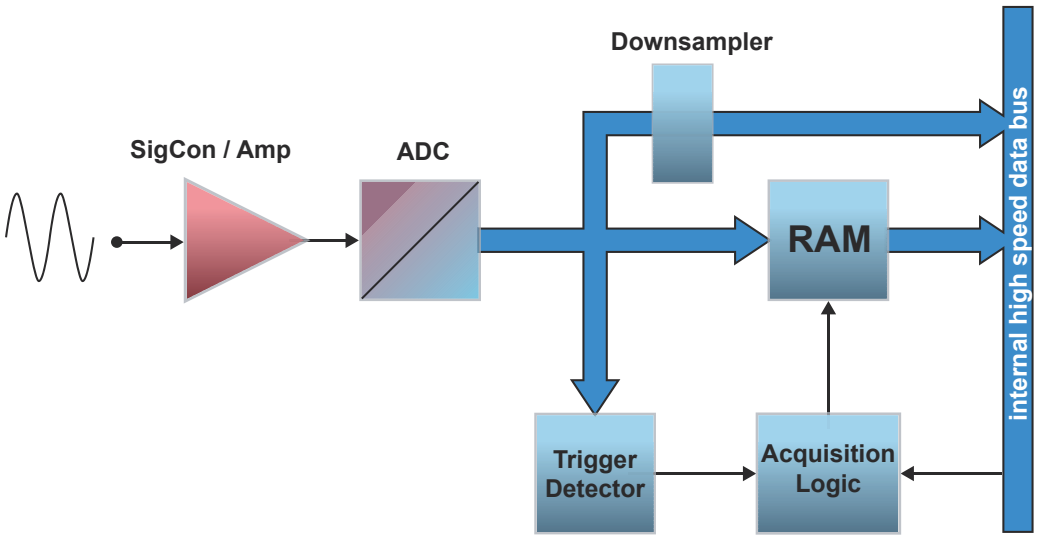


Figure 9.1: Simplified generic single channel data acquisition system

In the GEN17tA data acquisition system and the Perception software that goes with it, a separation is made between acquisition and storage. **Acquisition** is the act of digitizing analog data and making it available for monitoring or storage. **Storage** is the actual archiving of digitized data. **Recording** (verb) is acquisition + storage.

9.2 Recording

Since many of the features that are described here are controlled from within the Perception software, it is advised to read this section in combination with the corresponding sections in the Perception manual.

The GEN17tA/Perception combination provides the following acquisition controls:

- **RUN** The run command starts recording of data. Now the recorder(s) record(s) data until a stop command is issued. This stop command can be manually or triggered (when in sweep storage mode).
- **STOP** To stop or abort a recording.
- **PAUSE** This mode has two options:
  1. When no recording is active, it places the recorder in the pause or stand-by mode. Although the recorder is digitizing, no data is stored in memory or disk. This is useful for monitoring purposes.
  2. When a recording is active, it places the recorder in a hold mode. Although the recorder is digitizing, no data is stored in memory or disk. At the point when RUN is selected, the current recording continues. When STOP is selected, the recording is finished.

These recording controls are combined with the various storage modes.

9.3 Storage

The GEN17tA provides two storage paths, as shown in Figure 9.1 on page 121:

- Store data in on-board RAM at high speed
- Transfer data directly at reduced speed to the controlling PC or (when installed) to a local disk.

In addition to these storage paths, the GEN17tA provides two fundamental storage modes:

- **Sweeps:** data storage of predefined length. Sweeps typically use a trigger to define the start and end of the sweep.
- **Continuous:** data storage of an undefined length. The end of this storage mode can be defined by various events, as described later.

When data is stored, this data is organized in recordings. A recording is defined as all the data that has been stored between the start of acquisition (Record command) and the end of acquisition. The end can be defined in various ways. A recording can have one or multiple sweeps, a continuous data stream or a combination of both.

In Perception, a recording is organized as a PNRF file (Perception Native Recording File).

CAUTION

The GEN17tA RAM is volatile. Therefore, the acquired sweeps will need to be transferred to the PC for archiving.

The storage mode defines how data is digitized and saved. The continuous storage mode stores all data. The sweep storage mode stores only the sweeps. However, the resulting file - or recording - will be different for the various storage modes.

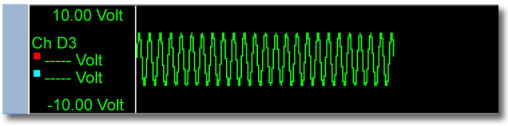


Figure 9.2: Run - Storage: Continuous

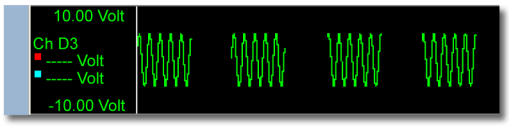


Figure 9.3: Run - Storage: Sweeps only

The basic storage modes can be combined to create more advanced storage modes:

Dual In this mode, sweeps and continuous data are stored. Therefore, the end result is a recording that comprises the higher speed sweeps as well as the lower speed continuous data between the sweeps.

9.3.1 More on sweeps

Figure 9.1 "Simplified generic single channel data acquisition system" on page 121 is a very simplified block diagram of the general concept of a single channel digitizer. Once the analog values have been converted by the ADC into binary codes, they are stored in successive order in a buffer memory, the on-board RAM. This memory can be divided into multiple segments to allow for the storage of multiple sweeps.

If the last storage location of a segment is filled and acquisition is still taking place, the first storage location is overwritten with a new sample, followed by the second storage location, etc.

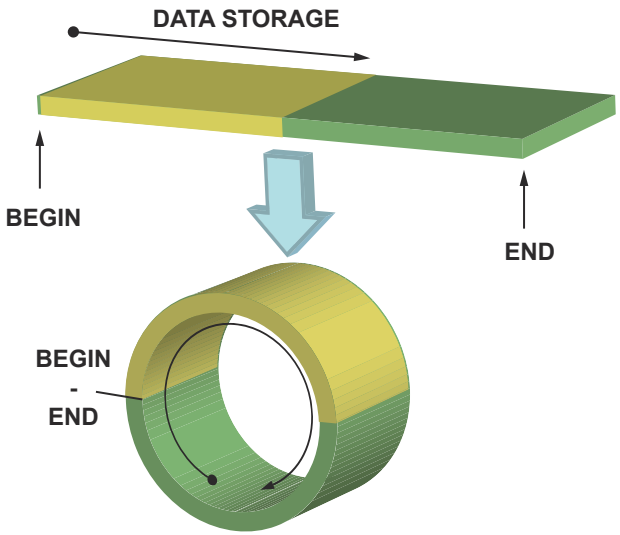


Figure 9.4: Ring buffer operation of memory

The physical memory therefore forms a ring buffer, into which information can be continuously added (see Figure 9.4). This process of filling the ring buffer memory terminates only when the recording logic indicates that the sweep must be ended. Once the sweep recording has stopped, the content of the buffer memory becomes available to the control PC for processing. This is also called **circular recording**. Sweep data is automatically moved from on-board RAM memory to the recording file.

9.3.2 Pre-trigger sweeps

As we have seen, data emerging from the ADC is stored in the buffer memory. When recording, the memory is continuously refreshed with new sample values, until storage is halted. The information available in the memory is a **history** of the recorded signal up to the moment of “end-of-sweep”. The extent of this history depends on the sample rate and the data storage capacity (length) of the memory. If we assume a memory length of 40 000 samples and a sample rate of 10 000 samples per second, then the time window of the history will be:

(EQ 1)

$$t_{window} = \frac{40000}{10000} = 4 \text{ seconds}$$

Storage into the ring buffer can be stopped only by a “stop” signal from the recorder. This signal is called the "trigger". For more information on triggering, please refer to chapter “Digital Trigger Modes” on page 130.

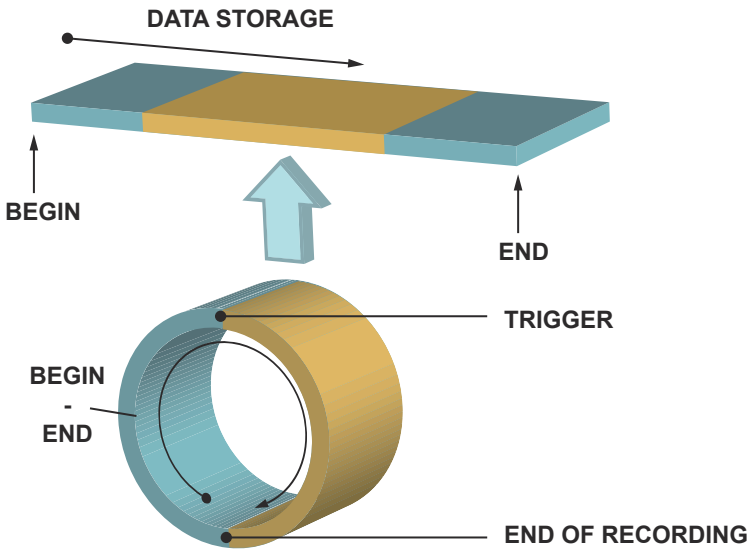


Figure 9.5: Ring buffer with trigger and end-of-recording

Since the trigger stops the storage, all stored information is termed pre-trigger information. When storage stops because the acquired signal has met a trigger condition, only pre-trigger information is available - information recorded before the signal met the trigger condition.

Figure 9.6: Full pre-trigger storage: pre-trigger = 100%

More often, one is interested in what happened just before and after the condition was met. To achieve this aim, a delay is introduced. Once the trigger condition is met, storage is stopped - not immediately, but only after a programmable delay counter has counted out. The memory now contains pre-trigger information and post-trigger information.

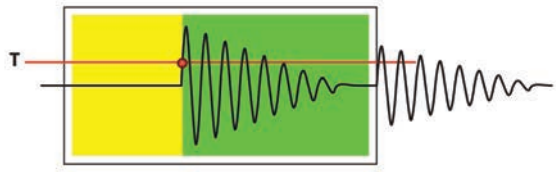


Figure 9.7: Pre-trigger / post-trigger storage: 0% < pre-trigger < 100%

The usage of a variable delay counter allows for a user-definable pre-trigger length. The length of the pre-trigger segment equals the length of the memory segment minus the delay. When the length of the delay is equal to, or exceeds, the length of the memory segment, only post-trigger information is available.

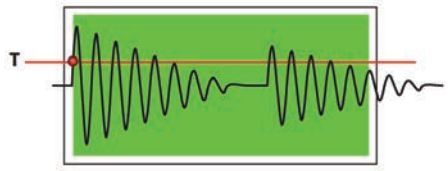


Figure 9.8: Full post-trigger storage: pre-trigger = 0%

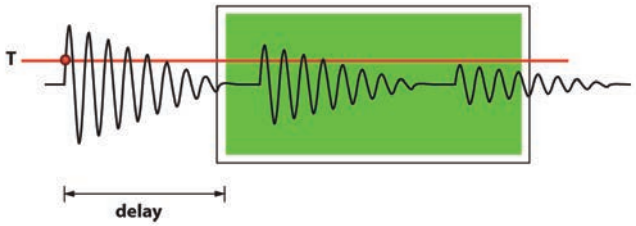


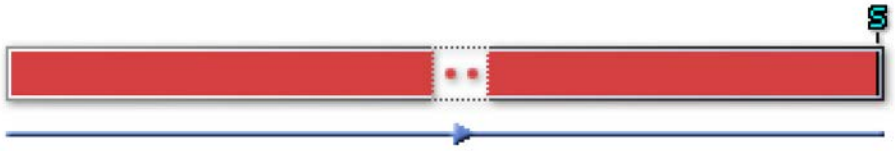
Figure 9.9: Delayed trigger storage: pre-trigger < 0%

9.3.3 More on continuous data storage

The most important difference between continuous data storage and sweeps in a GEN17tA is the fact that sweeps are stored in on-board volatile RAM, while continuous storage takes place on the controlling PC's hard disk (or local hard disk when installed).

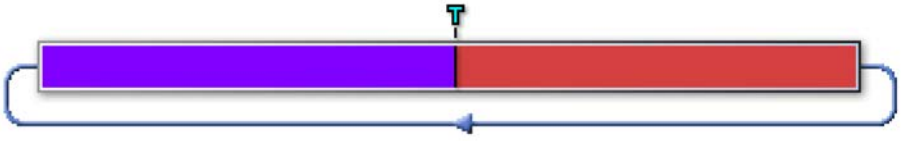
The continuous data storage provides three modes:

- **Standard** The continuous mode is standard when storage is started and is stopped manually as depicted below:



- **Circular** The continuous mode is circular when storage is started and stopped manually AND the length of the buffer is defined. Operation is similar to standard sweep storage, but storage is on the PC hard disk and not in volatile memory. In this mode, the **lead-out** is specified which is basically the same as the post-trigger segment in a sweep recording.

- **Stop on trigger** The continuous mode operates like a pre-trigger sweep, but with storage on the PC hard disk, not in volatile memory.



9.4 Time base

The power of modern data acquisition techniques is achieved by *digitizing* analog information. Digitizing is the conversion of the instantaneous value of an analog signal (static or dynamic) into a numeric value. When the signal varies, *sampling* the instantaneous amplitude at sufficiently rapid intervals converts this signal into a series of numbers that can represent the original analog signal.

Real-time sampling and time base

Real-time sampling is a straightforward sampling method and is the only method to record non-periodical phenomena. In this method, the intervals between the samples taken of the original signal are as short as possible and equidistant. If the sample rate used is high enough, the original signal can be reconstructed without any additional processing.

The sample rate is determined by the time base: the time base is a clock that generates pulses used to drive the A-to-D Convertor.

Sample rate values are base 10, e.g. 1 MHz, 100 kHz, 50 kHz, 2.5 Hz, etc. These values are derived from a main oscillator that operates at a base 10 frequency, e.g. 1 MHz.

10 Digital Trigger Modes

10.1 Introduction

Within the GEN17tA data acquisition system, every channel is equipped with a **trigger detector**, which makes it possible to record just the phenomenon of interest, instead of having to search the full memory to find it. The trigger detector gives the system the power to capture elusive, short and unpredictable events. It determines how easily the event of interest can be extracted.

The word **trigger** has a dual meaning in recording techniques. In the active sense, the instrument has triggered, indicating that the instrument has responded to a certain stimulus. In the passive sense, as in trigger point, it indicates the point (in time) when the instrument has triggered. In both cases, trigger refers to a known, pre-defined situation.

The trigger can be generated in several ways:

- by the user, i.e. **manually**
- using an externally applied signal, i.e. **external** trigger
- when the acquired **signal** complies with a certain condition: the trigger condition. Each channel within a recorder can trigger this recorder.

For transient recording, this last option is of great importance. To a large extent, the trigger facilities determine the application capabilities of the data acquisition system, i.e. how effectively the data can be captured.

In this chapter, the trigger capabilities of the GEN17tA data acquisition system will be explained in full detail.

Each channel within a recorder can trigger this recorder. This functionality is realized by combining all channel triggers into a logical OR combination. When one of the channels (or multiple channels) generates a trigger, the complete recorder triggers. Each channel's trigger detector can be switched off or set to one of the modes described in this chapter.

Note *This chapter describes all GEN series trigger options. However, not every acquisition card will support each described option. Check the specifications of each acquisition card to find out what options are supported for this specific card.*

10.2 Understanding digital triggering

Technically speaking, there are two approaches to determine the known, pre-defined situation of the signal: analog or digital.

Each channel in the GEN series system is equipped with a digital trigger detector. Digital triggering has the benefit of stable vertical reference levels, no horizontal jitter, and not depending on signal frequency.

A disadvantage of a digital trigger detector is its inability to detect events that occur between two consecutive samples. This does not usually interfere with normal operation because the event is not recorded anyway.

10.2.1 Digital trigger detector

Figure 10.1 shows a simplified diagram of a **single-level** digital trigger detector. Digitized values coming from the ADC are fed into an Arithmetic (and) Logic Unit – ALU. The value that comes out of the ALU is then referenced against a preset value (trigger level). The result can be either positive, i.e. the value is larger, or negative, i.e. the value is smaller. Based on this information, the level crossing detector verifies if a level crossing in the correct direction has occurred and, if so, sends out a trigger.

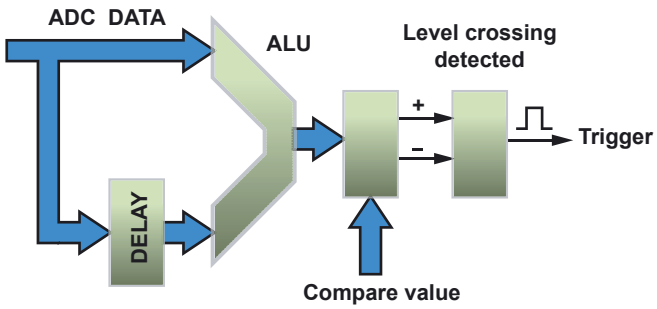


Figure 10.1: Single-level trigger detector

The delay register in front of the ALU is used to compare the ADC value with “older” values. This means that triggering does not react to specific levels, but to the differential signal or **slope**.

As explained later in this chapter, a signal must actually cross the preset level. This is to avoid erroneous triggering due to a small amount of noise on the signal. To make the trigger detector even more stable when noisy signals are used, the single-level trigger detector has been expanded with a **hysteresis**. After the level detector signals a level crossing, a new level crossing will only be signaled if the input signal first goes outside the hysteresis band and then returns to the trigger level.
For the advanced trigger modes, the single-level trigger detector with programmable hysteresis has been implemented twice to provide a **dual-level** trigger detector. Levels are usually referenced as *primary* trigger level and *secondary* trigger level.

10.2.2 Valid trigger conditions

Trigger detection is based on level crossing. A signal has to cross a specified level to be considered a trigger condition. As a consequence, reaching the required level is not a valid trigger condition. Since trigger detection is digital, inter-sample analog values are omitted.

In the following graphs, these conditions are shown.

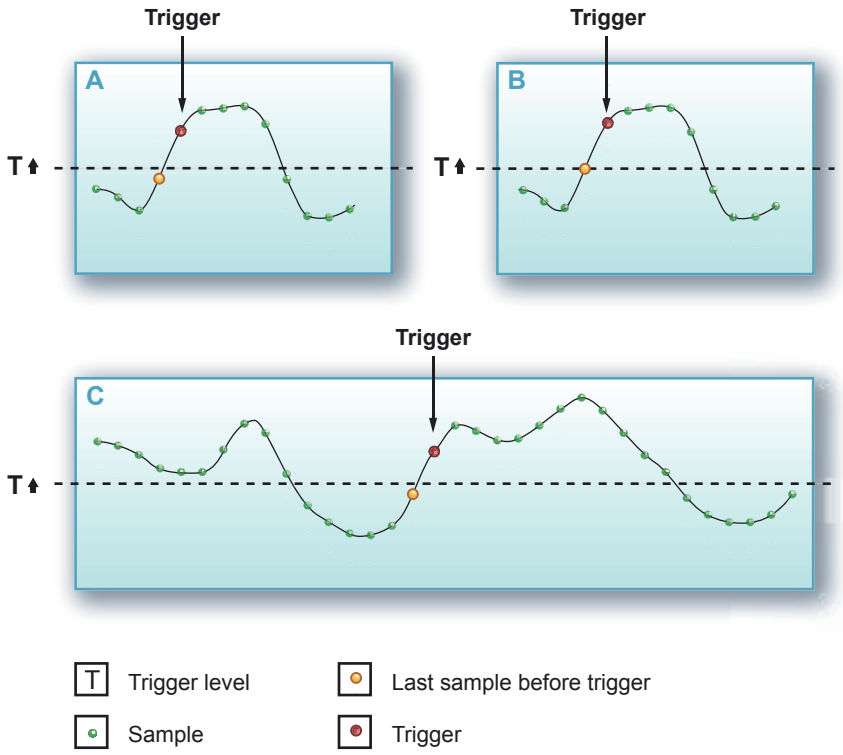


Figure 10.2: Level crossing detector

Figure 10.2 shows the basic trigger mode with a specified level (**T**) and a level crossing in a positive direction. In Figure 10.2 **(A)**, the trigger occurs on the first sample after the level crossing. Figure 10.2 **(B)** shows the situation in which a sample equals the set level. Trigger does not occur until a sample is actually above the required level.

Since the trigger detector requires a level crossing, no trigger occurs when a signal is above the set level when recording starts. This is depicted in Figure 10.2 **(C)**.

Figure 10.3 shows the influence of the additional hysteresis. Fundamentally, everything is the same as described earlier. The only difference now is that a second level (H) is used to “arm” the level trigger detector. Otherwise stated, the trigger level has been expanded to be a trigger zone that spans multiple levels.

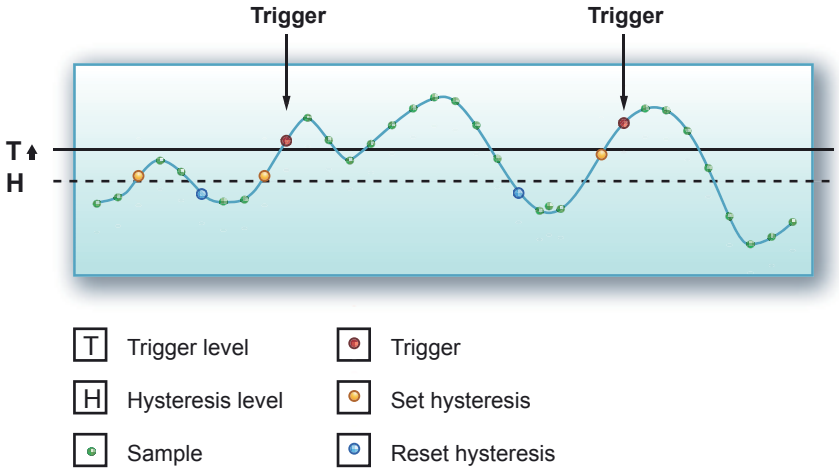


Figure 10.3: Trigger level hysteresis

10.3 Trigger modes

Using the various trigger modes, GEN17tA data acquisition system is expanded to an extremely versatile transient recorder. The trigger circuits may be configured to trigger on many types of phenomena. In this section, the different trigger modes and their extensions are discussed in detail.

10.3.1 Basic trigger mode

The basic trigger mode can be compared to the trigger mode available when using an analog trigger detector, for example as found on a classic scope.

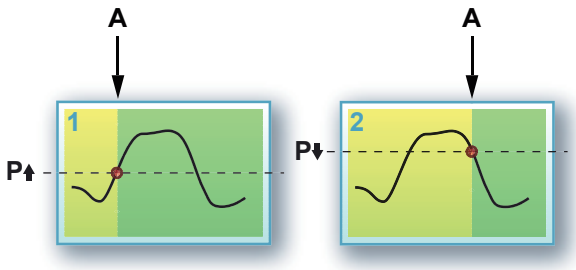


Figure 10.4: Basic trigger mode

A Trigger

In this mode, a single-level trigger detector is active, the primary level. As mentioned previously, the signal needs to actually cross the preset level. Both the level and direction of crossing can be selected.

Relevant settings for this mode:

- Mode: basic
- Primary level: any value within the input range
- Direction: positive or negative
- Hysteresis: any relevant value

10.3.2 Dual trigger mode

In dual trigger mode two detectors are active and working simultaneously: the primary level **P** and the secondary level **S**. With two levels, it is possible to define a range that the input signal must be within. As soon as the signal becomes larger than the upper level or smaller than the lower level, the detector generates a trigger. By inverting the slopes of both detectors, the trigger is generated when the signal returns into the specified range.

Figure 10.5 shows the various possibilities.

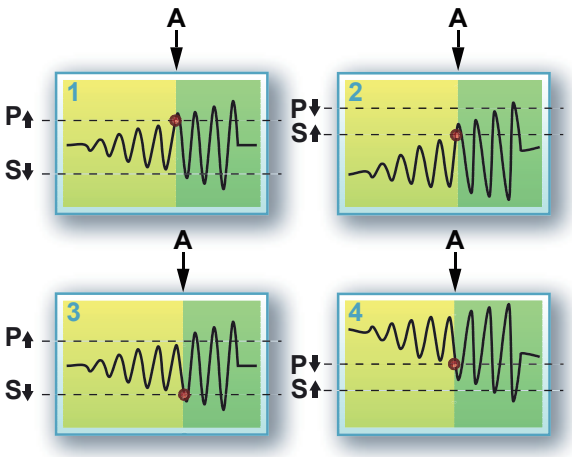


Figure 10.5: Dual trigger mode

A Trigger

Any value for each level and the slope of the primary level can be selected. The slope of the secondary level is automatically set to the opposite direction.

Diagrams **1** and **3** show a signal that exits the range. Diagrams **2** and **4** show signals that enter the range.

Relevant settings for this mode:

- Mode: dual
- Primary level: any value within the input range
- Secondary level: any value within the input range
- Direction: positive or negative for primary level; secondary level is automatically set to the opposite direction
- Hysteresis: any relevant value is used for both levels.

10.3.3 Trigger qualifier

The trigger detectors of a channel can also be used as qualifiers. A trigger qualifier is a situation that enables (arms) the recorder trigger features. The recorder trigger features are a combination of various channel, external, between-recorders and other trigger options.

There are two qualifier modes:

- Basic single-level qualifier. The level detector operates identical to "Basic trigger mode" on page 135.
- Dual-level qualifier. The level detector operates identical to "Dual trigger mode" on page 136.

When in qualifier mode, the output of the trigger detector is sent to a qualifier line of the recorder trigger logic. For more information on the recorder trigger features, please refer to "Recorder and system trigger" on page 138.

10.4 Recorder and system trigger

The trigger modes and features described so far are channel-based. Each analog channel within a GEN series system has a digital trigger detector. The trigger signals of all channels of a single recorder are combined through a logical OR to generate a combined trigger. This trigger can be combined with an external trigger and qualifiers. The final result is a recorder trigger. The triggers that are generated by individual recorders can be distributed to other recorders and mainframes.

The following simplified diagram is from the Perception software and shows the building blocks that make the complete recorder trigger logic. Please note that not all features may be available depending on the exact hardware used.

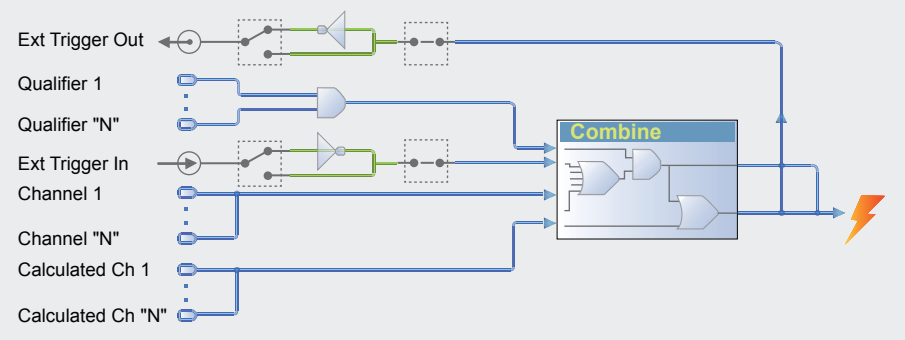


Figure 10.6: Recorder trigger logic

The heart of the recorder trigger logic is the “Combine” block. All trigger sources come together here. The trigger sources can generate a recorder trigger, depending on their settings, However, this can be blocked by qualifiers. If one of the qualifiers is not armed, no recorder trigger can be generated.

- **Channel 1 through N:**These are the channel triggers as described above. Please refer to chapter “Introduction of Digital Trigger Modes” on page 130.
- **External Trigger In:** This is an external trigger signal that is mainframe-related: The input connector is placed on the mainframe controller. Used to select rising or falling edge, all input cards in the mainframe use the same edge. Each input card can select to use the external trigger as a trigger source.
- **Qualifier 1 through N:** hese are the qualifiers as described above: Please refer to chapter "Trigger qualifier" on page 137.

- **External Trigger Out:** The recorder trigger can be used to send a trigger signal to the outside world. The output connector is placed on the mainframe controller. Used to select active High or Low level output, all input cards in the mainframe use the same output level. Each input card can select whether to send the trigger to the external trigger output.

10.5 Channel alarm

Each channel has the capability to generate an alarm. An alarm situation is detected with a basic dual level detector.

There are two alarm modes:

- Basic single-level alarm. The alarm line is active for as long as the signal exceeds the level in the specified direction. For more information on the level comparator, please refer to "Basic trigger mode" on page 135.
- Dual-level alarm. The alarm line is active for as long as the signal exceeds one of the two levels in the specified direction. For more information on the level comparators, please refer to "Dual trigger mode" on page 136.

The output of the alarm detector is sent to an alarm line and combined (OR-ed) with alarm conditions of the other channels and recorders. The result is available as an external output located on the mainframe controller.

11 Interface/Controller

11.1 Introduction

The Interface/Controller uses a high-end CPU with an embedded operating system. It is used to communicate with controlling computers and supports extra storage options.
Each complete mainframe houses an Interface/Controller, which enables data input and output so that the mainframes can be connected.

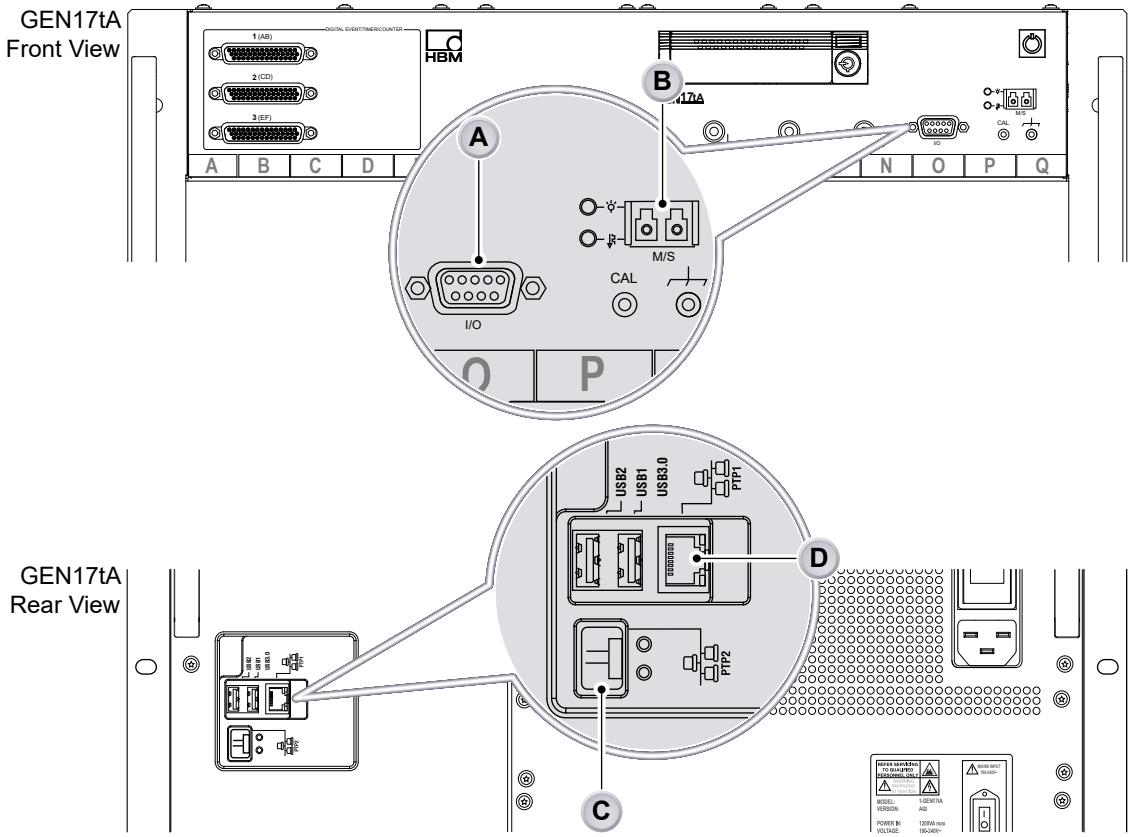


Figure 11.1: Interface/Controller

- **A** I/O connector (trigger in/out, clock in, event in/out, start/stop)
- **B** Master/Sync connector (optical)
- **C** PTP enabled network optical SFP slot (SFP module is optional)
- **D** PTP enabled network RJ45

The Interface/Controller has one standard Ethernet interface, one optical Ethernet interface with two activity LEDs and a Master/Sync connector with two activity LEDs and the I/O connector.

11.2 Communication and control

The GEN series uses standard TCP/IP protocol over Ethernet to communicate with the PC. The Interface/Controller provides access to the Ethernet network.

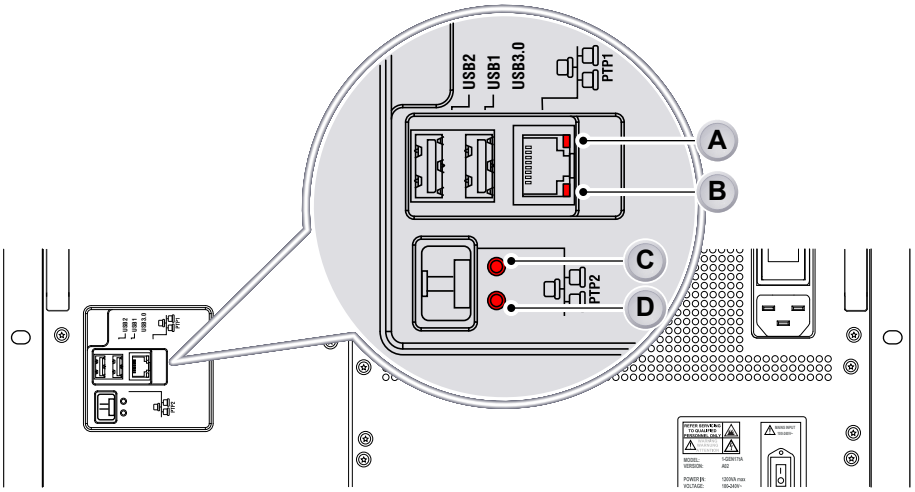


Figure 11.2: Ethernet LED indicators

A Link speed RJ45 network
B Activity LED RJ45 network
C Activity LED optical network
D Link speed LED optical network

Table 11.1: Ethernet LED indicators

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	No cable attached or no signal on cable
100 or 10 Mbit/s network connection	ON	OFF	Network connection with no data exchange
100 or 10 Mbit/s network connection	Blinking	OFF	Network connection with active data exchange
1 Gbit/s network connection	ON	ON	Network connection with no data exchange
1 Gbit/s network connection	Blinking	ON	Network connection with active data exchange

11.2.1 Network protocols and ports

All tethered GEN DAQ series mainframes use Ethernet protocols to communicate with the controlling PC. The following table gives an overview of the used protocols, ports, packet sizes and frequency of use on the network.

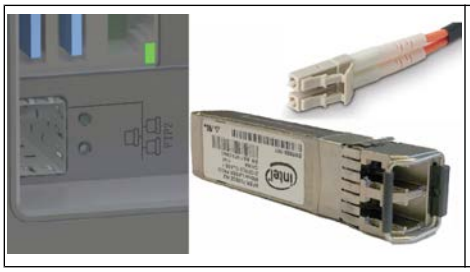
General TCP/IP IPv4 with standard Ethernet V2 fames (MTU = 1500 bytes) is used.

Specific protocols are used for:

Network protocols and ports	
Mainframe Identify	
Protocol	UDP (broadcast and directed)
Used ports	8004 (PC to mainframe) and 8005 (mainframe to PC)
Data size	Variable (<=1016 Bytes)
Frequency	When powering on / powering off / rebooting a mainframe When starting Perception Up to about 10 UDP frames each time, in both directions
More info	Packets have “PLAZADGRAM” at the start of the data area
Network Discovery Protocol	
Protocol	Multicast
Used IP addresses	239.255.77.76 and 239.255.77.77
Used IP ports	31419 (PC to mainframe) and 31418 (mainframe to PC)
Data size	Variable (< 2000 Bytes)
Frequency	When starting Perception When selecting Scan for Mainframes in Perception
Mainframe communication	
Protocol	TCP
Used ports	Connecting to Port 8003
Data size	Variable within MTU size
Data rate	Depending on storage speed, Ethernet Link speed and limited by network bandwidth. Currently maximum 120 MB/s on 1 Gbit Ethernet and 250 MB/s on 10 Gbit Ethernet ports.

Network protocols and ports	
Other protocols	
ARP, DNS	When supported on the network setup
DHCP, AutoIP	When enabled on this mainframe
iSCSI	Default port: 3260
PTP	v2, End-to-End, 1 sync per second

11.2.2 Using the 1 Gbit option connections



LC Connection Using the SFP + Option
LC optical connections that need an SFP device to enable their use with a LC connected optical cable.

The GEN series mainframes come with an optional 1 Gbit optical network support in the form of an SFP module.

The SFP receiver housing is part of the mainframe. Inserting a SFP module enables the use of optical Ethernet. The SFP module is offered in two different wavelengths: 850 nm or 1310 nm.

See GEN17tA data sheet for detailed usage and specifications.

11.3 Master/Sync connector

The GEN17tA Master/Sync connector supports both standard (compatible with legacy mainframes) and extended synchronization.

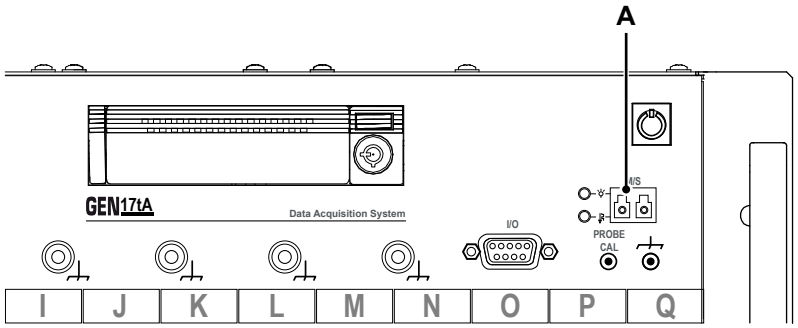


Figure 11.3: Interface/Controller

A Master/Sync connector (optical)

Standard Synchronization: Synchronizes the first sample in the recording for each mainframe, prevents frequency drift of the sample rates within each mainframe, synchronously exchanges every channel trigger connected to the Master/Sync trigger bus to/from each connected mainframe and automatically compensates for the cable length delay.

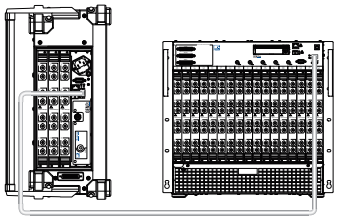
Extended Synchronization: Standard synchronization, Start/Stop and Pause of a recording across multiple mainframes, each controlled by a separate Perception. (Stop recording is a non-synchronous action). Synchronous manual trigger exchange (user software action to trigger all mainframes synchronously). Calculated channel trigger exchange (requires Perception V6.50 or higher).

For detailed specification, please refer to the GEN17tA data sheet.

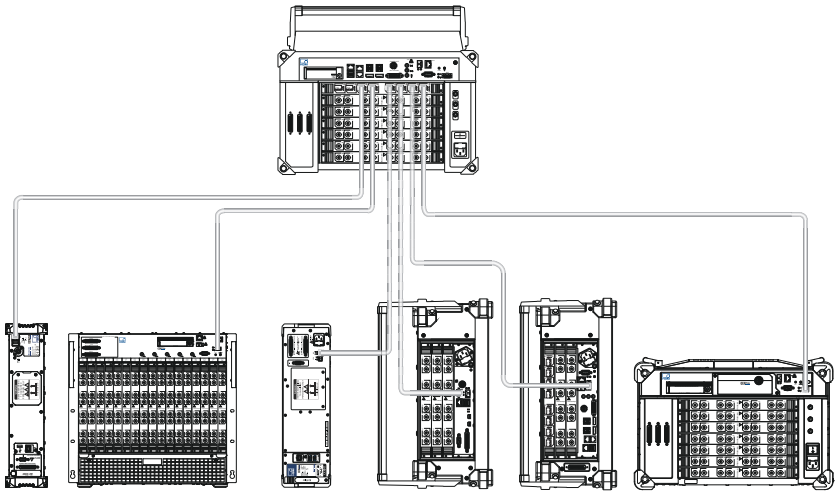
The GEN series can be operated as a fully synchronized Multi-Mainframe system with multiple mainframes using the Master/Sync connector.

The Master/Sync connector supports (please refer to chapter "Connecting the Master/Sync connector" on page 149 and "Connecting multiple mainframes using the Master/Sync card" on page 149 for wiring details):

- Directly connect to one mainframe using the Master/Sync connector. Each mainframe can then be Master or Sync mainframe.



- Connect as Sync mainframe to a group of mainframes in Master/Sync setup. One mainframe in this group must use the Master/Sync card option to be able to connect multiple Sync mainframes.



Master/Sync connector operating modes

The Master/Sync connector has three operating modes:

- Master
- Sync
- Stand-alone

In stand-alone mode, the Master/Sync connector is not used. Cables can be left attached, as no information is exchanged.

Fiber optic cable

The Master/Sync connection uses an optical duplex cable with LC connectors that connects two Master/Sync connectors. The maximum cable length supported is 500 m (For more information, please refer to "Calculating maximum fiber cable length" on page 479). As the connection is optical, no ground loops exist and the communication is not disturbed by external signal sources.

Figure 11.4: Example of a duplex LC® connector

LED indicators

On the front panel of the Master/Sync connector, two LEDs indicate the status of the link.

The icon is used to identify the signal detect function.

The icon is for data/synchronization identification.

A icon

B icon

The following table shows the function and possible combinations of the two LEDs.

Table 11.2: Master/Sync connector front panel LED indicators

FRONT PANEL LED INDICATORS			
Status			**Description**
No Link	off	off	No valid characters detected/ no optical signal detected
Optical signal detection/ initialization	on	off	Alignment characters detected
Receiving data	on	on	Receiving valid data

11.3.1 Connecting the Master/Sync connector

With the fiber optic cable, connect the Master/Sync connector of two mainframes.
In this setup, one mainframe must be set to Master while the other mainframe must then be set to Sync mainframe. In this setup, extended synchronization is used automatically.

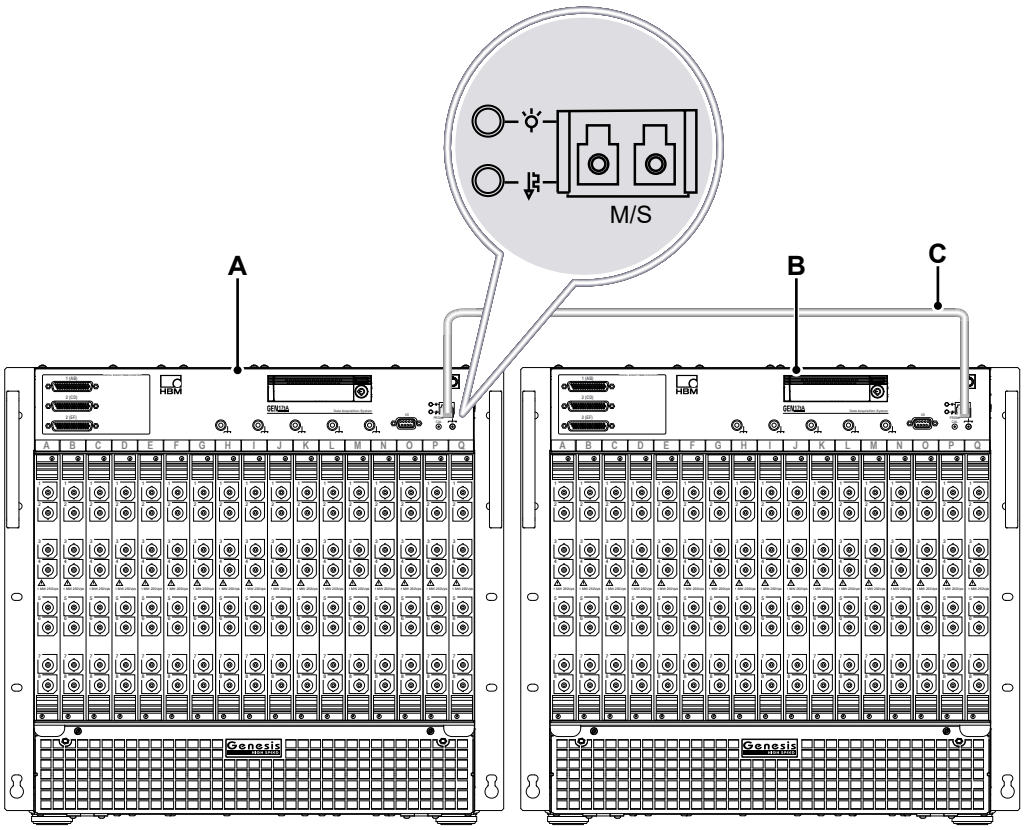


Figure 11.5: Connecting the Master/Sync

A Master mainframe

B Sync mainframe

C Fiber optic cable

11.3.2 Connecting multiple mainframes using the Master/Sync card

The multiple mainframe Master/Sync setup only works in a star configuration. All Master/Sync fiber optic cables are on one side connected to the Master mainframe while the other side connects to one Sync mainframe.

The master mainframe needs to be extended with one or more optional option carrier cards (G081). Each option carrier card can be extended with one or two Master output cards (G083).

Maximum Master/Sync overview			
	Option Carrier Card	Master Output Card	Sync Mainframes
GEN2tB	1	2	9
GEN3i	2	4	17
GEN3iA	2	4	17
GEN4tB	3	6	25
GEN7i	6	12	49
GEN7iA	6	12	49
GEN7tA	6	12	49
GEN17tA	16	32	129

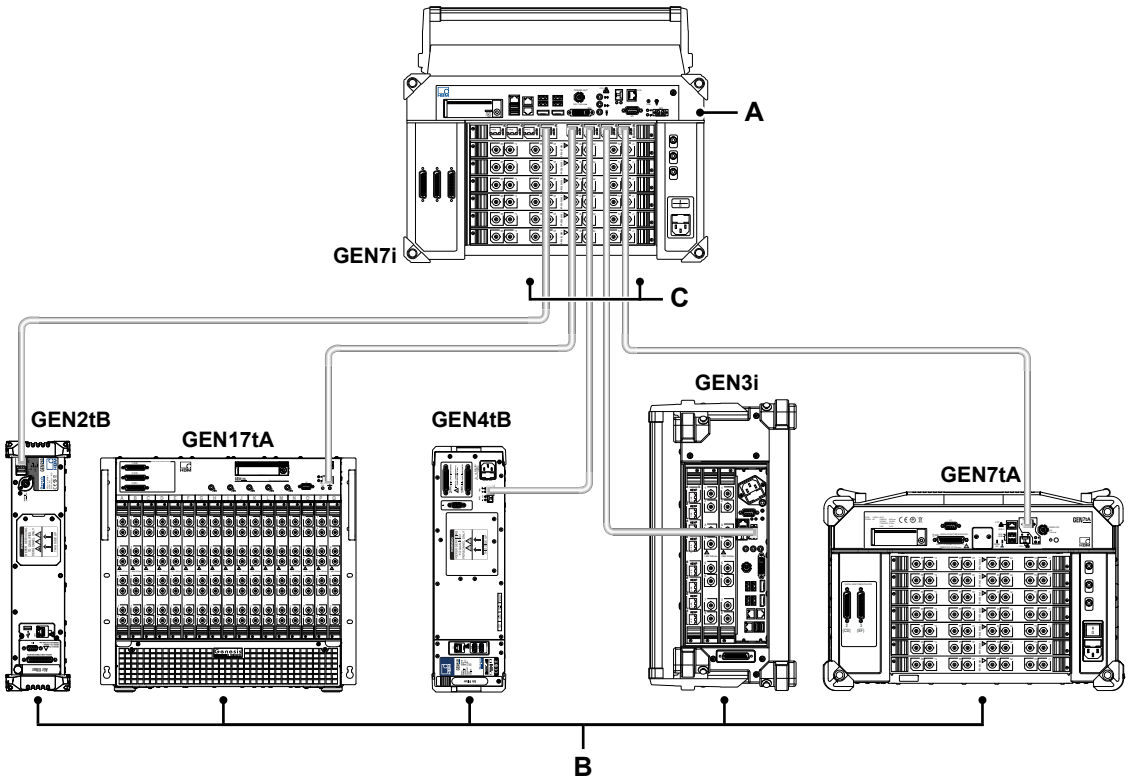


Figure 11.6: Master/Sync configuration with five sync mainframes

A Master mainframe

B Sync mainframes

C Fiber optic cable

1 Connect one of the connectors of the Master Output Card(s) (G083) to the Master/Sync connector of the Sync mainframe.

2 Connect one of the connectors of the Master Output Card(s) (G083) to the Master/Sync connector of the **second** Sync mainframe.

3 If **multiple** Sync mainframes are used repeat this setup until all Sync mainframes are connected.

11.3.3 Setting the Master/Sync operating modes

Each mainframe can be used as a Master or Sync mainframe. The operating modes are set up using the Perception software.

In the *Perception work* area:

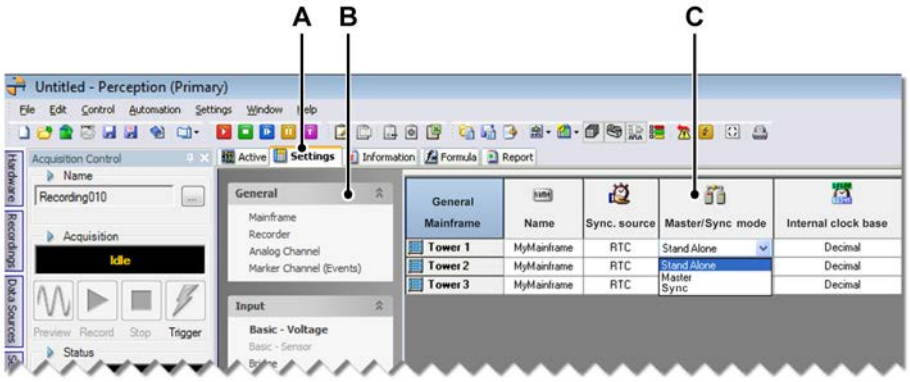


Figure 11.7: Perception work area with Master/Sync

A Settings tab

B General group

C Master/Sync mode column

To set the Master/Sync operation in the Perception software, proceed as follows:

1 Select the **Settings** sheet.
2 In the **Settings** sheet, go to the **General** group in the task pane and select **Mainframe**.
A list of available mainframes is displayed in the settings area.
3 Set the master:
   a Select the mainframe that should be used as Master.
   b Double-click on the **Master/Sync mode** cell to open it for modification.
   c In the drop-down list that appears, select **Master**.
4 Set one or more Sync mainframe(s):
   a Select the mainframe(s) that should be used as Sync mainframes(s).
   b Double-click on the **Master/Sync mode** cell to open it for modification.
   c In the drop-down list that appears, select **Sync**.

To disable the Master/Sync operation and set the mainframe to Stand-alone mode:

1 Select the mainframe(s) that should be used as Stand-alone.
2 Double-click on the **Master/Sync mode** cell to open it for modification.
3 In the drop-down list that appears, select **Stand-alone**.

HINT/TIP

Cables do not have to be removed, as the mainframe does not use the connected cable during stand-alone mode.

11.3.4 Synchronizing a Master/Sync setup to external time sources

In a Master/Sync setup, all time information is recorded by the Master mainframe only. Synchronization source selection on Sync mainframes is disabled as Sync mainframes are dedicated to follow the Master mainframe.

For the Master mainframe, the date and time are controlled by either the PC (RTC) , PTP master, IRIG or GPS, depending on the synchronization source selected. The source is selected in the Perception software.

In the *Perception work* area:

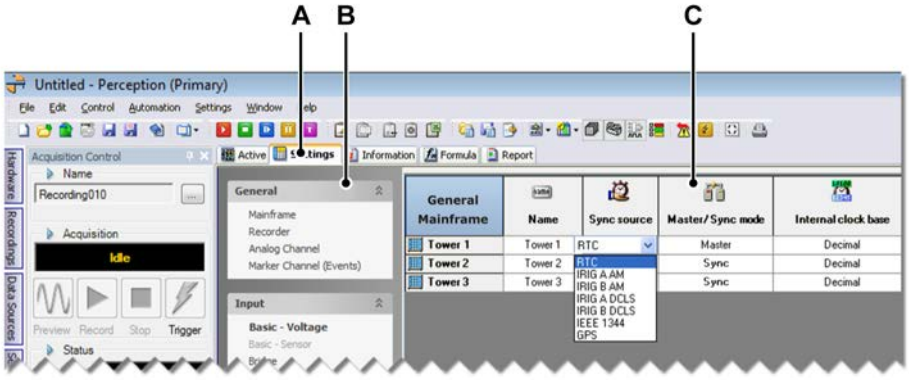


Figure 11.8: Perception work area synchronization source

A Settings tab

B General group

C Master/Sync source column

To set the synchronization source in the Perception software, proceed as follows:

1. Select the **Settings** sheet.
2. In the **Settings** sheet, go to the **General** group in the task pane and select **Mainframe**.
   A list of available mainframes is displayed in the settings area.
3. Select the Master mainframe.
4. Double-click on the **Sync source** cell to open it for modification.
5. In the drop-down list that appears, select the synchronization source that should be used.

For information on how to check synchronization, please refer to appendix "Master/Sync connection verification procedure" on page 403.

11.4 I/O connector

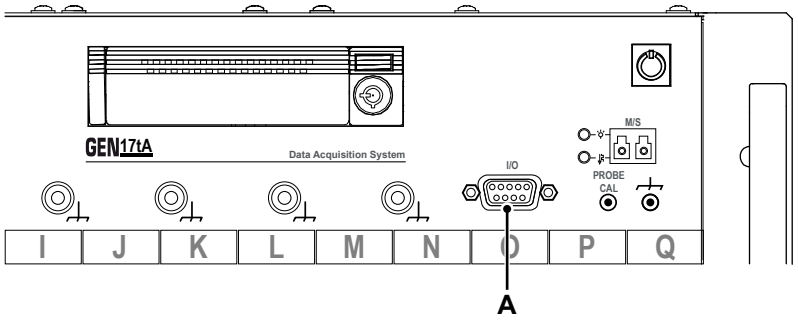


Figure 11.9: Interface/Controller

A I/O connector (trigger in/out, clock in, event in/out, start/stop)

The I/O connector comes with a BNC breakout cable for direct BNC cable connection to each function (see Figure 11.10).

PIN	Signal
PIN 1	External Event In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V

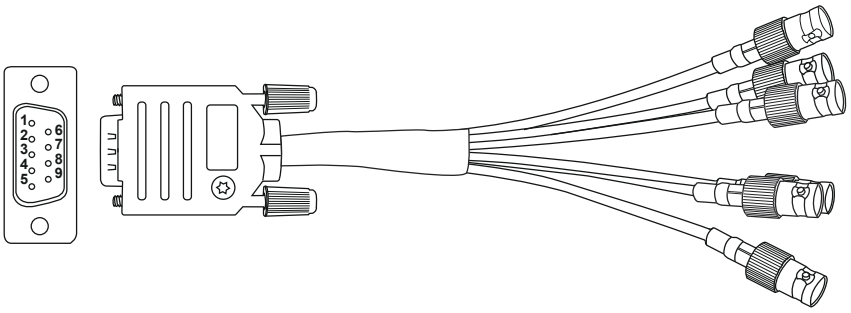


Figure 11.10: BNC breakout cable

11.4.1 I/O connector input overvoltage protection

All inputs of the I/O connector are over voltage protected. All inputs use the following schematic approach.

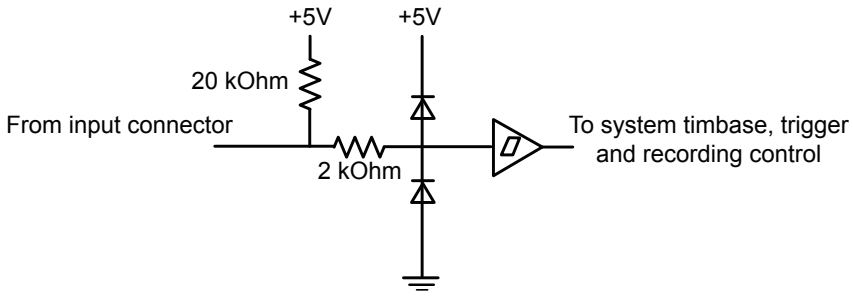


Figure 11.11: I/O connector schematic inputs

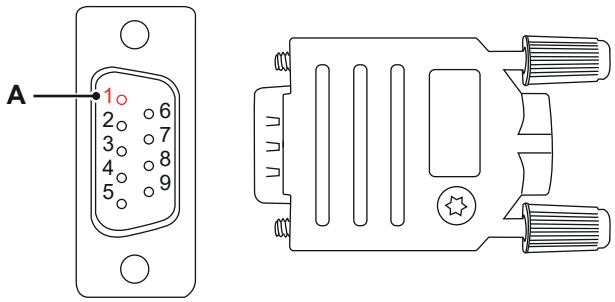
Due to the 20 kΩ pull-up resistor all inputs will be “TTL High” and only need an external short to signal ground to be operated. The 2 kΩ series resistor together with the diode clamps to ground and +5 V protect the digital circuitry up to the specified voltages.

The clamping diodes and other parasitic capacitors do create a capacitive load on your signal source and limit the signal bandwidth. To reach the required bandwidths detailed compensations are made not addressed in this block diagram.

11.4.2 I/O connector functions and connector pinning

A External Event In

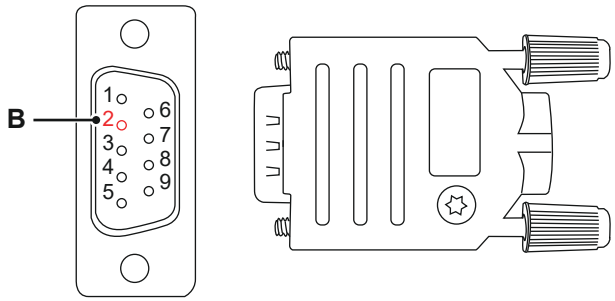
PIN	Signal
PIN 1	External Event In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V



This input is software selectable between **External Cycle Event In** and **Trigger Arm**.
External Cycle Event In can be used in RT-FDB context as cycle source. Trigger Arm can be used to arm triggers within in the mainframe. For more information about External Event In and RT-FDB usage, please refer to chapter "External Event In use with RT-FDB" on page 160.

B External Event Out

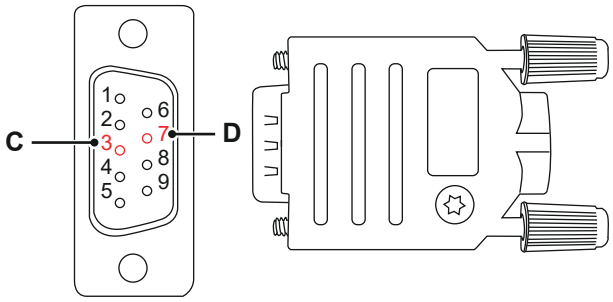
PIN	Signal
PIN 1	External Event In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V



This output is software selectable between **Alarm Out**, **Recording Active Out** and **Trigger End**. When *alarm* is selected, the output is driven by channel alarm detectors or RT-FDB alarm functions. When *recording active* is selected, the output is “high” while a recording is in progress. When recording in Trigger Arm mode with Trigger End enabled a pulse of 500 ms ± 100 ms is generated at the end of the sweep recording.

C/D External Trigger In/Out

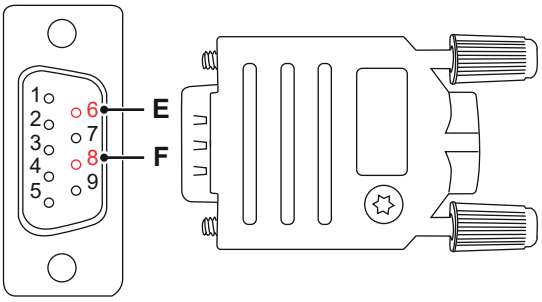
PIN Signal
PIN 1 - External Event In
PIN 2 - External Event Out
PIN 3 - External Trigger In
PIN 4 - Ground
PIN 5 - Ground
PIN 6 - External Start In
PIN 7 - External Trigger Out
PIN 8 - External Stop In
PIN 9 - +5V



This input and output are related to the recorder trigger logic. For more information, please refer to “Recorder and system trigger” on page 138.

E/F External Start In/External Stop In

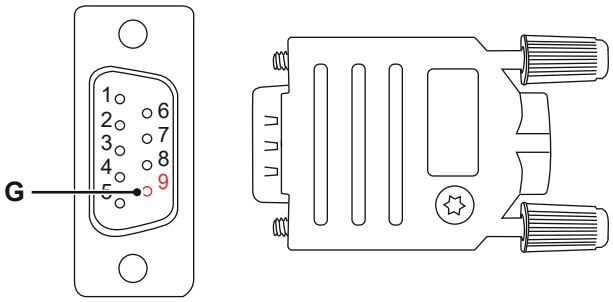
PIN Signal
PIN 1 - External Event In
PIN 2 - External Event Out
PIN 3 - External Trigger In
PIN 4 - Ground
PIN 5 - Ground
PIN 6 - External Start In
PIN 7 - External Trigger Out
PIN 8 - External Stop In
PIN 9 - +5V



For more information about External Start In/External Stop In, please refer to chapter "External Start In/External Stop In" on page 158.

G +5 V Power Out

PIN Signal
PIN 1 - External Event In
PIN 2 - External Event Out
PIN 3 - External Trigger In
PIN 4 - Ground
PIN 5 - Ground
PIN 6 - External Start In
PIN 7 - External Trigger Out
PIN 8 - External Stop In
PIN 9 - +5V



Output power	
Voltage	5 ± 0.5 V DC
Maximum current	0.1 A, continues short circuit protected

11.4.3 External Start In/External Stop In

The **External start/stop** (see Figure 11.12) settings are located in the **General/ Mainframe** setting page of the settings spreadsheet. The settings are only visible when **Advanced (All settings)** is enabled (see Figure 11.13).

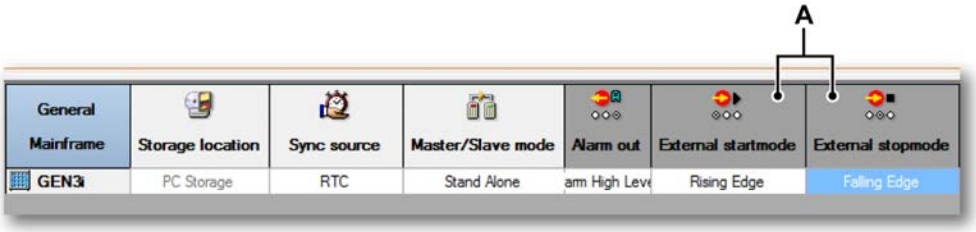


Figure 11.12: General/Mainframe settings

A External start/stop mode columns

To enable the advanced settings, right click on the table header (see Figure 11.13).

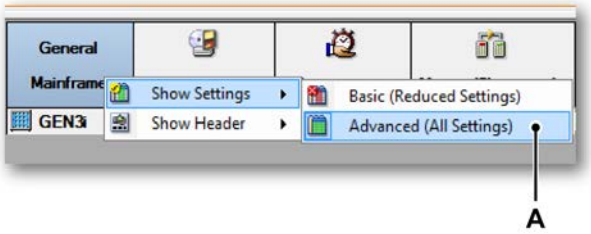
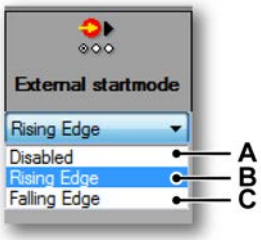


Figure 11.13: Show Settings - Advanced

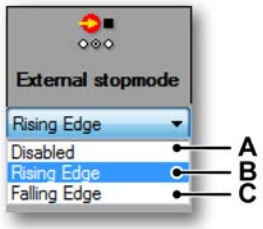
A Advanced (All Settings)

The **External startmode** setting can be used to configure the external start input.



A When selecting **Disabled**, the signal on the input is ignored.
B When selecting **Rising Edge**, a start is initiated when a rising edge is detected.
C When selecting **Falling Edge**, a start is initiated when a falling edge is detected.

The **External stopmode** setting can be used to configure the external stop input.



A When selecting **Disabled**, the signal on the input is ignored.
B When selecting **Rising Edge**, a stop is initiated when a rising edge is detected.
C When selecting **Falling Edge**, a stop is initiated when a falling edge is detected.

The minimum pulse width for both External Start In and External Stop In is 500 ns. Pulses shorter than 500 ns will be ignored, other pulse lengths can be configured.

As the Start/Stop events are software processed events, a one second response time typically passes before the Start/Stop is executed. After an event is received, a “disable” time period of 100 ms starts. The same event will not be detected during the disable time period. For example, if a Start event is received, a new Start event will not be detected for 100 ms. If, however, a Stop event occurred immediately after a Start event had been detected, the Stop event would be detected and processed immediately after the acquisition is started due to the Start event.

11.4.4 External Event In use with RT-FDB

The External Event In signal can be used as TTL input in RT-FDB. This signal can be used in the RT-FDB External Cycle Event In function. High frequent noise on the TTL input can be filtered using a debounce filter. The use of the debounce filter delays the signal before an event can be derived. This delay can only be compensated to filter settings up to 2 µs, see table below.

Note *High filter times shall only be compensated partially.*

Debounce settings	
Filter time (µs)	**0 µs (fully compensated)**
0.5	0 µs (fully compensated)
1	0 µs (fully compensated)
2	0 µs (fully compensated)
5	3 µs (2 µs compensated)
10	8 µs (2 µs compensated)

11.5 Option - Removable Solid State Drive (SSD)

The GEN17tA has a removable Solid State Drive bay built-in.

Figure 11.14: Solid State Drive (SSD)

No disk repair and/or data recovery tools exist. Do not attach the disk to a Windows® PC. The partitions are formatted as EXT4 and can only be handled by the Linux operating system.

HINT/TIP

When the GEN17tA Solid State Drive is enabled, the integrity of the partition is checked on regular basis during boot. This can result in longer boot times (up to 10 s or more) before the GEN17tA is ready for use. This is normal behavior.

For specifications and ordering information, please refer to the GEN17tA Data Sheet.

Verification

To verify that **Local Storage** is enabled:

1 Connect to the mainframe

2 Navigate to the **Settings** tab; **Mainframe Disk 1** must be visible:

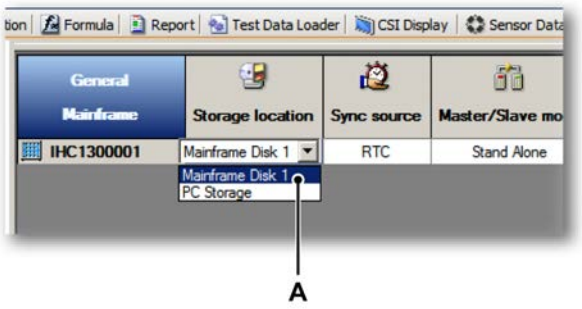


Figure 11.15: Storage location with Mainframe Disk 1 enabled

11.6 Option - Optical 1 Gbit Ethernet interface

The Interface/Controller supports an optical 1 Gbit Ethernet interface by means of an SFP module. An SFP module is a small, form-factor and pluggable transceiver that supports direct optical network connections.

WARNING

Laser Safety
The system is classified as a Class 1 laser product. The SFP uses an optical light source for data and command communication. It does not emit hazardous light, but direct exposure to the beam should be avoided.

This simple and powerful plug-in-and-use option enables the use of an optical network connection on the Interface/Controller. There are two models available to choose from:

- 1 Gbit (850 nm) - Multi Mode
- 1 Gbit (1310 nm) - Single Mode

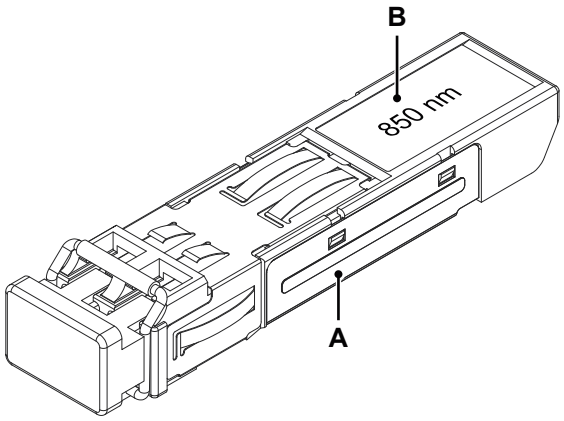


Figure 11.16: SFP optical network device

A SFP shown with dust cap and removal bar

B SFP label - 850 or 1310 nm

Note *1310 nm Single Mode (SM) and 850 nm Multi Mode (MM) optical fiber transceivers use specific cables. Therefore, make sure that the correct mode/ specification of fiber optic cable is used.*

Selecting cables and cable lengths:
Cables need to have different properties when they exceed certain lengths. These cable properties are based on the properties of light in an optical fiber.

Single Mode The cable is a type of cable that has a relatively small light-carrying core. Light in a small core makes fewer internal reflections so that the path of light is close to a straight line. Therefore, the light can travel further distances.

Multi Mode The cable is a type of cable that has a relatively large light-carrying core. Light in a larger core makes more reflections and can only travel shorter distances.

For specifications and ordering information, please refer to the GEN17tA data sheet.

For information on how to install and remove the SFP module, please refer to section "Installing a 1 Gbit SFP/10 Gbit SFP+ Module" on page 172.

11.7 Option - 10 Gbit Ethernet interface (SFP+ Module)

The 10 Gbit Ethernet option is a Factory installed, ready to use Ethernet option with two available Ethernet interfaces.

The 10 Gbit Ethernet card can be installed in addition to the standard on-board 1 Gbit Ethernet connection. The 10 Gbit Ethernet card allows you to increase the throughput speed of communication when compared to the standard 1 Gbit Ethernet. If installed, the 10 Gbit Ethernet option can replace the use of the standard 1 Gbit Ethernet connection.

WARNING

Laser Safety
The system is classified as a Class 1 laser product. The SFP uses an optical light source for data and command communication. It does not emit hazardous light, but it is recommended to avoid direct exposure to the beam.

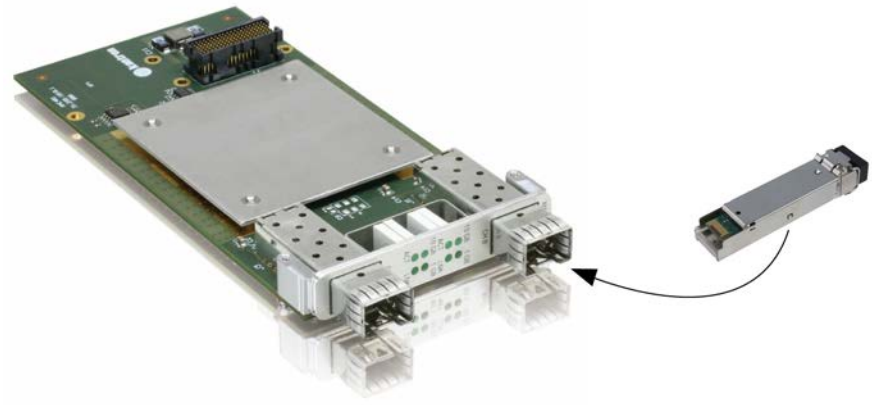


Figure 11.17: 10 Gbit Ethernet card - with SFP+ module

Note *The maximum 10 Gbit throughput speed is per-card. Throughput speed is therefore a shared specification for both interfaces combined. It is possible that two interfaces can be used at the same time but only when one interface is used for communication and the other is used for storage. Two interfaces cannot be used at the same time for storage purposes nor can they be used at the same time for communication purposes.*

Connections and using the 10 Gbit Option

	**A 10Gbit LC Connection Using the SFP+ Option** 10Gbit LC optical connections need an SFP+ module to enable their use with LC connected optical cable.
	**A 10Gbit RJ45 Connection Using the SFP+ Option** 10Gbit RJ45 copper connections need an SFP+ module to enable their use with RJ45 copper cable.

Note *The 10 Gbit speed rating can be achieved with **optimized settings** using compatible equipment and devices of similar speed ratings. Please see appendix "Optimal Windows® settings for 10 Gbit Ethernet card" in GEN series Data Acquistion manual for further details on the specific **optimized settings**.*

Front panel layout

The front panel of the 10 Gbit Ethernet option has the following layout:

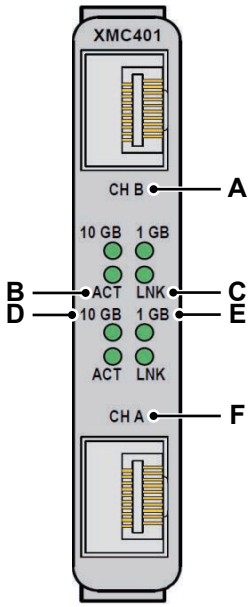


Figure 11.18: Front panel of XMC401 10 Gbit Ethernet card

A **CH B** = **NIC2** (Requires SFP+ module, not shown)

B ACT (green): Ethernet Activity (on when active)

C LNK (green): Ethernet Link (on when active)

D 10 Gbit (green): Ethernet Speed 10 Gigabit (always on)

E 1 Gbit (green): Ethernet Speed 1 Gigabit (always on)

F **CH A** = **NIC1** (Requires SFP+ module, not shown)

Figure 11.18 shows the two interfaces of this option without installed SFP+ option, for further details on the SFP+ options please see the next section.

Once the SFP+ option is installed in the 10 Gbit Ethernet interface, an LC optical cable can be connected.

10 Gbit Ethernet Option accessories

The types of 10 Gbit SFP+ module that are used with this Ethernet card are:

- 10 Gbit (850 nm) - Multi Mode
- 10 Gbit (1310 nm) - Single Mode
- 10 Gbit (RJ45) - Copper

Note *__SFP__ modules rated at 1 Gbit and are not suitable for this card. Please select the __SFP+__ modules which are rated at 10 Gbit.*

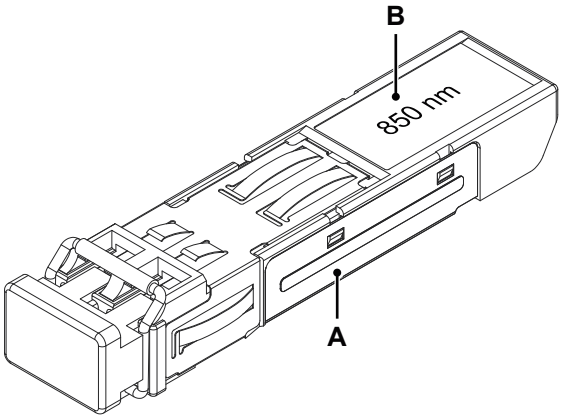


Figure 11.19: SFP Optical Network devices

A SFP shown with dust-cap and removal bar

B SFP label - 850 or 1310 nm

Note *1310 nm Single Mode (SM) and 850 nm Multi Mode (MM) optical fiber transceivers use specific cables. Therefore, make sure that the correct mode/ specification of fiber optic cable is used.*

Cable selection and lengths:

Cables require different properties when they exceed certain lengths based on the properties of light in an optical fiber.

Single Mode Cable is a type of cable that has a relatively small light carrying core and therefore makes fewer internal reflections so that the path of light is closer to a straight line and thus can travel further distances. This cable is suitable for 1310 nm SFP modules.

Multi Mode Cable is a type of cable that has a relatively thicker light carrying core. Light in a thicker core makes more reflections and is therefore only suited to shorter distances. This cable is suitable for 850 nm SFP modules.

For optical cable length calculation see chapter "Calculating maximum fiber cable length" on page 479.

For Installation and removal of the SFP+ module see section "Installing a 1 Gbit SFP/10 Gbit SFP+ Module" on page 172.

10 Gbit Ethernet card in GENDAQ series networks
There are several different ways to connect individual components together when using the 10 Gbit Ethernet card therefore this card allows the user more freedom to set up their system with different configurations.

The 10 Gbit Ethernet card can essentially be used to communicate at higher throughput speed of the standard 1 Gbit Ethernet or with more advanced setups can act as a manually switchable storage selector or even a dual communication and storage interface.

The following Figure 11.20 shows a simple setup using the 10 Gbit Ethernet card. A PC with an optical Ethernet interface which has SFP+ support is connected via optical cable to the interface of the 10 Gbit Ethernet card option of the GENDAQ unit. This setup utilizes the higher speed communication of the 10 Gbit Ethernet card for communication with Perception.

Figure 11.20: Basic setup - 10 Gbit Ethernet to PC

Connecting the 10 Gbit Ethernet Option to a PC
To be able to use this option you also need the correct connection or interface attached to your PC. The correct connection is not always an SFP+ module but there must be a network card or adaptor installed that supports the same specifications as the SFP+ modules used on the GENDAQ side.

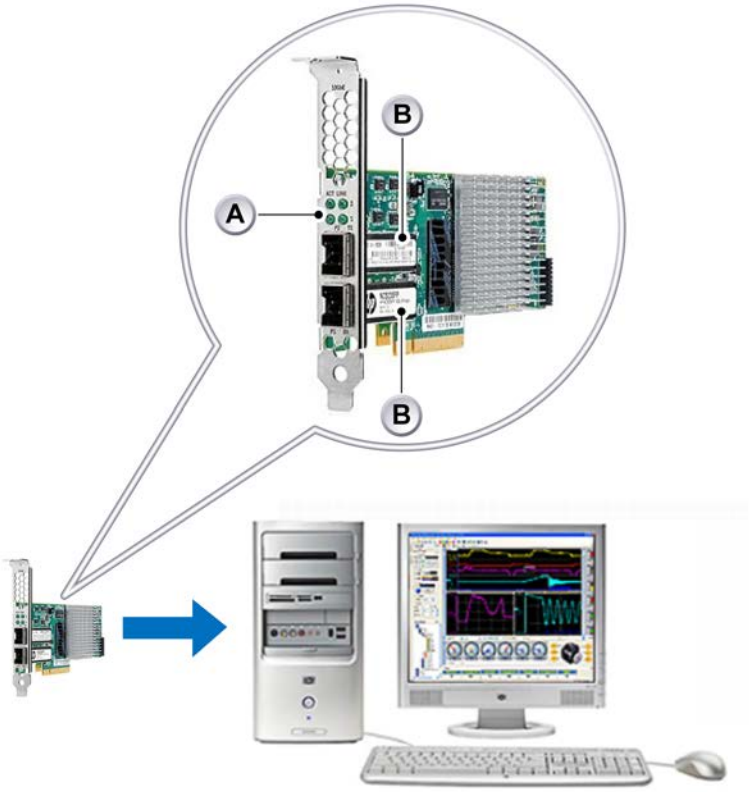


Figure 11.21: Connect the 10 Gbit Ethernet Option to a PC

A 10 Gbit Ethernet card

B SFP+ modules

Network Interface selection in Perception

With the 10 Gbit Ethernet option installed and ready to go you will be provided with the two following interfaces for selection:

- Optical 10 Gbit NIC1
- Optical 10 Gbit NIC2

In Perception these interfaces are available in the **Settings** menu > **Mainframe Network Setup** see Figure 11.22 below.

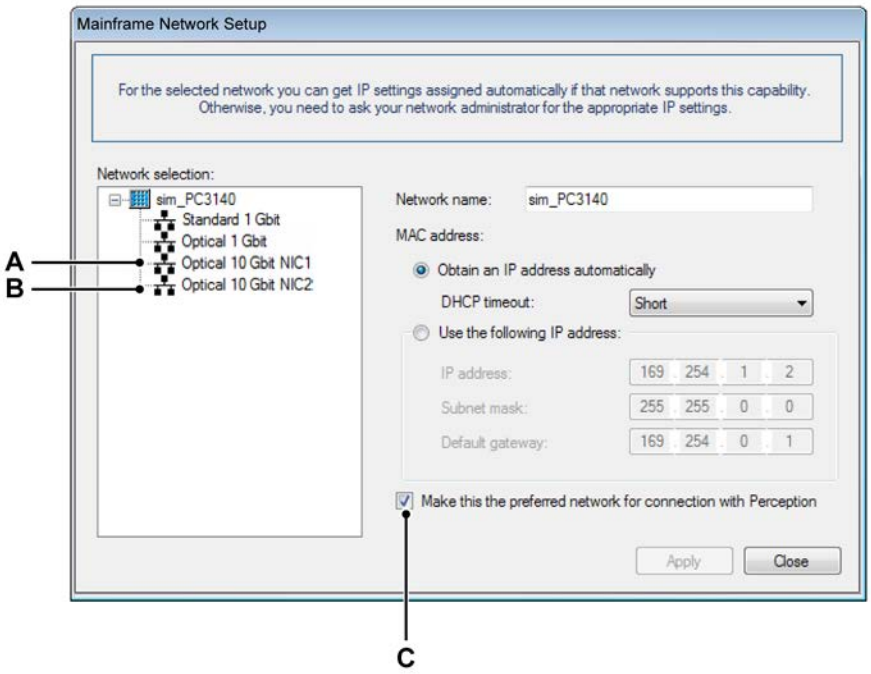


Figure 11.22: Mainframe Network Setup

A Optical 10 Gbit NIC1

B Optical 10 Gbit NIC2

C Make this the preferred network for connection with Perception

In **Mainframe Network Setup** you can define the IP address of each individual interface if needed.

If Perception finds more than one interface for **Network Selection** as shown in Figure 11.22, then the interface that has a Check in the box **Make this the preferred network connection with Perception** will be the interface used for communication with Perception. For the 10 Gbit Ethernet card check the box for the **Optical 10 Gbit NIC1 or 2**.

Click **Apply** then **Close** when done.

Windows® - optimum settings

IMPORTANT

To best achieve data transfer rates greater than 200 MB/s please make sure the following settings are introduced to your network adaptor via the settings in Windows®.

Windows® 10G network adapter settings:

- Interrupt moderation rate: **high**
- Receive side scaling ques: **8**
- Receive buffers: **2048**

Note *The above Windows® settings were tested and chosen using a specific setup of equipment (including the Intel® Ethernet Server adaptor x520). These setting may not be the optimal settings for your specific system.*

11.7.1 Installing a 1 Gbit SFP/10 Gbit SFP+ Module

Introduction

This section explains how to install and remove the Small Form Factor Pluggable (SFP or SFP+) transceiver device from any interface that supports SFP or SFP+ modules.

This device enables an optical network connection to be plugged directly into the front panel, in the optical network interface of the Interface/Controller. This option is also required in order to use the 10 Gbit Ethernet card.

Warnings

Before installing this device, please read and make sure that you have understood the following warnings, which are specific for this device.

Description of Electrostatic Discharge (ESD)

CAUTION

Electrostatic discharge (ESD) can cause damage to electronic devices if discharged into the device. Take steps to avoid such an occurrence.

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN17tA system, its connections or a plug-in card.

WARNING

Laser Safety

The system is classified as a Class 1 laser product. The SFP uses an optical light source for data and command communication. It does not emit hazardous light, but it is recommended to avoid direct exposure to the beam.

Installation steps

1 First, make sure that the mainframe unit is switched off. Then locate the available SFP slot and remove the plastic plug (if inserted).

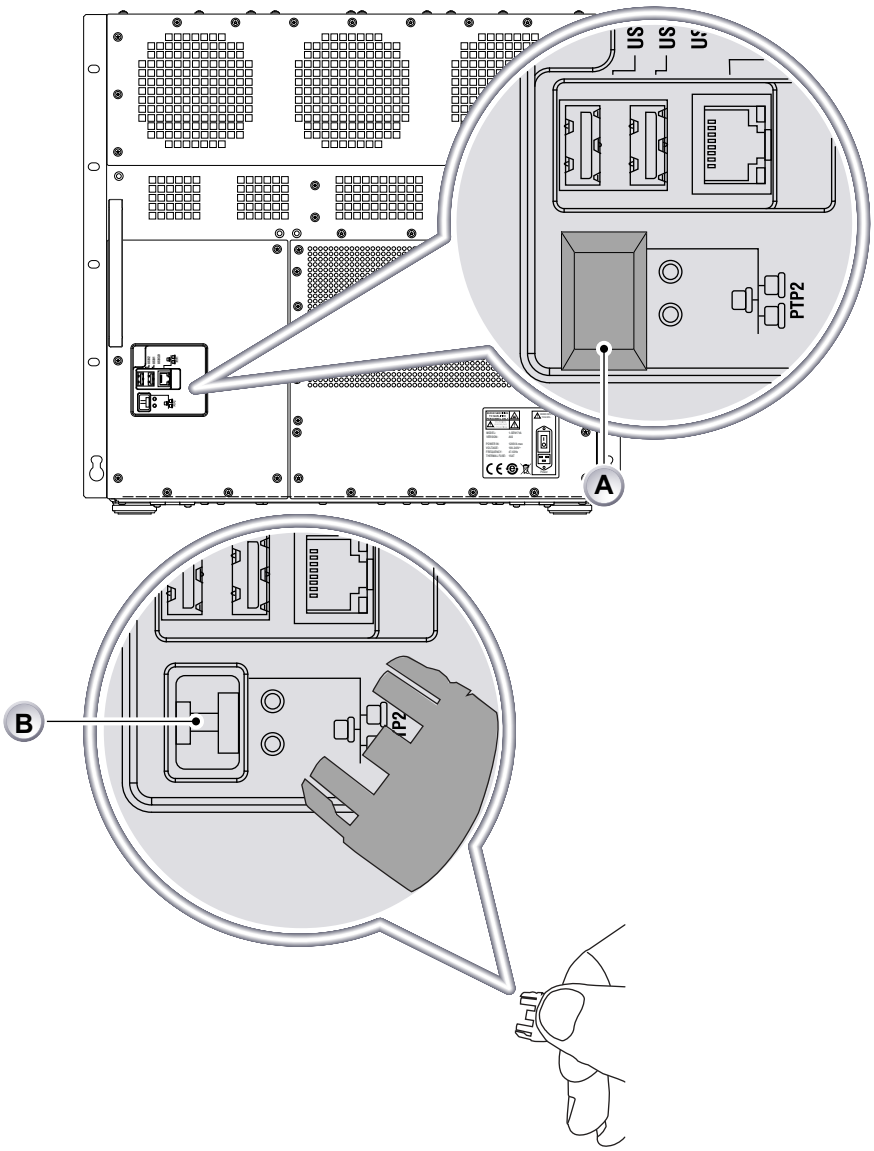


Figure 11.23: Interface/Controller SFP location

A Interface/Controller SFP location

B Remove cap

2 Grasp the module between fingers and thumb at the end with the small black removal bar. Push the back end into the available SFP slot, until you hear a click.

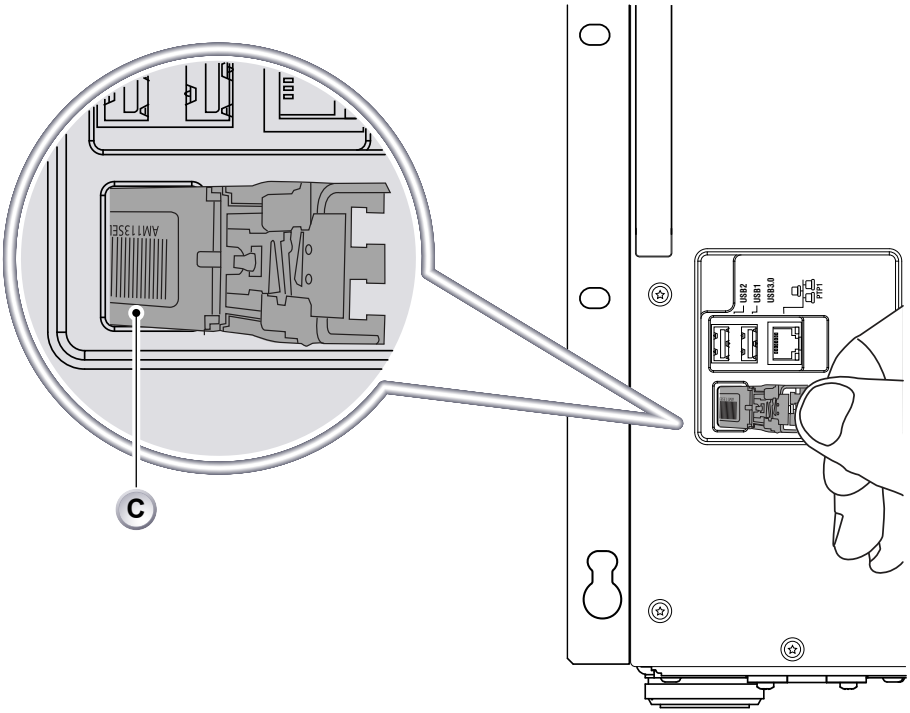


Figure 11.24: Insert device in SFP slot

C Insert device

3 Embedded software detects the device and automatically connects to it when the mainframe is powered on.

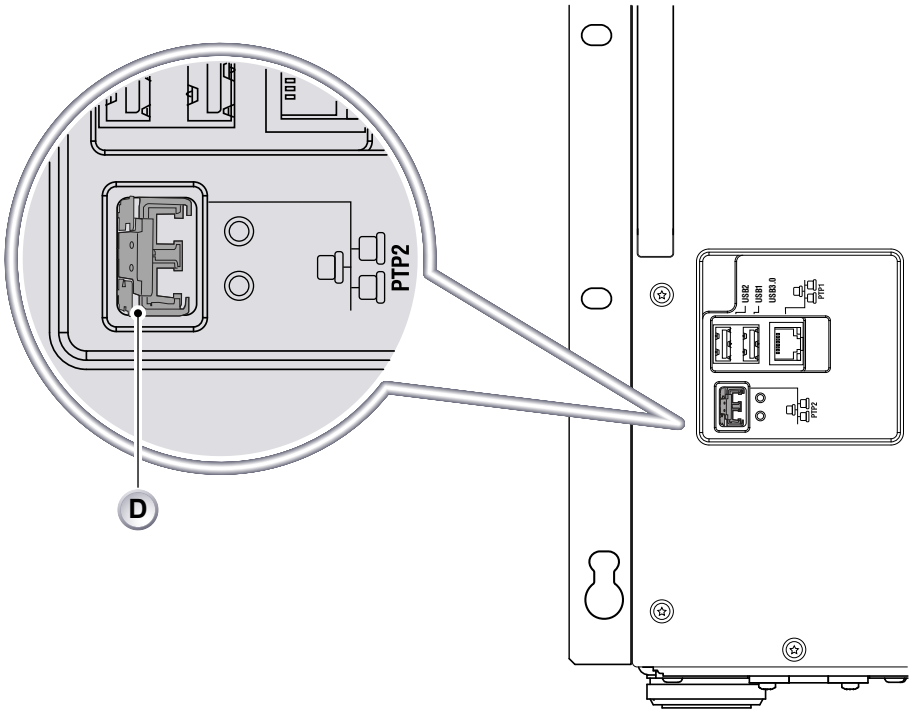


Figure 11.25: SFP slot with device

D Device being inserted

11.7.2 Removing a 1 Gbit SFP/10 Gbit SFP+ Module

To remove the module from the mainframe, first make sure that the mainframe is powered off. Then grasp the small black removal bar and pull it away and out from the mainframe. The spring-loaded removal bar releases the SFP from the front panel.

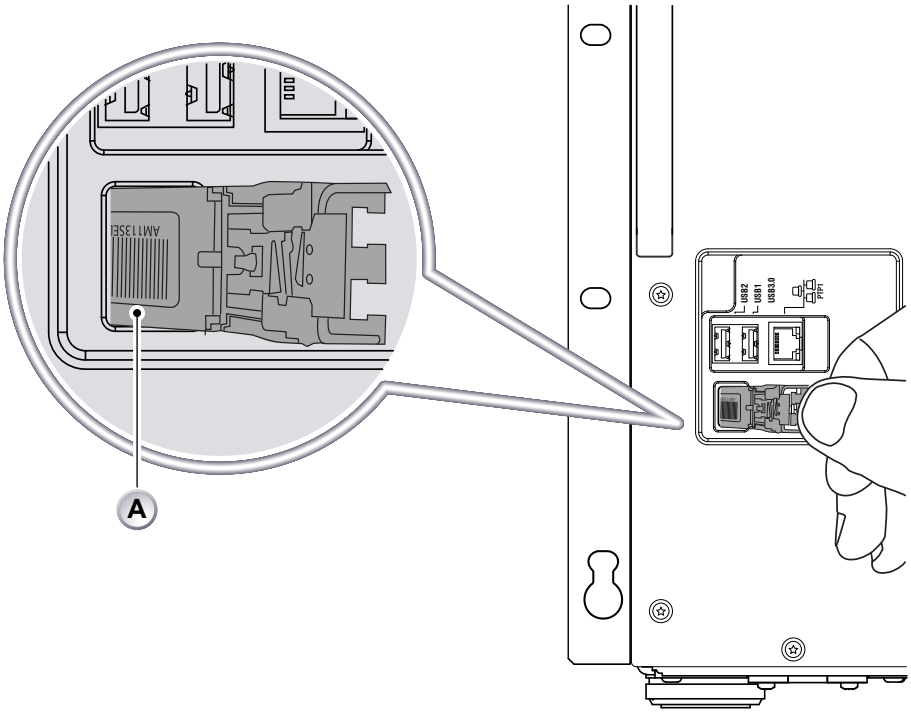


Figure 11.26: SFP slot - Remove device

A Remove device

Then, if available, replace the small plastic plug to protect the optical inlet.

11.8 Option - EtherCAT®

EtherCAT® is a state-of-the-art industrial Ethernet solution suiting the needs of modern industrial automation applications. EtherCAT® provides deterministic (real-time) distributed control. What makes EtherCAT® stand out when compared to other real-time Ethernet solutions are its unmatched performance, flexibility and cost effectiveness.

This chapter explains some of the generic EtherCAT® protocol principles. It provides a basic understanding of how EtherCAT® works.

Table 11.3: Terms and abbreviations

Term/ abbreviation	Description
CAN	Controller Area Network
CiA	CAN in Automation
CoE	CAN open over EtherCAT®
DC	Distributed Clocks
DPRAM	Dual Ported Random Access Memory
ESC	EtherCAT® Slave Controller
ESI	EtherCAT® Slave Information
ETG	EtherCAT® Technology Group
FMMU	Fieldbus Memory Management Unit
FoE	File access over EtherCAT®
IEEE	Institute of Electrical and Electronics Engineers
ESM	EtherCAT® State Machine
OSI Model	Open Systems Interconnection model
PDO	Process Data Object
PTP	Precision Time Protocol
SDO	Service Data Object
SII	Slave Information Interface

EtherCAT® is registered trademark and patented technology, licensed by Beckhoff Automation GmbH, Germany.

For more detailed information about EtherCAT® see ethercat.org.

11.8.1 EtherCAT® generic principles

The EtherCAT® functional principle is “Ethernet on the fly”. The EtherCAT® master sends out an Ethernet frame on the EtherCAT® fieldbus wire. This frame passes through all connected slave devices. The last slave in the chain returns the frame to the master by sending it back to the second last slave and so on. So, the frame passes each slave twice before returning to the master. This principle defines a control loop, where the master provides output values responding to received input values. For an example EtherCAT® topology see Figure 11.27.

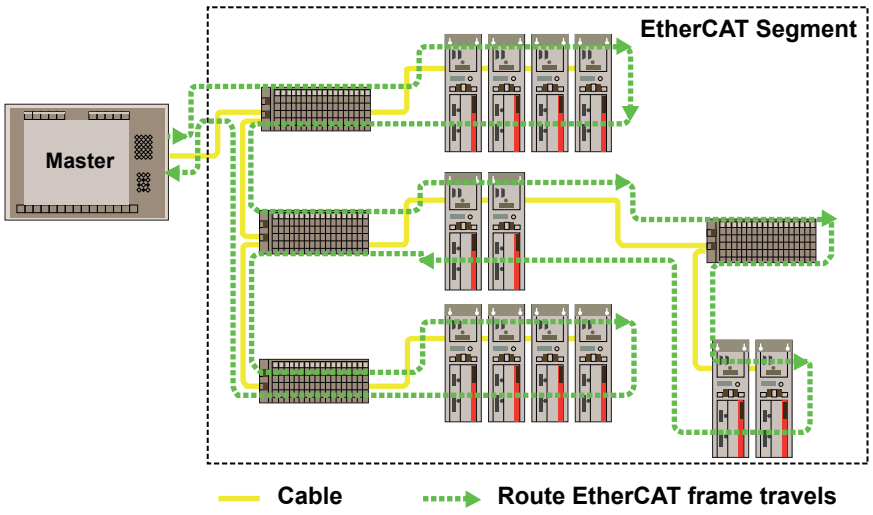


Figure 11.27: Example EtherCAT® Topology

11.8.2 EtherCAT® Slave Stack

The EtherCAT® protocol stack consists of several building blocks that are grouped in OSI Model layers as shown in Figure 11.28. The OSI Model provides a layered communication approach, whereby communication layers can be developed and modified independently. The EtherCAT® Slave Stack groups several OSI Model layers together as outlined in table below.

Table 11.4: OSI Model layer to EtherCAT® layer mapping

OSI Model layer		Function	EtherCAT® layer
7	Application	Translates demands placed on the communications stack in a form understood by the lower layers and vice versa.	Application [ETG.1000-5] [ETG.1000-6]
6	Presentation	Converts data to/from standardized network formats.	
5	Session	Creates and manages dialogue among lower layers.	
4	Transport	Provides transparent reliable data transfer (End-to-End transfer across a network which may include multiple links.	Data-link [ETG.1000-3] [ETG.1000-4]
3	Network	Performs message routing.	
2	Data-link	Controls access to the communication medium. Performs error detection and point-to-point transfer on a link.	
1	Physical	Encodes/decodes signals for transmission/ reception in a form appropriate to the communications medium. Specifies communication media characteristics.	Physical [ETG.1000-2]

Each EtherCAT® layer consists of the building blocks as shown in Figure 11.28

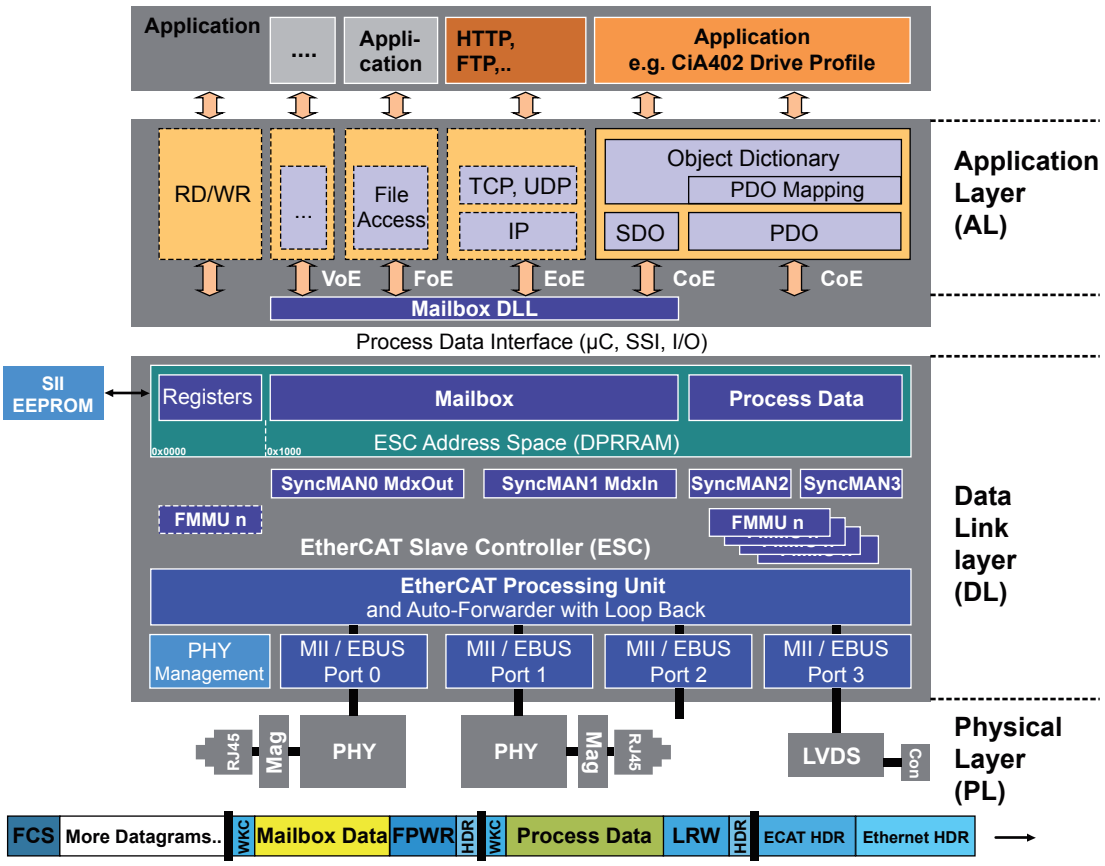


Figure 11.28: EtherCAT® Slave Stack overview

11.8.3 Physical Layer

The EtherCAT® Physical Layer defines the EtherCAT® transport media over which EtherCAT® frames are sent and how signals should be encoded and decoded over this media.

11.8.4 Data Link Layer

The EtherCAT® Data Link Layer controls access to the transport medium and provides basic time-critical messaging communication between devices connected to the EtherCAT® field bus. Within the Data Link Layer the following building blocks can be identified:

- **Ports**
  The Data Link Layer defines the concept of ports. One EtherCAT® slave device can support two, three or four ports. All ports have a loopback function that makes sure that the EtherCAT® control loop is always closed, no matter if ports are disconnected. This eliminates the need for manual bus termination as required by other industrial field bus solutions. See Figure 11.29 for more details.

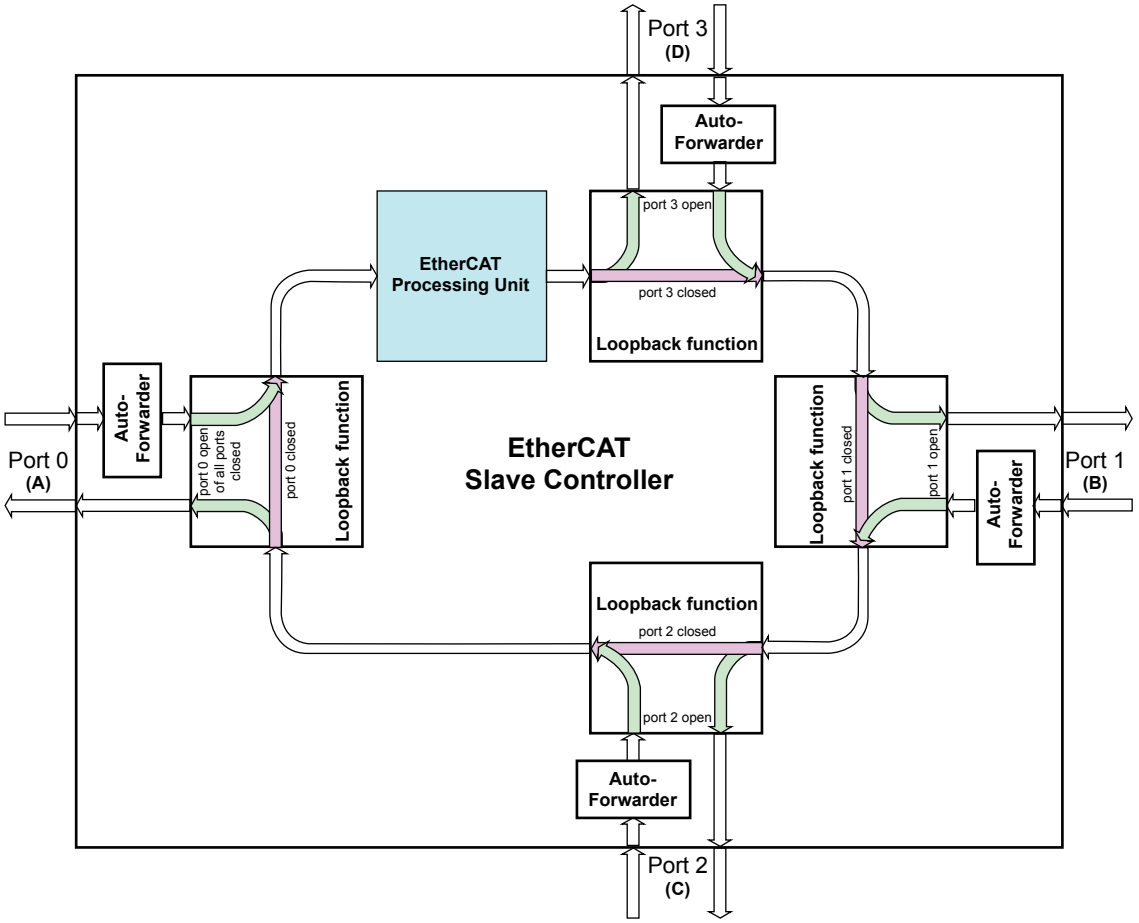


Figure 11.29: EtherCAT® auto forward and loopback ports

- **FMMU**
  An FMMU converts logical EtherCAT® frame data segment addresses to slave device physical memory addresses. FMMU's are configured by the master. FMMU's allow to use logical addressing for data segments that span multiple slave devices. Each FMMU always maps one cohesive logical address space to one cohesive physical address space.

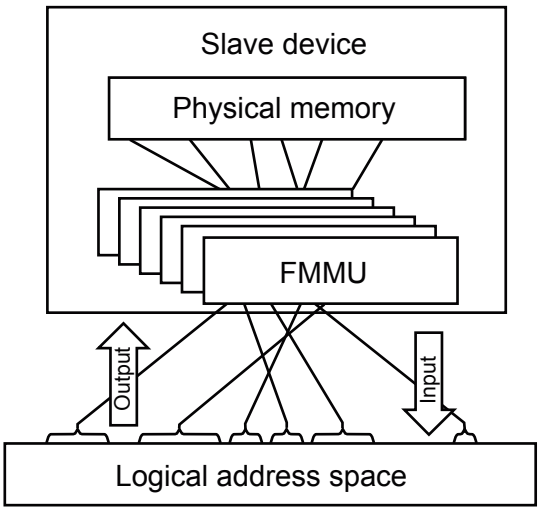


Figure 11.30: The FMMU mapping logical and physical memory addresses

- **SyncManager**
  A SyncManager controls the access to the slave´s physical memory. Each SyncManager channel defines a consistent area of physical memory. To use the slave´s physical memory in a coordinated fashion (e.g. to handle concurrent access of objects stored in physical memory), a SyncManager provides two ways of coordinated communication:
  1. Buffered mode, which allows consistent reading and writing in both directions. This mode is used for cyclic Process Data exchange.
  2. Mailbox mode, which enables interlocked communication. One entity fills in the data and the memory area is locked until the other entity reads out the data. This mode is used for on-demand data exchange.
- **Distributed Clocks**
  For synchronization a distributed clocks (DC) mechanism can be used, which leads to very low jitter, significantly less than 1 µs, even if the communication cycle jitters, which is equivalent to the IEEE 1588 Precision Time Protocol standard (PTP).

  The system clock is specified as a 64 bit counter with a base unit of 1 nanosecond starting at January 1, 2000, 0:00.

  For a detailed description of DC and its capabilities see [ETG.1000-4].

11.8.5 Application Layer

The EtherCAT® application layer provides user programs with means to access the underlying EtherCAT® field bus environment.

- **State Machine**
  Within the EtherCAT® protocol stack several state machines exist. From an EtherCAT® application's point of view the EtherCAT® State Machine (ESM) is the most important one. The role of the ESM is to inform the application about the communicative state of the underlying EtherCAT® field bus environment. Every EtherCAT® device (both master and slave) contains an ESM. The ESM reflects the current communicative state of an EtherCAT® device. Figure 11.31 shows all ESM states and possible state transitions.

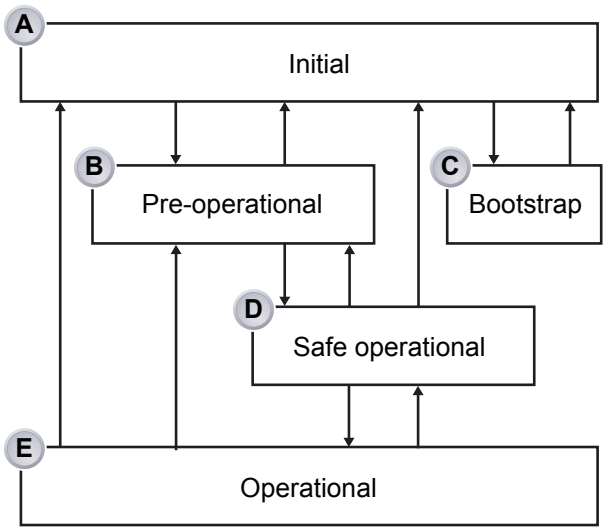


Figure 11.31: EtherCAT® State Machine diagram

A Init state
After EtherCAT® protocol stack initialization, the system enters the **Init** state. The **Init** state defines the root of the communication relationship between master and slave in the application layer. No direct communication between the master and slave is possible in this state. The master uses the **Init** state to initialize a set of slave configuration registers. If the slave supports mailbox communication, which Genesis systems do, the corresponding sync manager configurations are also done in the **Init** state.

B Pre-operational state
In the **Pre-operational** state mailbox communication is active. Both the master and slave can use the mailbox and the appropriate protocols to exchange application specific initializations and parameters. No process data communication is possible in this state.

C Bootstrap state
The optional Bootstrap state allows slave firmware downloads using the File over EtherCAT® (FoE) protocol.

D **Safe operational state**
In the **Safe operational** state the slave application provides current input data, but output data is not manipulated. The outputs are set to their “safe state”.

E **Operational state**
In the **Operational** state the slave application provides current input data and the master application provides current output data that manipulates the slave application’s outputs.

- **CoE**
  CoE is an EtherCAT® application layer protocol that defines a CANopen compatible infrastructure on top of EtherCAT®. All the performance advantages that EtherCAT® provides can be utilized by CoE. Both Process Data Objects (PDO) and Service Data Objects are supported providing cyclic and on-demand information exchange respectively. The CANopen Object Dictionary is also supported. CoE utilizes EtherCAT® mailbox communication to provide these services.

11.8.6 Setting up fieldbus output channels in GEN series mainframes

With Perception software it is possible to assign certain channels to be available on a fieldbus. The **R**eal-**T**ime **F**ormula **D**atabase (RT-FDB) channels can be configured for this purpose.

Note *Besides the RT-FDB channels, no other channel type can be published to the fieldbus.*

Real-time formula database

Perception 7.0 introduced channels that can be created by the real-time formula database. In short, these channels produce a user defined mathematical output. Inputs for this user defined math can be analog, Timer/Counter and event channels. The result of other RT-FDB channels can serve also as input. The example below shows a simple RT-FDB setup (see Figure 11.32).

Mainframe: MyMainframe | Resource usage: 1.84 % | Deployment status: Succeeded

Real-time Calculators Formula Database	Name	Expression	Units
MyMainframe			
1		Calculate the instantaneous power	
2	P_inst	MyEngine.U1 * MyEngine.I1 + MyEngine.U2 * MyEngine.I2 + MyEngine.U3 * MyEngine.I3	
3		Consider the cycle related results, using I1 as reference	
4	Filtered	@HWFilter(MyEngine.I1;1)	
5	Cycles	@CycleDetect(RTFormulas.Filtered)	
6	P_CycleBased	@CycleRMS(RTFormulas.P_inst; RTFormulas.Cycles)	Watt

Figure 11.32: Simple real-time formula database setup

Next to basic math like addition/subtraction, the RT-FDB formula database offers a wealth of predefined math. For more detailed information concerning RT-FDB formulas, please refer to the corresponding sections in the Perception manual.

RT-FDB channels can be made available on a fieldbus by selecting the associated check mark in the **Publish to...** column as shown in Figure 11.33.

Note *RT-FDB channels can be published to "CAN", "EtherCAT® or GENDAQAPI.*

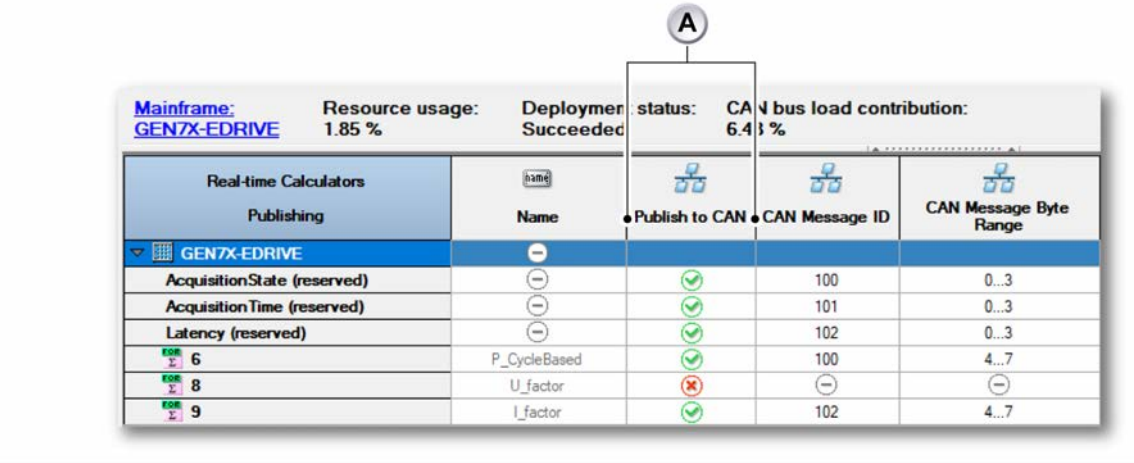


Figure 11.33: RT-FDB channels published to a fieldbus

A Publish to CAN column

Note *Not all RT-FDB channels can be published to the EtherCAT® bus. Only RT-FDB channels of the "Result type" {'Asynchronous', 'Scalar'} can be published.*

Preceding the RT-FDB channels that can be published, there are three reserved channels that can be published too:

Reserved channel	Meaning
Acquisition State	"1" if in Preview/Pause or Recording mode, "0" if not.
Acquisition Time [seconds]	Time at which the published samples are taken since start of Preview/Pause or Recording.
Latency [seconds]	Time between acquiring the samples and publishing the results.

11.8.7 Selecting the appropriate EtherCAT® configuration

A typical EtherCAT® slave has a “fixed” CoE object dictionary. This does not apply to a Genesis mainframe; during configuration the user can add/remove channels at will. Each change has impact on the object dictionary and ESI file. In turn this might require regeneration of the ENI file for the EtherCAT® master.

For the EtherCAT® bus two modes of operation are available:

- Static mode (see "Static mode" on page 187)
- Dynamic mode (see "Dynamic mode" on page 189)

Each mode has different behavior. The configuration modes (Static, Dynamic) can be set in the **EtherCAT configuration** column as shown below (Figure 11.34).

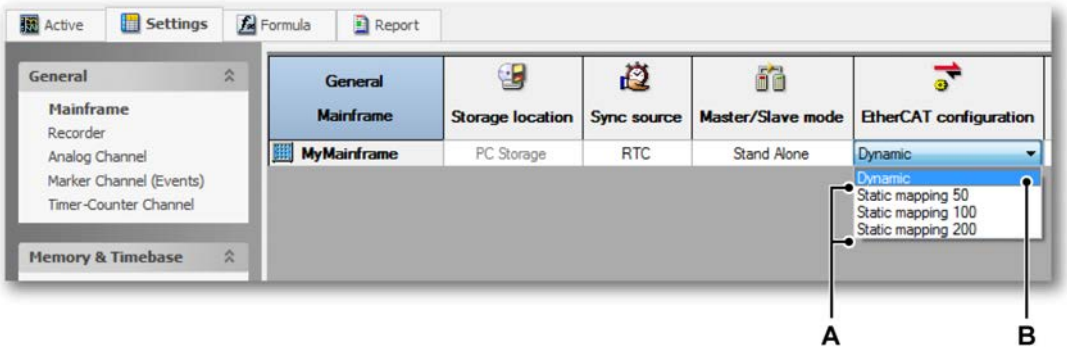


Figure 11.34: EtherCAT® configuration modes

A Static mode

B Dynamic mode

Static mode

In **Static mode** the CoE object dictionary contains a hard-coded layout of channels. It can be choosen between 50, 100 or 200 predefined channels. All CoE objects have predefined names like **Channel001**, **Channel002**, **Channel003**, … Each RT-FDB channel that is published to the bus is mapped on one of these predefined channels. This strategy allows to change the setup (or use different work benches) while still having the exact same ESI file. Therefore, no manual changes are required to the EtherCAT® master setup (e.g. ENI file), even when loading other workbenches.

Note *The Genesis EtherCAT® slave does update its internal CoE with all relevant RT-FDB channel name changes. This means that upon a bus scan in the master, the actual RT-FDB channel names would be available to the master.*

Figure 11.35 shows an example of a Static mode configuration. Only four RT-FDB channels were mapped to the bus. The remaining 47 channels are “present” in the CoE object dictionary but their values should be ignored.

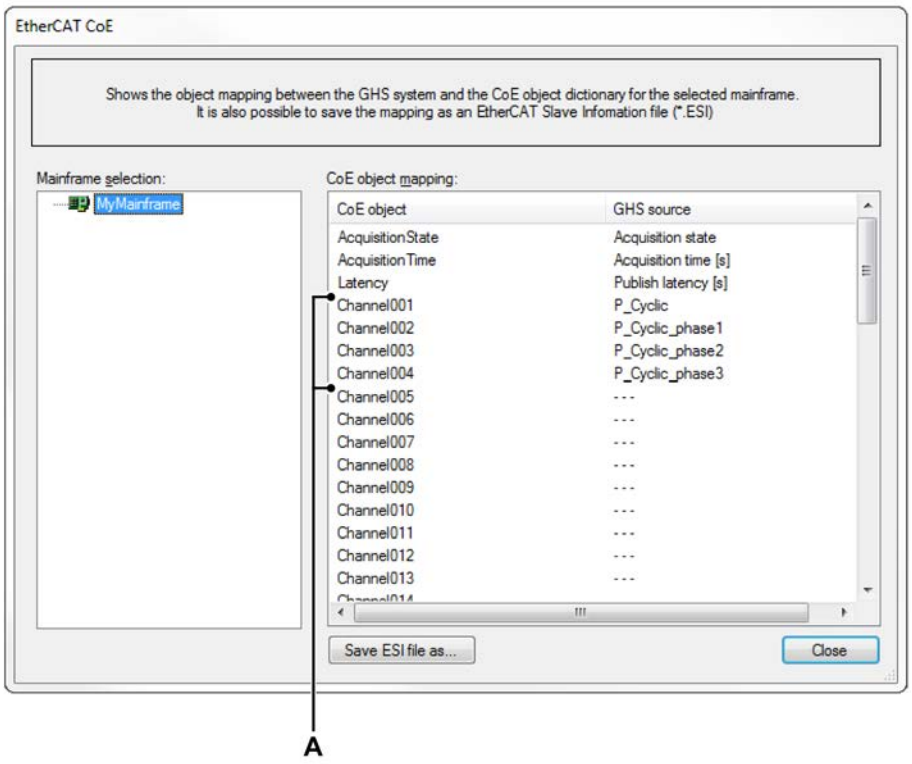


Figure 11.35: Example - Static configuration

A RT-FDB channels

HINT/TIP

Use Static mode when the workflow requires a one-time EtherCAT® master setup while still needing different Genesis setups at different times. Choose the proper amount of hard-coded channels necessary to capture all these different Genesis setups.

Dynamic mode

In **Dynamic mode** the CoE object dictionary contains an exact reflection of the RT-FDB channels that were selected for “EtherCAT® publishing”. Dynamic mode means that the CoE exactly follows the user defined published channels. The resulting ESI file also contains exactly these channels. As consequence each change in channel name or adding/removing of published channels (e.g. when loading a different virtual workbench) is reflected in the ESI file.
Figure 11.36 shows an example of a Dynamic mode configuration.

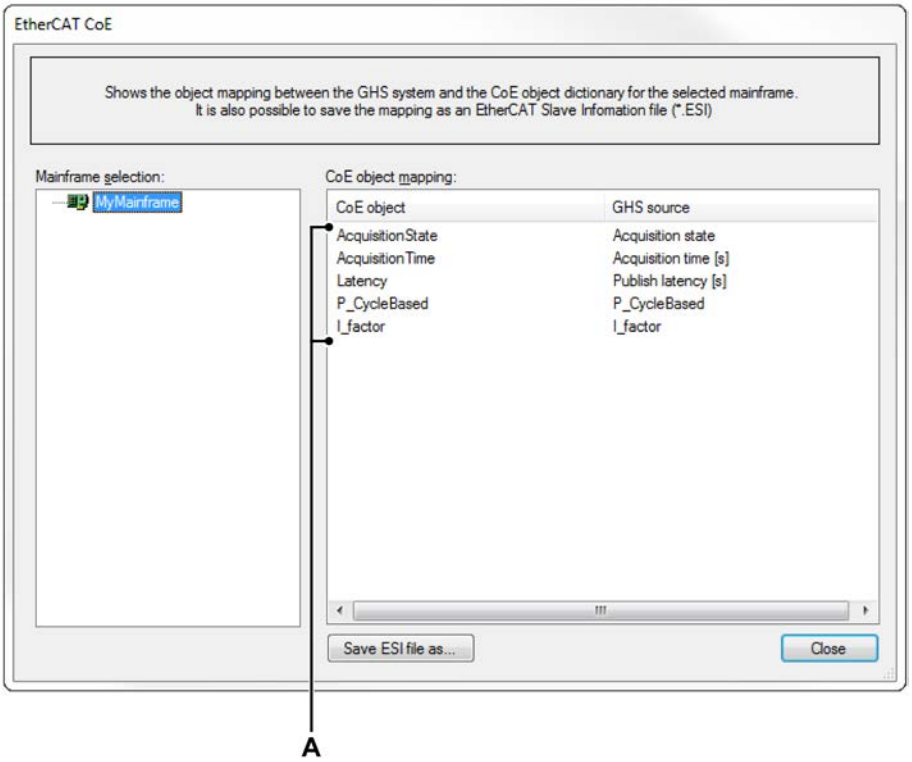


Figure 11.36: Example - Dynamic configuration

A User defined channels

HINT/TIP

Use the Dynamic mode when the setup is always the same (single virtual workbench) or when the EtherCAT® master can handle changing ESI files as part of the workflow. If the EtherCAT® bus load should be minimized (reduce PDO address space), the Dynamic mode is also the best mode to use.

11.8.8 CoE Object layout

Perception software offers control on which RT-FDB channels are published to the bus. Each RT-FDB channel that is flagged for publishing has an associated “object” in the CoE. In EtherCAT®, each “object” in turn has two “variables”. The table below shows the CoE object entry for an RT-FDB channel with name ”SomeChannel”.

Object	Variable	Type	Description
SomeChannel	Status	*USINT*	Status=0, Value should be ignored Status=1; Value is valid
SomeChannel	Value	*LREAL*	The sample value for this channel

Note *When the “Status” variable has the value “0”, the associated variable “”Value” is undefined. An EtherCAT® master software application must ignore the “Value” in that case!*

The following events within a Genesis mainframe will set the “Status” value to “0” (and invalidate the “Value”):

- The Genesis mainframe is in “idle” mode (does not apply to all hard-coded objects).
- The value of the associated RT-FDB channel should be ignored (e.g. due to an invalid “VNorm”).
- No cycles are detected for asynchronous RT-FDB channels.
- When EtherCAT® is in Static mode, all EtherCAT® channels that do not have a Genesis channel mapped to it have the “Status” value set to “0”.

A Genesis EtherCAT® slave also has some hard-coded objects in its CoE object dictionary. These objects and their meaning are listed in the following table.

CoE name	Type	Description
AcquistionState.Value	*USINT*	Value=0; mainframe in “Idle” mode Value=1, mainframe in “Recording” mode
AcquisitionTime.Value	*LREAL*	Indicates the exact mainframe time in seconds. Upon boot and when the mainframe enters “Recording” mode this value is reset to 0 sec.
Latency.Status	*USINT*	Status=0; Latency.Value is invalid and should be ignored Status=1; Latency.Value is valid
Latency.Value	*REAL*	All published RT-FDB channels are posted with the same fixed delay as indicated by this value. Units are in seconds.

11.8.9 EtherCAT® timing aspects

A Genesis EtherCAT® slave is designed to allow massive amounts of calculations (e.g., having 100 calculations running in parallel) while still keeping latency for all these results to a minimum. A Genesis EtherCAT® slave by default delivers all results to the bus with a fixed 1 millisecond (ms) latency. In different words: all results on the EtherCAT® bus represent the situation of exactly 1 ms ago. The reference for this depends on the applicable synchronization mode:

EtherCAT master sync mode	Latency is relative to…
Distributed Clocks	DC Sync0 signal
Sync manager Synchronized	SyncManager event signal

Note *Genesis EtherCAT® slaves do not support “Free running” mode.*

11.8.10 Fieldbus timing aspects

Certain types of RT-FDB formulas are “special” in the sense that they come with an additional **Latency**. The reason is that some formulas only can start processing all received samples upon receiving a new zero crossing. Perception indicates if/when this applies for a formula. Figure 11.37 shows an example, where @CycleFundamentalPhase() causes an additional latency increase of 60 us.

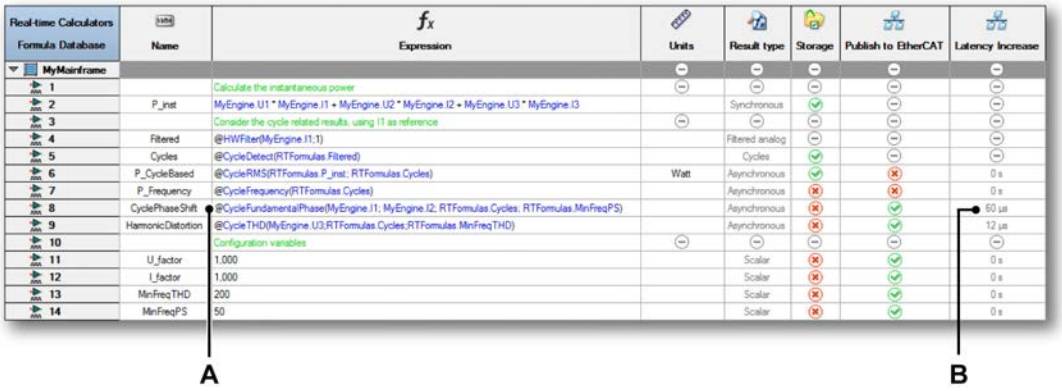


Figure 11.37: Fieldbus timing aspects

A Additional latency by formula @CycleFundamentalPhase()

B Latency increase value

A mainframe has a **System latency**. This is the sum of all formula latencies plus the offset of 1 ms. This **System latency** is available as a read-only mainframe setting (see Figure 11.38).

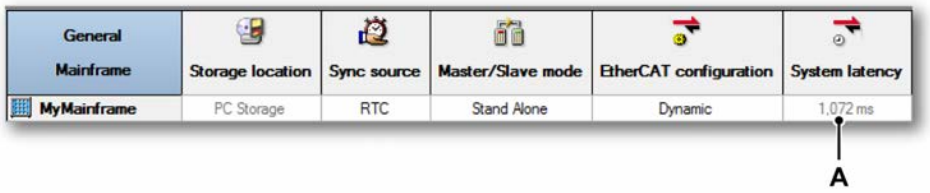


Figure 11.38: System latency

A System latency value

Note *All fieldbus channels are always published with the exact same “System latency”. This ensures that all data is published against the same clock.*

11.8.11 Aligning fieldbus latencies over multiple mainframes

As mentioned before, some formulas introduce an additional latency. The resulting “System Latency” might then differ for multiple mainframes. If these mainframes publish on the same fieldbus, the receiver would receive these samples from shifted clock domains.

Multiple mainframes can be delay aligned by **Extending latency**. The example below shows a setup of two mainframes with differing **System latency** (see Figure 11.39. The mainframe with lowest latency is latency extended to match the latency of the other mainframe. If the clocks of both mainframes are synchronized, both mainframes now publish to the fieldbus against the same clock.

Note *Latency cannot be extended beyond 30 milliseconds.*

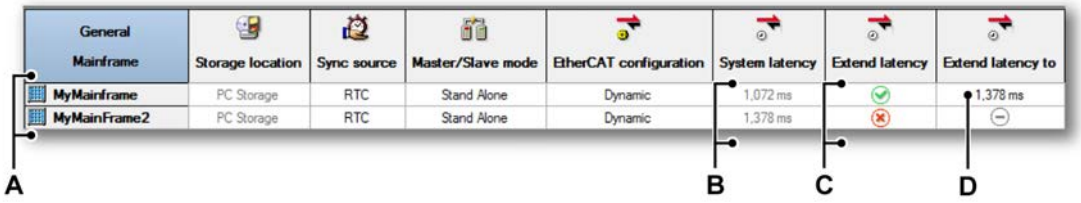


Figure 11.39: Multiple mainframes - delay aligned

A Multiple mainframes

B Differing system latency

C Delay aligned extended latency

D Lowest achievable latency with aligned mainframes

11.8.12 Supported EtherCAT® masters

The Genesis EtherCAT® software stack has been successfully tested against the following EtherCAT® masters/system integrators:

Vendor	EtherCAT® master/application
Beckhoff	Twincat
König PA	EtherCAT Studio
National Instruments	Veristand
Kristl & Seibt	Tornado
Kratzer	PATools
Siemens	CATS
MAHA	MAHA RT
Intest	Inova
ZF	Morpheé
AVL	Puma

11.8.13 EtherCAT® interfacing

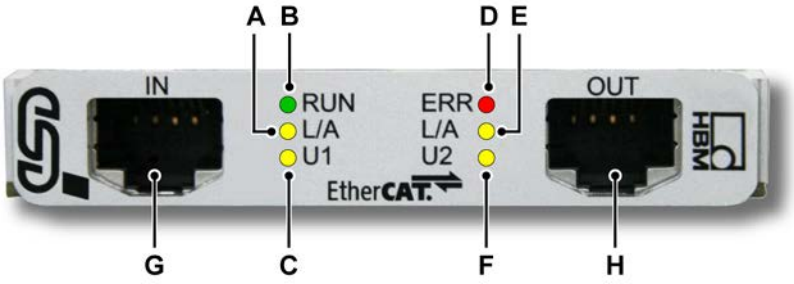


Figure 11.40: EtherCAT® Card with IN and OUT ports and status LEDs

A **L/A:** Link/Activity LED port IN

B **RUN:** Run LED

C **U1:** User 1 LED

D **ERR:** Error LED

E **L/A** Link Activity LED port OUT

F **U2:** User 2 LED

G EtherCAT® port **IN**

H EtherCAT® port **OUT**

The following table outlines how the status LEDs on the EtherCAT® card relate to the Genesis ESM state.

Table 11.5: Genesis ESM state versus status LEDs

Genesis ESM State	RUN status LED	L/A status LED	ERR status LED
Init	Off	Fast flashing	Off
Pre-operational	Slow flashing	Fast flashing	Off
Safe operational	Slower flashing	Fast flashing	Off
Operational	On	Fast flashing	Off
Operational → Init (after Perception introduced change in the CoE Dictionary)	–	–	On
Slave connected, but not included in master topology	Off	Fast flashing	Off

State machine

The ESM as described in Figure 11.31 is generic for all EtherCAT® slaves and masters. Normally ESM state transitions are always initiated by either the EtherCAT® master or slave. However, for Genesis systems, the actions performed in Perception trigger the state transitions to the *Init* state as depicted in Figure 11.41.

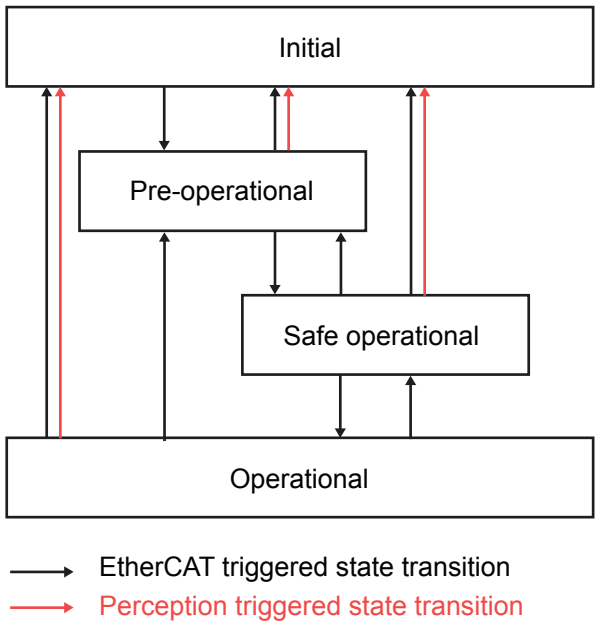


Figure 11.41: Genesis EtherCAT® State Machine diagram

Bootstrap state
The optional *Bootstrap* state as depicted in Figure 11.31 is not supported in Genesis systems.

Operational state
From an EtherCAT® perspective a Genesis system only provides inputs, no outputs. Since the **Operational** state only adds propagation of output compared to the **Pre-operational** state, for a Genesis system these two states have identical behavior.

Limitations
The EtherCAT® interface of a Genesis system has the following limitations:

- Multiple interface support
  Genesis systems support only one EtherCAT® interface module per system.
- Process data update interval
  The minimum supported cyclic Process Data update interval is 1 millisecond (e.g. the maximum update rate is 1 kHz).
- PDO Mapping

Note *The number of channels that can be mapped as CoE PDO is limited to 240.*

11.8.14 Troubleshooting

This chapter provides some pointers and guidelines for a selection of problems a user may experience while using the Genesis system in combination with EtherCAT®.

Situation:

- The EtherCAT® master is in the *Operational* state.
- The Genesis EtherCAT® slave is in the *Operational* state and transfers current values to the EtherCAT® master.

Symptoms:

- The Genesis EtherCAT® all of a sudden transitioned to the *Init* state.
- The EtherCAT® master no longer receives current values from the Genesis EtherCAT® slave.

Cause:

The reason for a Genesis system to transition from *Operational* to *Init* state is that its CoE Object Dictionary has changed.

Solution:

When Genesis is configured in Dynamic mode the EtherCAT® master must rescan the EtherCAT® fieldbus every time its CoE Object Dictionary changes.
For both the Static and Dynamic modes, the EtherCAT® master must request the mainframe to go to Operational mode (according to the EtherCAT® state machine definition as described in
Figure 11.31 "EtherCAT® State Machine diagram" on page 184).

11.9 Option - CAN FD out

With the **CAN out** option it is possible to output acquired data, processed by the Real-time Formula database, periodically on a CAN bus.

This chapter explains some general CAN principles and how to configure CAN output in the Perception software.

Table 11.6: Terms and abbreviations

Term/abbreviation	Description
CAN	Controller Area Network
CAN FD	CAN with flexible data rate
CiA	CAN in Automation
RT-FDB	Real-Time Formula Database

11.9.1 Option - USB to CAN FD out

CAN out is realized using an USB to CAN FD converter as shown in Figure 11.42.

Figure 11.42: USB to CAN FD converter

A Status LED

Note *The USB to CAN FD Converter is tested conform “CE ElectroMagnetic Compatibility (EMC) Directive 2004/108/EC” as “Information Technology Equipment” using EN-55022 and EN-55024 standards.*

Note *To use the USB to CAN FD converter a free USB port is needed on the GEN series mainframe. If no USB port is available on the GEN series mainframe it is possible that it can be made available by a USB port cover replacement. Please contact custom systems at: customsystems@hbm.com.*

Note *The USB to CAN FD converter is only used for the option CAN **out**, this means that currently data can only be output via the converter, CAN input via the USB to CAN FD converter is **not** possible.*

The following table shows the different states indicated by the status LED in the converter.

Status LED of USB to CAN FD converter

Color/status	Meaning	Remark
Green / on	Driver is connected to the USB to CAN FD converter.	Occurs during boot, automatically switches to next state.
Green / slow blinking	Application is connected to the USB to CAN FD converter.	Normal condition when USB to CAN FD converter is ready to use.
Green / fast blinking	Data is transmitted via the USB to CAN FD converter.	Normal condition when USB to CAN FD converter is in use.
Red / blinking	An error is occurring during the transmission of CAN data.	Automatic recovery takes place when the error condition is removed.
Orange / fast blinking	Identification of the USB to CAN FD converter.	Not implemented in GEN Series software.

The physical connection to the CAN bus is realized with a USB to CAN FD converter as shown in Figure 11.42 on page 198.

The pin assignment of the 9 pin male D-Sub connector of the USB to CAN FD converter is shown in Figure 11.43.

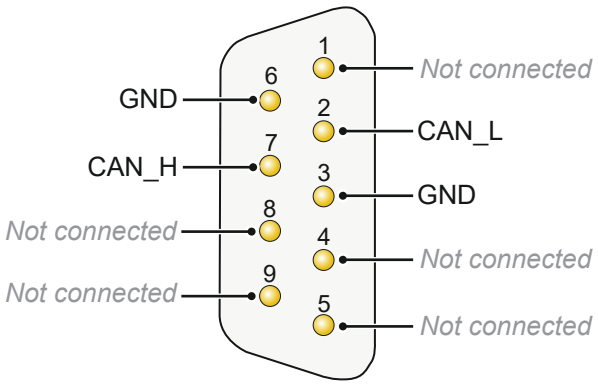
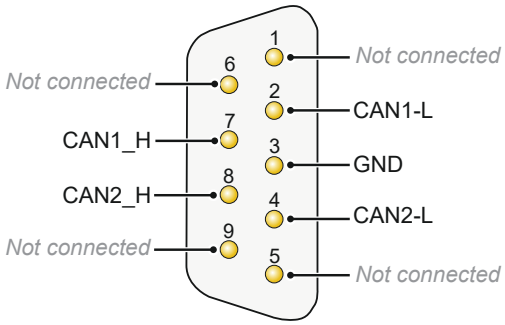


Figure 11.43: Pin assignment of the D-Sub connector of the USB to CAN FD converter

The CAN bus connection via D-Sub, 9-pin is in accordance with CiA® 303-1.

11.9.2 Option carrier card with integrated CAN FD controller (Customer special)

The GHS system supports the PEAK CAN FD mPCIe modules. These CAN modules can be mounted into the GHS and connected via the PCIe bus to the mainframes. The GEN2tB and GEN4tB support this directly on the interface module, for customer specials the OCC can be used to connect this CAN device.



For more information, please refer to chapters "CAN generic principles" on page 201 and "CAN Trouble-shooting" on page 405.

11.9.3 CAN generic principles

CAN is a message oriented multi-master messaging protocol for quick serial data exchange. It is developed in the early 1980's and became an international standard in 1994 (ISO 11898). It is used for communication between electronic devices in automotive and factory automation.

CAN FD is an enhanced version of the CAN protocol which supports larger payloads and higher data rates, fulfilling the requirements for higher bandwidth networks. More specifically, the option CAN out is configured to be compliant to ISO CAN FD according to ISO standard 11898-2.

This CAN specification only describes the lower two layers of the OSI model, see Figure 11.44.

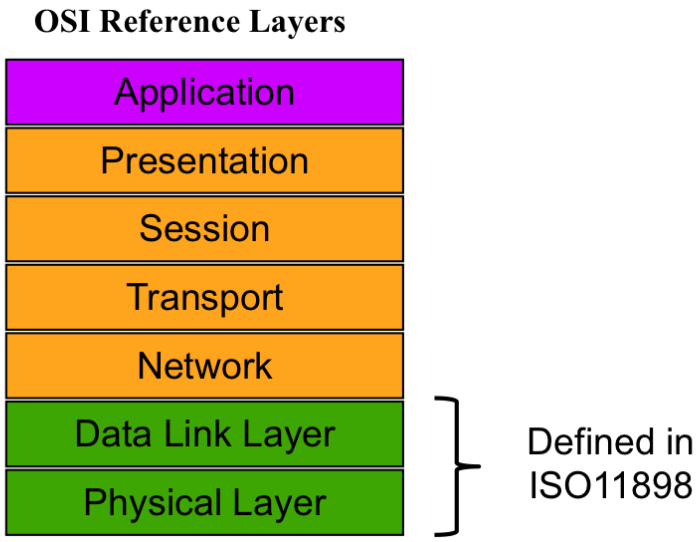


Figure 11.44: OSI layers defined by CAN

For more information about "Data link layer" and "Physical layer", please refer to "Data link layer" on page 203 and "Application layer" on page 205.

11.9.4 Physical layer

A twisted-pair copper cable with common ground is normally used as the physical transmission medium. Signal levels are according to ISO 11898-2 and are shown in Figure 11.45.

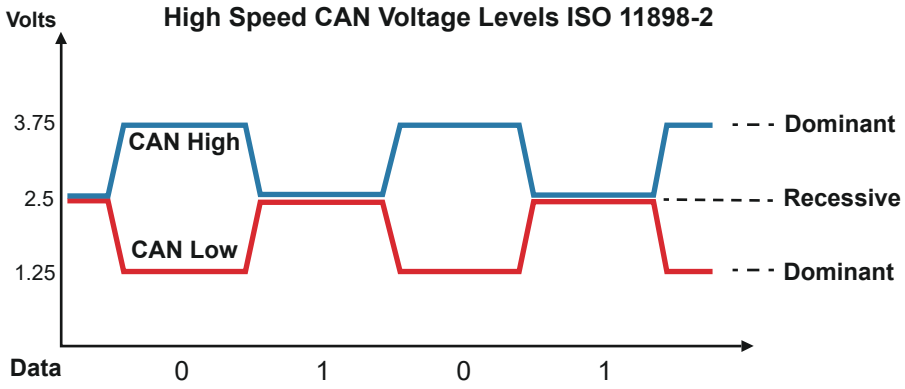


Figure 11.45: Signal levels

11.9.5 Data link layer

The CAN data link layer distinguishes between CAN frames with 11 bit identifiers (base frames) and CAN frames with 29 bit identifiers (extended frames). Currently only base frames are supported by the CAN out option. There is also a distinction between **CAN 2.0** and **CAN FD**. These types are both supported and can be selected in the mainframe setup dialog in the **CAN bus mode** section (see Figure 11.46).

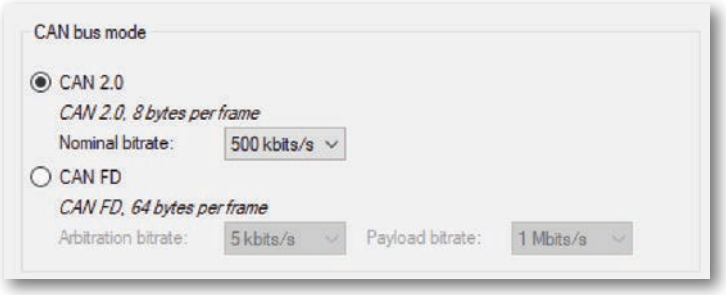


Figure 11.46: Selection of CAN bus mode

The layout of both types of message frames is shown below in Figure 11.47.

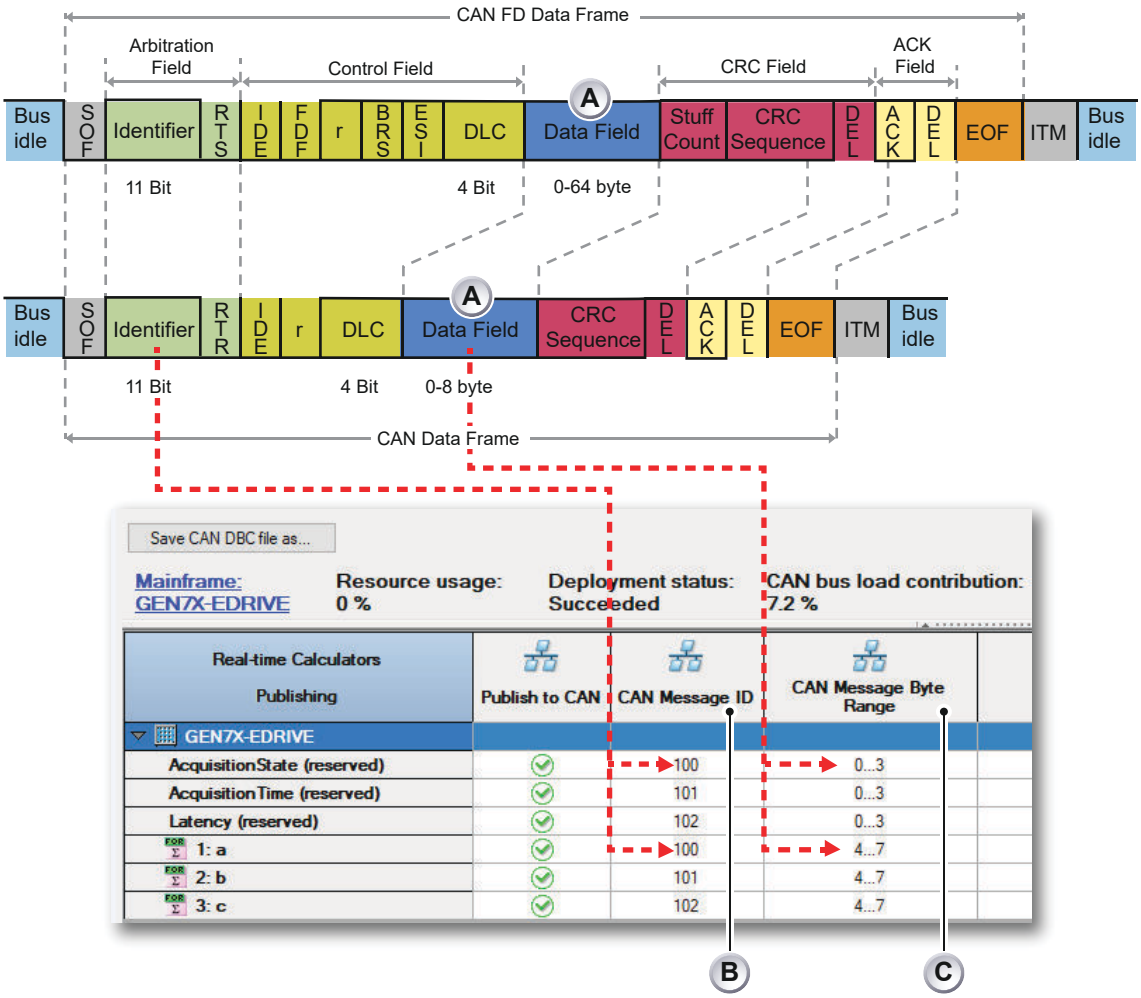


Figure 11.47: CAN 2.0 and CAN FD frame in relation to the publish settings in the Perception software

A Data Field

B CAN Message ID

C CAN Message Byte Range

With the **CAN message ID (B)** the identifier of the CAN message is selected. With the **CAN Message Byte Range (C)** the position of the value published on the CAN bus within the **Data Field (A)** is selected. Please note that the same **CAN message ID** can be used multiple times since multiple values can be published in one CAN message. All signals are published on the CAN bus as a 32 bit floating point values. That means that CAN 2.0 frames can contain one or two signals while CAN FD frames can contain up to 16 signals.

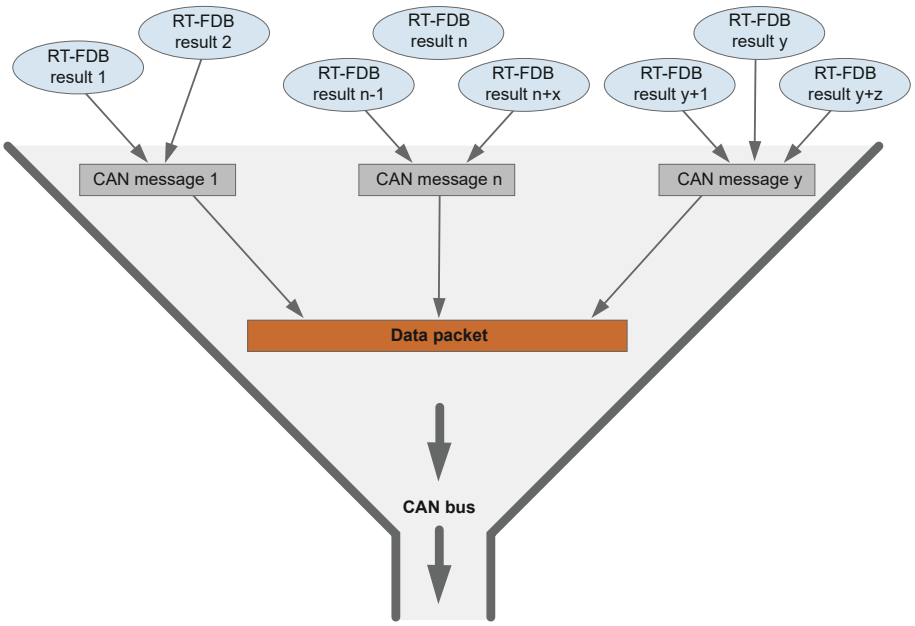


Figure 11.48: CAN bus load contribution

Multiple RT-FDB results can be sent in one CAN 2.0 or CAN FD message, multiple CAN 2.0 or CAN FD messages are combined to a data packet which is published on the CAN bus. A data packet is attempted to be published at the CAN bus completely, even if it is interrupted by a higher priority CAN message.

Depending on the CAN bus mode, bitrate, update rate, number of CAN messages and number of RT-FDB results per CAN message a certain number of RT-FDB results can be published on the bus. The percentage of the bus which will be used by the CAN messages output by the mainframe is shown (see Figure 11.48).

11.9.6 Application layer

Note *The application level support for CAN only assists composing raw CAN messages.*

11.9.7 Setting up CAN channels in Genesis

With Perception software it is possible to publish certain channels to the CAN bus. How to do this is explained in chapter "Setting up fieldbus output channels in GEN series mainframes" on page 185.

11.9.8 Selecting the appropriate CAN configuration

The CAN bus behavior of the GEN series mainframe can be configured in the **CAN Bus Setup** dialog (see Figure 11.49).

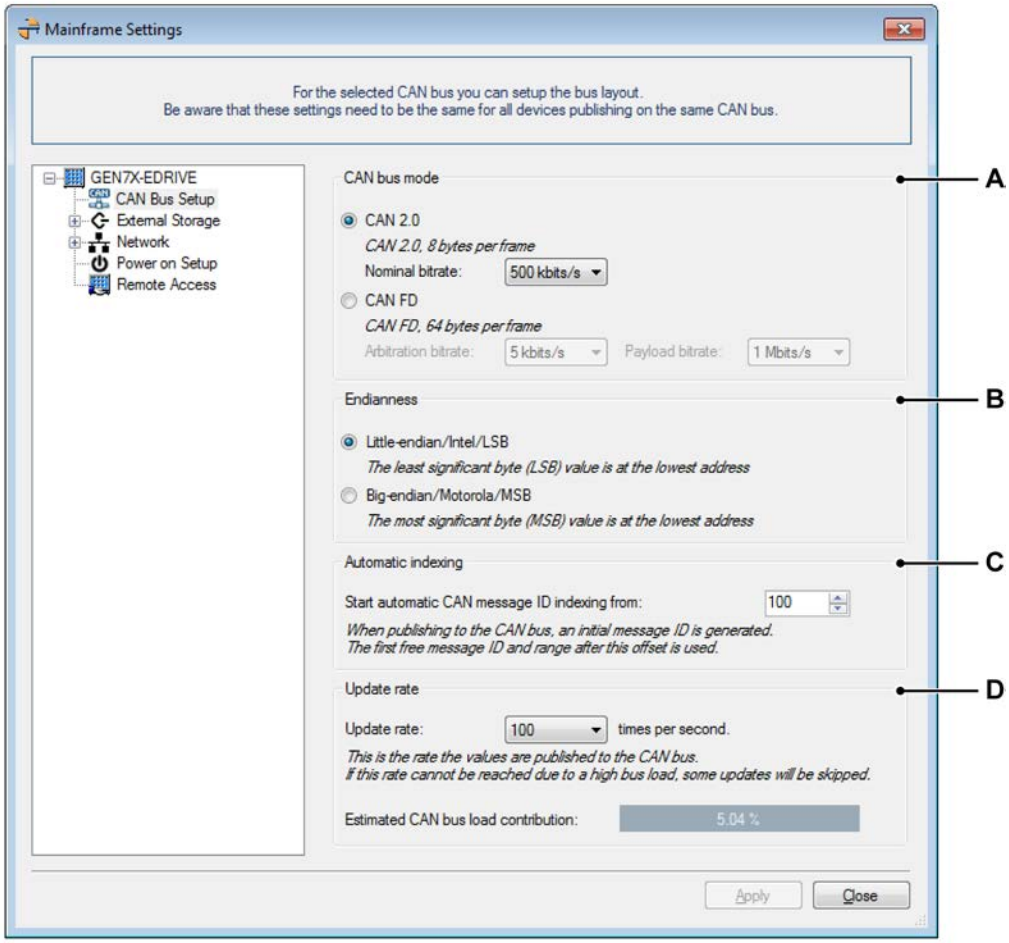


Figure 11.49: CAN Bus setup dialog

A With the **CAN bus mode** the type of CAN messages are selected, **CAN 2.0** or **CAN FD**. In table below the possible nominal bitrates of CAN 2.0 or Arbitration- and Payload bitrates for CAN FD are listed.

Table 11.7: Possible bitrates

CAN 2.0	**CAN FD**	
Nominal bitrate	**Arbitration bitrate**	**Payload bitrate**
5 kbits/s	5 kbits/s	1 Mbits/s
10 kbits/s	10 kbits/s	2 Mbits/s
20 kbits/s	20 kbits/s	4 Mbits/s
100 kbits/s	100 kbits/s	6 Mbits/s
125 kbits/s	125 kbits/s	10 Mbits/s
250 kbits/s	250 kbits/s	12 Mbits/s
500 kbits/s	500 kbits/s	-
800 kbits/s	800 kbits/s	-
1 Mbits/s	1 Mbits/s	-

B With **Endianness** the byte order of the floats within the message is selectable between little endian or big endian.

C **Automatic indexing** is used to configure the index of the first CAN message on the CAN bus, next messages are, by default, assigned the next free position on the CAN bus (from the mainframe's point of view) where first CAN message byte range is increased and then the CAN message ID.

D The **Update rate** controls the rate at which all CAN messages are put on the bus. The table below lists the possible update rates.

Table 11.8: Possible update rates

Update rate
1 time per second
5 times per second
10 times per second
50 times per second
100 times per second
500 times per second

11.9.9 CAN DBC file

When signals are configured to be output on the CAN bus, Perception software offers functionality to store the configured channels in a vector CAN database, a DBC file. A DBC file contains definitions of CAN messages and signals. The DBC format is proprietary of Vector Informatik GmbH.

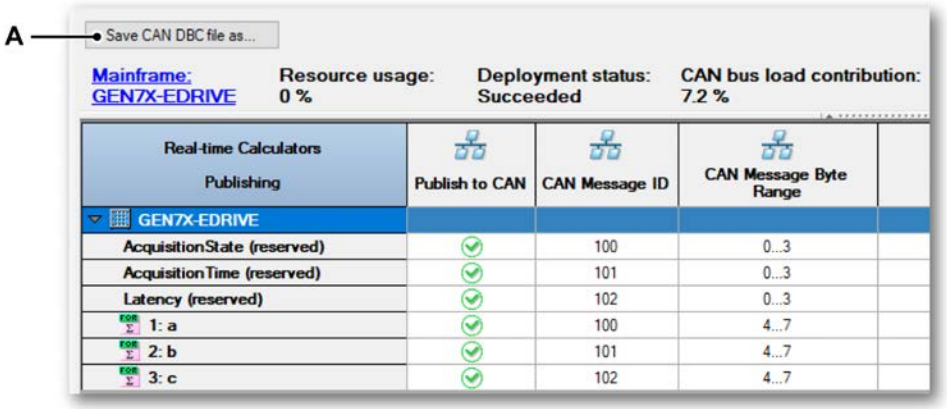


Figure 11.50: Save as CAN DBC file

A Button to save CAN DBC file

Below the content of the ".dbc" file of the configuration of Figure 11.50 is listed.

```
VERSION ""

NS_ :
                SIG_VALTYPE_
                CM_
BS_:

BU_: GenesisMainframe

BO_ 100 GENSeriesData: 8 GenesisMainframe
SG_ AcquisitionState : 0|32@1+ (1.000000,0.000000)
[0.000000|0.000000] "-" Vector__XXX
SG_ a : 32|32@1+ (1.000000,0.000000) [0.000000|0.000000]
"" Vector__XXX

BO_ 101 GENSeriesData: 8 GenesisMainframe
SG_ AcquisitionTime : 0|32@1+ (1.000000,0.000000)
[0.000000|0.000000] "seconds" Vector__XXX
SG_ b : 32|32@1+ (1.000000,0.000000) [0.000000|0.000000]
"" Vector__XXX

BO_ 102 GENSeriesData: 8 GenesisMainframe
SG_ Latency : 0|32@1+ (1.000000,0.000000) [0.000000|
0.000000] "seconds" Vector__XXX
SG_ c : 32|32@1+ (1.000000,0.000000) [0.000000|0.000000]
"" Vector__XXX

CM_ " TEST ";

SIG_VALTYPE_ 100 AcquisitionState : 1;
SIG_VALTYPE_ 100 a : 1;
SIG_VALTYPE_ 101 AcquisitionTime : 1;
SIG_VALTYPE_ 101 b : 1;
SIG_VALTYPE_ 102 Latency : 1;
SIG_VALTYPE_ 102 c : 1;
```

11.9.10 CAN timing aspects

Signals are published on the CAN bus at a rate specified by the update rate (Figure 11.51). The published signals are all sampled against the same timestamp. Example: when the update rate is set to 10 times per second, there will be updates on the bus against the exact timestamps:

- t = 0
- t = 100 ms
- t = 300 ms
- etc.

Independent of the update rate, two timing aspects are important to know:

- After calculation of all data of a snapshot is finished, publishing CAN messages of this snapshot to the CAN bus must be initiated within 25 ms.
- After initiating publishing CAN messages on the bus, publishing can be delayed for maximum 100 ms before it is cancelled.

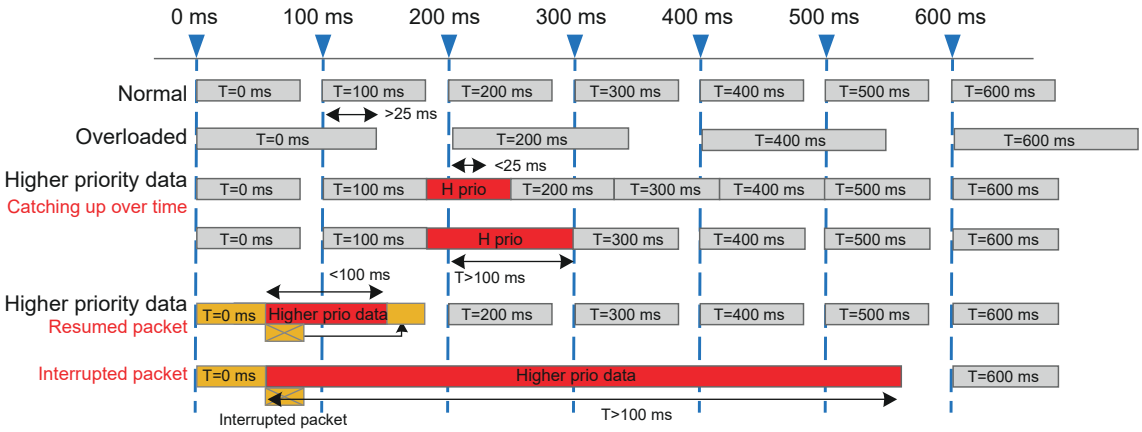


Figure 11.51: CAN message timing

After sampling the data, output to the CAN bus is started after a certain period of time. This period depends on the RT-FDB calculations that are executed. More on this is explained in chapter "Fieldbus timing aspects" on page 192.

11.9.11 More CAN timing aspects

For more information about CAN timing aspects, please refer to chapters "Fieldbus timing aspects" on page 192 and "Aligning fieldbus latencies over multiple mainframes" on page 193.

11.9.12 Working with CAN out

In order to use CAN out when using a USB to CAN FD converter, a GEN series mainframe must be booted with a USB to CAN FD converter plugged into the USB port. If the USB to CAN FD converter is plugged in after the mainframe was booted Perception software shows the next message if or when connected to the mainframe. When using the integrated CAN FD controller this is not an issue.

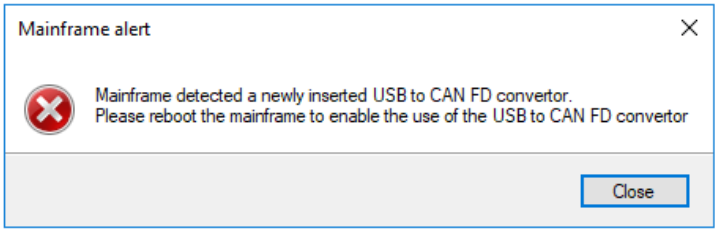


Figure 11.52: Mainframe alert of newly inserted USB to CAN FD converter

When the mainframe is booted with a USB to CAN FD converter connected, the converter is visible in the hardware tree in Perception (see Figure 11.53).

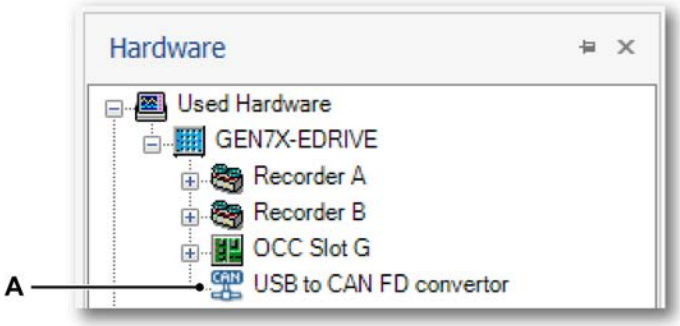


Figure 11.53: USB to CAN FD converter in the hardware tree

A USB to CAN FD converter

Publishing to GEN DAQ API, CAN and EtherCAT® is mutual exclusive. The table below shows the possible publish options.

Table 11.9: Possible output with CAN, EtherCAT® or GENDAQAPI

GEN DAQ API	CAN	EtherCAT®	Possible to publish to
✓	✗	✗	GENDAQAPI
✓	✓	✗	CAN
✓	✗	✓	EtherCAT®
✓	✓	✓	CAN

11.9.13 CAN Trouble-shooting

Please refer to chapter "CAN Trouble-shooting" on page 405.
This chapter provides some pointers and guidelines for a selection of problems a user may experience while using the GEN series mainframe in combination with the option CAN out.

12 Input Cards

12.1 Available input cards

Model overview (Part 1)

Model	Basic	Basic sensor	Bridge	IEPE	Piezoelectric	RTD	Thermocouples	Current loop	Galvanic isolation	Analog resolution [Bits]	Maximum sample rate [S/s] (not multiplexed)
GN310B	✓								✓	18	2 M
GN311B	✓								✓	18	200 k
GN610B	✓								✓	18	2 M
GN611B	✓								✓	18	200 k
GN815	✓			✓					✓	18	2 M
GN816	✓			✓					✓	18	200 k
GN840B	✓	✓	✓	✓	✓	✓	✓	✓	✓	24	500 k
GN1640B	✓	✓	✓	✓	✓	✓	✓	✓	✓	24	500 k
GN1202B	✓									14	100 M
GN8101B	✓									14	250 M
GN8102B	✓									14	100 M
GN8103B	✓									14	25 M
GN3210	✓			✓	✓					24	250 k
GN3211	✓									24	20 k

Model overview (Part 2)

Model	Analog channels / card	Analog resolution [Bits]	Maximum sample rate [S/s] (not multiplexed)	Digital events / card	Digital Timer/Counters / card	Memory / card (Shared by channels)	Standard streaming	Fast Streaming	Slot width
GN310B	6	18	2 M	16	2	2 GB		✔	1
GN311B	6	18	200 k	16	2	2 GB		✔	1
GN610B	6	18	2 M	16	2	2 GB		✔	1
GN611B	6	18	200 k	16	2	2 GB		✔	1
GN815	8	18	2 M	16	2	2 GB	✔	✔	1
GN816	8	18	200 k	16	2	200 MB	✔	✔	1
GN840B	8	24	500 k	16	2	2 GB		✔	1
GN1640B	16	24	500 k	16	2	2 GB		✔	2
GN1202B	(1)	(1)	100 M	16	2	8 GB		✔	1
GN8101B	8	14	250 M	16	2	8 GB		✔	1
GN8102B	8	14	100 M	16	2	8 GB		✔	1
GN8103B	8	14	25 M	16	2	8 GB		✔	1
GN3210	32	24	250 k	16	2	2 GB	✔		1
GN3211	32	24	20 k	16	2	200 MB	✔		1

(1) 12 Optical fiber transmitter channels supported. For details see table "Optical Fiber Transmitter Channels" on page 215.

Optical Fiber Transmitter Channels

Transmitter
Every transmitter is a single channel unit. Every unit has an unbalanced differential input, amplifier, analog anti-alias filter and ADC with an optical data and control link to the receiver card. The receiver card has the recording logic, sample rate selection and memory.

Model	Receiver card	Power	Sample rate	Resolution	Isolation
GN110	GN1202B	Battery	100 MS/s	14 bit	User application defined
GN111	GN1202B	Battery	25 MS/s	15 bit	User application defined
GN112	GN1202B	120/ 240 V AC	100 MS/s	14 bit	1800 V RMS
GN113	GN1202B	120/ 240 V AC	25 MS/s	15 bit	1800 V RMS

12.2 GN310B (2 MS/s), GN311B (200kS/s) Power Analyzer input cards

- **Accuracy 0.015% of reading, 0.02% of range**
- **3 power channels (U and I)**
- **5 voltage ranges up to ± 1500 V DC**
- **7 current ranges up to ± 2 A**
- **2 Digital channels for torque and speed**
- **Real-time computations of RMS, P, S, Q, λ, η, cosφ, THD, i_alpha, i_ beta and more**
- **Full bandwidth power calculations**
- **Fundamental power calculations**
- **Phase matched anti-alias protection**
- **1 ms latency real-time output**
- **18 bit at 2 MS/s (200 kS/s) sample rate**
- **Triggering on real-time power results**

The power card GN310B offers three power channels, each one consisting of one voltage input and one current (or voltage) input. The voltage inputs start at ± 50 V to ± 1500 V in five ranges, allowing to scale the inputs to best match your signal level to achieve minimum measurement uncertainty.
The current inputs start at ± 75 mA to ± 2 A, in seven range and uses internal burden resistors to support all common zero flux current transducers on the market. All current inputs can be switched to “voltage mode” to connect current clamps or Rogowski coils.
Tested up to 7.4 kV, the isolation allows for safe measurements up to 1000 V CAT IV and 1500 V DC.
Full wide band power measurements allows for optimum efficiency calculations, where the optional unique multi stage anti-alias digital Bessel / Butterworth or Elliptic filters using 11 or 12 orders guarantees superior phase match, ultra-low noise and alias free results in noisy environments.
The two Timer/Counters and the G070A torque/RPM adapter allow for direct interfacing to HBM torque transducers or other torque and speed sensors.
The real-time formula database offers predefined or custom analysis. Power calculations like RMS, P, Q, S, cosφ, λ, or η come out of the box, be it for wideband signals or the fundamental only. Advanced formulas allow real-time transformations to obtain α and β space vectors or d, q currents of an electric drive system. All results can be transferred to an automation system in real-time using GEN DAQ API and the optional CAN FD or EtherCAT® (1 ms latency) interfaces of the mainframe.

For specification and ordering information, please refer to the GEN310B/ GN311B data sheet.

12.2.1 Measuring voltages

WARNING

High bandwidth and measurement cabling

Due to the high bandwidth measurement capabilities of the acquisition card, combined with the high measurement sensitivity of the card, it is important to pay close attention to the measurement cabling.

Some advice to prevent measuring unwanted disturbances:

- Keep measurement cables as short as possible in order to reduce the reception of environmental disturbances.
- Use shielded cables. The cable should have the measurement cables paired inside a shield. Preferably, the shield should be connected to the chassis of the measurement Genesis High Speed equipment. Alternatively, the shield could also be connected to the chassis of the object under test.

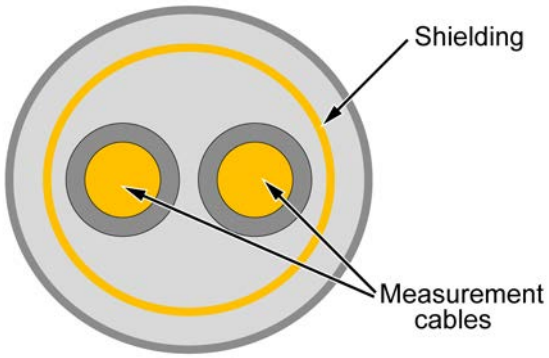


Figure 12.1: Shielded cable principles

HBM KAB290 cables are designed to meet this setup:

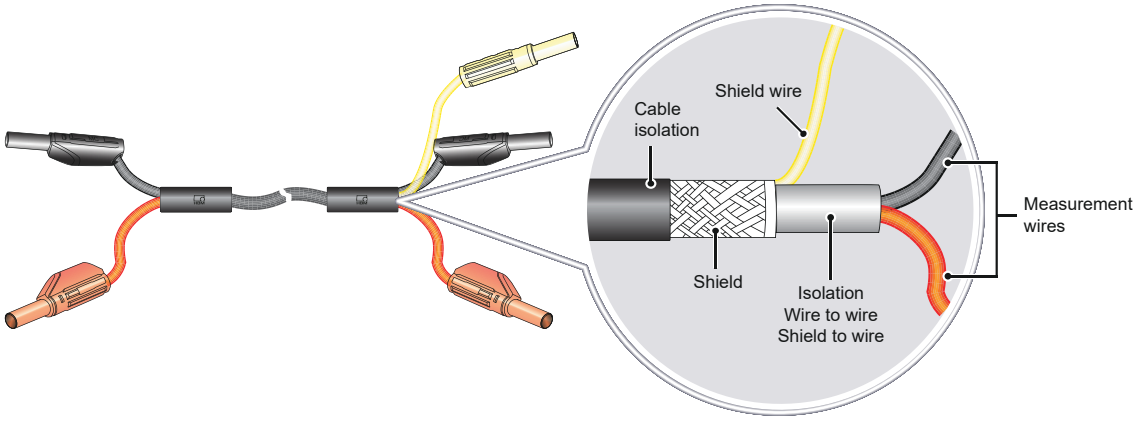


Figure 12.2: Shielded cable setup

More KAB290 details can be found in the GN310B/GN311B data sheet specifications.

- For high frequency disturbances where high bandwidth measurement is not required, the measurement bandwidth can be reduced by using the lowpass filter of the acquisition card.
- If unshielded cables are used, keep them as close together as possible, i.e. position them next to each other (to keep the loop small).
- Make sure that measurement cables that are used for measuring high dynamic or distorting signals are not closely positioned to measurement cables used for measuring small sensitive signals.
- Keep all measurement cables well separated from cables connected to high switching loads or motor cables.
- Separate measurement equipment and cables from potentially interfering equipment like frequency inverters or wireless equipment.

General cabling remark: Only use properly rated cables to measure the signal. Both the voltage and current rating should be matched to the signal for measurements.

WARNING

This instrument must be properly grounded.

When using this card, HBM advise using the standard GEN series protective ground connections to ensure that the entire unit is grounded.
Please see section "Connecting power" on page 64 for further details.

WARNING

Overvoltage and current protection

All voltage inputs are protected against voltage overload and current inputs against current overload. This is specified for the high voltage channels at ± 2 kV DC.

- Current inputs 2.5 A peak for all current ranges.
- Low voltage inputs 60 V peak for all ranges.

Exceeding these limits, particularly when connected to potentially high-current sources, can cause severe damage that is not covered by the manufacturer's warranty.

WARNING

Disconnect voltages before removing the card from the system.

The measuring circuit can carry hazardous voltages and should be disconnected before the card is removed from the card slot of the measurement system.

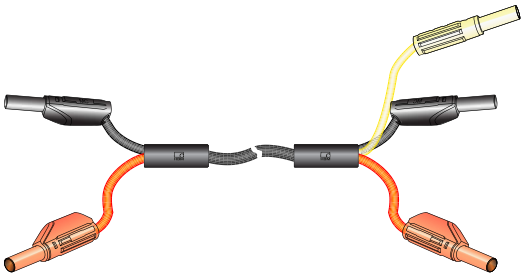
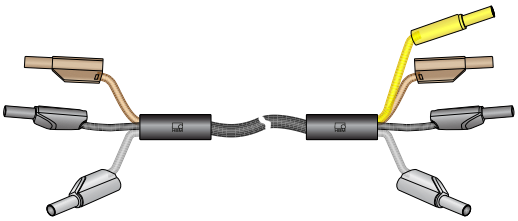
WARNING

High voltage and qualified personnel

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that all cards with working voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience, as well as their knowledge of the relevant provisions, are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

WARNING

Connectors and cables

Rating	Connectors	Example
≤ 60 V DC, ≤ 30 V RMS		Not recommended by HBM
≤ 600 V CAT		HBM KAB290
		HBM KAB2128
≤ 1000 V CAT IV, ≤ 1500 V DC CAT III		Stäubli: XMF-419

12.2.2 Connecting 3 Phase Artificial Star Adapter

Insert the Star Adapter into the GN310B/GN311B card **COMPLETELY** before applying high voltage to the Star Adapter.

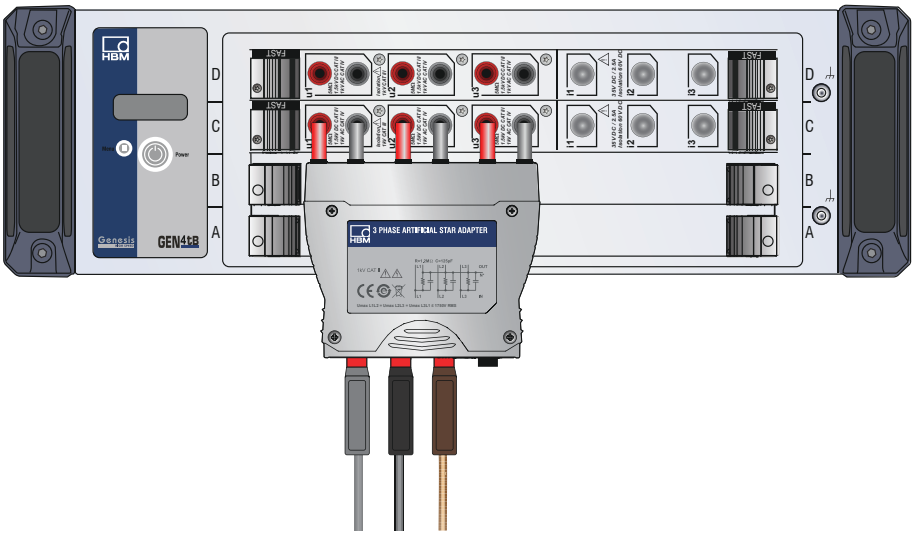
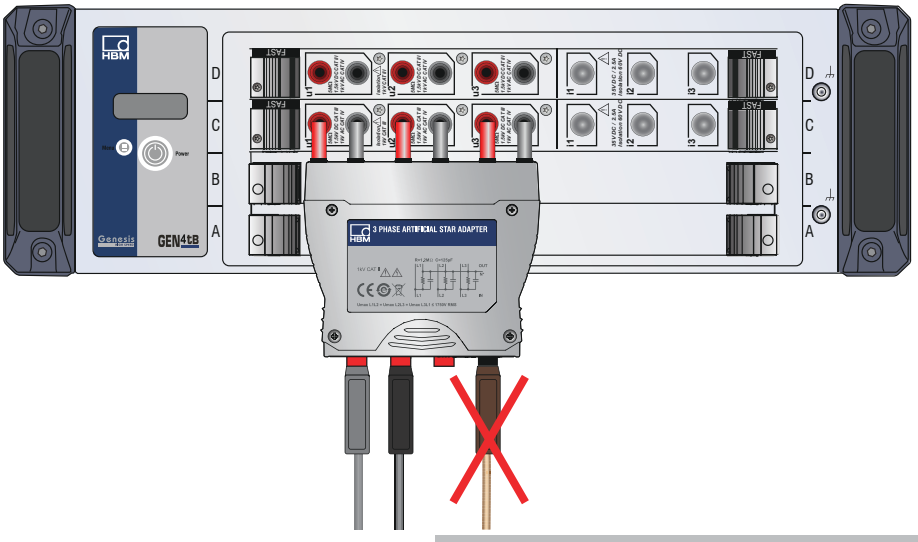


Figure 12.3: Artifical Star Adapter connections procedure (1)



Do **NOT** connect a phase signal to the Star Adapter neutral **N*** pin.

Figure 12.4: Artifical Star Adapter connections procedure (2)

A typical setup could look like this:

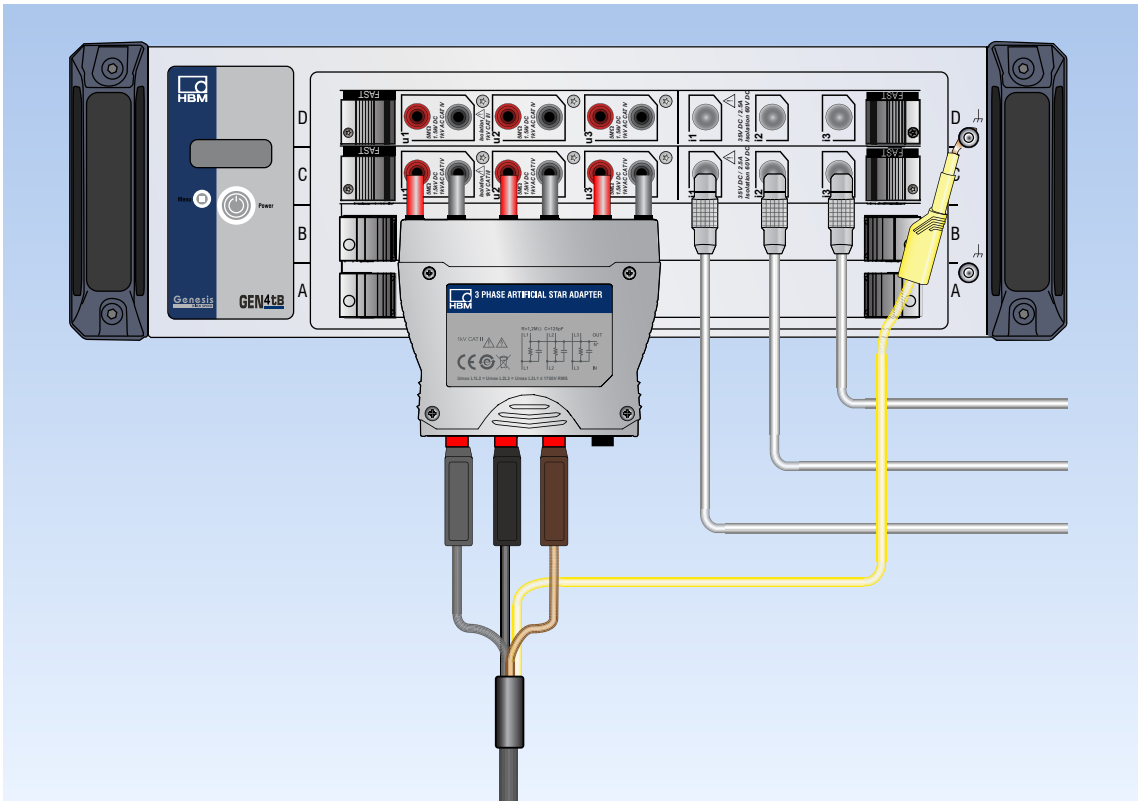


Figure 12.5: GN310B/GN311B Power card connection

12.2.3 Measuring currents

The GN310B/GN311B card offers 3 current channels using a 4-pin LEMO connector.

The current channels offer two ways of measuring current:

1. Current as **current** input to two built-in shunt resistors.
   Typically used for current transducer measurements.
2. Current as **voltage** input.
   Typically used for current probe measurements.

The next sections explain how to use the current channels in specific setups.

Characteristics current channel:

- The input Lemo connector outer shell is connected to the system ground for shielding purposes.
- The isolated ground is externally accessible and is current return line, as shown in Figure 12.6.

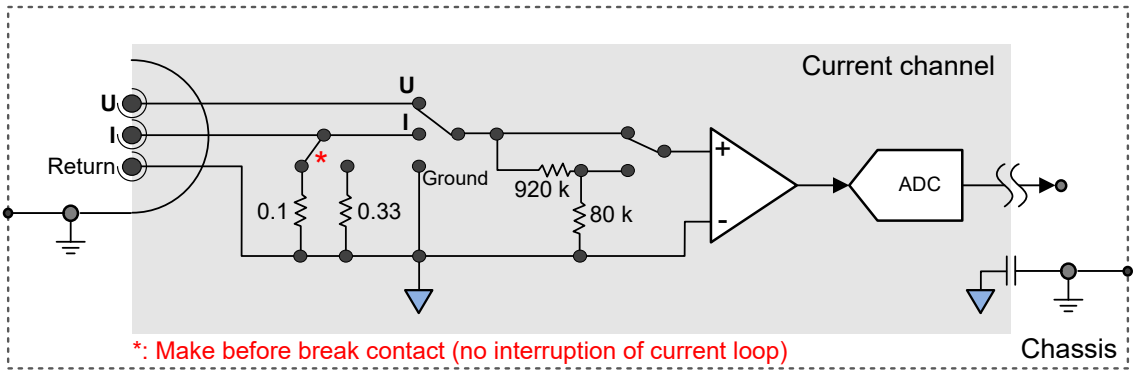


Figure 12.6: Single-ended isolated current channel

GN310B/GN311B Current Connector and Pinning	
GN310B/GN311B front panel connector	LEMO EPG.1B.304.HLN
Mating connector	LEMO FGG.1B.304.GLAD52 (Check cable collet selection details)*

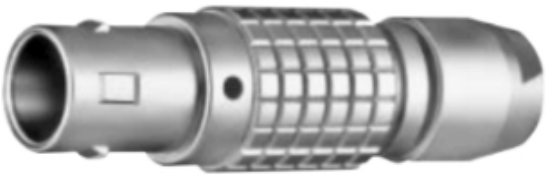


Figure 12.7: FGG.1B.304.GLAD52 mating LEMO connector

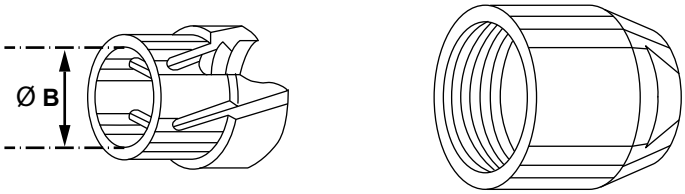


Figure 12.8: Cable colllet setup

* Cable collet selection:	Minimum cable diameter ØB	Maximum cable diameter ØB
M27	2.2 mm	2.7 mm
M31	2.7 mm	3.1 mm
D42	3.1 mm	4.2 mm
D52	4.2 mm	5.2 mm
D62	5.2 mm	6.2 mm
D72	6.2 mm	7.2 mm
D76	7.2 mm	7.6 mm

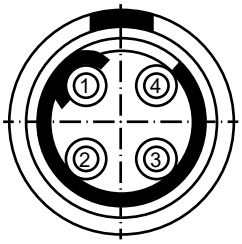


Figure 12.9: Cable connector soldering view

Signal name (Cable/Connector color)	**Pin number**
Current input (White/Blue)	1
Voltage input (Brown/Red)	2
Ground/shield (Yellow/Yellow)	3
Input return/Isolated ground (Green/Black)	4

GN310B/GN311B: Current Channel: Voltage mode and cabling

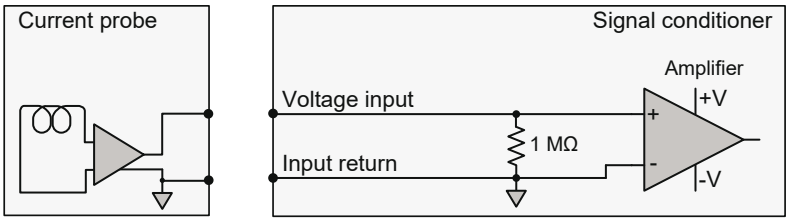


Figure 12.10: Current channel: Voltage mode block diagram (1-KAB2137-2)

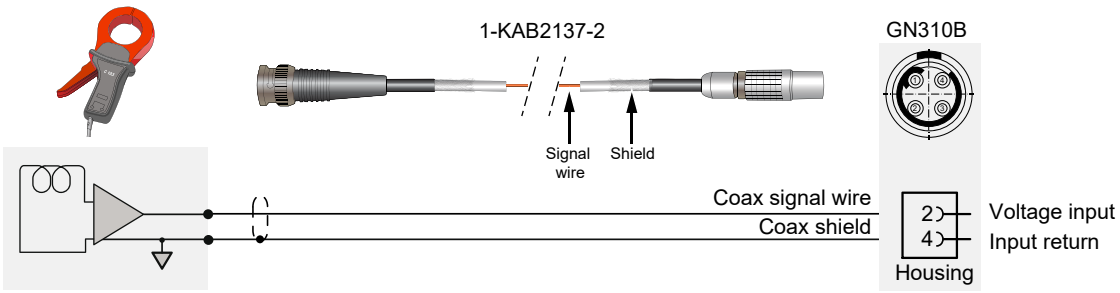


Figure 12.11: Recommended Voltage mode connection (1-KAB2137-2)

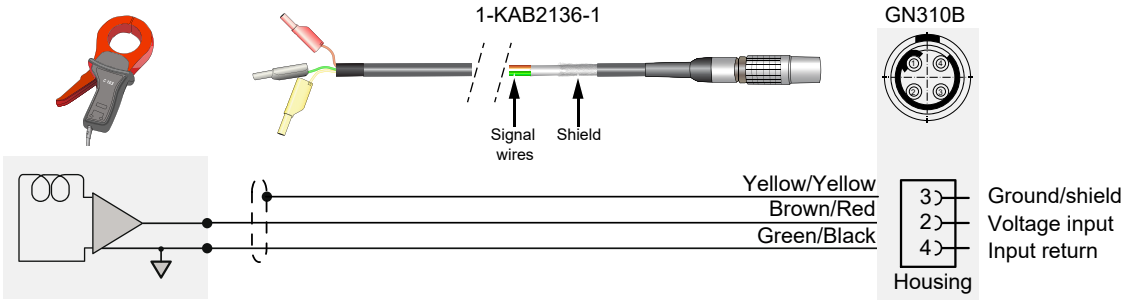


Figure 12.12: Alternative Voltage mode connection (1-KAB2136-1)

GN310B/GN311B: Current Channel: Current mode and cabling

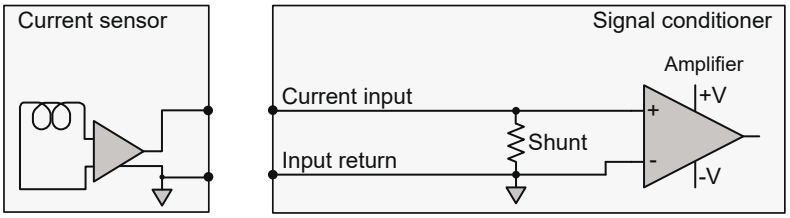


Figure 12.13: Current channel: Current mode block diagram (1-KAB2136-1)

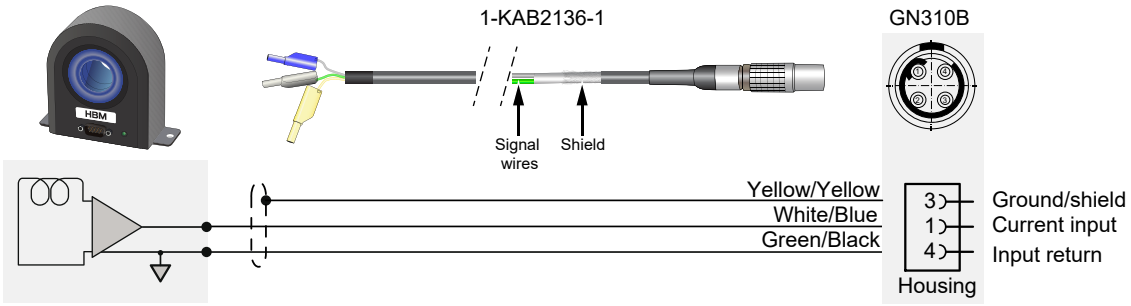


Figure 12.14: Recommended Current mode connection (1-KAB2136-1)

12.2.4 Connecting HBM current transducers

To connect HBM current transducers (1-CTSxxxID) and the interface unit (1-CTPSIU-6-1U) to the GN310B/GN311B card you need the following cables.

- 1-KAB2134-2 GN31XB-CTPSIU 2M LEMO-XLR CURRENT cable
- 1-KAB2133-xx CURRENT TRANSDUCER POWER SUPPLY cable

Use these cables according the diagram below to connect all parts together.

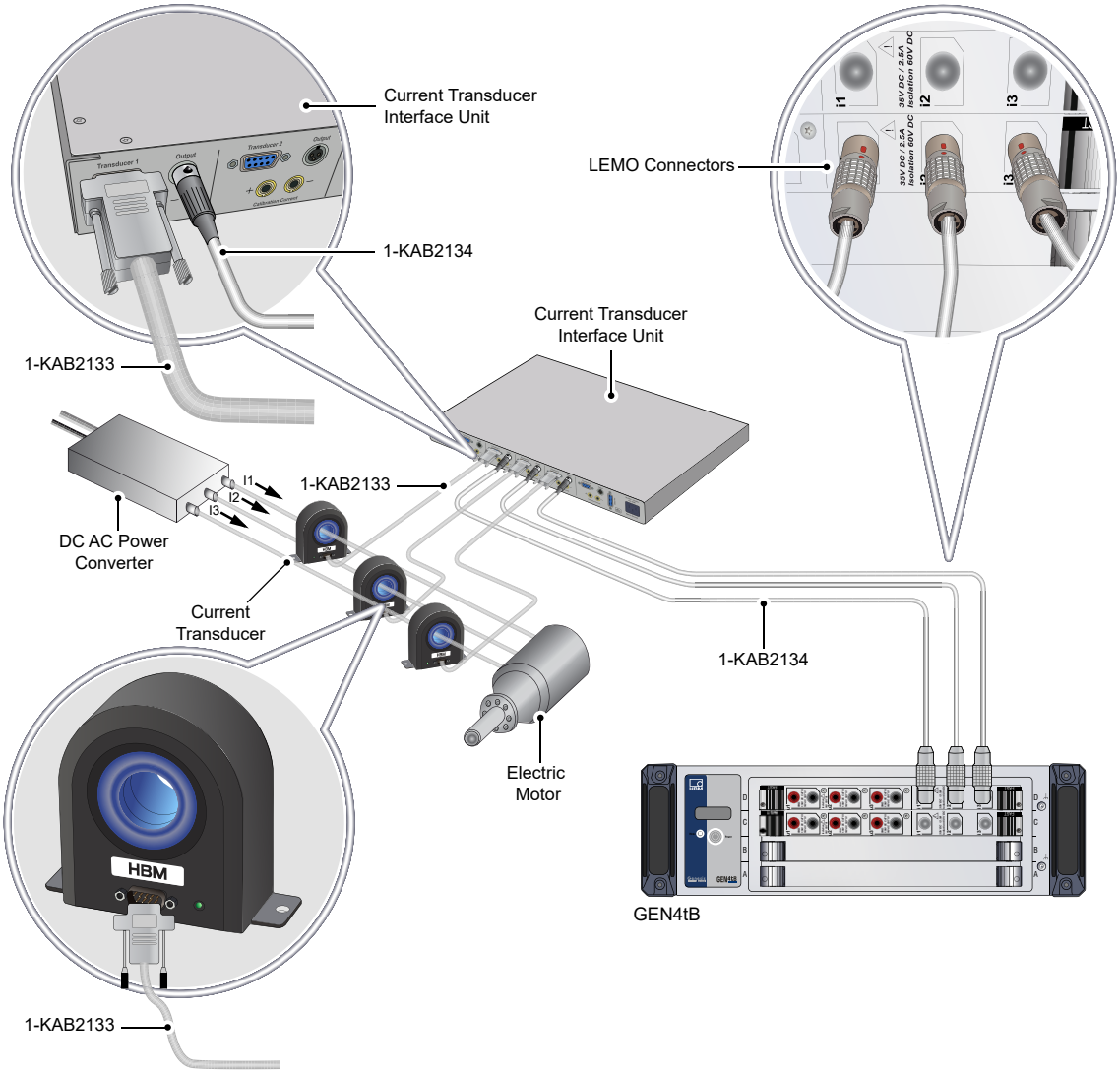


Figure 12.15: Current transducer connection diagram

All required accessories, can be found in the GN310/GN311B data sheets specifications.

12.2.5 Connecting LEM current transducers

To connect LEM current transducers and the interface unit to the GN310B/ GN311B card you need the following cables.

- 1-KAB2136-1 GN31XB 1M LEMO-BANANA VOLT&CURRENT cable
- 1-KAB2133-xx CURRENT TRANSDUCER POWER SUPPLY cable

Use these cable according the diagram below to connect all parts together.

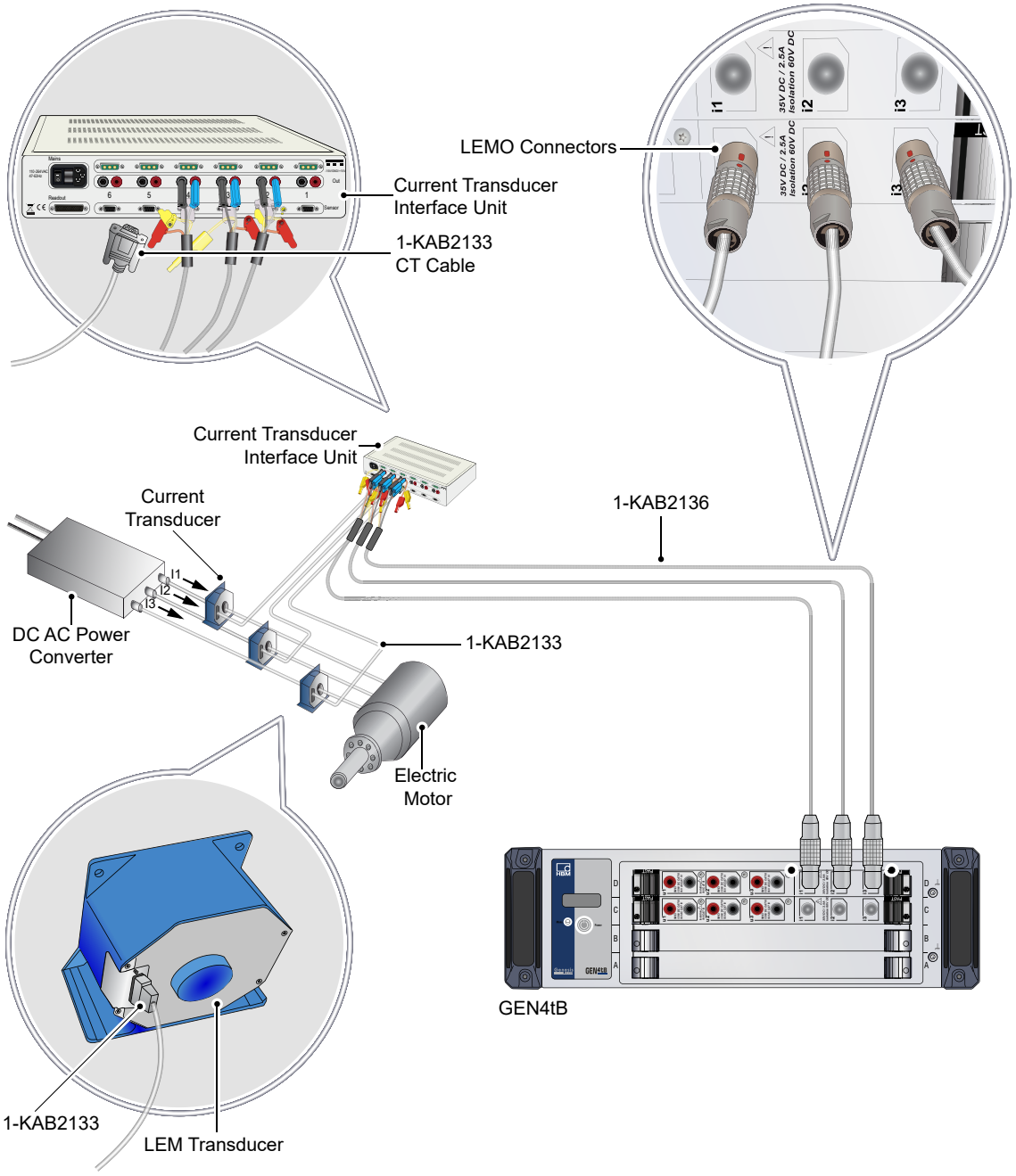


Figure 12.16: LEM current transducer connection diagram

12.2.6 Understanding the GN310B/GN311B category rating

Safety according to the harmonized standard

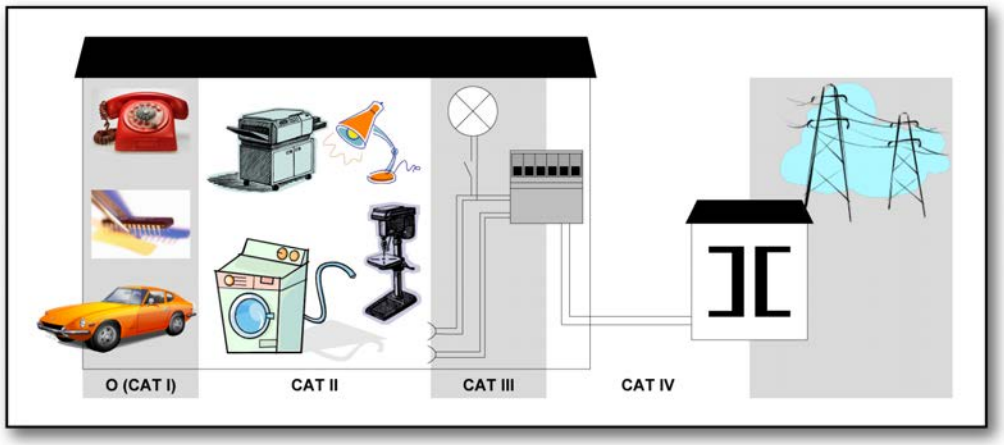


Figure 12.17: Category indication in accordance with IEC 61010-2-030:2010

Example: A measurement device is specified as 1000 V CAT IV, maximum input to chassis voltage 1000 V CAT III.

Table 12.1: Basic insulation test voltages in accordance with IEC 61010-2-030:2010

Nominal voltage [V RMS or V DC]	IEC 61010-2-030:2010 BASIC insulation		
	5 sec. AC test [V RMS]		
	CAT II	CAT III	CAT IV
≤ 150	1.350	1.390	2.210
> 150 ≤ 300	1.500	2.210	3.310
> 300 ≤ 600	2.210	3.310	4.260
> 600 ≤ 1 000	3.310	4.260	6.600

Table 12.2: Reinforced insulation test voltages in accordance with IEC 61010-2-030:2010

Nominal voltage line-to-neutral AC RMS or DC of $_{MAINS}$ being measured	IEC 61010-2-030:2010 Reinforced insulation		
	5 sec. AC test [V RMS]		
	CAT II	CAT III	CAT IV
≤ 150	2.700	2.210	3.510
> 150 ≤ 300	3.000	3.510	5.400
> 300 ≤ 600	3.510	5.400	7.400
> 600 ≤ 1 000	5.400	7.400	11.940

Using the tables “Basic/Reinforced insulation test voltages in accordance with IEC 61010-2-030:2010”, it can be concluded that this specification informs the user that a high voltage input within the device has passed the insulation test; 5 sec at 6600 V RMS for the rating of 1000 V CAT IV basic insulation.

For a voltage channel, input to chassis has passed the isolation tests of 5 sec at 7400 V RMS for the rating of 1000 V CAT III reinforced insulation.
Tested up to 7400 V RMS for 5 s, the reinforced and double insulation allows for safe measurements up to 1000 V CAT III (without probes) from voltage channel to chassis.

12.2.7 Understanding the GN310B/GN311B high voltage input

The high voltage signal input channels of the GN310B/GN311B are of the balanced type. This means that both inputs within one channel pair are exactly the same. The only difference is an opposite polarity or sign. A (simplified) schematic representation of the input channel can be found below (see Figure 12.18).
The input channels are of the isolated type. This means that the input channel and amplifier are fully isolated from (earth) ground. Fully isolated in this context means a very high resistance and very small capacitive coupling to ground.

Characteristics per channel:

- The Resistance/Capacitance from each terminal to ground is identical.
- Both terminals have isolated connectors (i.e. isolated from system ground).
- The isolated ground is not externally accessible, as shown in Figure 12.18.

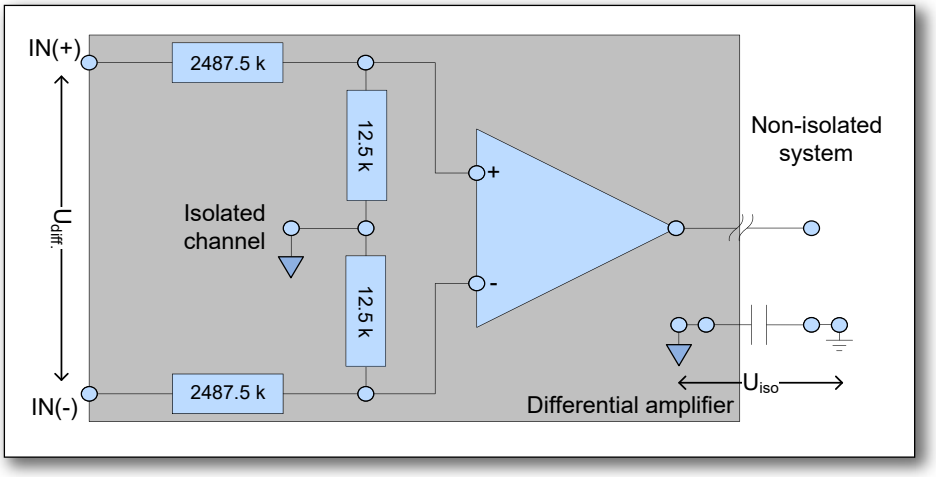


Figure 12.18: Isolated balanced input channel

(Not) using probes:
Using passive voltage probes together with balanced isolated inputs is very difficult and not recommended. The main reason for this is that there is no ground reference for the probe to divide the input voltage.

12.2.8 GN310B/GN311B Isolation Voltage channel

An overview of the GN310B/GN311B card isolation and input is shown in the figures below. The isolation within a voltage channel is qualified as 1500 V DC and 1000 V CAT IV basic. The insulation of the voltage channel to chassis is qualified as 1000 V CAT III and 600 V CAT IV reinforced or double. If one voltage channel has its common mode at +1000 V and one at -1000 V (with respect to chassis), the voltage between the two channels is 2000 V. The standards at which the card is certified is IEC61010-1:2010 and IEC61010-2-030:2010.

Voltage Channels Isolation IEC 61010-2-030:2010

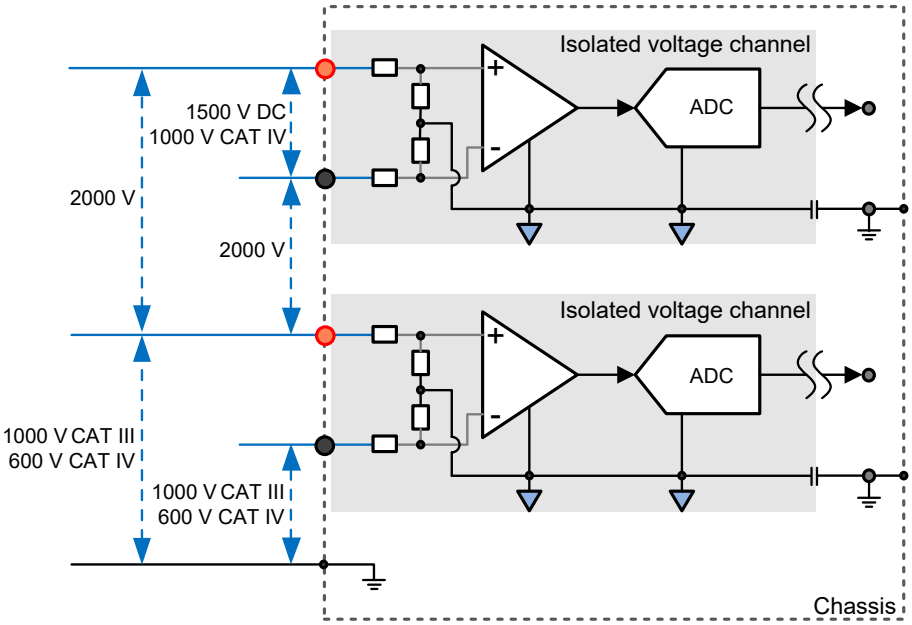


Figure 12.19: Voltage channels isolation ratings

Positive input pin to negative input pin	1500 V DC, 1000 V CAT IV
Input pin to chassis	1000 V CAT III, 600 V CAT IV
Channel to channel	2000 V RMS

Note *Each of the specifications have to be met. The most stringent specification applies in each situation.*

- The insulation between the voltage channel and chassis is classified as **REINFORCED** or **DOUBLE**. This can be seen as double insulation, which is necessary because the chassis might be accessible (conductive parts can be touched) to users (personal safety).

- Insulation within a voltage channel is **BASIC**, since a channel is not accessible. Therefore, there is no direct risk to users (product safety).
- **REINFORCED** or **SUPPLEMENTARY** insulation has higher test voltages than **BASIC** insulation.

Voltage Channel - Maximum voltage overview
In the following figures is shown which voltage can be applied, based on the environment where the product is installed in. CAT II or CAT III rating (see Figure 12.20); CAT IV rating (see Figure 12.21).

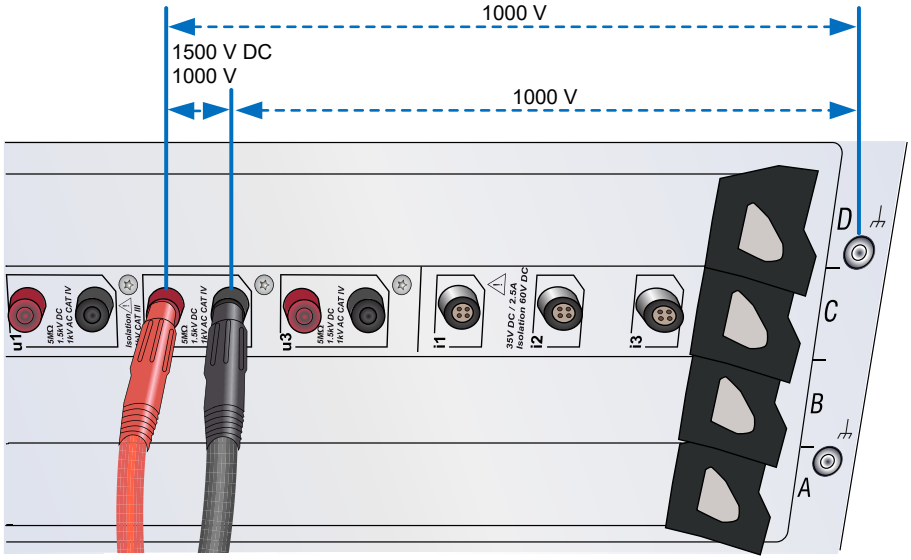


Figure 12.20: Environment without CAT rating

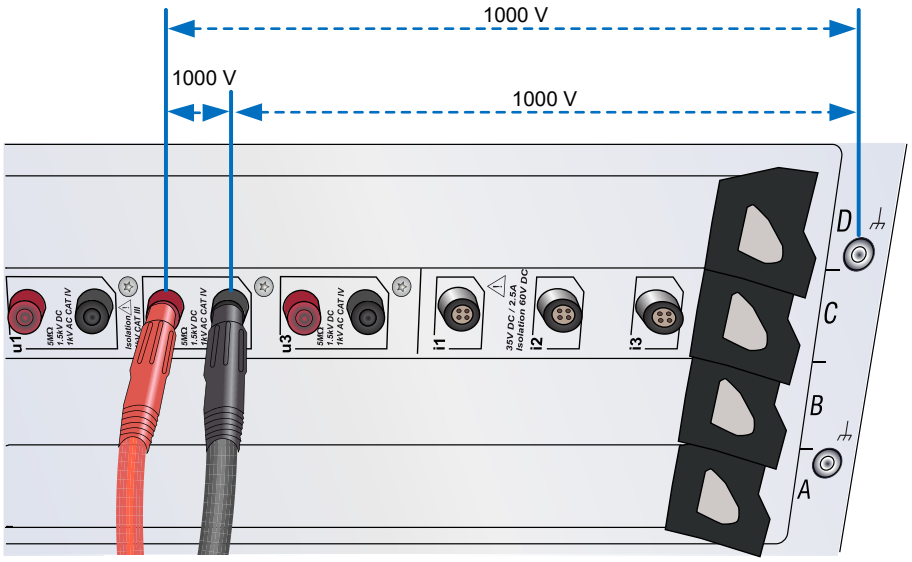


Figure 12.21: Environment with CAT II and CAT III

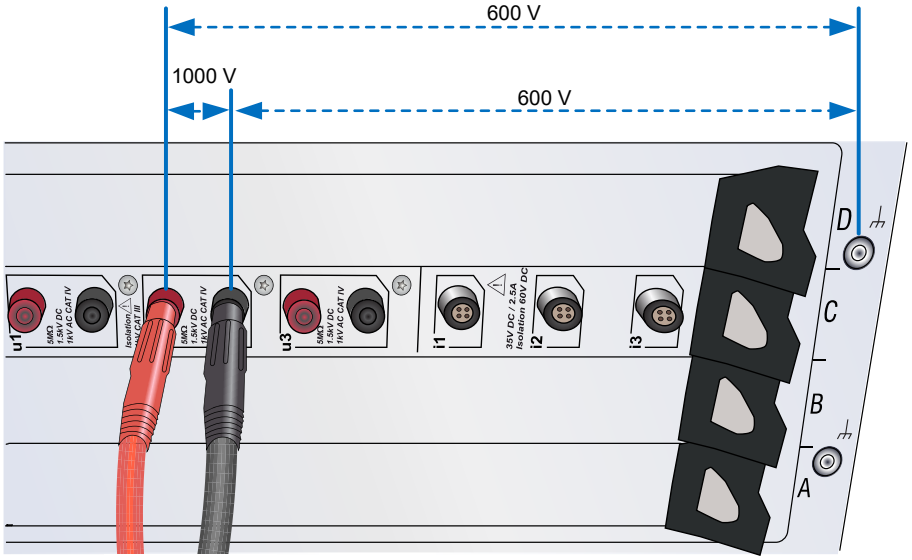


Figure 12.22: Environment with CAT IV

Voltage Channel - Safe and unsafe connections

In the following figures is shown how a GN310B/GN311B power card has to be connected. Safe connection (see Figure 12.23), unsafe connections (see Figure 12.24 and Figure 12.25).

WARNING

Make sure the cable connectors are put COMPLETELY into the input of the GN310B/GN311B power card.

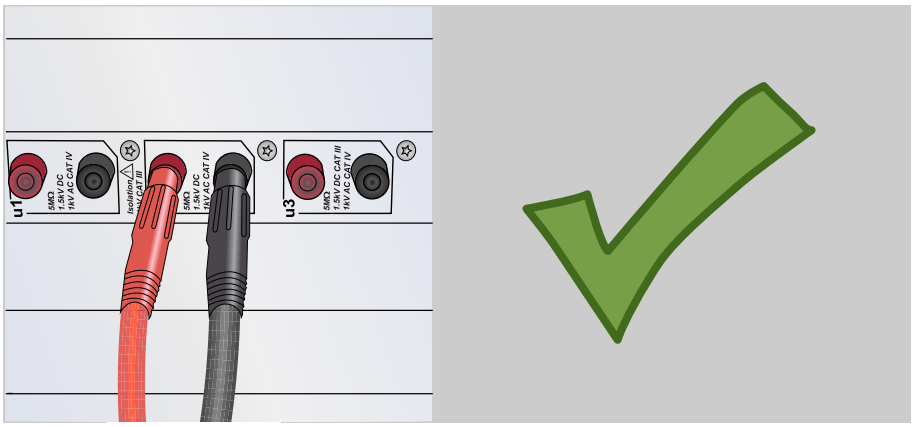


Figure 12.23: GN310B/GN311B Power card - safe connection

WARNING

Do not leave one of the connectors unconnected per differential pair.

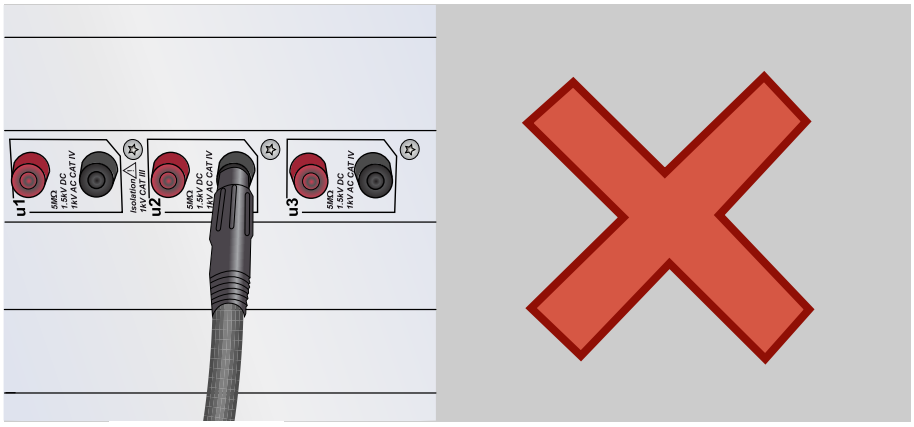


Figure 12.24: GN310B/GN311B Power card - unsafe connection (1)

WARNING

A differential pair can be recognized by the black box around it.

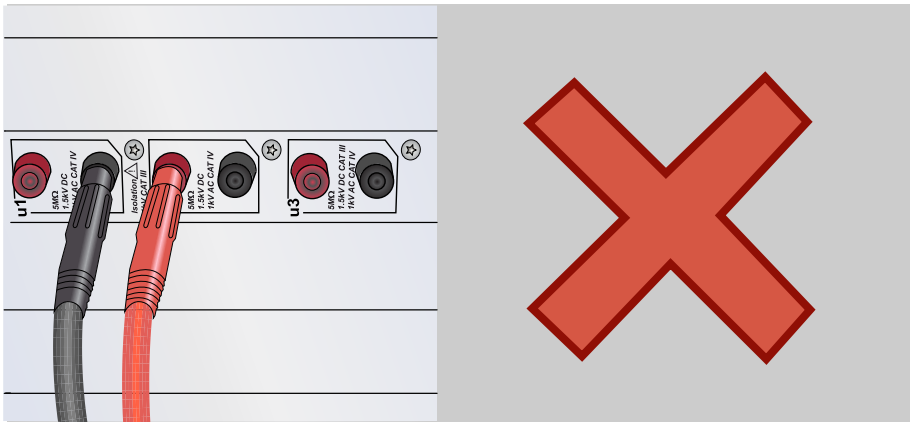


Figure 12.25: GN310B/GN311B Power card - unsafe connection (2)

12.2.9 GN310B/GN311B Isolation Current channel

The specified ± 20 V DC voltage range of the Current channel inputs in voltage mode is such that it falls below the low voltage limit as specified in IEC61010-1.

The isolation of the Current channel inputs is in line with the limit for safe voltage and currents as mentioned above.

Current Channels Isolation IEC 61010-2-030:2010

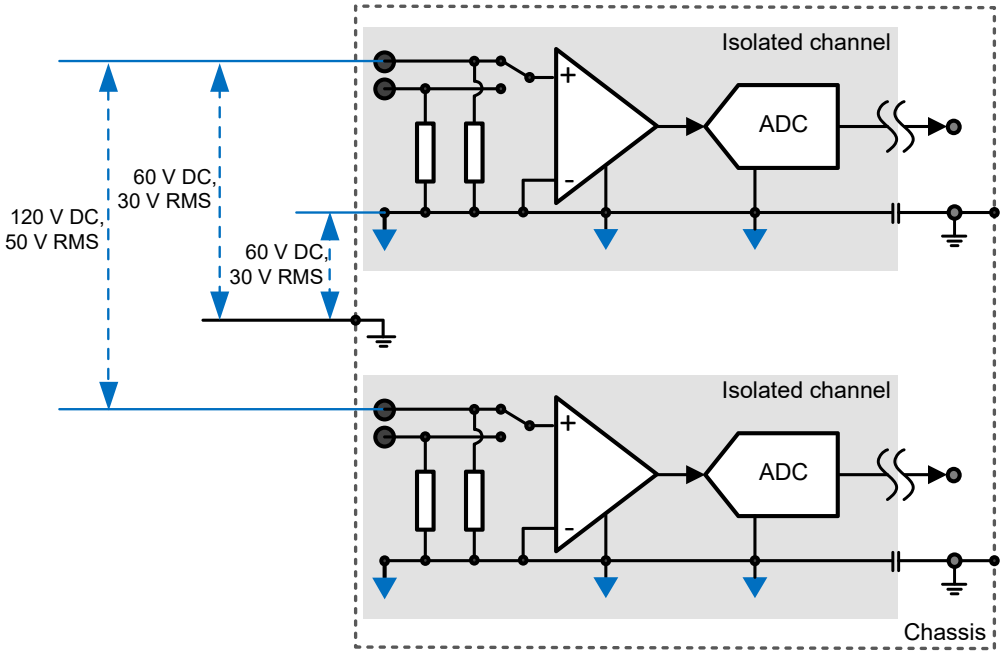


Figure 12.26: Current channels isolation ratings

Input pin to chassis	± 60 V DC, 30 V RMS
Channel to channel	120 V DC, 50 V RMS

The input channels of the GN310B and GN311B are isolated. This means that the input channel and amplifier are fully isolated from (earth) ground. In this context, fully isolated means a very high resistance and a very small capacitive coupling to ground. This is for safety and to avoid ground loops.

12.2.10 GN310B/GN311B type testing of the HV channels

Channel to chassis voltages (and test voltages)
To qualify the insulation as 1000 V CAT III and 600 V CAT IV, certain tests are performed on some cards during the engineering design qualification phase. These tests are known as type tests. These tests are described in the IEC61010-1:2010 and IEC61010-2-030:2010 standards. The principle of the tests is described below.

For the isolation barrier test, the AC test below (see Figure 12.27) is used. The test value meets the requirements for 1000 V CAT III and 600 V CAT IV. Tests are conducted for 5 s (testing electric strength of solid insulation) and 1 minute (long term stress of solid insulation). For details, please refer to IEC61010-1 and IEC 61010-2-030.

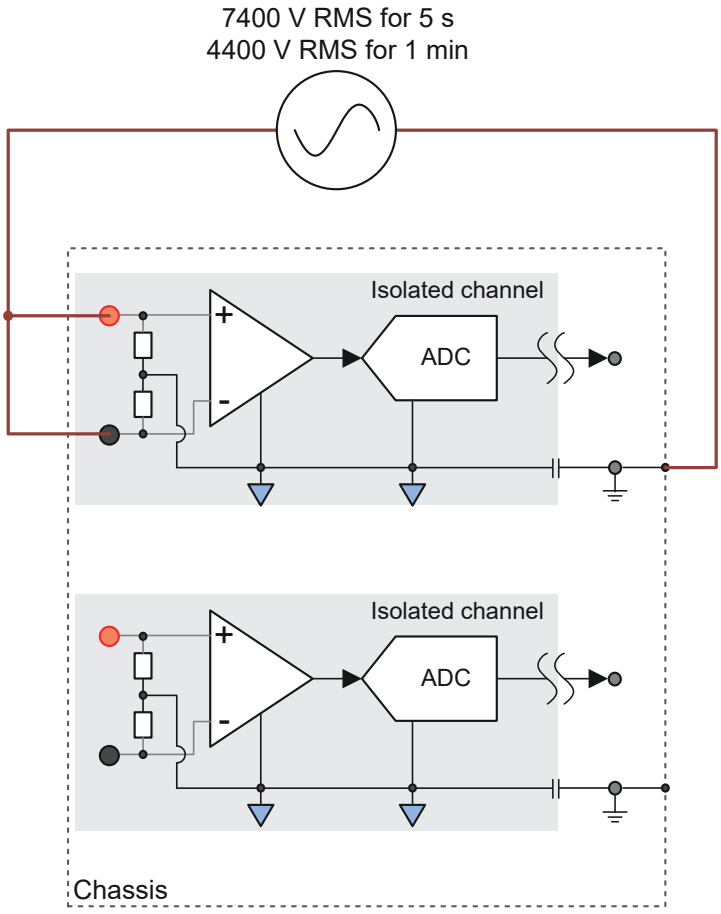


Figure 12.27: AC type test channel to chassis

Within high voltage channel isolation test (harmonized standard)
For the channel input test, the AC tests below (see Figure 12.28) is used. The test value meets the requirements for 1000 V CAT IV BASIC. Tests are conducted for 5 seconds and one minute. For details, please refer to IEC61010-2-030.

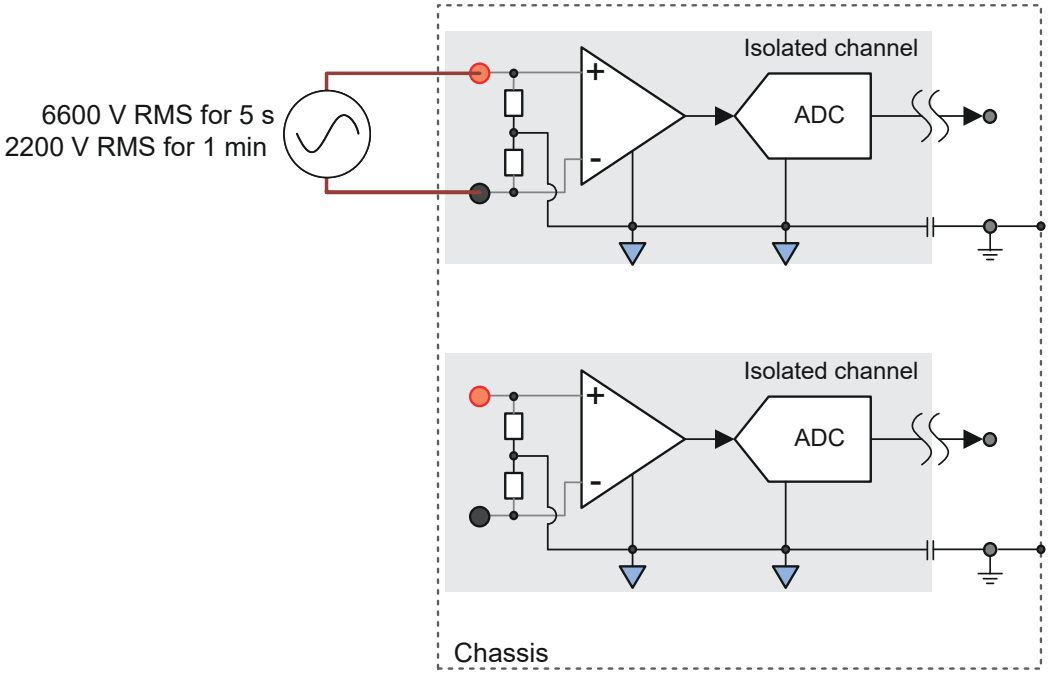


Figure 12.28: AC type test channel input (1000 V CAT IV) rating

High potential test

The type tests are performed on a selection of cards to test the design. Every card produced undergoes a production test to verify that the card has been produced correctly and that the card is safe. The tests are called “hipot” (high potential) tests (see Figure 12.29 and Figure 12.30).

The tests are performed in two steps to make sure that the channels that are side by side on the card can withstand the high potential voltages.

1 The inputs of Channel 1 and 3 are tested using a 4400 V RMS common mode signal with signal low attached to chassis ground and the inputs of Channel 2 connected to chassis ground.
2 The inputs of Channel 2 is tested using a 4400 V RMS common mode signal with signal low attached to chassis ground and the inputs of Channels 1 and 3 all connected to chassis ground.

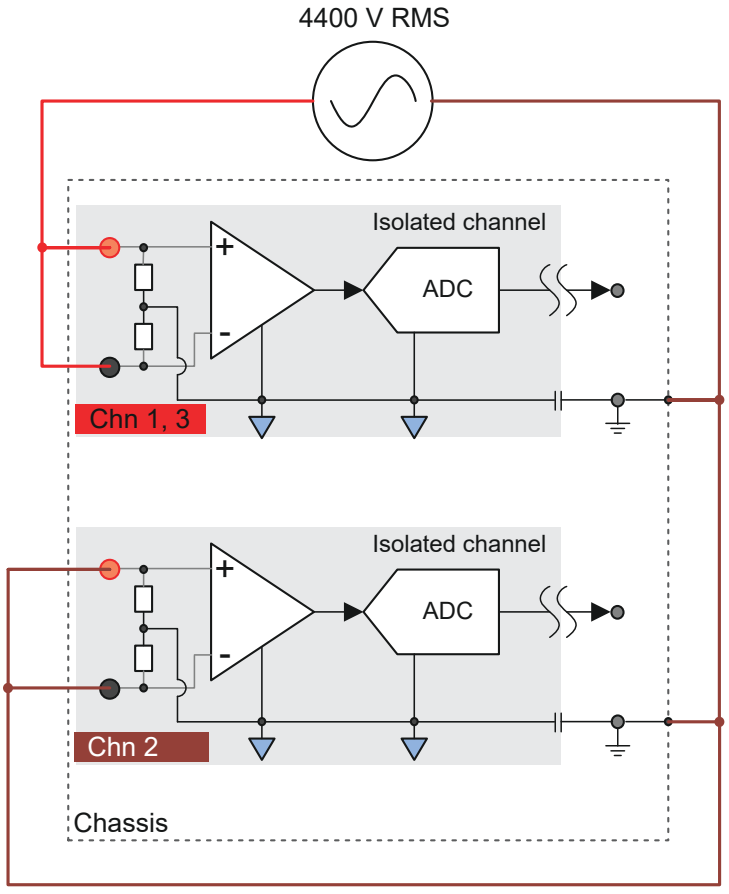


Figure 12.29: Hipot testing Channels 1 and 3

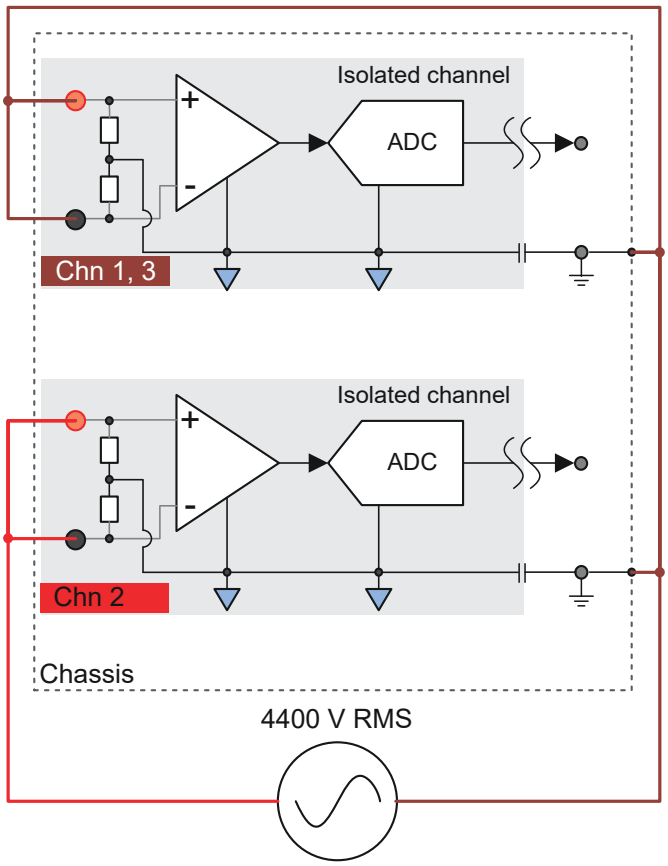


Figure 12.30: Hipot testing Channel 2

Engineering tests

Besides the type tests and the production tests, HBM has also performed several engineering tests to verify the robustness of the design during the engineering design qualification phase.

Component tests

Every component crossing the isolation barrier is tested and/or examined to make sure it will pass the type test. The test voltage used is the same high voltage DC that is used for the type tests, as well as an additional impulse voltage of up to ± 7000 V. The test impulse uses a 1.2 µs rise time and an amplitude reduction of 50% of the maximum peak voltage in 50 µs after the peak has been reached.

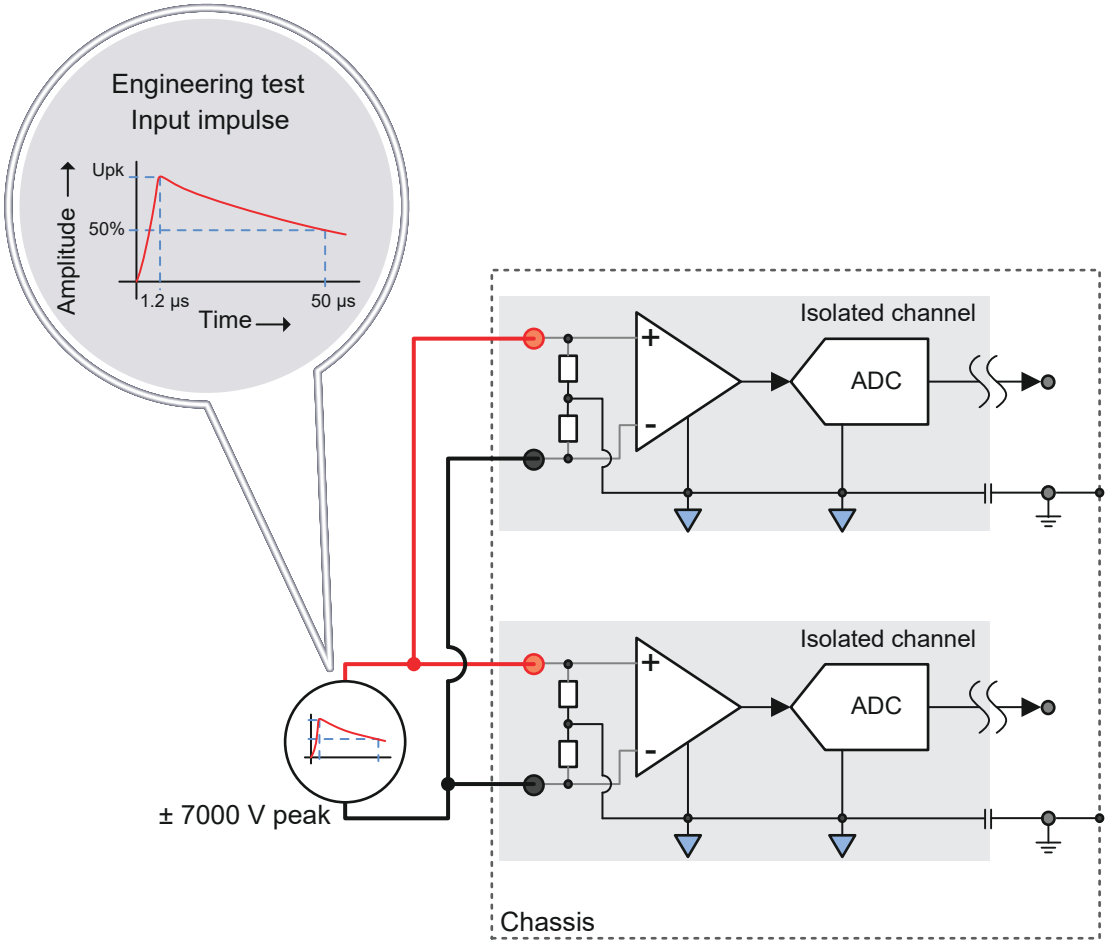


Figure 12.31: Example of 1.2/50 µs impulse

12.3 Isolated 1kV input cards

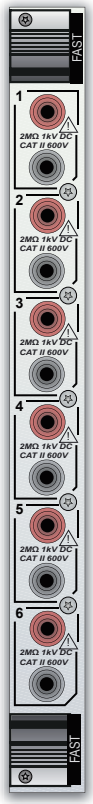
12.3.1 GN610B, Isolated 1kV 2MS/s input card with real-time formula database

- **6 analog channels**
- **Isolated, balanced differential inputs**
- **± 10 mV to ± 1000 V input range**
- **Basic accuracy 0.02%**
- **Basic power accuracy 0.02%**
- **600 V RMS CAT II reinforced insulation, tested up to 6.4 kV**
- **Analog/digital anti-alias filters**
- **18 bit at 2 MS/s sample rate**
- **Real-time formula database calculators**
- **Triggering on real-time results**
- **Digital Event/Timer/Counter support**
- **1 kV RMS CAT IV probe**
- **5 kV RMS certified probe**

The isolated balanced differential input offers voltage ranges from ± 10 mV to ± 1000 V.
Tested up to 6.4 kV, the reinforced insulation allows for safe measurements up to 600 V RMS CAT II (without probes).
Anti-alias protection is achieved by a unique, multi stage approach. The first stage combines a 7-pole analog anti-alias filter with the Analog-to-Digital converter to create an alias free digital data stream at constant rate of 2 MS/s.
The two Timer/Counters and the G070A torque/RPM adapter allow for direct interfacing to HBM torque transducers or other torque and speed sensors.
The real-time formula database calculators offer math routines to solve almost any real-time mathematical challenge. Dynamic digital cycle detection enables real-time storage as well as 1 µs latency digital output of calculation results like True-RMS on all analog, torque, angle, speed and Timer/Counter channels.
Channel to channel math creates computed channels with 1 µs latency obtaining mechanical power and/or multiphase (not limited to three) electric power (P, Q, S) or even efficiency calculations. Real-time calculated results can be used to trigger the recording or signal alarms to the external world.

For specification and ordering information, please refer to the GN610B data sheet.

12.3.2 GN611B, Isolated 1kV 200kS/s input card with real-time formula database



- **6 analog channels**
- **Isolated, balanced differential inputs**
- **± 10 mV to ± 1000 V input range**
- **Basic accuracy 0.02%**
- **Basic power accuracy 0.02%**
- **600 V RMS CAT II reinforced insulation, tested up to 6.4 kV**
- **Analog/digital anti-alias filters**
- **18 bit at 200 kS/s sample rate**
- **Real-time formula database calculators**
- **Triggering on real-time results**
- **Digital Event/Timer/Counter support**
- **1 kV RMS CAT IV probe**
- **5 kV RMS certified probe**

The isolated balanced differential input offers voltage ranges from ± 10 mV to ± 1000 V.
Tested up to 6.4 kV, the reinforced insulation allows for safe measurements up to 600 V RMS CAT II (without probes).
Anti-alias protection is achieved by a unique, multi stage approach. The first stage combines a 7-pole analog anti-alias filter with the Analog-to-Digital converter to create an alias free digital data stream at constant rate of 2 MS/s.
The two Timer/Counters and the G070A torque/RPM adapter allow for direct interfacing to HBM torque transducers or other torque and speed sensors.
The real-time formula database calculators offer math routines to solve almost any real-time mathematical challenge. Dynamic digital cycle detection enables real-time storage as well as 1 µs latency digital output of calculation results like True-RMS on all analog, torque, angle, speed and Timer/Counter channels.
Channel to channel math creates computed channels with 1 µs latency obtaining mechanical power and/or multiphase (not limited to three) electric power (P, Q, S) or even efficiency calculations. Real-time calculated results can be used to trigger the recording or signal alarms to the external world.

For specification and ordering information, please refer to the GN611B data sheet.

12.3.3 Using the GN610B/GN611B

WARNING

High bandwidth and measurement cabling

Due to the high bandwidth measurement capabilities of the acquisition card, combined with the high measurement sensitivity of the card, it is important to pay close attention to the measurement cabling.

Some advice to prevent measuring unwanted disturbances:

- Keep measurement cables as short as possible in order to reduce the reception of environmental disturbances.
- Use shielded cables. The cable should have the measurement cables paired inside a shield. Preferably, the shield should be connected to the chassis of the measurement Genesis High Speed equipment. Alternatively, the shield could also be connected to the chassis of the object under test.

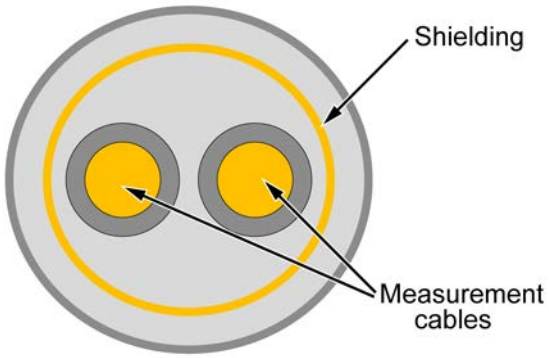


Figure 12.32: Shielded cable principles

HBM KAB290 cables are designed to meet this setup:

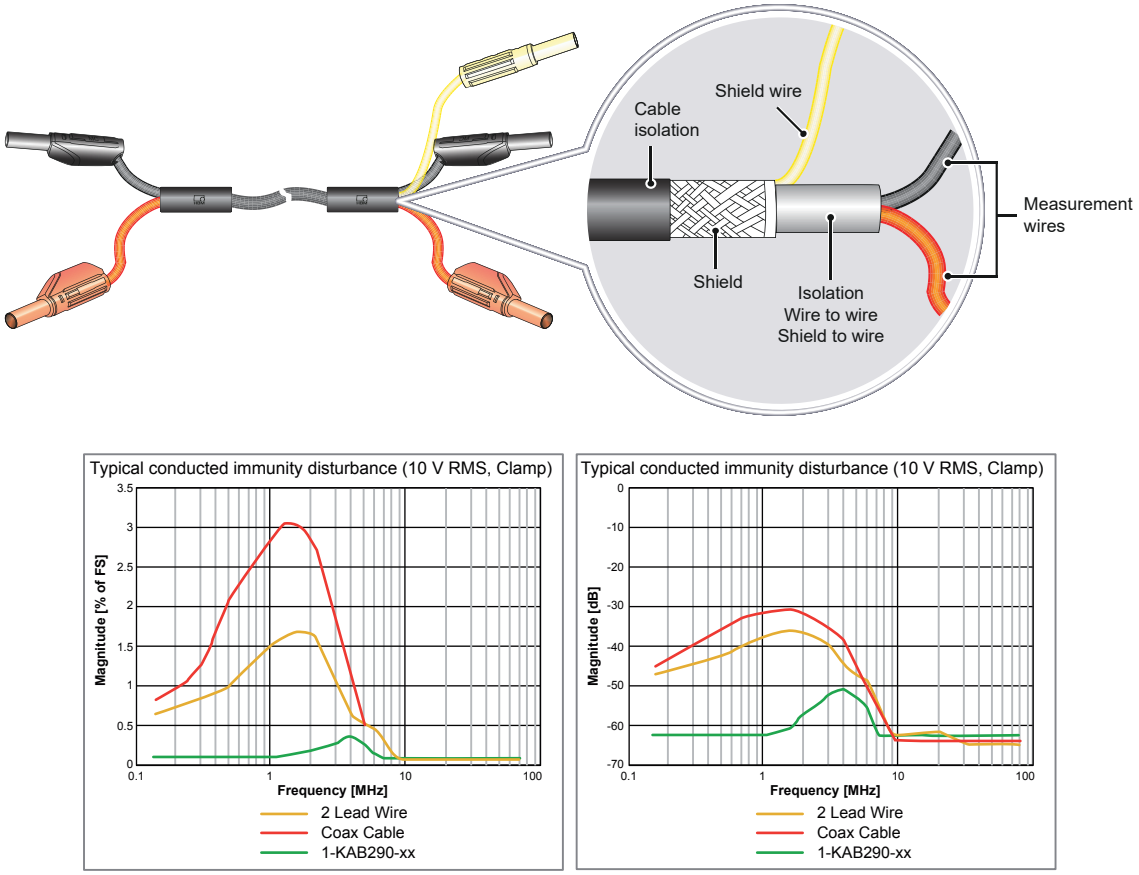


Figure 12.33: Shielded cable setup

More KAB290 details can be found in the GN610B/GN611B data sheet specifications.

- For high frequency disturbances where high bandwidth measurement is not required, the measurement bandwidth can be reduced by using the lowpass filter of the acquisition card.
- If unshielded cables are used, keep them as close together as possible, i.e. position them next to each other (to keep the loop small).
- Make sure that measurement cables that are used for measuring high dynamic or distorting signals are not closely positioned to measurement cables used for measuring small sensitive signals.
- Keep all measurement cables well separated from cables connected to high switching loads or motor cables.
- Separate measurement equipment and cables from potentially interfering equipment like frequency inverters or wireless equipment.

General cabling remark: Only use properly rated cables to measure the signal. Both the voltage and current rating should be matched to the signal for measurements.

WARNING

This instrument must be properly grounded.

When using this card, HBM advise using the standard GEN series protective ground connections to ensure that the entire unit is grounded.
Please see section "Connecting power" on page 64 for further details.

If connection to a protective ground is not possible for any reason, then please refer to the international safety standard EN 50191:2000

WARNING

Overvoltage and current protection

All signal inputs are protected against voltage overload. This is specified at ± 1000 V for all ranges except for the ± 1000 V range that is limited to ± 1250 V. Exceeding these limits, particularly when connected to potentially high-current sources, can cause severe damage that is not covered by the manufacturer's warranty.

WARNING

Disconnect voltages before removing the card from the system.

The measuring circuit can carry hazardous voltages and should be disconnected before the card is removed from the card slot of the measurement system.

WARNING

High voltage and qualified personnel

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that all cards with working voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience, as well as their knowledge of the relevant provisions, are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

WARNING

Connectors and cables

Do not use non-protected or non-shrouded connectors.
The following connectors are not safe to use with this card and must not be used (see Figure 12.34).

Figure 12.34: Unsafe connectors

The inputs on the 1kV card are compatible with the following connectors and cables (see Figure 12.35). All cables used with the 1kV card must support 1000 V DC (or 1000 V AC peak) and 600 V CAT II. All required cables and connectors can be found in the the GN610B/GN611B data sheet specifications.

Figure 12.35: Safe connectors

12.3.4 Understanding the GN610B/GN611B category rating

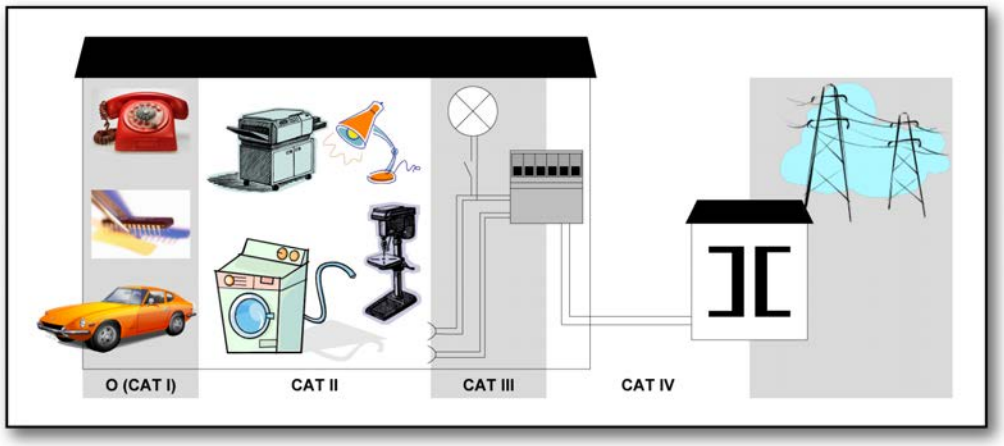


Figure 12.36: Category indication in accordance with IEC 61010-2-030:2010

Example: A measurement device is specified as 600 V CAT II, maximum input voltage 1000 V DC.

Table 12.3: Insulation test voltages in accordance with IEC 61010-2-030:2010

Nominal voltage (V RMS or V DC)	IEC 61010-2-030:2010					
	5 sec. AC test (V RMS)			Impulse test (V)		
	CAT II	CAT III	CAT IV	CAT II	CAT III	CAT IV
≤ 150	840	1.390	2.210	1.550	2.500	4.000
> 150 ≤ 300	1.390	2.210	3.310	2.500	4.000	6.000
> 300 ≤ 600	2.210	3.310	4.260	4.000	6.000	8.000
> 600 ≤ 1 000	3.310	4.260	6.600	6.000	8.000	12.000

Using the table above, it can be concluded that this specification informs the user that a voltage channel within the device has passed the insulation test; 5 sec at 5.4 k RMS. The maximum operating input voltage of the voltage channel is 1.5 kV DC. This voltage channel of the device is to be used to measure 1.5 kV_{DC} CAT III, 1 kV CAT IV basic.

12.3.5 Understanding the GN610B/GN611B input

The signal input channels of the GN610B/GN611B are of the balanced type. This means that both inputs within one channel pair are exactly the same. The only difference is an opposite polarity or sign. A (simplified) schematic representation of the input channel can be found below.
The input channels are of the isolated type. This means that the input channel and amplifier are fully isolated from (earth) ground. Fully isolated in this context means a very high resistance and very small capacitive coupling to ground.

Characteristics per channel:

- The Resistance/Capacitance from each terminal to ground is identical.
- Both terminals have isolated connectors (i.e. isolated from system ground).
- The isolated ground is not externally accessible, as shown in Figure 12.37.

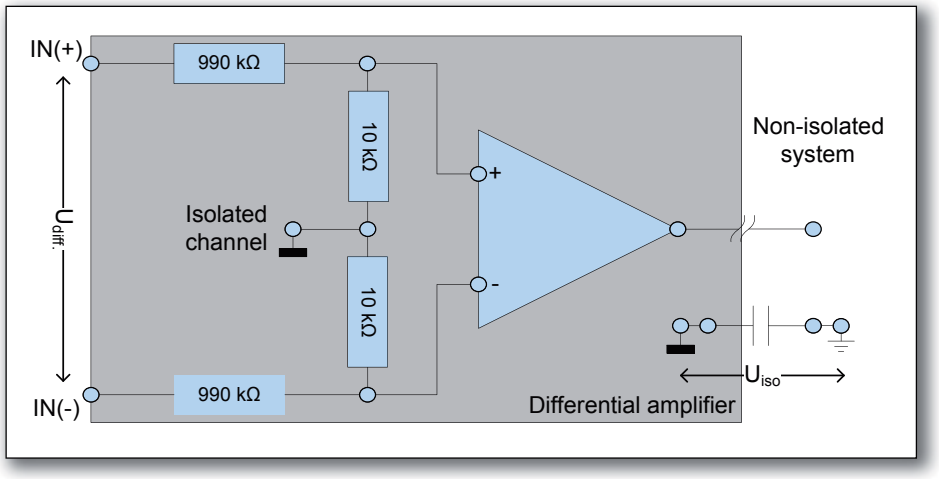


Figure 12.37: Isolated balanced input channel

(Not) using probes:
Using passive voltage probes together with balanced isolated inputs is very difficult and not recommended. The main reason for this is that there is no ground reference for the probe to divide the input voltage.

Looking at Figure 12.37, the GN610B/GN611B specifies U IN(+), U IN(-) and | Uiso| ≤ 1 kV. Using a standard passive 10:1 probe, combined with the GN610B/GN611B results in the situation shown in Figure 12.38.

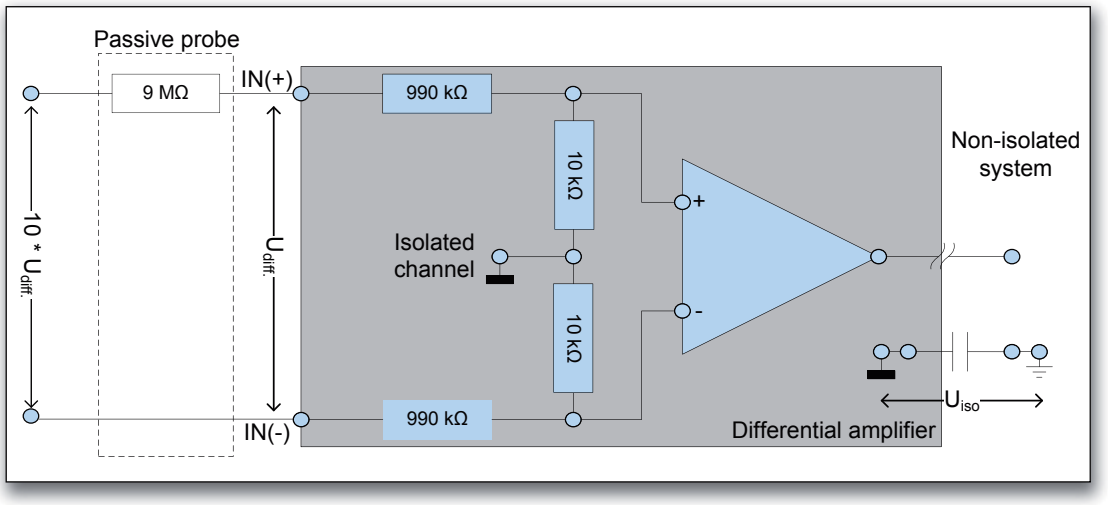


Figure 12.38: Isolated balanced input channel with passive probe

Example1:

In this setup, U IN(-) is not divided, so it is required that |U IN(-)| ≤ 1 kV. Assuming that U IN(-) is connected to 0 V, the voltages at U_{iso} and U IN(+) can be calculated:

Assuming:	U IN(-) = 0V 10:1 probe used, probe input voltage applied is 10* U_{diff}
Results in:	U IN(+) = 10 * U_{diff} / 11M * 2M = 1.82 * U_{diff} U_{iso} = 10 * U_{diff}/ 11M * 1M = 0.91 * U_{diff}

Due to the 2 MΩ impedance between U IN(+) and U IN(-), the probe does not divide by 10, but by 5.5 (10 / 1.82). So if the maximum specified U_{diff} of 1 kV is considered, this smaller division factor results in the U IN(+) level being way above the channels specification.

Example2:

Since U IN(-) is not divided, there are very strict consideration on how signals can be attached. Assume the U IN(+) and U IN(-) are reversed by accident. We can calculate U_{iso} and U IN(-).

Assuming:	U IN(-) = 10 * U_{diff} U IN(+) = 0 V
Results in:	U_{iso} = 10 * U_{diff} / 11M * 10M = 9.1 * U_{diff}

If the maximum specified U_{diff} of 1 kV is considered, both U IN(-) and U_{iso} are way above the channels specification.

12.3.6 Using the High Precision Differential Probe

Figure 12.39: High Precision Differential Probe (HDP)

The High Precision Differential Probe is designed to reduce the resistive/current load on the device under test by increasing the input impedance to 10 MΩ with 0.2% inaccuracy. The use of the 10:1 divider reduces the lowest user range to ± 0.1 V. The highest input range is ± 1000 V due to the maximum voltage rating of the probe.

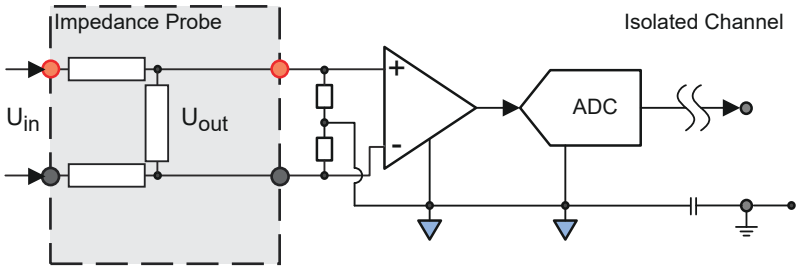


Figure 12.40: High Precision Differential Probe concept

Different to standard probes the HDP uses a balanced input divider, that matches both the resistive and capacitive characteristics of the GN610B/ GN611B acquisition cards. Therefore users do not need to perform probe compensations before using this probe.

Standard this probe uses a divide by 10 input stage. Either use the Perception Sensor Database to apply the correct probe or use a technical unit multiplier 10 to scale the channels input sensitivity to match the attached probe.

IMPORTANT

Although the HDP probe uses a divide by 10 factor, the highest available input range is not scaled by a factor of 10. The HDP is not specified to be used above 1000 V RMS. So both highest input range and maximum isolation voltages are unchanged when using the HDP probe together with the GN610B/GN611B acquisition cards.

To increase the maximum input range of the GN610B/GN611B input card a similar HDP probe concept can be used. However as the channels are NOT connected to earth the isolation specification of 1000 V RMS will not be increased by such a probe design. Extra care must be taken to prevent over voltages on the input pins of the GN610B/GN611B acquisition cards.

It is recommended to use the following approach:

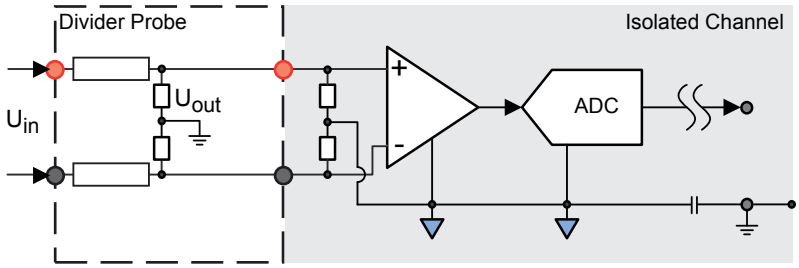


Figure 12.41: Differential Probe concept with common mode divider

In this setup the output of the probe is dividing the input U_{in} to earth on both inputs.

WARNING

Make sure when using such a probe the U+ and U- of the GN610B/GN611B channel never exceeds the specification of 1000 V DC.

IMPORTANT

This probe concept increases the input voltage levels while maintaining the protection of the GN610B/GN611B acquisition cards. Care must be taken that the full isolated measurement is lost as the probe is attached to earth. It's recommended to use high impedance series resistors to keep both the current load on the device under test low as well as any potential ground loop currents low.

12.3.7 Measuring currents

Note *The GN610B/GN611B acquisition cards do not support direct current measurements. The use of current shunts, current clamps and/or current transducers is required to measure currents.*

A typical setup using a **HBM Current Transducer** could look like this:

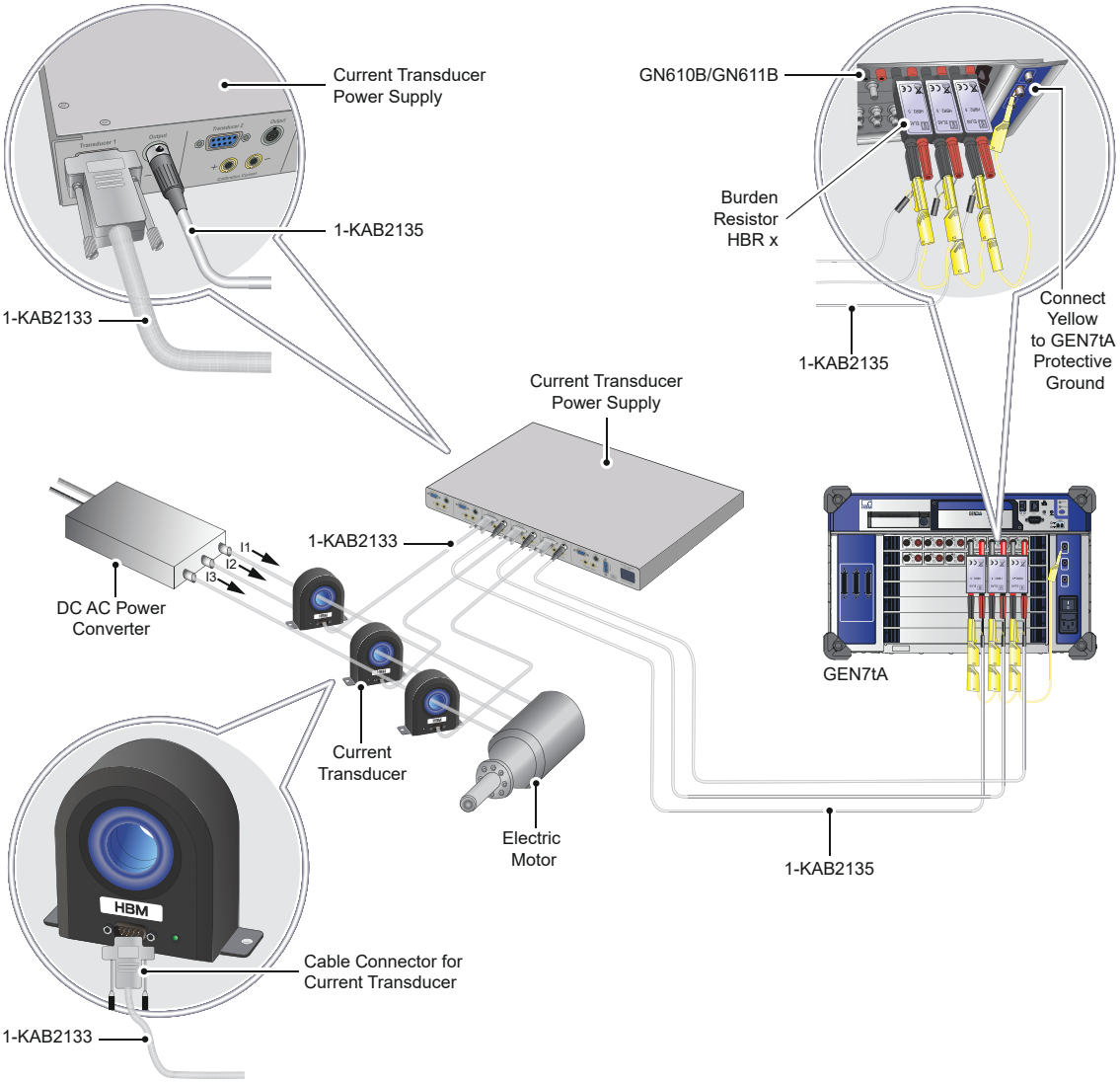


Figure 12.42: Current transducer connection diagram

A typical setup using a **LEM Current Transducer** could look like this:

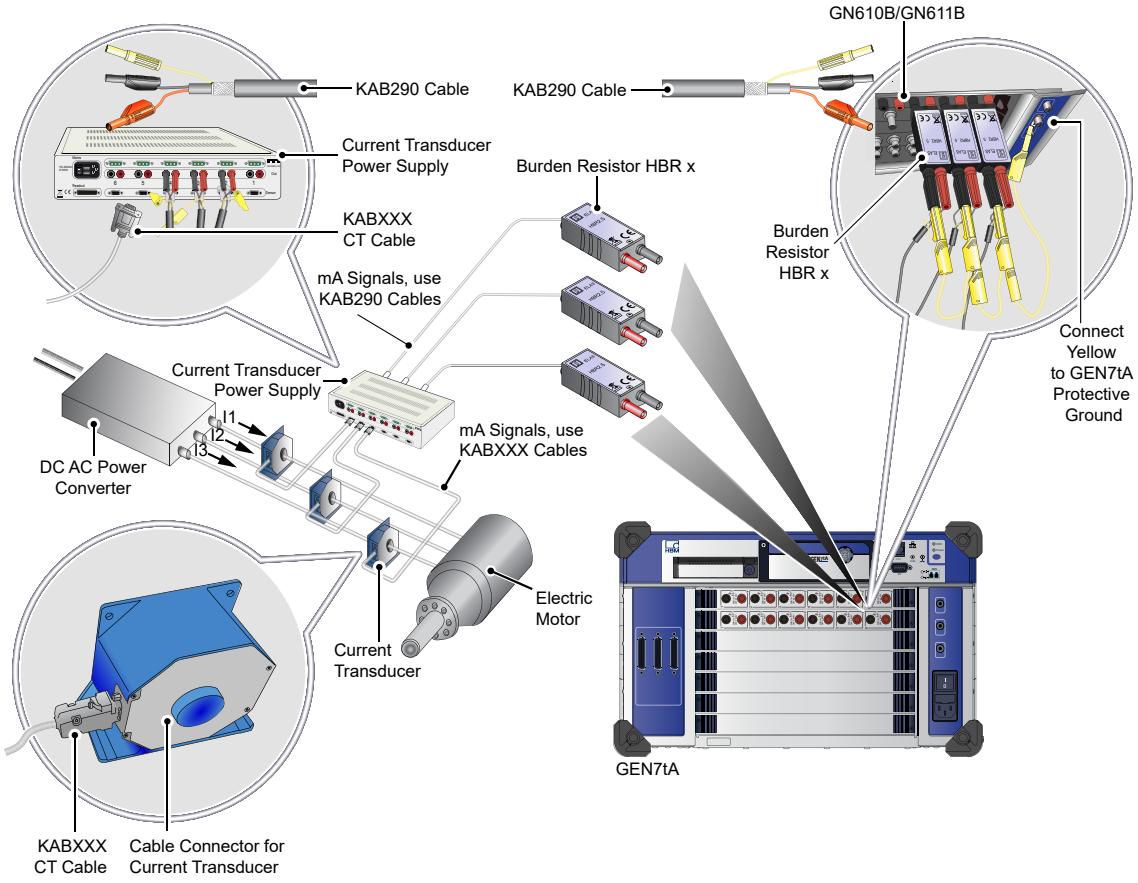


Figure 12.43: Current transducer connection diagram

All required accessories, can be found in the GN610/GN611B data sheets.

12.3.8 GN610B/GN611B Isolation and type testing

An overview of the GN610B/GN611B card isolation and input is shown below (see Figure 12.44). The isolation of the channel to chassis is 1000 V RMS and is also qualified as 600 V CAT II (or 300 V CAT III). The common mode of the differential input channel (isolated GND) can be 1000 V RMS with respect to the chassis. If one channel has its common mode at +1000 V and one at -1000 V (with respect to chassis), the voltage between the two channels is 2000 V. The standards at which the card is certified is IEC61010-1:2010 and IEC61010-2-030:2010.

Isolation	
Input signal to chassis	1000 V RMS, 600 V CAT II (REINFORCED)
Channel to chassis	1000 V RMS, 600 V CAT II (REINFORCED)
Channel to channel	2000 V RMS, (BASIC)

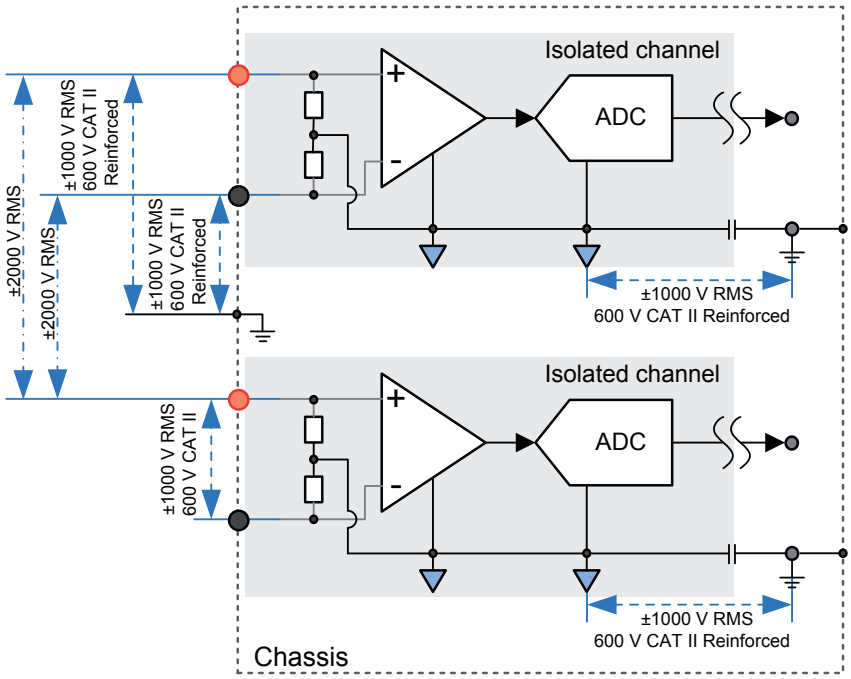


Figure 12.44: Isolation 1kV card overview

- The isolation between the channel and chassis is classified as **REINFORCED**. This can be seen as double isolation, which is necessary because the chassis might be accessible (conductive parts can be touched) to users (personal safety).
- Isolation between channels is **BASIC**, since a channel is not accessible. Therefore, there is no direct risk to users (product safety).
- **REINFORCED** or **DOUBLE** insulation has higher test values than **BASIC** insulation.

Channel to chassis isolation test

To qualify the isolation as 1000 V RMS and 600 V CAT II (REINFORCED), certain tests are performed on some cards during the engineering design qualification phase. These tests are known as type tests. These tests are described in the IEC61010-1:2010 and IEC61010-2-030:2010 standards. The principle of the tests is described below.

For the isolation barrier test, both the DC and AC tests below (see Figure 12.45 and Figure 12.46) are used with DC voltage √2 higher than the AC voltage. The test value meets the requirements for 600 V CAT II REINFORCED. The test value for 1000 V RMS is lower and therefore also covered by this test. Tests are conducted for one minute. For details, please refer to IEC61010.

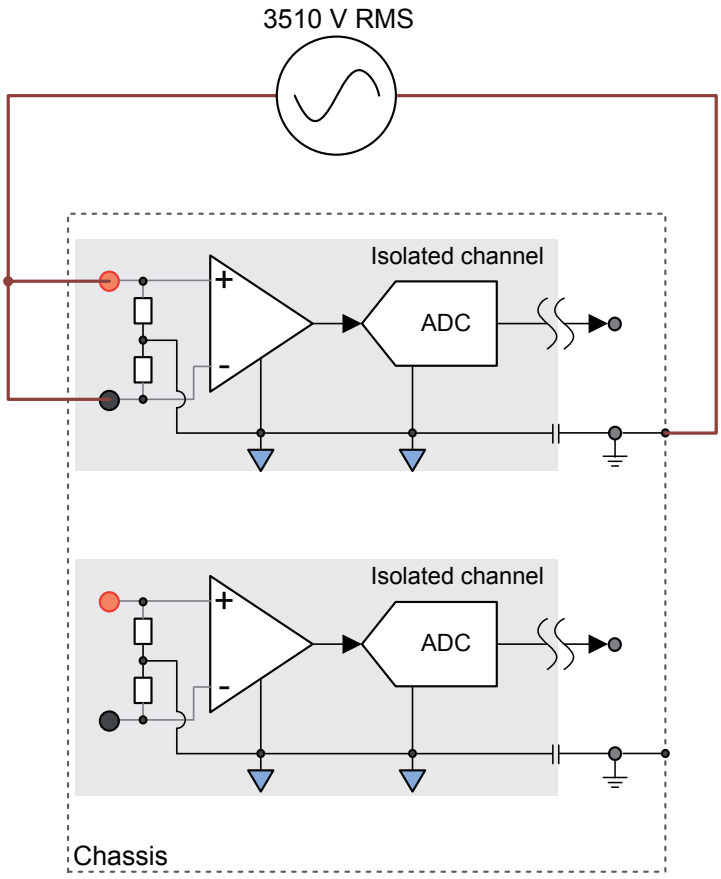


Figure 12.45: AC type test channel to chassis

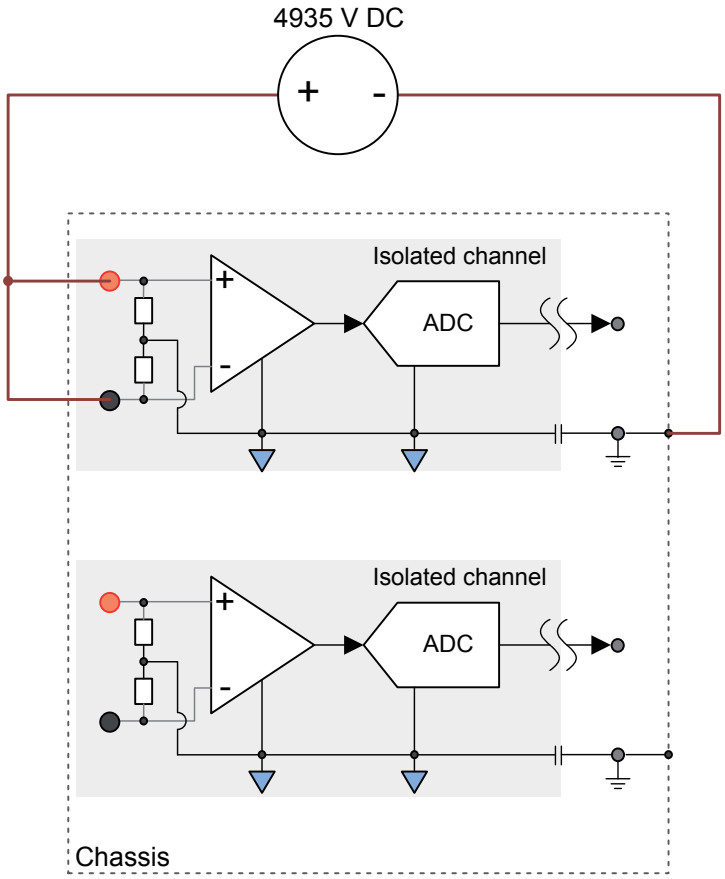


Figure 12.46: DC type test channel to chassis

Channel to channel isolation test

For the channel to channel test, both the DC and AC tests below (see Figure 12.47 and Figure 12.48) are used with DC voltage √2 higher than the AC voltage. The test value meets the requirements for 600 V CAT II REINFORCED. The value for 2000 V RMS BASIC is lower and therefore also covered by this test. Tests are conducted for one minute. For details, please refer to IEC61010-1.

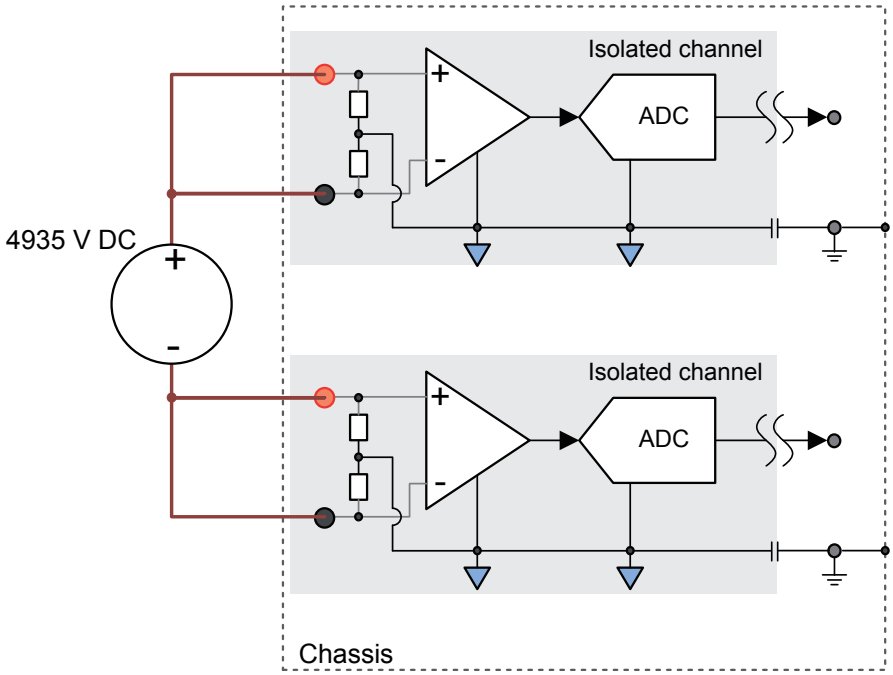


Figure 12.47: DC type test channel to channel

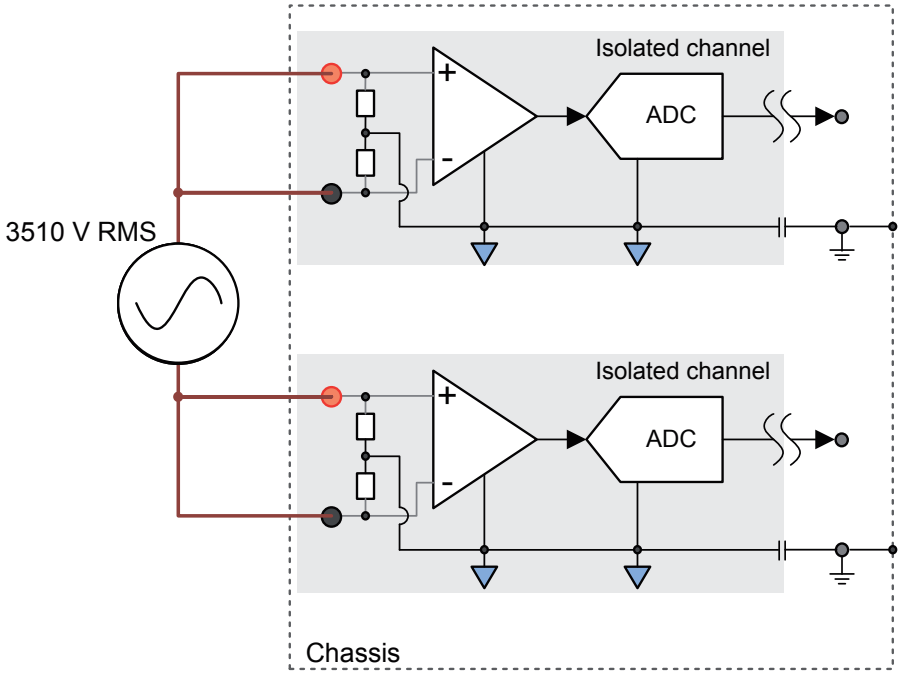


Figure 12.48: AC type test channel to channel

High potential test

The type tests are performed on a selection of cards to test the design. Every card produced undergoes a production test to verify that the card has been designed correctly and that the card is safe. The tests are called “hipot” (high potential) tests (see Figure 12.49 and Figure 12.50).

The tests are performed in two steps to make sure that the channels that are side by side on the card can withstand the high potential voltages.

1 The inputs of Channel 1, 3 and 5 are tested using a 1500 V RMS common mode signal with signal negative attached to chassis ground and the inputs of Channel 2, 4 and 6 all connected to chassis ground.
2 The inputs of Channel 2, 4 and 6 are tested using a 1500 V RMS common mode signal with signal negative attached to chassis ground and the inputs of Channels 1, 3 and 5 all connected to chassis ground.

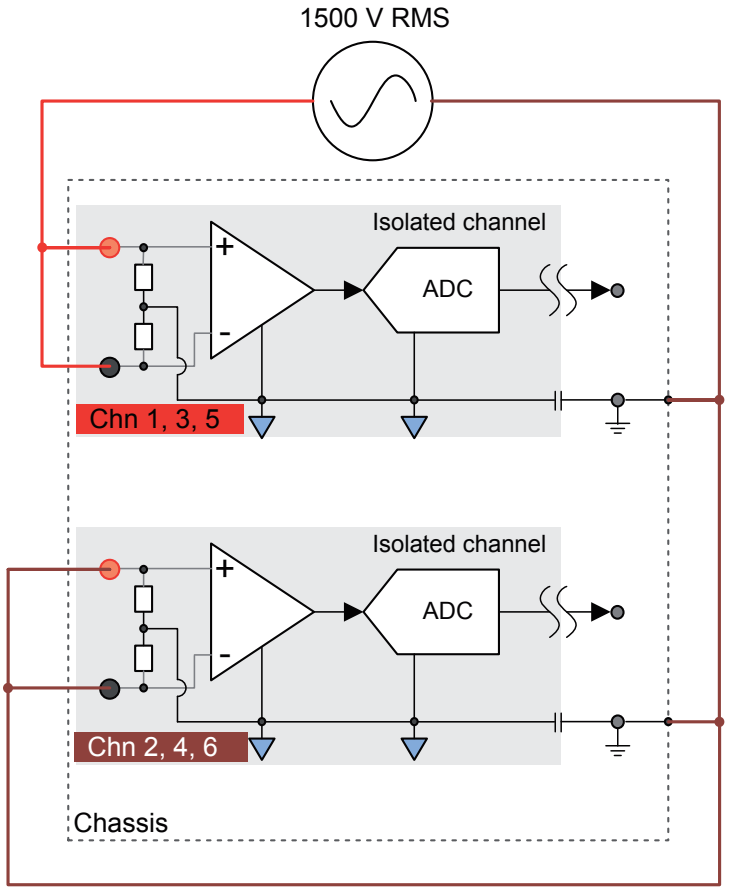


Figure 12.49: Hipot testing Channels 1, 3 and 5

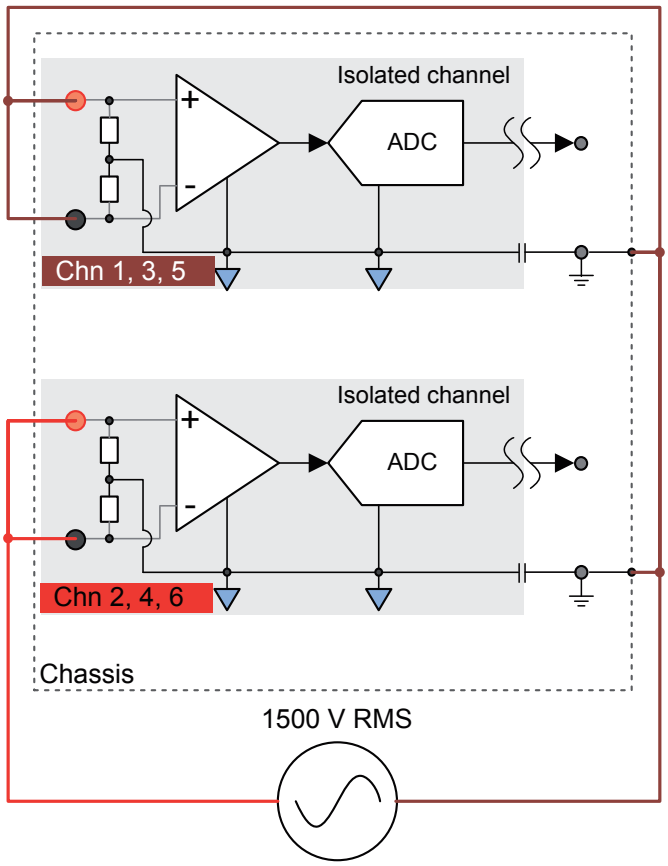


Figure 12.50: Hipot testing Channels 2, 4 and 6

Engineering tests
Besides the type tests and the production tests, HBM has also performed several engineering tests to verify the robustness of the design during the engineering design qualification phase.

Component tests
Every component crossing the isolation barrier is tested and/or examined to make sure it will pass the type test. The test voltage used is the same high voltage DC that is used for the type tests, as well as an additional impulse voltage of up to 6 kV. The test voltage uses a 1.2 µs rise time and an amplitude reduction of 50% of the maximum peak voltage in 50 µs after the peak has been reached.

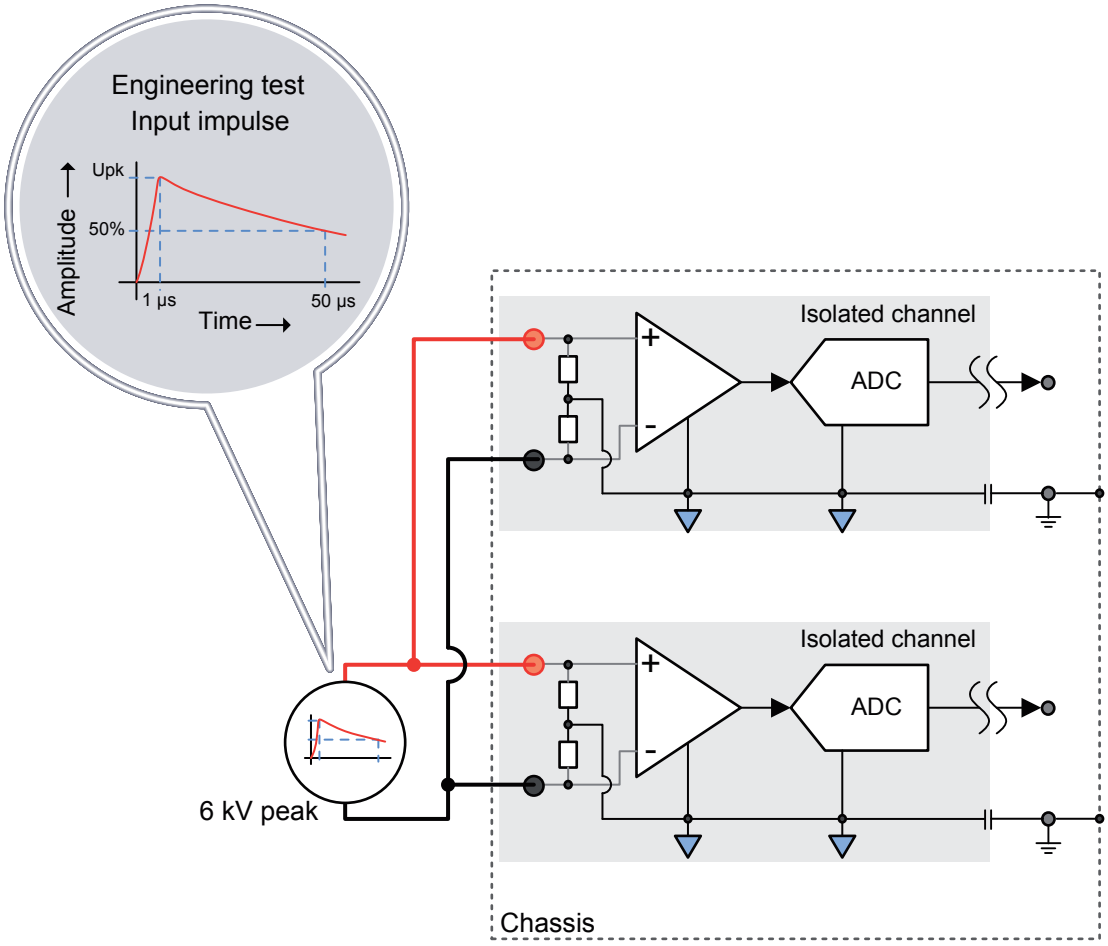


Figure 12.51: Example of 1.2/50 µs impulse

Active input switch test

To guarantee the stability of the channels, the input relays are tested with the maximum input voltage (1000 V) applied. The inputs of the channels have been switched from isolated GND to DC by the input relay, resulting in the 1000 V being applied to the input as a step pulse.

This test is performed with the highest input range (± 1000 V) and repeated with the lowest input range (± 20 mV). Both tests are performed with an input voltage of 1000 V and repeated over 1000 times. These tests have all passed successfully.

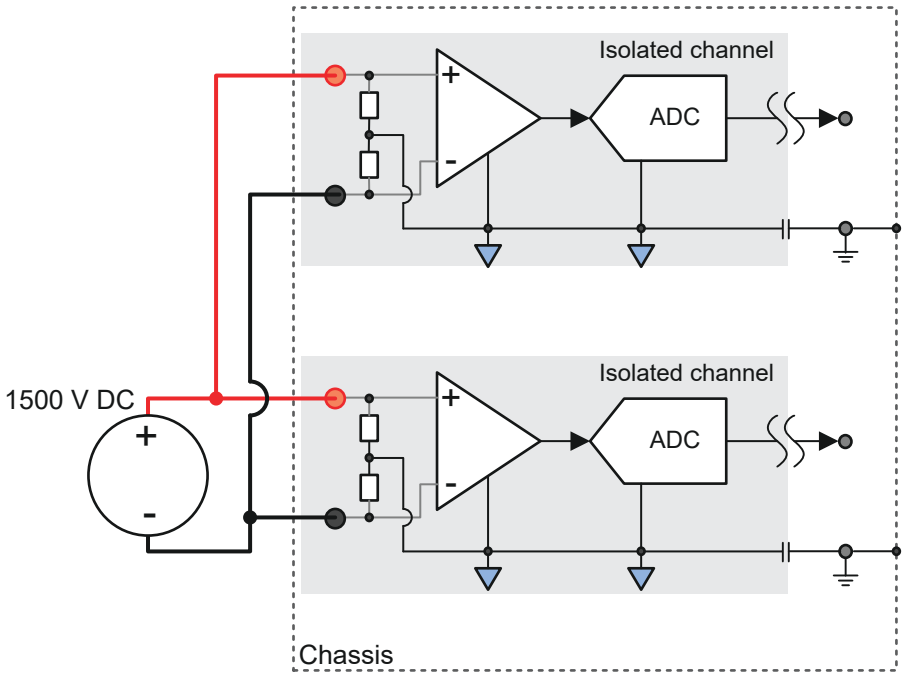


Figure 12.52: Engineering input switching test

12.3.9 GN610B/GN611B protection mechanisms

Overvoltage and current protection

All signal inputs are protected against voltage overload. This is specified at ± 1000 V for all ranges, except for the ± 1000 V range that is limited to ± 1250 V. Exceeding these limits can damage the input card.

GN610B/GN611B input overload protection

The input section has several methods to protect against voltage overload on the input.

Every selected input range allows a 200% overload without any change of input resistance or auto ranging. This 200% overrange is designed to allow for smaller voltage overloads without affecting the measurement. Within this 200% overload, the amplifier is also able to respond with normal rise/fall times and the signal is restored within the standard selected range.

When exceeding the 200% overload, the input impedance might start to increase. The impedance increase lowers the input current. A positive side effect of the lowered current is that the dissipated heat is lowered. It is the excessive heat dissipation that typically damages the input channel.

The first action of the system is to add an additional current load to the input signal to create an extra voltage drop in the input series resistance. The resulting additional current depends on several factors and is therefore unpredictable. A negative side effect of this additional current is that the extra power is dissipated in the input section, which in turn results in additional heat dissipation.

Secondly, the input section starts switching to disconnect itself from the input signal to reduce the power dissipated within the lower ranges of the amplifier (≤ ± 5 V ranges).

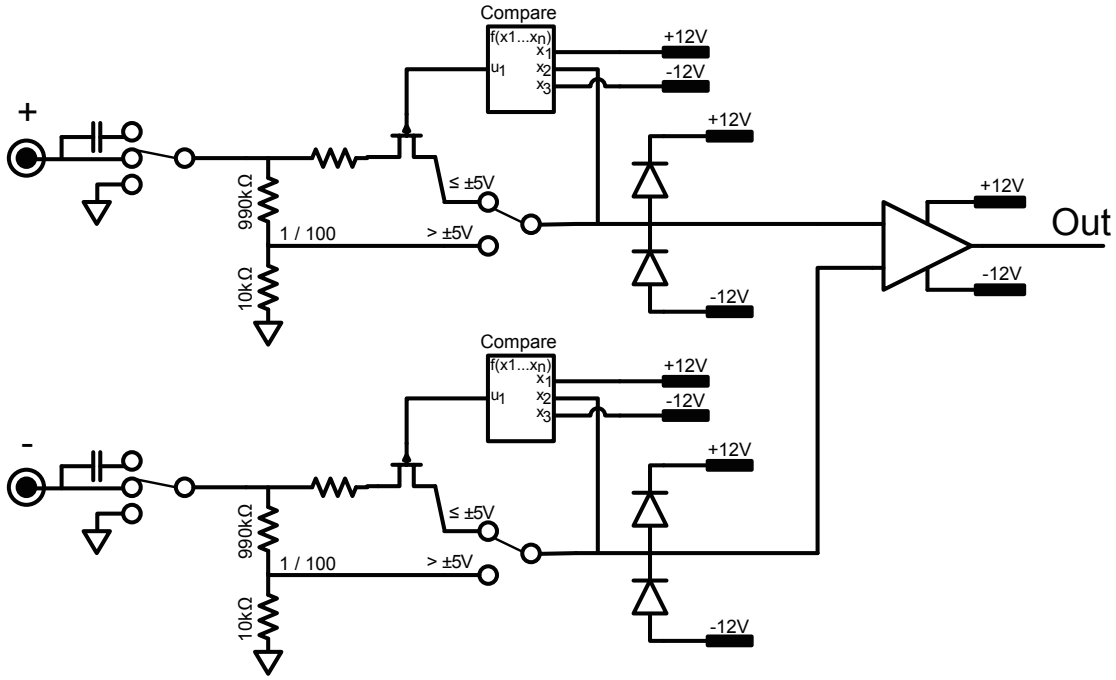


Figure 12.53: Input overload protection - Schematic diagram

Thermal monitor of the input channels
Any overload results in extra heat being generated within the channel. The extra heat is the result of the extra current flowing through the input resistance. The extra heat is also caused by internal amplifier sections driving their local output to maximum levels, which creates excessive heating within the amplifier.

As a third protective mechanism, every input is equipped with a thermal sensor to monitor the local temperature. When the local temperature reaches maximum levels, the system automatically starts changing the input range that has been selected by the user to reduce the dissipated heat. As the heat dissipation does not start the auto ranging immediately, short overloads do not result in auto ranging. A longer overload leads to a higher local temperature, which starts the auto ranging process.

Whenever an overload pushes local temperature to exceed the maximum level, the input range is adapted to a range that is less sensitive by a factor of ten. For example, if the user has selected a range of ± 40 mV and it is necessary, the system changes the range to ± 400 mV. As this might not be enough due to an even higher overvoltage, the system keeps monitoring the local temperature. If the local temperature is not reduced within the expected response time, the system automatically increases the input range by a factor of 10 for a second or third time or however many times it requires to reach safe conditions that do not increase the local temperature anymore.

Every one of the automatic range changes is identified within the measurement data. Not only is the measured input scaled with the adapted input range correctly, but the exact moment when the automatic range change happens is also identified within Perception software.

As the highest range that can be selected, ± 1 kV is the ultimate protection for the system to disconnect the input from the external signal source. This step is only executed if the system is in the ± 1 kV range and the local temperature is still outside maximum operating limits. Disconnecting from the external signal source is done by grounding the input. When inputs are grounded, the only connections to the external signal are the input connectors and the input pin of the ground relay.

Thermal shutdown in critical conditions

This protective scheme allows for any overload that the input could be confronted with during normal operation. For any other failure that could result in excessive heat dissipation, the GEN series probes have a last protective stage built in. When local temperatures reach critical limits, the system automatically turns off the mains power to prevent damage to the system or other systems near the GEN series system. Maximum and critical temperatures are defined as such that it is very unlikely the system would ever reach these critical temperatures when operating within its specified conditions.

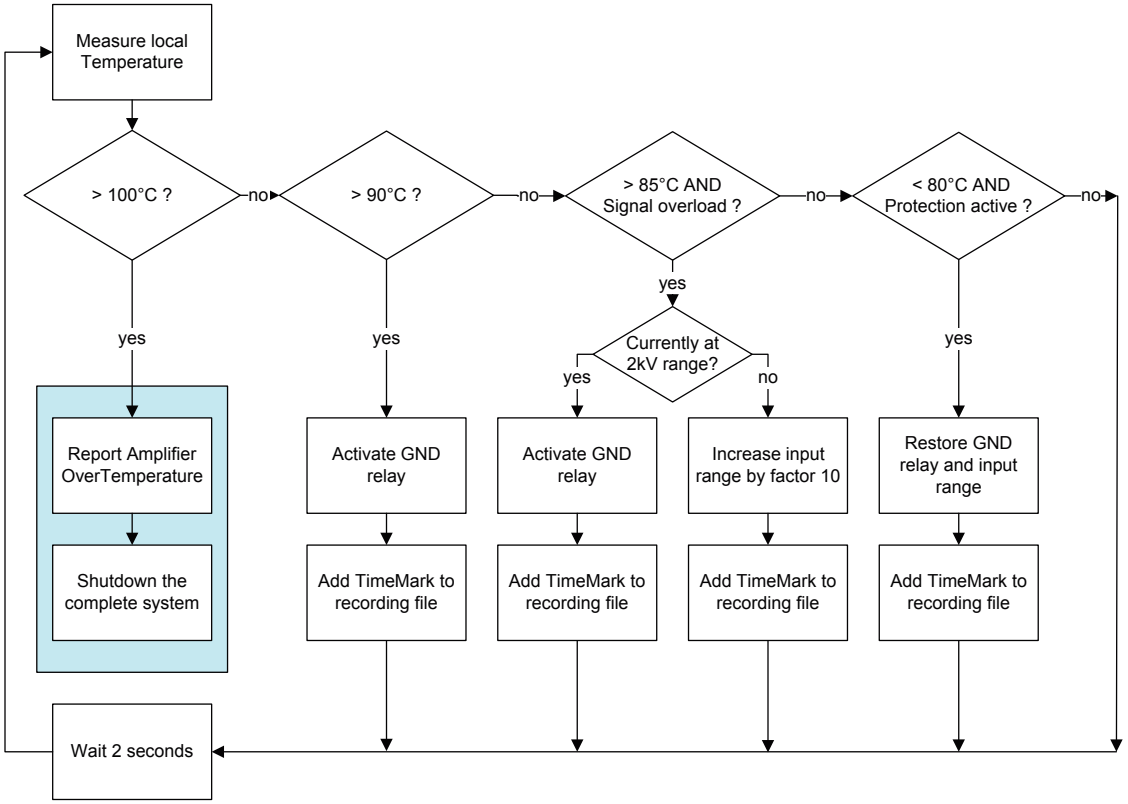


Figure 12.54: Automatic thermal overload response

Restore range selected by user automatically

As the GEN series system is designed to measure 24 hours a day, 7 days a week, the automatic range switching has the negative side effect of reducing the sensitivity of the amplifier. During the actual overload, the channel is unable to measure the input signal. Therefore, there are no extra negative side effects. If the overload disappears and the system runs unattended, the input range that is selected automatically will not be the best measurement range. Therefore, the amplifier "remembers" the range that the user originally selected and restores this range as soon as regular thermal conditions are restored. A temporary large overload will then only result in input sensitivity that is adjusted temporarily.

The automatic range adaptation is started due to thermal conditions typically as a result channel input overload. Therefore, the overload might still be present. If this is the case the automatic range restore restarts, the thermal increase and leads to re-trigger the automatic range adaption process and the overload is handled exactly the same way as before.

If the overload is permanent, the system keeps on automatic ranging to reduce the dissipated heat. The system then restores the range selected by the user, causing overheating again and thereby restarting the automatic ranging process again. This cycle will repeat forever until the overload condition disappears.

12.4 Isolated Basic/IEPE cards

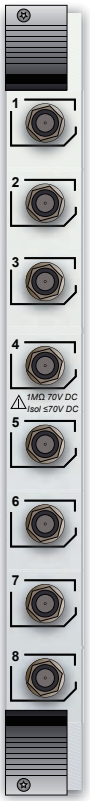
12.4.1 GN815, Isolated Basic/IEPE 2MS/s input card

- **IEPE transducer support**
- **TEDS Class 1 support for IEPE**
- **Isolated, unbalanced differential inputs**
- **± 10 mV to ± 50 V input range**
- **Analog/digital anti-alias filters**
- **18 bit at 2 MS/s sample rate**
- **8 analog channels**
- **2 GB memory**
- **Isolated metal BNC per channel**
- **Real-time cyclic calculators**
- **Triggering on real-time results**
- **Digital Event/Timer/Counter support**
- **1 kV RMS CAT II probe**
- **1 kV RMS differential probe**
- **Current clamps and burdens**

The GEN DAQ Basic/IEPE ISO 2 MS/s Input Card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or probes and current clamps.
This card also supports IEPE transducers and TEDS Class 1 for easy setup of the acquisition channels. Built-in diagnostics supports automatic sensor connected, open or shorted detection.
The amplifier provides voltage inputs from ± 10 mV to ± 50 V. Optimum anti-alias protection is achieved by the 7-pole analog anti-alias filter combined with a fixed 2 MS/s sampling Analog-to-Digital converter. The digital filters operating at the full ADC sample rate offer a large range of high order anti-alias filter characteristics with precise phase match and noise-free digital output.
For true real-time analysis, the card offers real-time cycle or timer based calculations. Automatic zero crossing detection allows for asynchronous true RMS, mean and other calculations that can be used to trigger the recording.
The GEN DAQ series input card offers 16 digital input events, two digital output events and two Timer/Counter channels.
Using voltage probes a single-ended 600 V RMS CAT III / 1000 V CAT II or a differential 1000 V RMS CAT III (1000 V RMS common mode) measurement range is created. The use of current clamps and external burdens allow for direct current measurements.

For specification and ordering information, please refer to the GN815 data sheet.

12.4.2 GN816, Isolated Basic/IEPE 200kS/s input card



- **IEPE transducer support**
- **TEDS Class 1 support for IEPE**
- **Isolated, unbalanced differential inputs**
- **± 10 mV to ± 50 V input range**
- **Analog/digital anti-alias filters**
- **18 bit at 200 kS/s sample rate**
- **8 analog channels**
- **200 MB memory**
- **Isolated metal BNC per channel**
- **Real-time cyclic calculators**
- **Triggering on real-time results**
- **Digital Event/Timer/Counter support**
- **1 kV RMS CAT II probe**
- **1 kV RMS differential probe**
- **Current clamps and burdens**

The GEN DAQ Basic/IEPE ISO 200 kS/s Input Card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or probes and current clamps.
This card also supports IEPE transducers and TEDS Class 1 for easy setup of the acquisition channels. Built-in diagnostics supports automatic sensor connected, open or shorted detection.
The amplifier provides voltage inputs from ± 10 mV to ± 50 V. Optimum anti-alias protection is achieved by the 7-pole analog anti-alias filter combined with a fixed 2 MS/s sampling Analog-to-Digital converter. The digital filters operating at the full ADC sample rate offer a large range of high order anti-alias filter characteristics with precise phase match and noise-free digital output.
For true real-time analysis, the card offers real-time cycle or timer based calculations. Automatic zero crossing detection allows for asynchronous true RMS, mean and other calculations that can be used to trigger the recording.
The GEN DAQ series input card offers 16 digital input events, two digital output events and two Timer/Counter channels.
Using voltage probes a single-ended 600 V RMS CAT III / 1000 V CAT II or a differential 1000 V RMS CAT III (1000 V RMS common mode) measurement range is created. The use of current clamps and external burdens allow for direct current measurements.

For specification and ordering information, please refer to the GN816 data sheet.

12.4.3 Using the GN815 and GN816

WARNING

High bandwidth and measurement cabling

Due to the high bandwidth measurement capabilities of the acquisition card, combined with the high measurement sensitivity of the card, it is important to pay close attention to the measurement cabling.

Some advice to prevent measuring unwanted disturbances:

- Keep measurement cables as short as possible in order to reduce the reception of environmental disturbances.
- Use shielded cables. The cable should have the measurement cables paired inside a shield. Preferably, the shield should be connected to the chassis of the measurement Genesis High Speed equipment. Alternatively, the shield could also be connected to the chassis of the object under test.

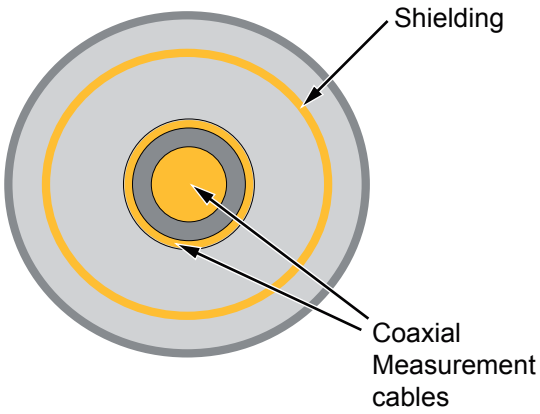


Figure 12.55: Shielded cable

- For high frequency disturbances where high bandwidth measurement is not required, the measurement bandwidth can be reduced by using the lowpass filter of the acquisition card.
- If unshielded cables are used, keep them as close together as possible, i.e. position them next to each other (to keep the loop small).
- Make sure that measurement cables that are used for measuring high dynamic or distorting signals are not closely positioned to measurement cables used for measuring small sensitive signals.

- Keep all measurement cables well separated from cables connected to high switching loads or motor cables.
- Separate measurement equipment and cables from potentially interfering equipment like frequency inverters or wireless equipment.

General cabling remark: Only use properly rated cables to measure the signal. Both the voltage and current rating should be matched to the signal for measurements.

WARNING

This instrument must be properly grounded.

When using this card, HBM advise using the standard GEN series protective ground connections to ensure that the entire unit is grounded.
Please see section "Connecting power" on page 64 for further details.

If connection to a protective ground is not possible for any reason, then please refer to the international safety standard EN 50191:2000

WARNING

Overvoltage and current protection

The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is inactive as long as the input voltage is less than 200% of the selected input range.

WARNING

Disconnect voltages before removing the card from the system.

The measuring circuit can carry hazardous voltages and should be disconnected before the card is removed from the card slot of the measurement system.

WARNING

Connectors and cables

The specified ± 50 V DC voltage range of the Isolated Basic acquisition card is such that it falls below the low voltage limit as specified in IEC61010-1.

The limit for safe voltage and currents is set in the IEC61010-1 standard in Section 6.3 – limit values for accessible parts. The limits are:

Table 12.4: Limit for safe voltage and currents is set in the IEC61010-1

	Normal operation	Single fault condition
Voltage	70 V DC	140 V DC
	33 V RMS	55 V RMS
	46.7 V peak	78 V peak
Current	2 mA DC	15m A DC
	0.5 mA RMS	3.5m A RMS
	0.7 mA peak	5 mA peak

It is good practice to use isolated measurement cables. However, since the voltage range of the Isolated Basic card falls below the low voltage limit for accessible parts, non-protected or non-shrouded connectors can also be used with this card.

Figure 12.56: Safe connectors for use with Isolated Basic acquisition cards

12.4.4 Understanding the GN815 and GN816 isolation

The specified ± 50 V DC voltage range of the Isolated Basic acquisition card is such that it falls below the low voltage limit as specified in IEC61010.

The isolation of the Isolated Basic card (GN815 and GN816) is in line with the limit for safe voltage and currents as mentioned above.

Table 12.5: Limit for safe voltage and currents (GN815 and GN816)

Input signal to input signal	± 140 V DC, 55 V RMS (low voltage limit)
Input signal-to-chassis	± 70 V DC, 33 V RMS (low voltage limit)
Channel to chassis	± 70 V DC, 33 V RMS (low voltage limit)
Channel to channel	± 70 V DC, 33 V RMS (low voltage limit)
Nondestructive, to chassis (earth)	± 70 V DC, 33 V RMS AC (low voltage limit)

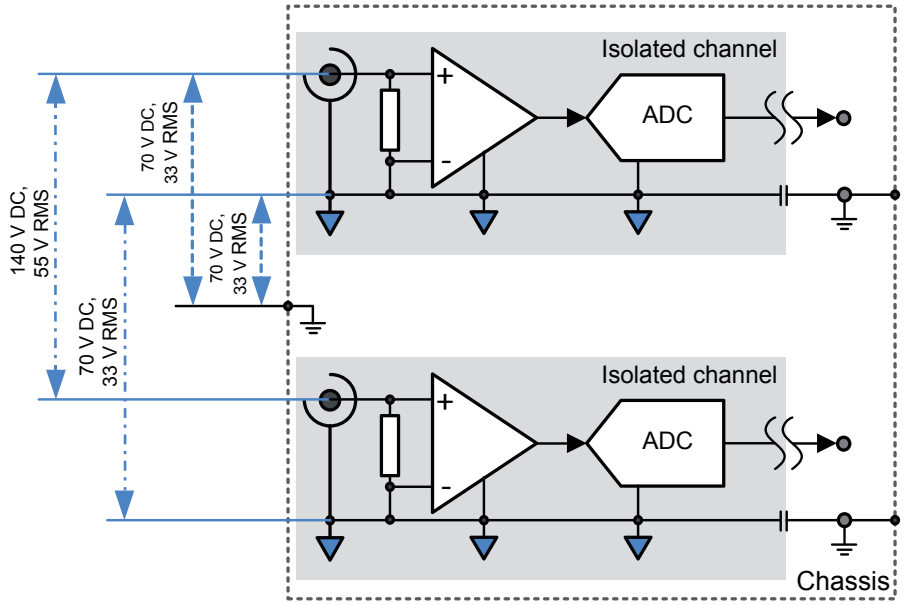


Figure 12.57: Isolation of the Isolated Basic card (GN815/GN816)

12.4.5 Understanding the GN815 and GN816 input

The isolation of the GN815's and GN816's signal input channels are single-ended (also termed unbalanced isolated or unbalanced differential isolated).

This means that one signal of both inputs within one channel pair is directly connected to the isolated channel ground (this is the outer signal of the BNC plug). The other signal is connected to the conditioning amplifier.

A (simplified) schematic representation of the input channel of the GN815 and GN816 can be found below.

The input channels of the GN816 and GN816 are isolated. This means that the input channel and amplifier are fully isolated from (earth) ground. In this context, fully isolated means a very high resistance and a very small capacitive coupling to ground. This is for safety and to avoid ground loops.

Characteristics per channel:

- The input BNC connector is isolated from the system ground.
- The isolated ground is externally accessible, as shown in Figure 12.58.

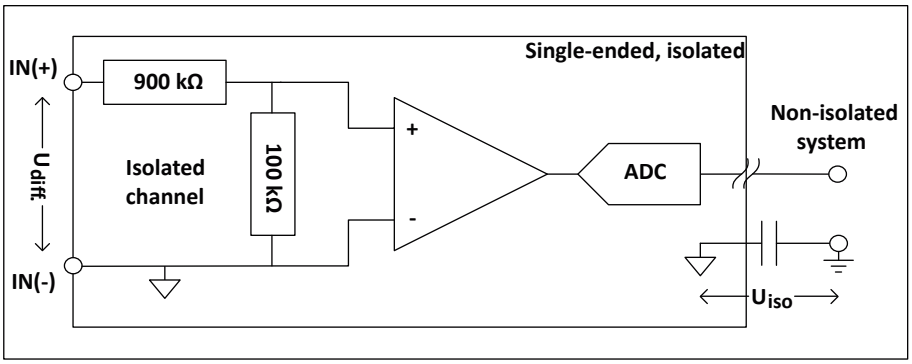


Figure 12.58: Single-ended isolated input channel

Using probes:

It is possible to use passive voltage probes with single-ended isolated inputs.

Using a standard passive 10:1 probe in combination with the GN815 and GN816 results in the situation shown in Figure 12.59.

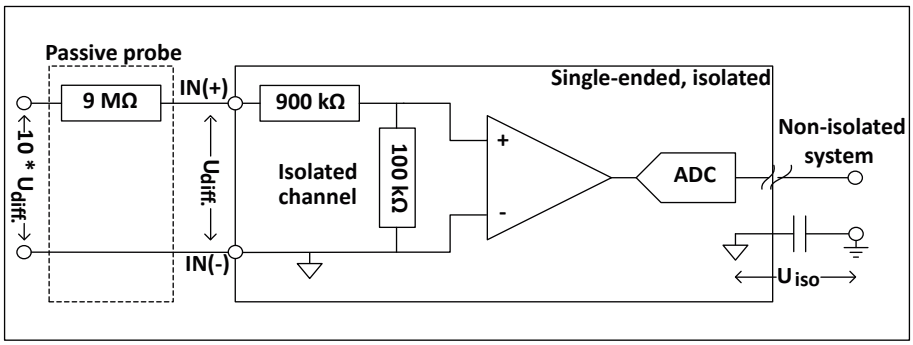


Figure 12.59: Input channel with a standard 10:1 passive probe

Using a high voltage passive 10:1 probe in combination with the GN815 and GN816 results in the situation shown in Figure 12.60. The voltage division is done externally in the probe to maintain accuracy.

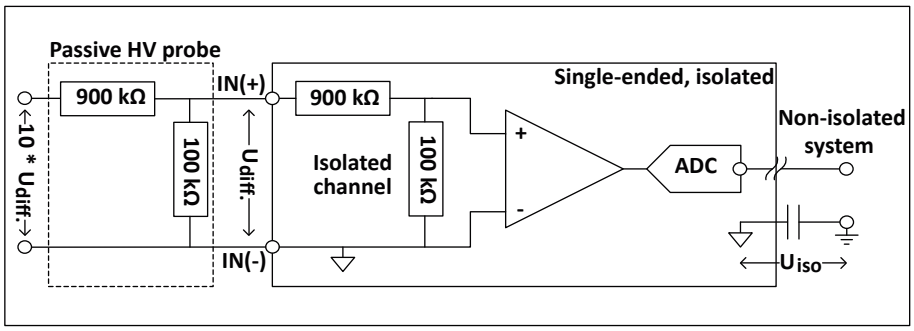


Figure 12.60: Input channel with a high voltage 10:1 passive probe

12.4.6 GN815 and GN816 Input overload protection

The input section has several methods to protect against voltage overload on the input.

Every selected input range allows a 200% overload without any change of input resistance or auto ranging. This 200% overrange is designed to allow for smaller voltage overloads without affecting the measurement. Within this 200% overload, the amplifier is also able to respond with normal rise/fall times and the signal is restored within the standard selected range.

When exceeding the 200% overload, the input channel might start to take protective actions.

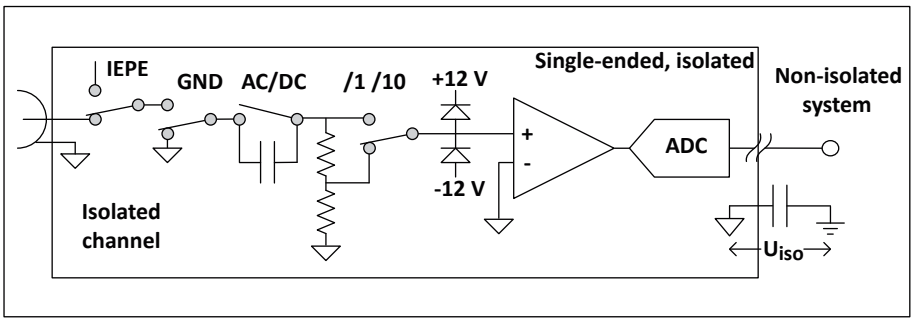


Figure 12.61: Input overload protection - Schematic diagram

The **first** action of the system is to add an additional current load to the input signal to create an extra voltage drop in the input series resistance. The resulting additional current depends on several factors and is therefore unpredictable. A negative side effect of this additional current is that the extra power is dissipated in the input section, which in turn results in additional heat dissipation.

Thermal monitor of the input channels
Any overload results in extra heat being generated within the channel. The extra heat is the result of the extra current flowing through the input resistance. The extra heat is also caused by internal amplifier sections driving their local output to maximum levels, which creates excessive heating within the amplifier.

The **second** action of the system is to react to the increased temperature in the channel as a result of the overvoltage. Every input is equipped with a thermal sensor to monitor the local temperature. When the local temperature reaches maximum levels, the system automatically starts changing input range selected by the user to reduce the dissipated heat. As the heat dissipation does not start the auto ranging immediately, short overloads do not result in auto ranging. A longer overload leads to higher local temperature, which starts the auto ranging process. The system automatically increases the input range for as many times as it requires to reach a safe conditions that do not increase the local temperature anymore.
Every one of the automatic range changes is identified within the measurement data. Not only is the measured input scaled with the adapted input range correctly, but the exact moment when the automatic range change happens is also identified within Perception software.

Restore range selected by user automatically
As the GEN series system is designed to measure 24 hours a day, 7 days a week, the automatic range switching has the negative side effect of reducing the sensitivity of the amplifier. During the actual overload, the channel is unable to measure the input signal. Therefore, there are no extra negative side effects. If the overload disappears and the system runs unattended, the input range that is selected automatically will not be the best measurement range. Therefore, the amplifier "remembers" the range that the user originally selected and restores this range as soon as regular thermal conditions are restored. A temporary large overload will then only result in input sensitivity that is adjusted temporarily.

The automatic range adaptation is started due to thermal conditions typically as a result channel input overload. Therefore, the overload might still be present. If this is the case the automatic range restore restarts, the thermal increase and leads to re-trigger the automatic range adaption process and the overload is handled exactly the same way as before.

The **third** action of the system takes effect if the second action is unsuccessful and the local temperature remains outside of the maximum operating limits. The input signal is disconnected from the channel. Grounding the input disconnects the input signal from the external signal source. When inputs are grounded, the only connections to the external signal are the input connectors and the ground relay's input pin.

Thermal shutdown in critical conditions

This protective scheme allows for any overload that the input could be confronted with during normal operation. For any other failure that could result in excessive heat dissipation, the GEN series probes have a last protective stage built in. When local temperatures reach critical limits, the system automatically turns off the mains power to prevent damage to the system or other systems near the GEN series system. Maximum and critical temperatures are defined as such that it is very unlikely the system would ever reach these critical temperatures when operating within its specified conditions.

12.5 Basic high speed input card

12.5.1 GN8101B/GN8102B/GN8103B, Basic 250, 100, 25 M/s input cards

- **8 analog channels**
- **Single-ended inputs**
- **1 MΩ or 50 Ω termination**
- **± 10 mV to ± 100 V input range**
- **Analog/digital anti-alias filters**
- **14/16 bit resolution**
- **Real-time formula database**
- **Digital Event/Timer/Counter**
- **Multi sweep transient recorder**
- **Continuous/Dual sample rate**
- **Differential input using probes**

The input card is a general purpose single-ended voltage input card. An external active differential probe supports measuring the differential signal directly at the source and creates the best high frequency common mode suppression possible.
For high frequency measurements, the inputs support a built-in 50 Ω termination option. The use of the 50 Ω termination supports voltage inputs from ± 10 mV to ± 5 V. The alternative 1 MΩ termination provides voltage inputs up to ± 100 V.
In multi sweep transient recorder mode triggers can be recorded without any re-arm time between sweeps, combined with sweep stretch to create variable post-trigger lengths.
Optimum anti-alias protection is achieved by the 6-pole analog anti-alias filter combined with a fixed high speed sampling Analog-to-Digital converter.
For sample rates 100 MS/s and lower, the digital anti-alias filter allows for a large range of high order filter characteristics with precise phase match and noise-free digital output.
The real-time formula database calculators option offers math routines to solve many real-time mathematical challenge like obtaining mechanical power and/or multi-phase (not limited to three) electric power (P, Q, S) or even efficiency calculations.
Every cycle based result from the real-time formula database can be transferred in real-time to the EtherCAT® output card.
Using voltage probes a single-ended 600 V RMS CAT III / 1000 V CAT II or a differential 1000 V RMS CAT III (1000 V RMS common mode) measurement range is created. The use of current clamps and external burdens allow for direct current measurements.

For specification and ordering information, please refer to the GN8101B, GN8102B, GN8103B data sheet.

12.6 High resolution universal input card

12.6.1 GN840/GN1640 Universal 500 kS/s 8/16 channel input cards

- **Ranges ± 0.2 mV/V up to ± 500 mV/V**
- **Quarter/Half/Full bridge**
- **6 wire configuration**
- **Quick sensor test (shunt)**
- **Voltage excited sensors**
- **IEPE sensors**
- **IEEE 1451.4 TEDS class 1, 2 and 3**
- **Piezoelectric/Charge sensors**
- **4 to 20 mA sensors**
- **Pt10, Pt100, Pt500, Pt1000 and Pt2000 (3 and 4 wire RTD)**
- **Thermocouples K, J, T, B, E, N, R, S, C**
- **Resistor value**
- **33 V RMS Isolation**
- **Analog/digital anti-alias filters**
- **500 kS/s sample rate/channel**
- **24 bit ADC resolution**

The Universal Sensor Card supports quarter, half and full bridges with built-in 350 Ω and 120 Ω quarter bridge completion resistors. The shunt resistor offers a quick test of the sensor.
In IEPE mode the card supports open and shorted wire detection and TEDS sensor setup. Thermocouples, piezoelectric, RTD and 4 to 20 mA sensors are all directly supported.
All sensor types connect to the input without external adapters.
Measurement ranges starting at ± 0.2 mV/V up to ± 500 mV/V and sensor impedance from 17 Ω up to 10 kΩ support virtually any sensor.
Superior, best in class anti-alias protection is achieved by a unique, multi stage approach.
The first stage the Sigma Delta converter with built in anti-aliasing filter creates an alias free digital data stream at constant rate of 500 kS/s.
The second stage feeds the 500 kS/s data stream into a user selectable digital filter, to reduce the signal to the desired maximum bandwidth. The digital filter supports both 11 or 12 orders as well as Bessel/Butterworth or Elliptic filter characteristics.
The third stage decimates the 500 kS/s filtered signal to the desired sample rate.

The digital filter before decimation guarantees a superior phase match, ultra-low noise and alias free result.
The optional real-time formula database calculators solve almost any mathematical challenge. Real-time digital cycle detection enables periodic results like PeakToPeak. Real-time channel to channel sample math can reverse calculate crosstalk interdependencies within a three axes force sensor. Calculated results can be used to trigger the recording or signal alarms to the external world.
For more information on the High resolution universal input card, please refer to the GN840B, GN1640B data sheet.

Supported sensor modes

- "Basic mode and cabling" on page 283
- "Bridge mode and cabling" on page 284
- "Basic sensor and cabling" on page 288
- "Integrated Electronic Piezoelectric (IEPE) mode and cabling" on page 289
- "Piezoelectric (Charge) mode and cabling" on page 290
- "Resistive Temperature Detectors (RTD) mode and cabling" on page 291
- "Current loop mode and cabling" on page 295
- "Thermocouple mode and cabling" on page 296

12.6.2 Basic mode and cabling

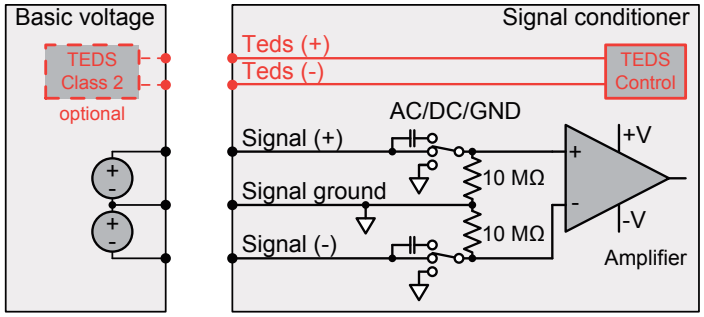


Figure 12.62: Basic mode block diagram

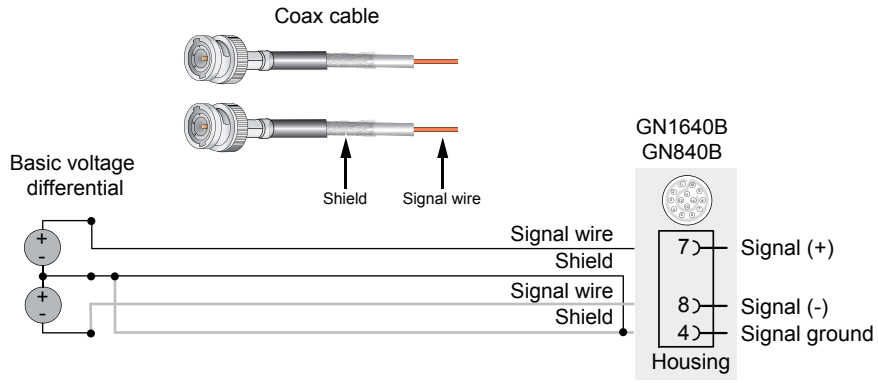


Figure 12.63: Recommended basic voltage differential connection

12.6.3 Bridge mode and cabling

Bridge amplifier configuration

Input diagrams and typical connection diagrams for the GN840B/GN1640B bridge mode are shown on this and the following pages. For the maximum versatility, the amplifiers allow a wide range of configurations. A minimum of three wires are necessary for a quarter- or half-bridge sensor and four wires for a full bridge. Optional remote sensing of excitation voltage is supported for precision transducer applications, which adds two wires. If remote sense is not required, the sense wires must be connected within the channel connector as the sense lines are always active. Remote shunt calibration is possible with the addition of one more wire. An isolated common is provided for preferred double shielding.

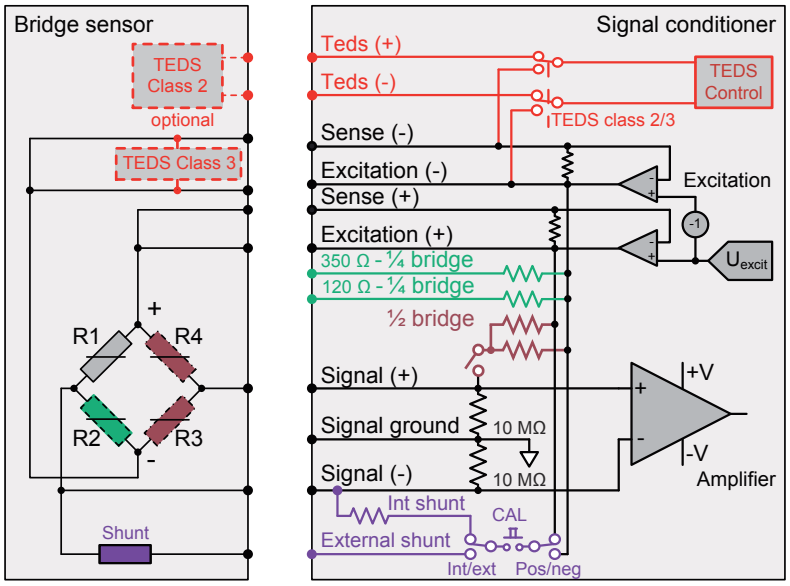


Figure 12.64: Bridge mode block diagram

Bridge completion

Each bridge amplifier channel contains a pair of fixed 10 kΩ resistors for half bridge completion that can be switched in by software control. Additional pins on the input connector provide a precision 120 Ω and 350 Ω resistor for quarter-bridge completion.

Sense lines
Remote sensing of excitation voltage, is commonly recommended for use with precision, commercial transducers to prevent lead-wire resistance changes (due to changes in either temperature or length) from affecting transducer span, or sensitivity. Lead-wire attenuation presents a potentially significant error source in transducers utilizing a Wheatstone bridge circuit. The lead-wires represent a parasitic resistance, and a portion of the excitation voltage intended for the bridge circuit is dropped in the lead-wire system, reducing the voltage actually present at the transducer, and effectively reducing the transducer sensitivity.

Bridge balance
The bridge circuit is only in balance (has zero output when the bridge voltage is applied) when R1 / R2 = R4 / R3. Taking the various resistance tolerances on the strain gauge(s), resistors and lead wires into account, an initial unbalance is invariably present. Adjusting the initial balance so that there is zero output at zero strain is achieved by bridge balancing.

Shunt calibration
Each bridge amplifier channel contains 100 KΩ, 0.1% fixed precision resistor that can be switched in by software control. With a gage factor of 2.00, this resistor simulates the following values of deflection for various bridge configurations.

Table 12.6: Deflection for various bridge configurations

	100 KΩ		
BRIDGE	**1000 Ω**	**350 Ω**	**120 Ω**
mV/V	2.4888	0.873	0.299
µstr full bridge	1244	437	150
µstr $^1/_2$ bridge	2488	873	300
µstr $^1/_4$ bridge	4975	1747	600

A second calibration resistor can be connected to the connector pin externally. Either one of the shunt calibration resistors can be switched in by software control to provide multi-point calibration and linearity verification.

Shielding and immunity increase
Using high bandwidth amplifiers like the GN840B/GN1640B, any external disturbance typically is immediately reflected in the measured signal. To minimize external disturbance pick-up the excitation, sense and signal leads are generally separately twisted and shielded within the cable to minimize the cross-coupling that would otherwise occur.

Double shielding is strongly recommended to maximum disturbance reduction. Attach the signal ground to an inner shield of the double shielded cable. The inner shield is as close as possible to a potential that is equal to the common mode voltage of the bridge. The shield now minimizes the potential difference between the internal conductors and the inner shield, thereby reducing the amount and levels of partial discharges between them. In all cases, the shield is terminated only at the conditioner terminal.

When the inner shield is surrounded by an outer shield that is terminated to ground at the mainframe connector. The ground shield is used to keep most of the external disturbances away.

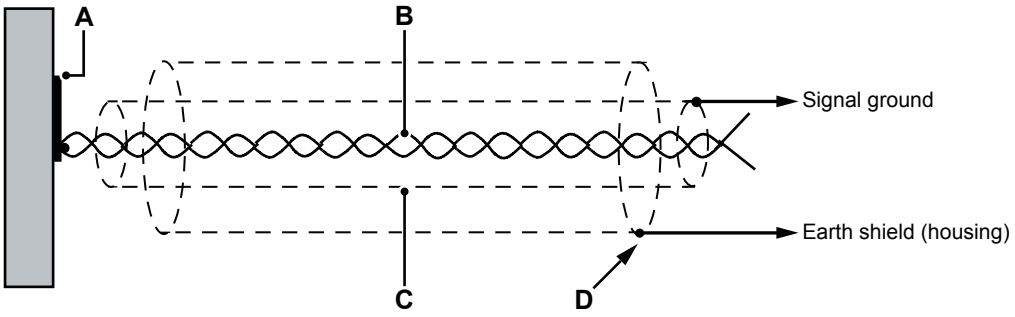


Figure 12.65: Double shielded cable to minimize induced noise

A Strain gauges

B Signal conductors

C Inner shield
Signal ground

D Outer shield
Terminated at connector (measurement channel)

Various bridge configurations

The diagrams below shows possible bridge configurations.

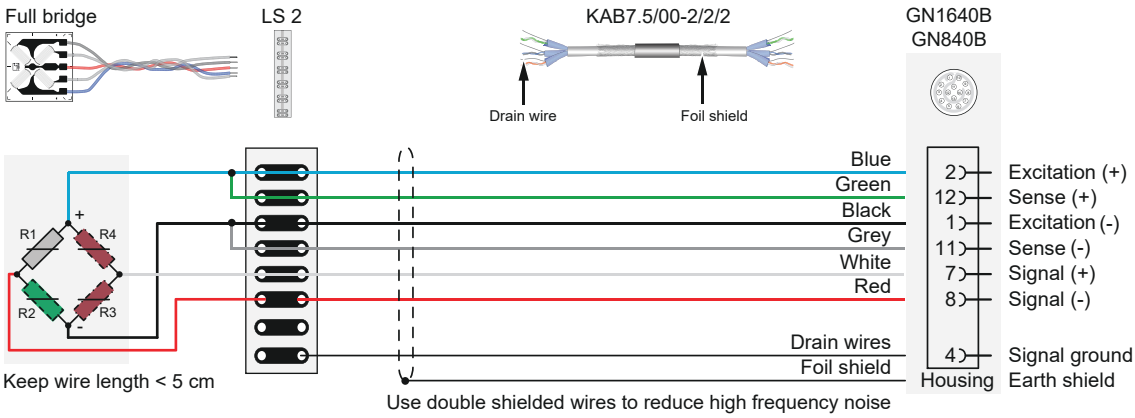


Figure 12.66: Recommended 6 wire full bridge connection (more options are available)

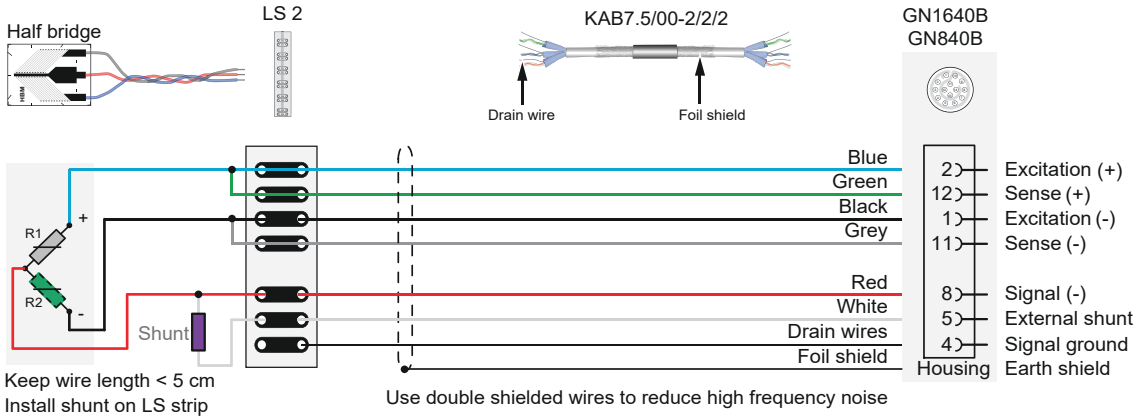


Figure 12.67: Recommended 6 wire half bridge with shunt resistor connection (more options are available)

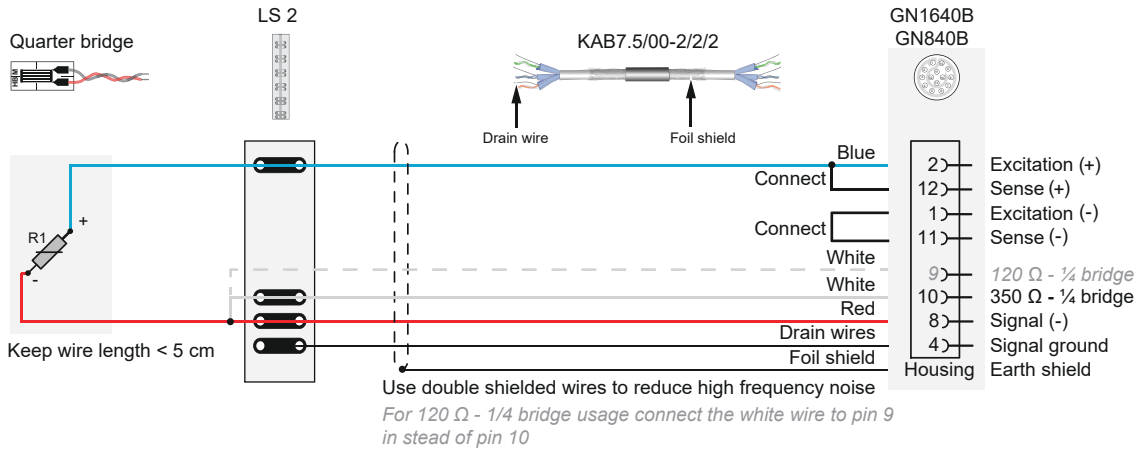


Figure 12.68: Recommended 3 wire 350 Ω quarter bridge connection (more options are available)

12.6.4 Basic sensor and cabling

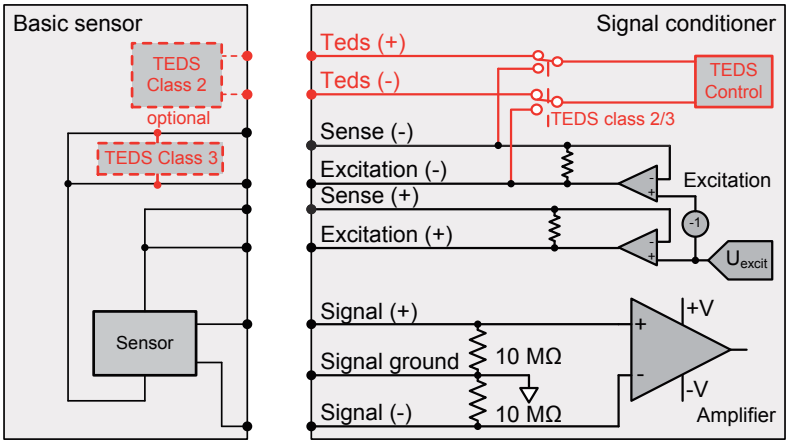


Figure 12.69: Basic sensor mode block diagram

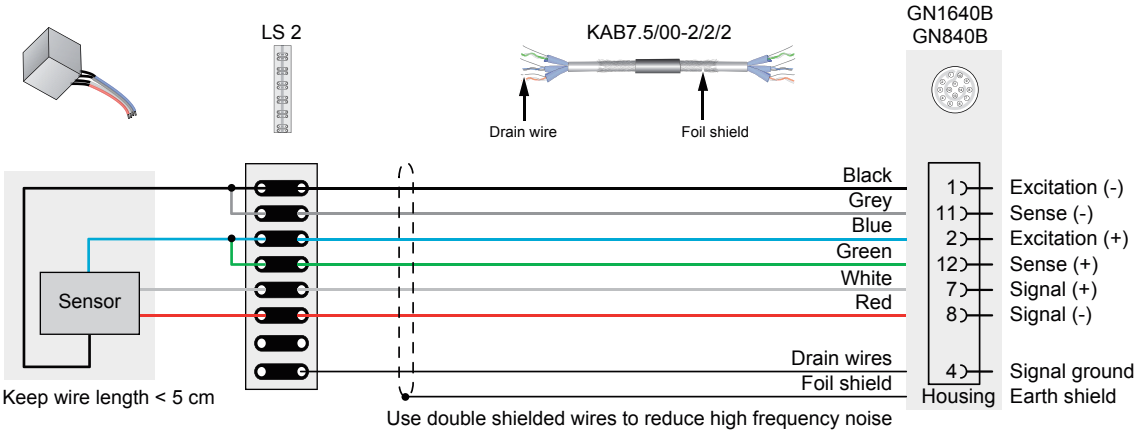


Figure 12.70: Recommended 6 wire basic sensor connection (more options are available)

12.6.5 Integrated Electronic Piezoelectric (IEPE) mode and cabling

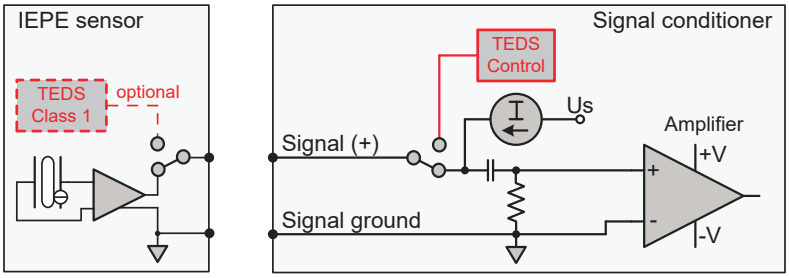


Figure 12.71: IEPE mode block diagram

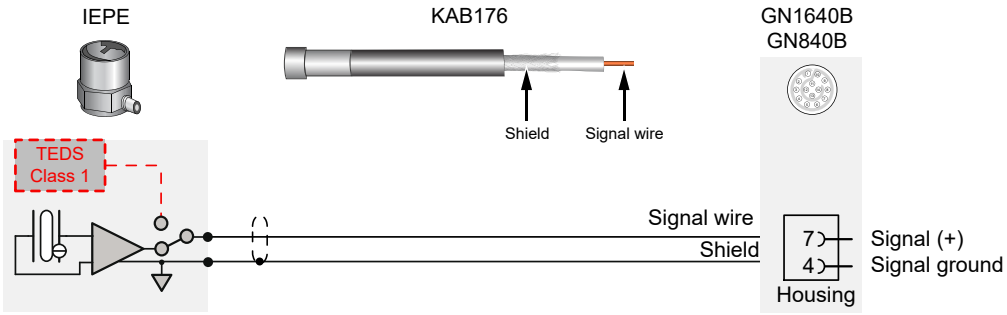


Figure 12.72: Recommended IEPE connection

12.6.6 Piezoelectric (Charge) mode and cabling

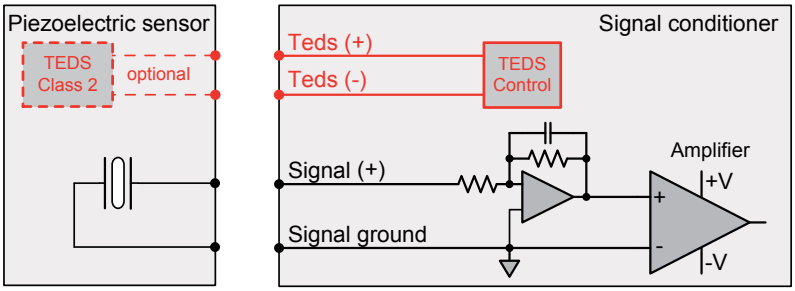


Figure 12.73: Piezoelectric mode block diagram

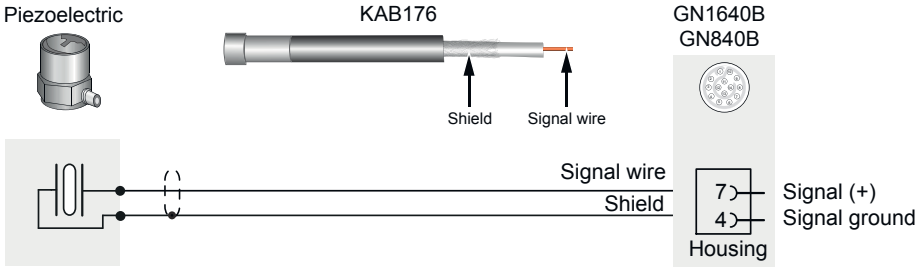


Figure 12.74: Recommended piezoelectric connection

12.6.7 Resistive Temperature Detectors (RTD) mode and cabling

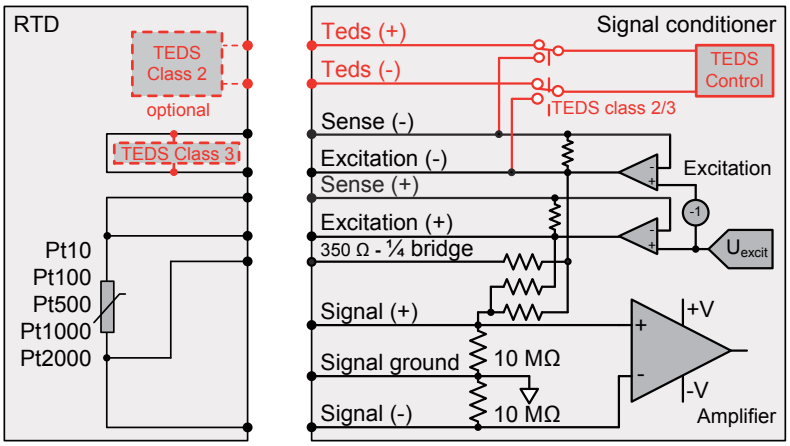


Figure 12.75: RTD mode block diagram

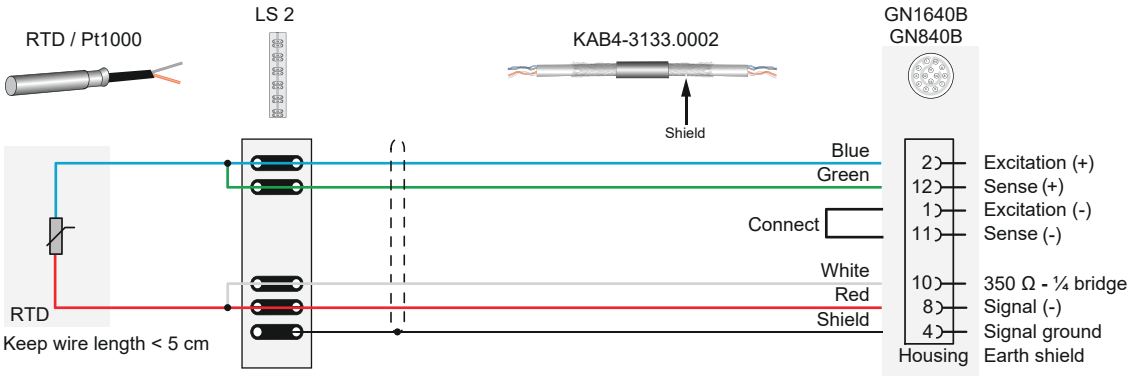


Figure 12.76: Recommended 4 wire RTD connection (more options are available)

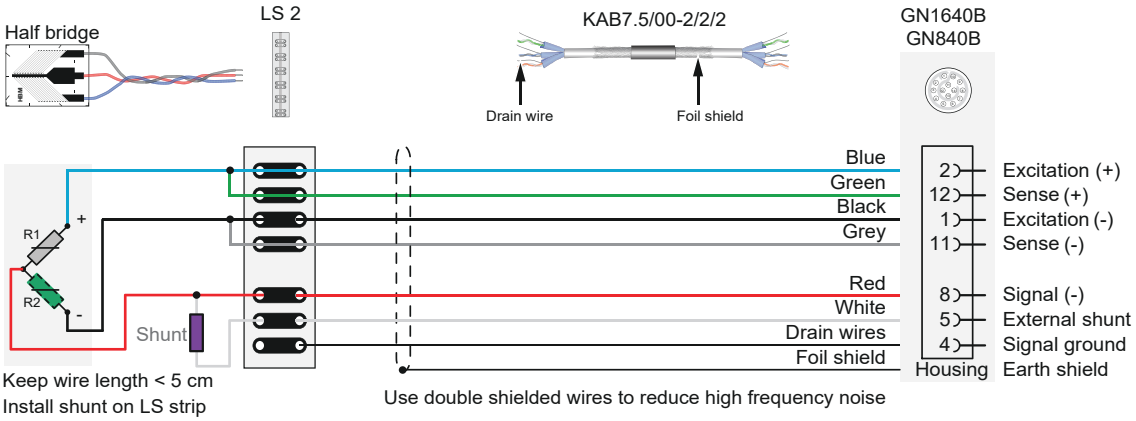
12.6.8 Resistance mode

The resistance measurement is based on the bridge of Wheatstone. This measurement can be implemented using two modes:

- Half bridge
- Quarter bridge

The impedance of the wiring can influence the measurement. The half bridge setup gives the best trade-off between simple schematics and performance. The quarter bridge schematics are another alternative, but can influence the resistance values of the bridge significantly.
The details of the bridge setup are described in a separate chapter, see chapter "Bridge mode and cabling" on page 284.

The accuracy of the resistance measurement can be influenced by choosing the completion resistor (R2) optimally. Accuracy improves if value of the completion resistor is chosen near the resistance to measure. The relation between UR and R is asymptotic, see formulas (Figure 12.78) and figures (Figure 12.77 / Figure 12.78) below.
The GN840B/GN1640B supports two internal completion resistors, respectively 350 Ω and 120 Ω. The completion resistor can also be setup externally by the user in half bridge mode.



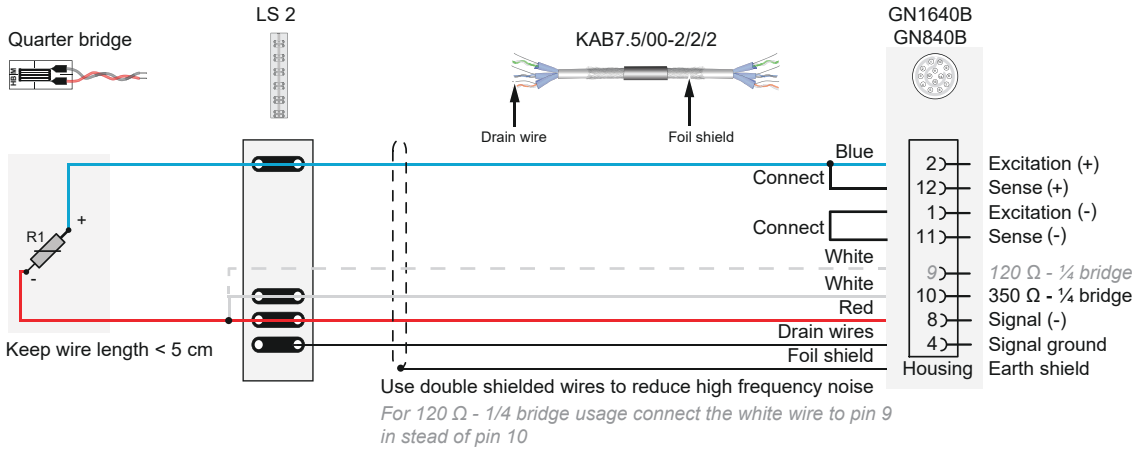


Figure 12.77: Half and quarter bridge schematics

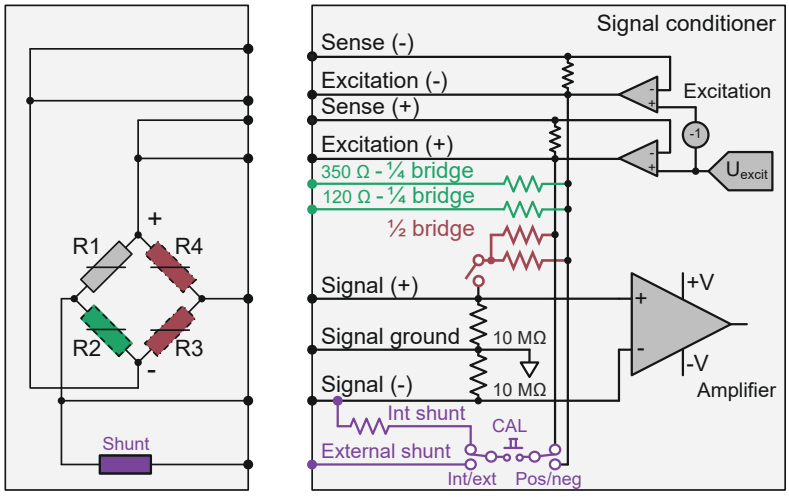


Figure 12.78: Resistance mode block diagram

U_R = signal(+) – signal (-)

U_{exc} = excitation voltage

$$U_R = U_{exc} \left(\frac{1}{2} - \frac{R1}{R1 + R2}\right)$$

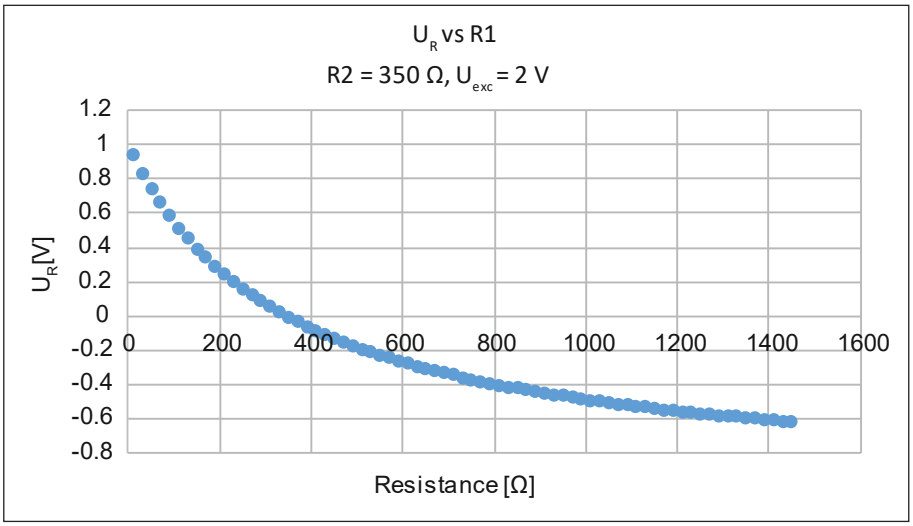


Figure 12.79: Resistance U^R vs. R1

Converting the measured voltage U_R to resistance via the asymptotic curve goes hand in hand with an increasing non-linear error in the resistance read out.

12.6.9 Current loop mode and cabling

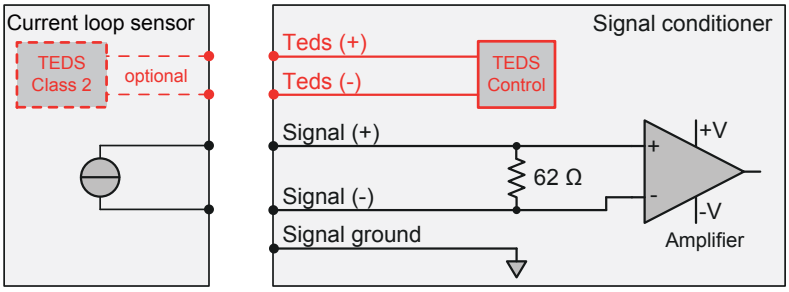


Figure 12.80: Current loop mode block diagram

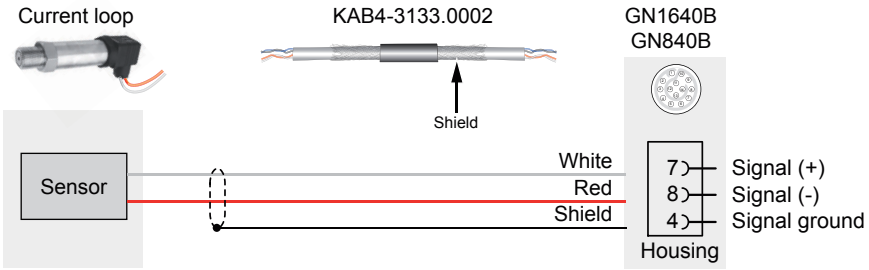


Figure 12.81: Recommended current loop connection

12.6.10 Thermocouple mode and cabling

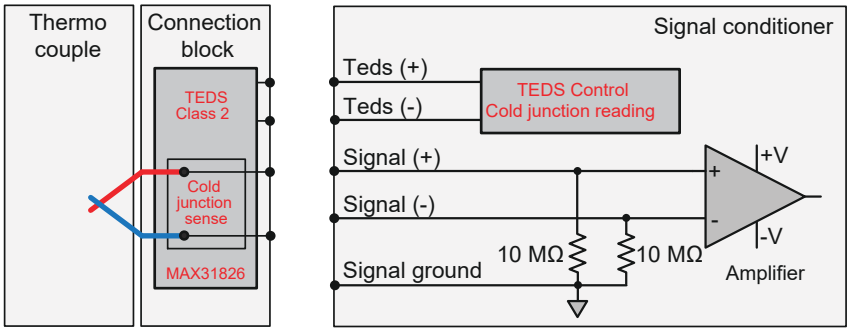


Figure 12.82: Thermocouple mode block diagram

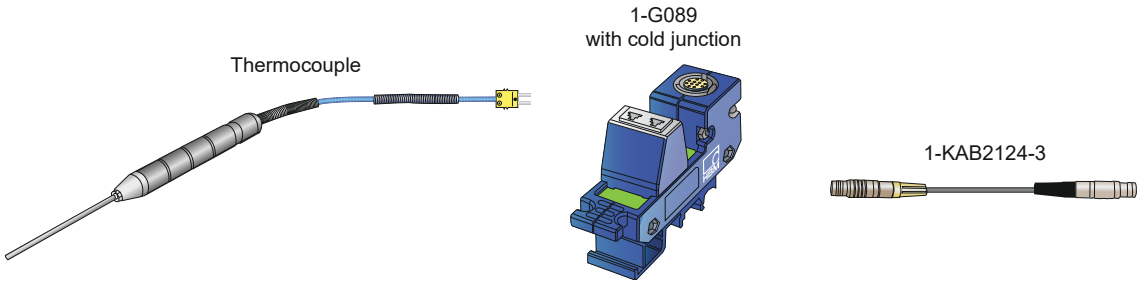


Figure 12.83: Recommended thermocouple tools

12.6.11 DIN rail breakout

HINT/TIP

For quick connect and reconnect din rail breakouts are available.

Three different models exist:

1 Generic breakout G088

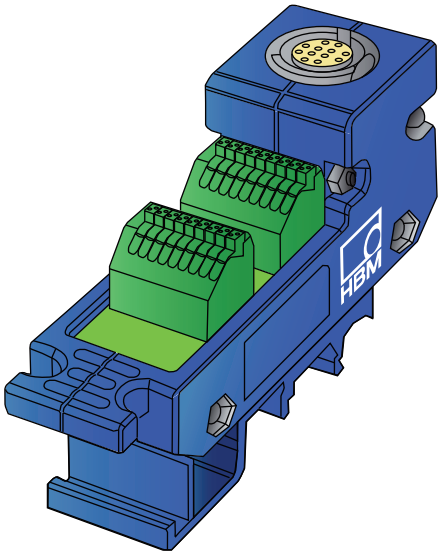


Figure 12.84: DIN rail mountable breakout block (1-G088-02)

The G088 supports spring/push-in connectors for all wire connection to/ from the GN840B/GN1640B card. It is especially suited to support Bridge/ Basic sensor/RTD/Current loop sensors.

The breakout supports wire connections for TEDS class 2 and 3.

2 Thermocouple breakout G089

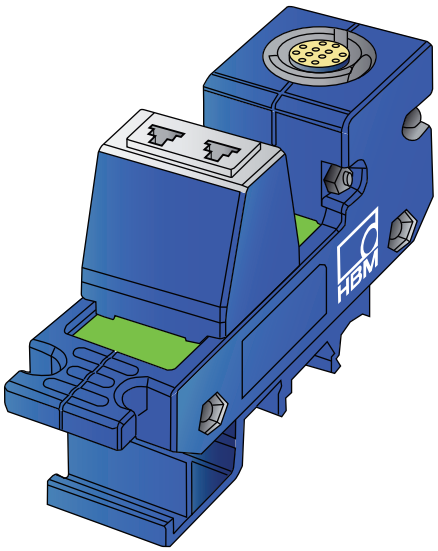


Figure 12.85: DIN rail mountable breakout block (1-G089-02)

The G089 is specifically designed to support thermocouple input connections to/from the GN840B/GN1640B card. The built-in digital cold junction sensor is used by the GN840B/GN1640B card to compensate the thermal errors caused by the sensor to measurement junction.

The breakout supports a flash memory to enable TEDS information to be written into the breakout. Using TEDS, the breakout can be made uniquely recognizable by the controlling software, avoiding hours of system setups.

3 Basic/IEPE/piezoelectric breakout terminal G090

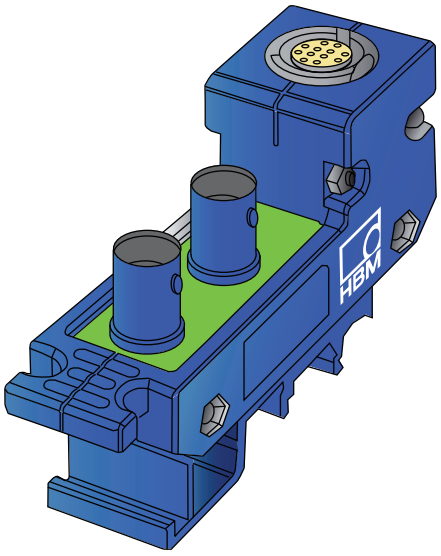


Figure 12.86: DIN rail mountable breakout block (1-G090-02)

The G090 is specifically designed to support BNC input connections to/from the GN840B/GN1640B card. The breakout supports two isolated metal BNCs to allow full differential input wiring.

In basic voltage mode the software allows the selection of differential or single-ended input only.

In IEPE and piezoelectric mode the input is automatically selected as single-ended.

The breakout supports a flash memory to enable TEDS information to be written into the breakout . Using TEDS, the breakout can be made uniquely recognizable by the controlling software, avoiding hours of system setups.

12.6.12 Flexible wiring

HINT/TIP

Using the different terminals, cables and other existing support material a flexible wiring setup can be created to match almost any wish list.

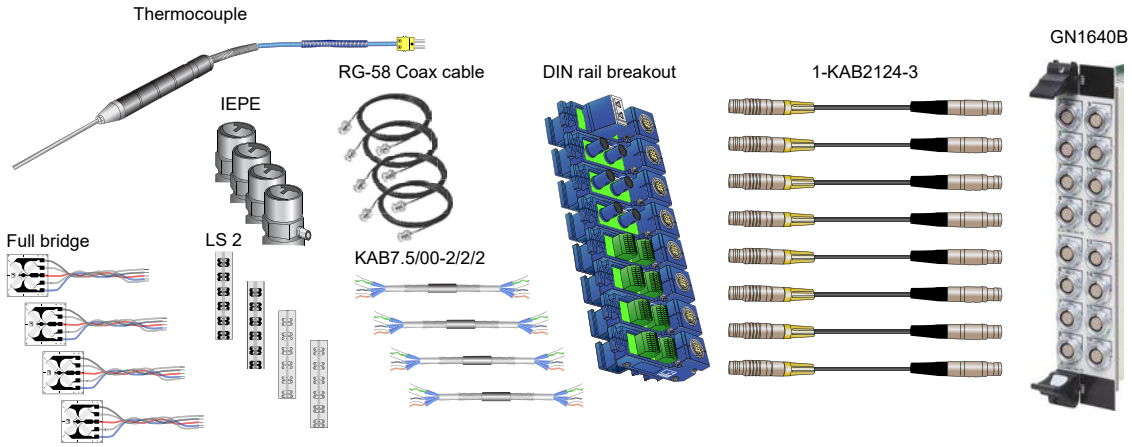


Figure 12.87: Flexible wire diagram (bridge probe)

Contact custom systems at: customsystems@hbm.com for more options and or support on your wiring requests.

12.7 Optical fiber isolated input card

12.7.1 GN1202B, Optical fiber isolated 100 MS/s input card

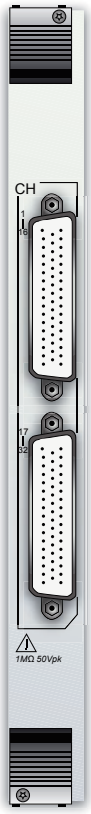
- **12 transmitters per receiver card**
- **Digital fiber optic connection, noise/error and drift free**
- **Cable length up to 1000 m**
- **Automatic cable length phase compensation**
- **Battery powered transmitter**
- **Continuous powered transmitter with 1.8 kV RMS isolation**
- **± 20 mV to ± 100 V input ranges**
- **Analog/digital anti-alias filters**
- **Calibration values stored in transmitter**
- **25 MS/s** or **100 MS/s transmitter**
- **15 or 14 bit resolution**
- **Real-time formula database calculators**
- **Triggering on real-time results**
- **Digital Event/Timer/Counter support**

The optical fiber isolated system consists of up to 12 transmitter units connected to the GN1202B receiver card built into a GEN series mainframe using a fiber optic cable.
By converting the analog signal into a digital signal and transmitting the signal to the receiver card via fiber optic cable, the transmission does not add any drift or error to the measured signal. The automatic cable length compensation phase-matches all fiber optic isolated channels to any standard analog input channel.
The GN112 and GN113 transmitters offer continuous powered isolation at 1.8 kV RMS, while the GN110 and GN111 transmitters offer higher isolation options using battery power with a continuous operation time of 30 hours.
Superior, best in class anti-alias protection is achieved by a unique, multi stage approach. The first stage combination of a 6-pole analog anti-alias filter combined with the Analog-to-Digital converter creates an alias free digital data stream at constant rate of 100 MS/s.
The second stage feeds the 100 MS/s data stream into a user selectable digital filter, to reduce the signal to the desired maximum bandwidth. The digital filter supports 8 orders Bessel or Butterworth filter characteristics.
The third stage decimates the 100 MS/s filtered signal to the desired sample rate.
The digital filter before decimation guarantees a superior phase match, ultra-low noise and alias free result.

The real-time formula database calculators offer math routines to solve almost any real-time mathematical challenge. Dynamic digital cycle detection enables real-time storage as well as 1 µs latency digital output of calculation results like True-RMS on all analog, torque, angle, speed and Timer/Counter channels. Channel to channel math creates computed channels with 1 µs latency obtaining mechanical power and/or multiphase (not limited to three) electric power (P, Q, S) or even efficiency calculations. Real-time calculated results can be used to trigger the recording or signal alarms to the external world.
For specification and ordering information, please refer to the GN1202B data sheet.

12.8 High resolution IEPE and Charge input cards

12.8.1 GN3210 IEPE and charge 250 kS/s input card



- **Charge transducer support**
- **IEPE transducer support**
- **TEDS class 1 support for IEPE**
- **32 analog channels**
- **Balanced differential inputs**
- **± 10 mV to ± 20 V input range**
- **Analog/digital anti-alias filters**
- **Digital Elliptic bandpass filters**
- **250 kS/s sample rate**
- **24 bit resolution**
- **Real-time cycle based calculators with triggering on calculated result**
- **Digital Event/Timer/Counter support**
- **Up to ± 10 kV input range using passive probe (option)**
- **Up to ± 1.2 kA input range using current clamp (option)**

In differential mode, the card can be used in electrically noisy environments. The CMRR of the true differential amplifiers ensures high signal fidelity.
When using the passive voltage probe and/or the current clamp options, the card can be used as an entry-level electrical-input amplifier to measure high voltages and currents.
In single-ended mode, the card can serve as a cost effective input for preconditioned signals to be recorded with the GEN DAQ series of products.
In IEPE mode the card supports open and shorted wire detection and TEDS sensor setup, with excellent price/performance ratio for an array of IEPE based sensors (accelerometers, microphones, etc.).
The high dynamic range of the amplifier and the 24 bit A/D converter as well as the excellent band-pass flatness up to a 100 kHz bandwidth ensure phase alignment and accurate amplitude measurements.
In charge mode, the card can be used directly with charge type sensors, such as piezoelectric accelerometers or pressure transducers.
Superior, best in class anti-alias protection is achieved by a unique, multi stage approach. The first stage the Sigma Delta converter with built-in anti-aliasing filter creates an alias free digital data stream at constant rate of 250 kS/s.
The second stage feeds the 250 kS/s data stream into a user selectable digital filter, to reduce the signal to the desired maximum bandwidth. The digital filter supports both 11 or 12 orders as well as Bessel/Butterworth or Elliptic filter characteristics.
The third stage decimates the 250 kS/s filtered signal to the desired sample rate.

The digital filter before decimation guarantees a superior phase match, ultra-low noise and alias free result.
For specification and ordering information, please refer to the GN3210 data sheet.

12.8.2 GN3211 basic 20 kS/s input card

- **32 analog channels**
- **Balanced differential inputs**
- **± 10 mV to ± 20 V input range**
- **Analog/digital anti-alias filters**
- **20 kS/s sample rate**
- **16 bit resolution**
- **Real-time cycle based calculators with triggering on calculated result**
- **Digital Event support**
- **Up to ± 10 kV input range using passive probe (option)**
- **Up to ± 1.2 kA input range using current clamp (option)**

In differential mode, the card can be used in electrically noisy environments. The CMRR of the true differential amplifiers ensures high signal fidelity.
When using the passive voltage probe and/or the current clamp options, the card can be used as an entry-level electrical-input amplifier to measure high voltages and currents.
Calibrating the probes and clamps with the channels and storing calibration results in the Perception Sensor Database can increase the accuracy well above the accuracy rating of the probe or clamp.
In single-ended mode, the data acquisition card can serve as a cost effective input for preconditioned signals to be recorded with the GEN DAQ series of products.
Superior, best in class anti-alias protection is achieved by a unique, multi stage approach. The first stage the Sigma Delta converter with built-in anti-aliasing filter creates an alias free digital data stream at constant rate of 250 kS/s.
The second stage feeds the 250 kS/s data stream into a user selectable digital filter, to reduce the signal to the desired maximum bandwidth. The digital filter supports both 11 or 12 orders as well as Bessel/Butterworth or Elliptic filter characteristics.
The third stage decimates the 250 kS/s filtered signal to the desired sample rate.
The digital filter before decimation guarantees a superior phase match, ultra-low noise and alias free result.

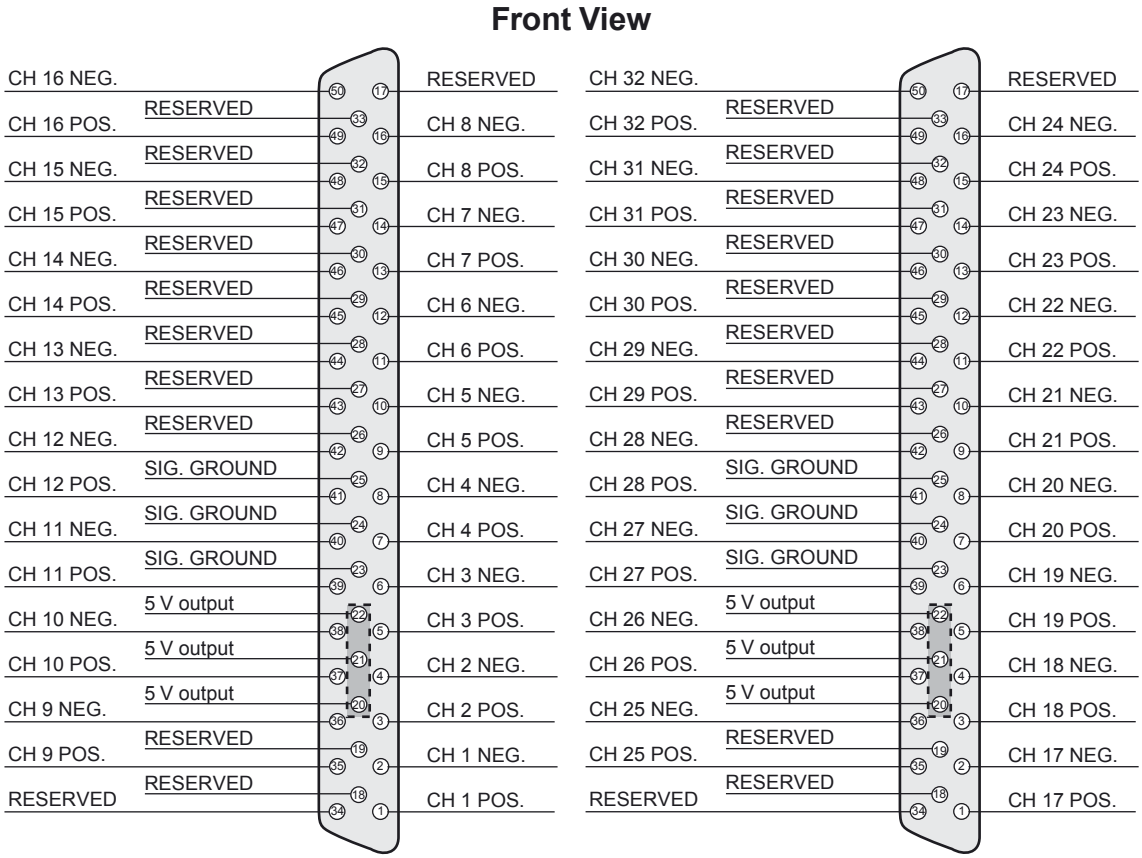


Figure 12.88: Pin diagram for top 16 channel connector (left), Bottom 16 channel connector (right)

Note *Both positive and negative pins must be connected to avoid erroneous measurement results with noise.*

Note *There are three output pins available on each connector. Each pin's output voltage is 5 V. The maximum current for each pins is 0.1 A. When connecting all three pins 0.3 A can be used.*
Over current protection is add for the maximum 0.3 A using an automatic resettable fuse.

For more information on the 16/32 Channel Basic Card 20 kS/s input card, please refer to the GN3211 data sheet.

13 Option Cards

13.1 Option Carrier Card (OCC)

The option carrier card is used to add all kinds of additional digital interfaces to the outside world. See chapter "Option cards supported" on page 308 for the supported option cards.

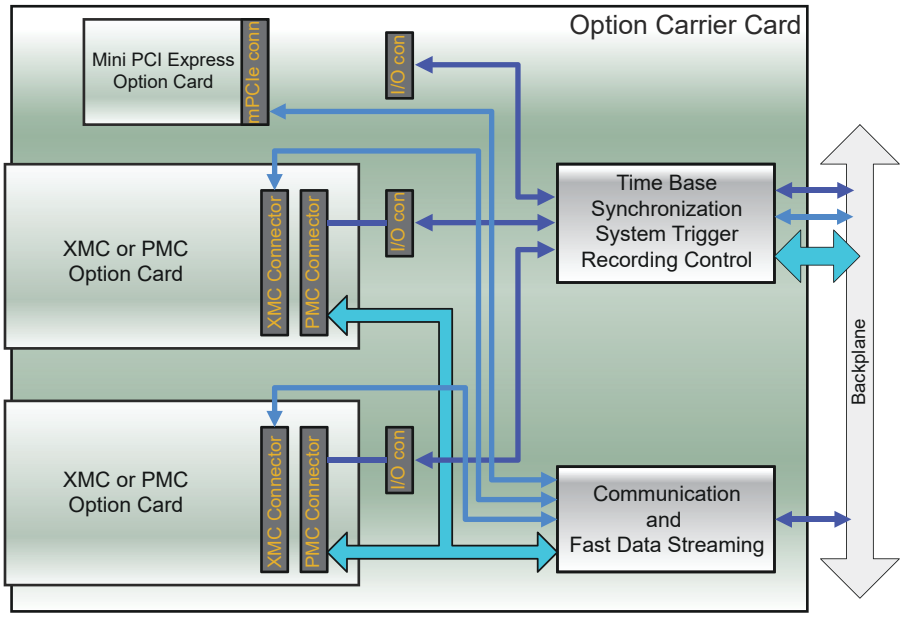


Figure 13.1: Block diagram option carrier card

The OCC supports two XMC/PMC slots and one mini PCI express slot. Each of these form factors are industrial type form factors that are widely used in the industry.

A standard OCC uses one slot of the mainframe. When adding an OCC, it is recommend to start using the last slot of the mainframe first. This preference only exists because of the first slots of each mainframe are attached to the mainframes Digital Event/Timer/Counter connectors. The OCC has no support for these connectors, so it is best to use data acquisition cards in the first slots. The OCC can be used in every slot of the mainframe. To enable the use of a mainframe at least one acquisition card needs to be installed.

13.1.1 Option cards supported

At release of this manual the following option cards are supported:

Part number	Function
G064	10 Gbit Ethernet card, optical
G082	EtherCAT®
G083	Master Output Card (Synchronize Sync mainframes)
G084	10 Gbit Ethernet card, electrical

See GEN17tA data sheet for detailed usage and specification of the option carrier card and all of the option cards supported.

14 GEN series Synchronization Methods

14.1 GEN series synchronization methods compared

GEN series systems support four different synchronization methods. Each method has its own advantages and disadvantages. It is mostly the customer's application use that determines the correct choice.

Synchronization overview				
	Master/ Sync(1)	**PTP(2)**	**GPS(3)**	**IRIG(4)**
Signal Phase	Very good	Very good	Good	Average/Good
Trigger(s) / Sweep(s)	Very good	Average and extra cabling required	Average and extra cabling required	Average and extra cabling required
Absolute time of day	When combined with PTP	When using a synchronized Grandmaster	Always	When using a synchronized IRIG source
Start of recording	Very good	Average	Average	Average
Stop of recording	Average	Average	Average	Average

(1) G081 + G083 options

(2) Standard option

(3) G002B option

(4) G001B option

As the GEN series systems support several recording modes, the impact of each of these choices needs to be considered with respect to the recording mode.

14.1.1 Signal phase shift synchronization

Since typical GEN series applications use sample rates ranging from 10 kS/s to 250 MS/s, channel to channel phase match is the vital system characteristic.

Channel to channel phase shift is defined as the phase/time differences measured between two channels recording the exact same signal. Phase shifts should therefore not be measured by comparing the first or last samples of a recording or sweep. Measuring phase shift should compare a single signal recorded by mulitple mainframes and then establish the exact time difference of the different signals when shown within Perception.

A quick and easy verification method uses a square wave and compares the rising edge of the square wave. Make sure to use a square wave signal with a time period that is longer than the expected phase match. This avoids larger phase errors being missed, as the different subsequent rising edges cannot be separated from each other. For example, a square wave of 100 kHz (10 µs period time) and a phase shift of 10 µs would show a 100% synchronized trace. Lowering the square wave frequency to 10 kHz would suddenly show the 10 µs phase error. When in doubt, lower the frequency and measure again.

HINT/TIP

As a square wave has an instantaneous transition by definition, it is not possible to establish phase shifts smaller than a single sample period. A complex but more accurate phase shift measurement uses a sine wave with a period time that is ten times lower than the specified phase shift. Using a computed best fit sine wave on both signals allows for the extraction of the sine waves phase at point X of each trace. The difference between each calculated sine wave's phase is the phase shift between channels.

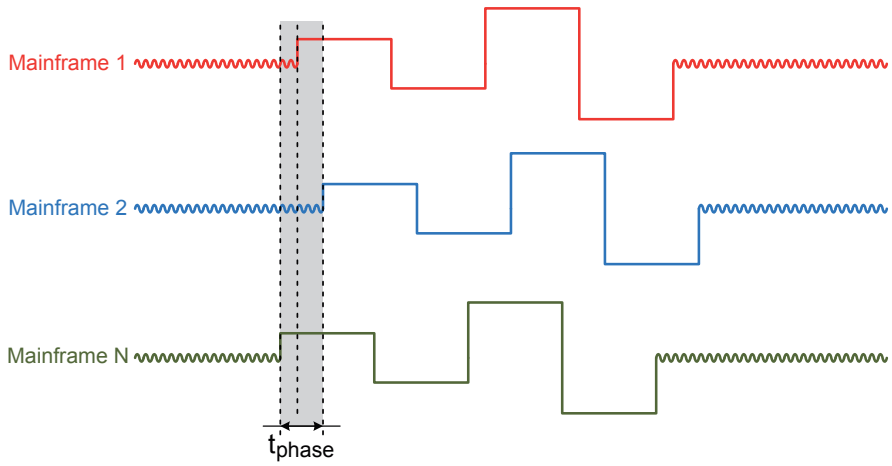


Figure 14.1: Determining phase shift

HINT/TIP

Master/Sync and PTP are typically the best choices for phase synchronizing multiple GEN series systems. PTP does not support trigger exchange and should therefore typically be used when using the continuous recording user mode within Perception.

14.1.2 Trigger synchronization

When in Single sweep, Multiple sweep, Slow-Fast Sweep or dual rate mode, the second most important synchronization, after the channel to channel phase match, is the trigger exchange. As sweeps are always initiated by a trigger, the trigger point within each mainframe defines the start and end of the sweep period.

It is important to know that sweeps are shown with the trigger aligned at t_0. The net effect is that triggers received with a time delay are actually time shifted in the software, as if these triggers had happened 100% synchronous in time. If triggers are not 100% synchronous in all systems, signal phase shifts are introduced by this effect.

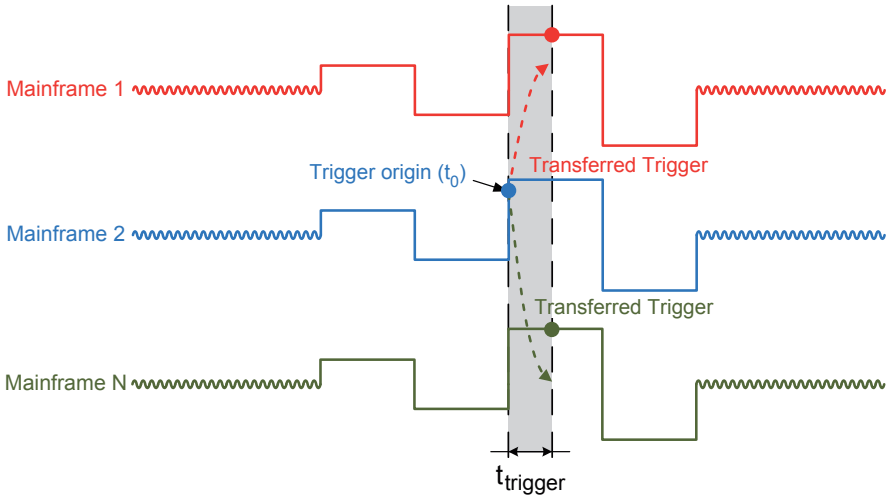


Figure 14.2: Triggering due to trigger transfer delays

The measured signals above appear within Perception as follows:

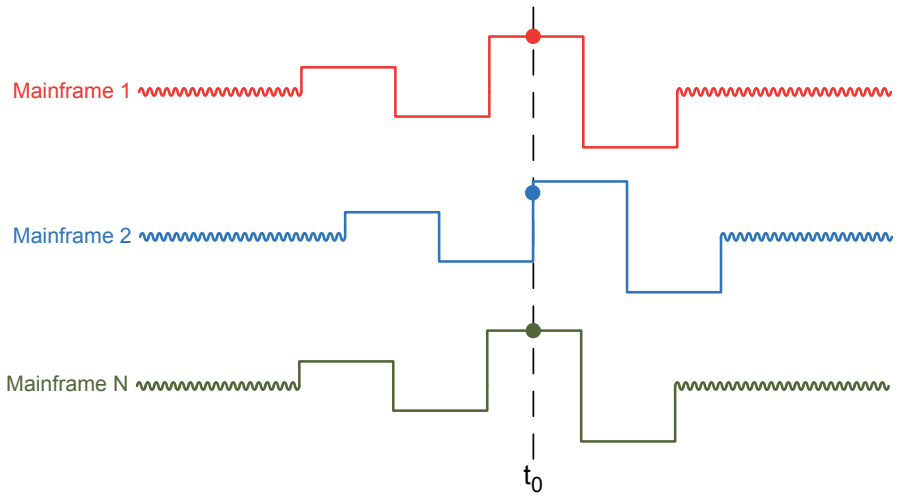


Figure 14.3: Signal phase shift introduced by t_0 alignment caused by trigger transfer delays

14.1.3 Absolute time of day synchronization

The relevancy of this synchronization is a pure user application requirement. GEN series systems are synchronized to the controlling PC when Perception makes the first connection to the mainframe. If the PC is connected to the internet or an intranet, the NTP process running within the operating system allows the GEN series mainframe to synchronize to approximately one second to the absolute time of day.

In most cases, this time indication meets the generic requirements to trace the time of day that the recording was made.

HINT/TIP

GEN series systems store this time inside the PNRF file and set the file date/time to this same time as well. However, copying files from one storage medium to the next, such as during archiving, might change the file date and time listed. Perception software only uses the date/time stored inside the PNRF recording file. This information is never affected by the adjustment that might occur while transferring the datafile.

If GEN series recorded data needs to be correlated to other (GEN series) systems that are not directly synchronized to the same time source, a more accurate absolute time of day is required to enable data correlation at a later point in time.

HINT/TIP

Whenever a GEN series recording is made using any of the available synchronization methods, the need for absolute time of day synchronization is not required to get a correct signal phase match.

A typical use of absolute time of day synchronization would be two GEN series systems, each at different locations that cannot be connected by wires. Using GPS absolute time synchronization would allow recorded data to be compared, even if these two systems were not connected.

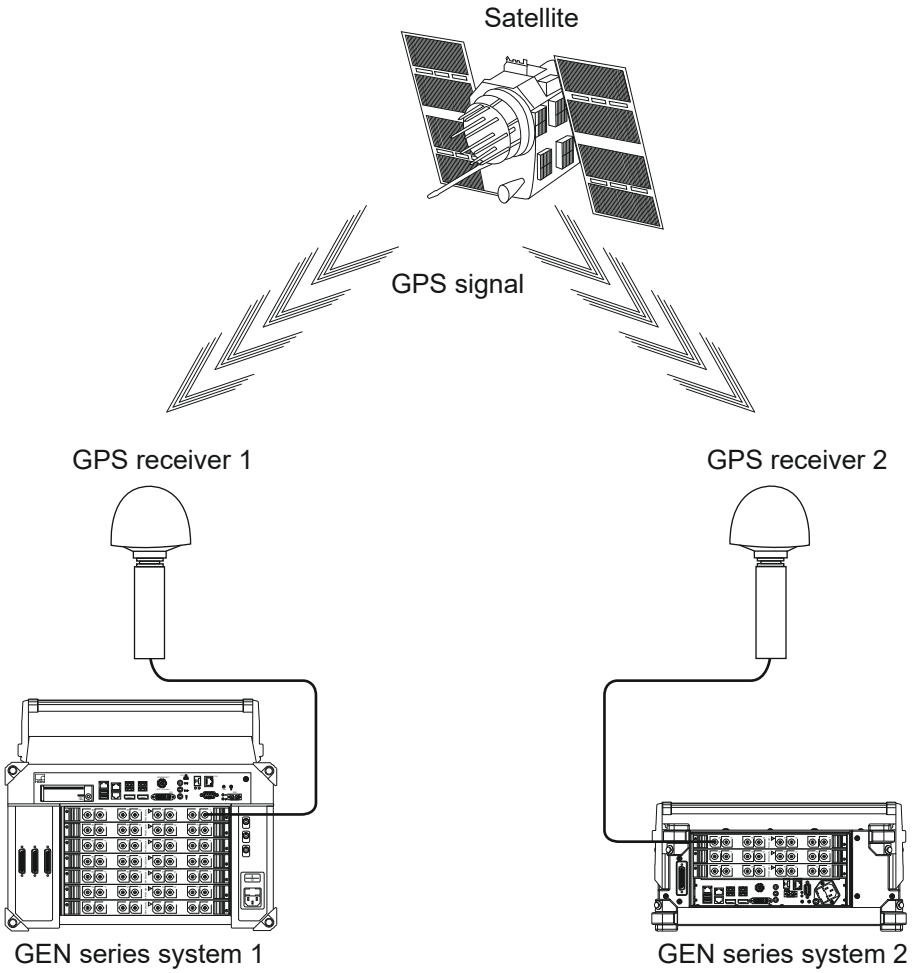


Figure 14.4: Typical GPS absolute time of day setup

14.1.4 Start/Stop synchronization

When using multiple mainframes in continuous mode, expectations are typically that the first sample of each channel aligns. However, depending on how the start and stop actions are synchronized, this might not be the reality. The response time within GEN series systems is not specified, e.g. the time from when the Start button has been pressed to when the mainframe actually captures the first sample. The response time varies and is dependent on a number of parameters, e.g. the number of acquisition cards within the mainframe and the the speed of the Windows® PC. Given this variation in response, a system start should be executed in time to guarantee the recording of all important data.

When in Single sweep, Multiple sweep or Slow-Fast Sweep mode, the start and stop synchronization of the recording is irrelevant. The entire recorded sweep data is determined by the trigger origin with a fixed pre- and post-trigger time frame. In sweep-based recordings, the acquisition system is typically started first. Checks on all system parts are then performed and the first trigger is inserted only when all systems are ready.

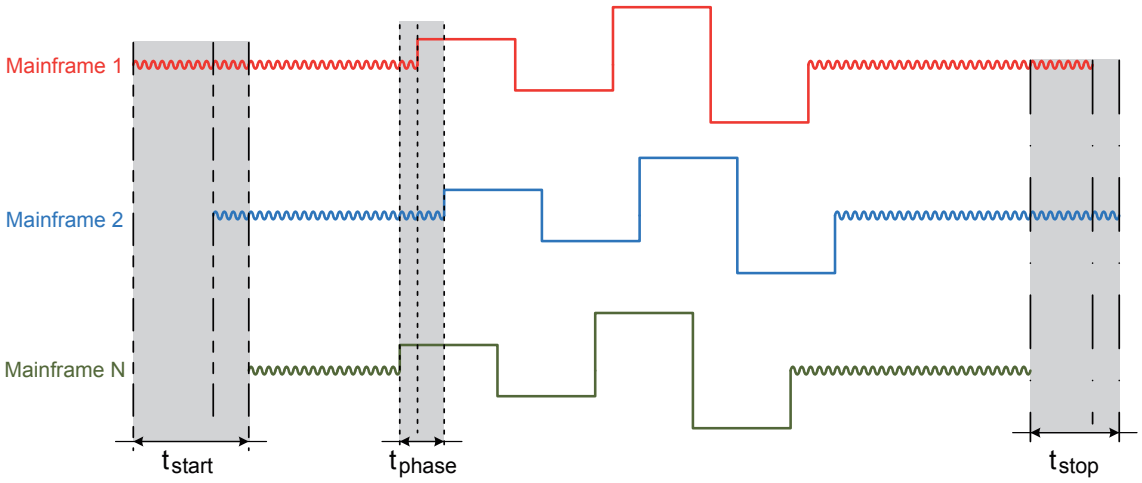


Figure 14.5: Measuring start/stop synchronization accuracy

14.1.5 Synchronization specification overview

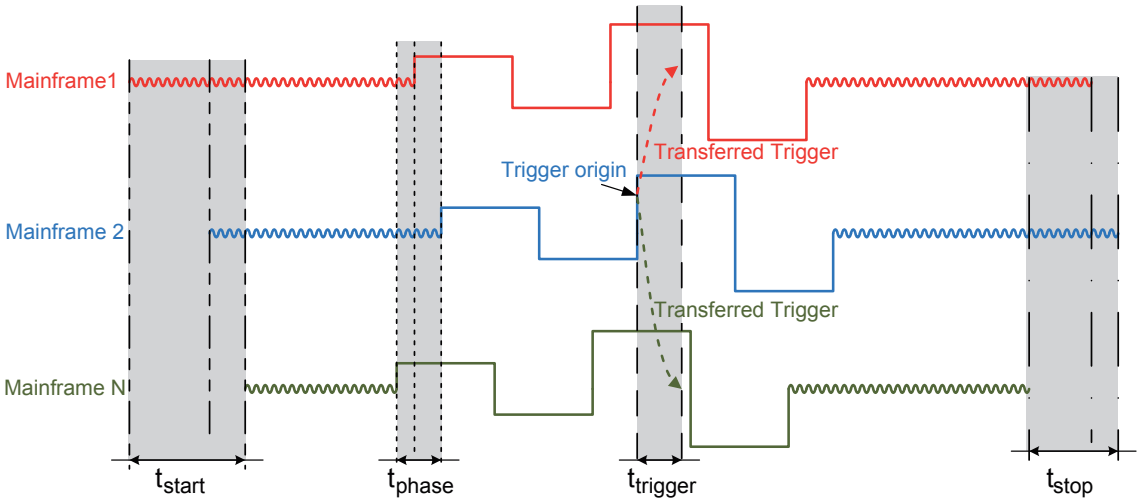


Figure 14.6: Synchronization specification overview

	t_{phase} (1)	t_{start} (2)	t_{stop} (3)	$t_{trigger}$ (4) (5)	**QuantumX Support**
Synchronization source					
Master/ Sync	≤ 150 ns	≤ cable delay	≤ 1 s	≤ 150 ns	Combined using PTP
PTP	≤ 150 ns	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)	Yes
No synchronization source					
Mainframes simultaneous connected by Perception	≤ 1 s	≤ 1 s	≤ 1 s	≤ 1 s	--
Additional error after connection	≤ 0.5 s/hour	≤ 0.5 s/hour	≤ 0.5 s/hour	≤ 0.5 s/hour	--

(1) t_{phase} Maximum phase difference between signals. *(This specification is not affected by any of the other specifications).*

(2) t_{start} Maximum delay between start of recording of each mainframe.

(3) t_{stop} Maximum delay between stop of recording of each mainframe.

(4) $t_{trigger}$ Maximum delay to transfer a trigger from a mainframe to all other mainframes.

(5) **Note** on trigger exchange
Trigger exchange is included in the Master/Sync connection cable. All other synchronization modes require that the mainframes are connected from each External Trigger Out to each External Trigger In on all mainframes in order to exchange triggers.

14.2 PTP

14.2.1 PTP technology background(1)

(1) Source: Wikipedia® the free encyclopedia

The **Precision Time Protocol (PTP)** is a protocol used to synchronize clocks throughout a computer network. On a local area network, it achieves clock accuracy in the sub-microsecond range, making it suitable for measurement and control systems.

PTP was originally defined in the **IEEE 1588-2002** standard, officially entitled *"Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems"* and published in 2002. In 2008, a revised standard, **IEEE 1588-2008** was released. This new version, also known as PTP Version 2, improves accuracy, precision and robustness but is not backwards compatible with the original 2002 version.

Architecture

The IEEE 1588 standards describe a hierarchical master-slave architecture for clock distribution. Under this architecture, a time distribution system consists of one or more types of communication media (network segments) and one or more clocks. An ordinary clock is a device with a single network connection and is either the source (master) of or destination (slave) for a synchronization reference. A boundary clock has multiple network connections and can accurately bridge synchronization from one network segment to another. A synchronization master is selected for each of the network segments in the system. The root timing reference is called the grandmaster. The grandmaster transmits synchronization information to the clocks residing on its network segment.

The boundary clocks with a presence on that segment then relay accurate time to the other segments to which they are also connected.

A simplified PTP system frequently consists of ordinary clocks connected to a single network. No boundary clocks are used. A grandmaster is elected and all other clocks synchronize directly to it. IEEE 1588-2008 introduces a clock associated with network equipment used to convey PTP messages. The transparent clock modifies PTP messages as they pass through the device. Timestamps in the messages are corrected for time spent traversing the network equipment. This scheme improves distribution accuracy by compensating for delivery variability across the network.

14.2.2 PTP Protocol details

Synchronization and management of a PTP system is achieved through the exchange of messages across the communications medium. To this end, PTP uses the following message types.

- **Sync, Delay_Req, Follow_Up** and **Delay_Resp** messages are used by ordinary and boundary clocks and communicate time-related information used to synchronize clocks across the network.
- **Pdelay_Req, Pdelay_Resp** and **Pdelay_Resp_Follow_Up** are used by transparent clocks to measure delays across the communications medium so that they can be compensated for by the system. Transparent clocks and these messages associated with them are not available in IEEE 1588-2002.
- **Announce** messages are used by the best master clock algorithm in IEEE 1588-2008 to build a clock hierarchy and to select the grandmaster.
- **Management** messages are used by network management to monitor, configure and maintain a PTP system.
- **Signaling** messages are used for non-time-critical communications between clocks. Signaling messages were introduced in IEEE 1588-2008.

Messages are categorized as **Event** and **General** messages. Event messages are time-critical in that accuracy in transmission and receipt timestamp accuracy directly affects clock distribution accuracy.

Event messages:

- Sync
- Delay_Req
- Pdelay_Req
- Pdelay_resp

General messages :

- Announce
- Follow_Up
- Delay_Resp
- Pdelay_Resp_Follow_Up

General messages are more conventional protocol data units in that the data in these messages is of importance to PTP, but their transmission and receipt timestamps are not.

Management and **Signaling** messages are members of the **General** message class.

14.2.3 Best master clock algorithm (BMC)

The **best master clock** (BMC) algorithm performs a distributed selection of the best candidate clock based on the following clock properties:

- **Identifier**
  A universally unique numeric identifier for the clock. This is typically constructed based on a device's MAC address.
- **Quality**
  Both versions of IEEE 1588 attempt to quantify clock quality based on expected timing deviation, technology used to implement the clock or location in a stratum schema, although only V1 knows a data field stratum. PTPv2 defines the overall quality of a clock by using the data fields clockAccuracy and clockClass.
- **Priority**
  An administratively assigned precedence hint used by the BMC to help select a grandmaster for the PTP domain. IEEE 1588-2002 used a single boolean variable to indicate precedence. IEEE 1588-2008 features two 8 bit priority fields.
- **Variance**
  A clock's estimate of its stability based on observation of its performance against the PTP reference.

IEEE 1588-2008 uses a hierarchical selection algorithm based on the following properties, in the indicated order:

1 Priority 1
2 Class
3 Accuracy
4 Variance
5 Priority 2
6 Unique identifier (tie breaker)

(1) “PTP technology background”, “PTP Protocol details” and “Best master clock algorithm”: Source: Wikipedia® the free encyclopedia

HBM systems use the following details for BMC:

	GEN3i/GEN3iA/GEN7i/ GEN7iA GEN2tB/GEN4tB/ GEN7tA/GEN17tA	**QuantumX (B hardware)**
Priority 1	128	128
Class	248	248
Accuracy	FE	FE
Variance	FFFF	FFFF
Priority 2	122	128

When using any of the HBM systems listed in this table, the systems in the leftmost column are granted Master rights based on the BMC algorithm. Adjustments to synchronize to an external clock result in small deviations of the sample period. Technically speaking, this could be seen as jitter on the ADC clock. Depending on the jitter value, this results in noise, especially during frequency domain evaluations (FFT).
If sample rates are higher, the small corrections are relatively large compared to the same adjustment to sample rates that are 100 times lower. Therefore, the faster sampling systems are prioritized within the HBM range to become clock master.

HINT/TIP

For each field, the smallest value will wins. For example, if Priority 1 for System A is smaller when compared to System B, all the other fields are no longer monitored/analyzed, as the weight of the first field outweighs all other fields.

14.2.4 PTP switch types

Within the PTP specification, two types of switches are defined:

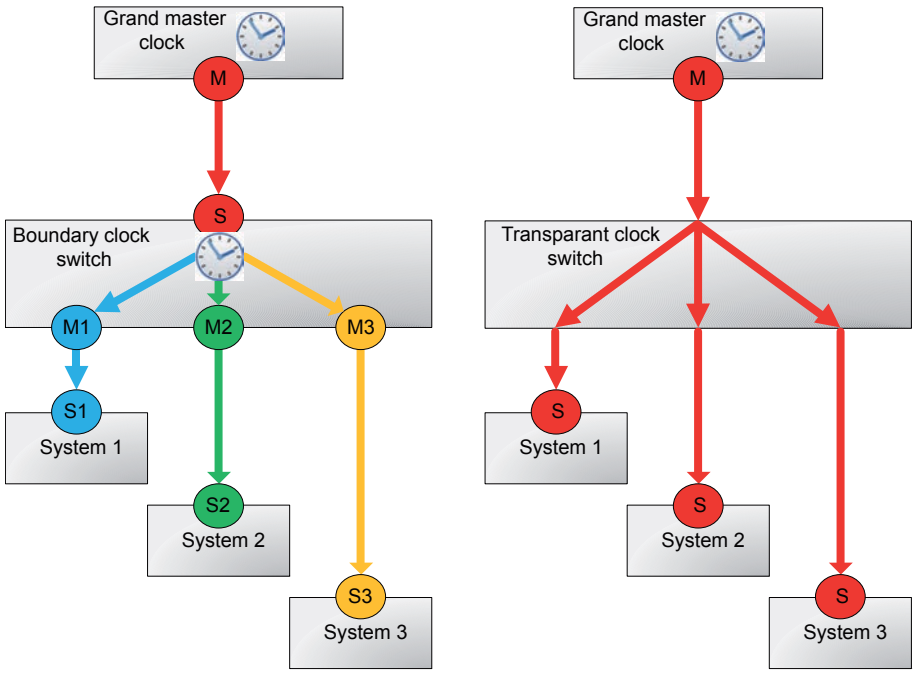
- Boundary clock switches
- Transparent clock switches

Boundary clock

Boundary clocks are defined within a PTP system to be integrated in place where standard network switches or routers are used. Boundary clocks are defined as PTP clocks with more than a single PTP port, with each port providing access to a separate PTP communication path. The boundary clock acts as an interface between separate PTP domains intercepting and processing all PTP messages and passing all other network traffic. The BMC algorithm is used by the boundary clock to select the best clock any port can see. The chosen port (the one that receives the best clock) is set as a slave and all other ports of the boundary clock are asserted as masters to their domain (to forward the clock).

Transparent clock

Transparent clocks have been added to Version 2 of the standard as an improved method of forming cascaded topologies. Rather than acting as a multi-port ordinary clock as boundary clocks do, transparent clocks update a newly introduced time-interval field within PTP event messages. This 64 bit time-interval correction field allows for switch delay compensation to a potential accuracy of less than a picosecond. There are two types of transparent clocks, End-to-End and Peer-to-Peer. End-to-End transparent clocks update the time interval field for the delay associated with individual packet transfers, whereas Peer-to-Peer transparent clocks measure the line delay associated with the ingress transmission path and include this delay in the correction field also. Peer-to-Peer transparent clocks can allow for faster reconfiguration after network topology changes.



Boundary clock operation

Transparent clock operation

Figure 14.7: Boundary clock versus transparent clock switch synchronization mode

Switches using boundary clocks

Switches using boundary clocks have a built-in clock and they create separate synchronization domains by segmenting the synchronization path from the master clock to several slave clocks. As a result, systems downstream of a boundary clock do not communicate PTP messages with the selected (grand) master directly. Standard Ethernet messages are passed through the switch while synchronization messages are used to synchronize the boundary slave clock.

HINT/TIP

As boundary clock switches create their own internal clock, the overall stability and/or accuracy of the grandmaster clock is no longer available for any of the attached systems.

Switches using transparent clocks
Switches using transparent clocks forward the master clock synchronization message to every port of the switch. The time required to transfer the message from the incoming port to the outgoing port must be measured and transferred together with the original synchronization message. There are two methods used to communicate the internal delay information to the original synchronization messages:

- End-to-End
- Peer-to-Peer

Each of these two methods has its advantages and disadvantages.

End-to-End transparent clocks
End-to-End transparent clocks create a higher load on the master clock, as the master “sees” all the slaves. End-to-End transparent clocks support a 1:N topology with one master communicating with a large number of slaves. They are, however, good for linear systems with a number of daisy-chained clocks.

Peer-to-Peer transparent clocks
Peer-to-Peer clocks avoid the higher master load, but introduce the need to be aware of how the synchronization messages are routed through the network topology. They cannot resolve 1:N topologies, as they cannot determine which line delay is being calculated and they must also maintain path delay measurements.

One-Step and Two-Step clock synchronization
PTP allows for two different types of time stamping methods:

- **One-Step** clock synchronization
  One-Step clocks update time information by adjusting the time information within the original synchronization messages (sync and delay request) on-the-fly.
- **Two-Step** clock synchronization
  Two-Step clocks transmit the precise timestamps of packets using additional general messages (follow-up and delay response).

A One-Step End-to-End transparent clock updates for switch delay in sync and delay request messages as they pass through the switch while a Two-Step transparent clock updates a field in the non-time-critical general message.

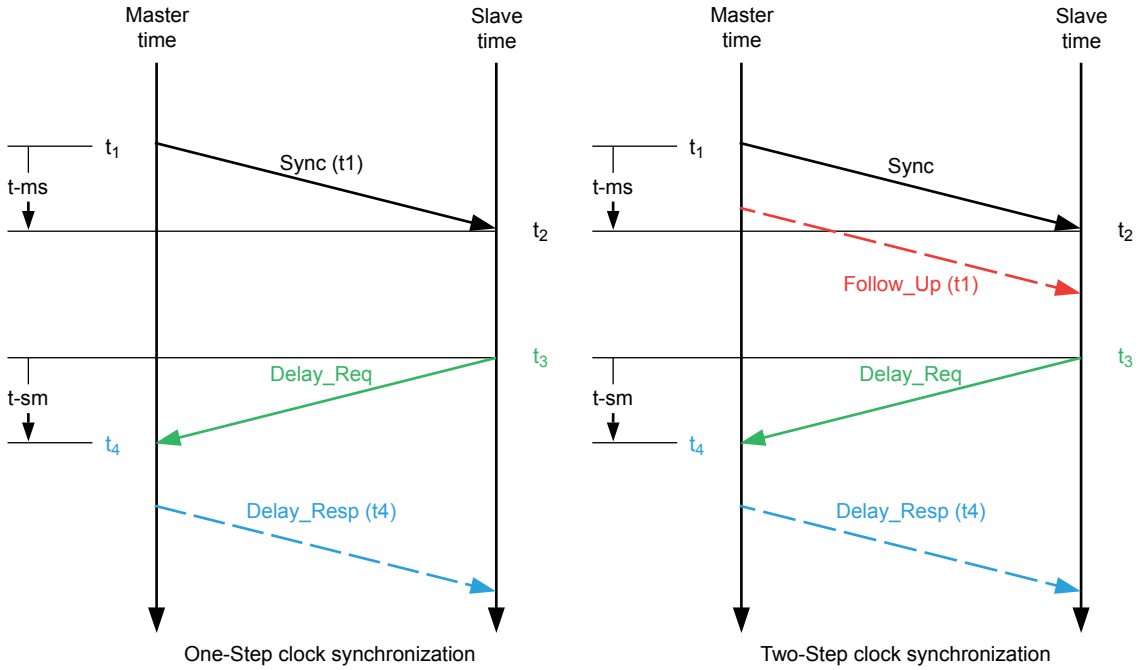


Figure 14.8: One-Step versus Two-Step clock synchronization

HBM systems are designed to work with End-to-End Two-Step PTP protocol only. Switches that do not support the End-to-End Two-Step PTP protocol are not tested or supported by HBM.

14.2.5 Transparent clock switch synchronization

The operation of PTP relies on a measurement of the communication path delay between the time source, referred to as a master, and the receiver, referred to as a slave. This process involves a message transaction between the master and slave where the precise moments of transmit and receive are measured - preferably at the hardware level. Messages containing current time information are adjusted to account for their path delay, therefore providing a more accurate representation of the time information conveyed. The path delay measurement process of PTP involves the precision timing of two messages - a sync message and a delay request. The average path delay of the two messages gives the one-way delay. This, however, assumes that the communication path is completely symmetric. This assumption does not hold in a switched network, however, largely due to the buffering process within Ethernet switches. PTP allows transparent clocks to measure and account for this delay in a time-interval field within timing packets, thus making the switches temporary transparent to master and slave nodes. Transparent clocks must perform this operation very accurately and at the communication speed without introducing more delays. The End-to-End transparent clock forwards all messages just as a normal switch does.

Message-based synchronization

PTP is based upon the transfer of network datagrams to determine system properties and to convey time information. A delay measurement principle is used to determine path delay, which is then accounted for in the adjustment of local clocks. At start-up, a master/slave hierarchy is created using what is called the Best Master Clock (BMC) algorithm to determine which clock has the best source of time. The BMC algorithm is then run continuously to quickly adjust for changes in network configuration. Synchronization is achieved using a series of message transactions between master and slaves. There are five message types - Sync, Delay Request, Follow Up, Delay Response and Management - which are used for all aspects of the protocol. A sequence of message transactions takes place to synchronize a pair of clocks as shown in Figure 14.9.

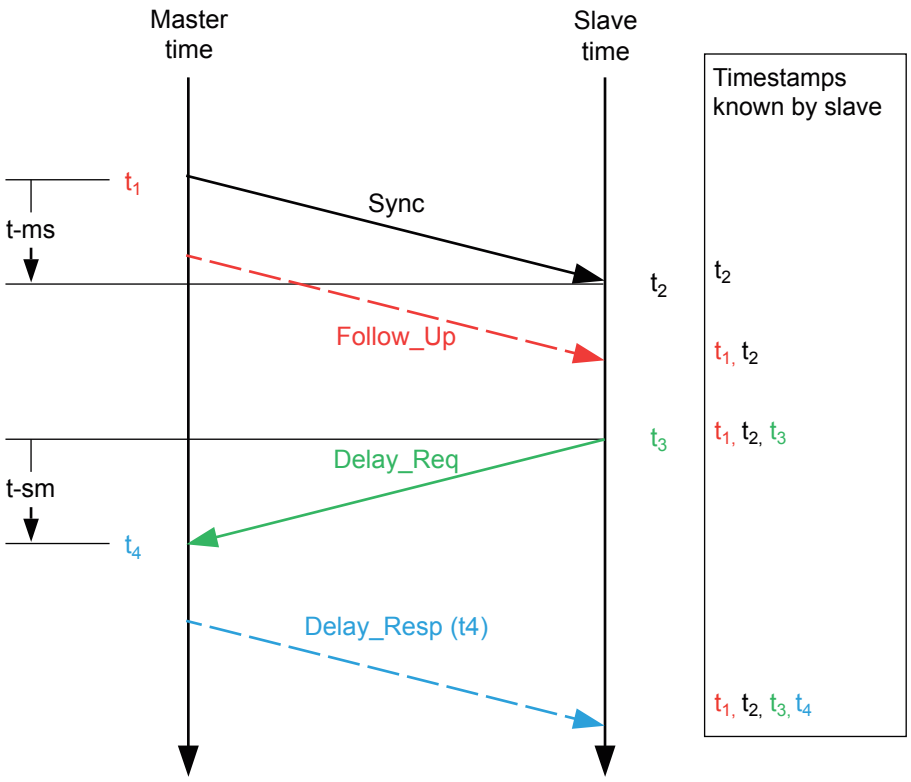


Figure 14.9: Master/Slave offset measurement

The message exchange process is as follows:

1. The master sends a **Sync** message to the slave and notes the time, $\mathbf{t_1}$, at which it was sent.
2. The slave receives the **Sync** message and notes the time of reception, $\mathbf{t_2}$.
3. The master conveys the **timestamp $\mathbf{t_1}$** to the slave the by either
   - **a** Embedding the **timestamp $\mathbf{t_1}$** in the **Sync** message (One-Step). This requires some sort of hardware processing for highest accuracy and precision

     or
   - **b** Embedding the **timestamp $\mathbf{t_1}$** in a **Follow_Up** message (Two-Step).
4. The slave sends a **Delay_Req** message to the master and notes the time, $\mathbf{t_3}$, at which it was sent.
5. The master receives the **Delay_Req** message and notes the time of reception, $\mathbf{t_4}$.
6. The master conveys the **timestamp $\mathbf{t_4}$** to the slave the by embedding it in a **Delay_Resp** message.

After this message exchange, the slave has four timestamps from which both the slave offset (time offset by which the slave clock leads or lags the master) and the network delay (the time taken for packets to traverse the network link between the two nodes) can be determined.

The link delay can be calculated as follows:

$$\text{MasterSlave}_{\text{delay}} = t_{ms} = t_2 - t_1$$

$$\text{SlaveMaster}_{\text{delay}} = t_{sm} = t_4 - t_3$$

In each case, the time differences refer to times taken from different clocks which may be offset from each other. However, if the assumption is made that the delay in one direction is the same as the delay in the opposite direction, then the two equations can be combined as follows:

$$\text{Delay} = \frac{(t_2 - t_1) + (t_4 - t_3)}{2}$$

From Figure 14.9, it can be seen that the slave clock offset (the time interval by which the slave leads the master) is given by:

$$\text{Offset} = t_2 - (t_1 + Delay)$$

Substituting from Figure 14.9 above:

$$\text{Offset} = t_2 - (t_1 + ½\,[(t_2 - t_1) + (t_4 - t_3)])$$

rearranging results in:

$$\begin{aligned}\text{Offset} &= t_2 - t_1 - ½t_2 + ½t_1 - ½t_4 + ½t_3 \\ &= ½(2 \times t_2 - 2 \times t_1 - t_2 + t_1 - t_4 + t_3) \\ &= \frac{(t_2 - t_1) - (t_4 - t_3)}{2}\end{aligned}$$

If two sets of Sync and Follow up messages are sent, then the drift between the two clocks (the phase change rate) can be found by comparing the Δtime between the successive sync messages.

$$\text{Drift} = \frac{\Delta time_{slave} - \Delta time_{master}}{\Delta time_{master}}$$

HINT/TIP

Grand masters might have a setting to control the number of synchronization events sent per second time interval. For GEN series system to synchronize to a PTP grandmaster within its published specifications, a minimum of one PTP synchronization per second is required. Two updates per second improves the short-term stability. Higher update rates have not proven to be more stable.

Switch delays

The majority of Ethernet switches on the market use a store-and-forward method to decide where to send individual packets. Incoming packets are stored in local memory. The packet is checked for errors before being sent out from the appropriate port/ports. This process introduces variations in the forward and return latency time of the packet. The variations in these delays mean that the assumption that packet delay is the same in each direction is invalid, thus rendering the path delay calculations of PTP inoperable. This issue has been compensated for with the use of two special switches, **boundary clocks** and **transparent clocks**. For more information, please refer to "PTP switch types" on page 321.

14.2.6 Common terms used in IEEE 1588

(source www.nist.gov/el/isd/ieee/terms1588.cfm)

- **Boundary clock:** A boundary clock is a clock with more than a single PTP port, with each PTP port providing access to a separate PTP communication path. Boundary clocks are used to eliminate fluctuations produced by routers and similar network elements.
- **Clock:** A device providing a measurement of the passage of time since a defined epoch. There are two types of clocks in 1588: boundary clocks and ordinary clocks.
- **Direct communication:** The communication of PTP information between two PTP clocks with no intervening boundary clock is termed a direct communication.
- **External synchronization:** It is often desirable to synchronize a single clock to an external source of time, for example to a GPS system to establish a UTC time base. This synchronization is accomplished by means other than those specified by 1588 and is referred to as external synchronization.
- **Grandmaster clock:** Within a collection of 1588 clocks, one clock, the grandmaster clock, serves as the primary source of time to which all others are ultimately synchronized.
- **Master clock:** A system of 1588 clocks may be segmented into regions separated by boundary clocks. Within each region, there is a single clock, the master clock, serving as the primary source of time. These master clocks turn synchronize to other master clocks and ultimately to the grandmaster clock.
- **Ordinary clock:** An ordinary clock is a 1588 clock with a single PTP port.
- **Preferred master clock set:** 1588 allows for the definition of a set of clocks that are favored over those not so designated in the selection of the grandmaster clock.
- **PTP:** PTP is an acronym for **P**recision **T**ime **P**rotocol, the name used in the standard for the protocol.
- **PTP domain:** A PTP domain is a collection of one or more PTP subdomains. A subdomain is a logical grouping of 1588 clocks that synchronize to each other using the PTP protocol, but that are not necessarily synchronized to PTP clocks in another PTP subdomain. Subdomains provide a way of implementing disjoint sets of clocks, sharing a common network, but maintaining independent synchronization within each set.
- **PTP message:** There are five designated messages types defined by 1588: Sync, Delay_Req, Follow-up, Delay_Resp, and Management. Multicast communication: 1588 requires that PTP messages be communicated via a multicast. In this style of communication, any node may post a message and all nodes in the same segment of a subdomain receive this message. Boundary clocks define the segments within a subdomain.

- **Synchronized clocks:** Two clocks are synchronized to a specified uncertainty if they have the same epoch and measurements of any time interval by both clocks differ by no more than the specified uncertainty. The timestamps generated by two synchronized clocks for the same event differ by no more than the specified uncertainty.

14.2.7 PTP and Master/Sync

When using PTP in combination with Master/Sync synchronization, these two synchronization protocols interact. The Master/Sync master synchronizes to the PTP master clock and the Master/Sync Sync mainframes follow their Master/Sync Master.

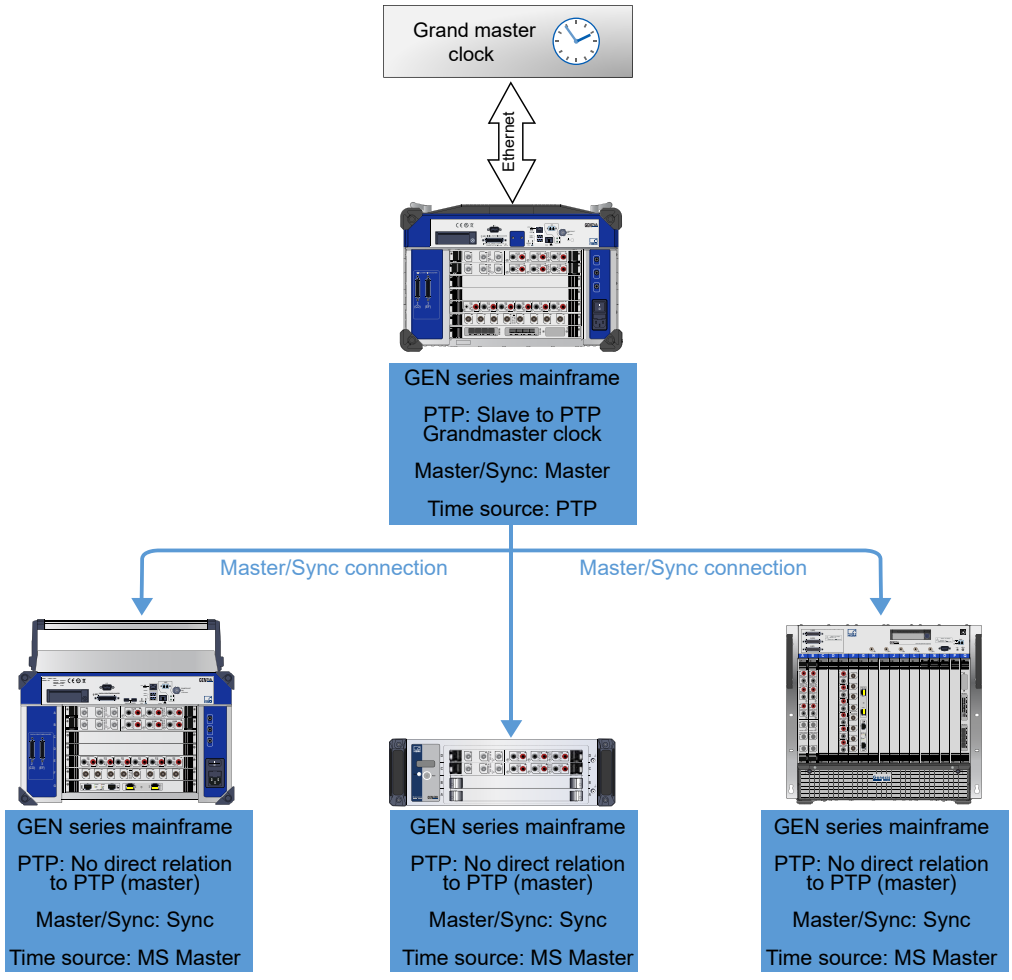


Figure 14.10: Grandmaster clock with Master/Sync connected Sync mainframes

The PTP synchronization process “oscillates” due to a certain control strategy. To align PTP synchronization and Master/Sync synchronization the amount of oscillation in this PTP synchronization process needs to be sufficiently large. In fact, this required oscillation range exceeds the tightest PTP tolerance of 150 ns. Therefore, once a mainframe is set to be a MS Master, the PTP tolerance will be fixed to 1000 ns*.

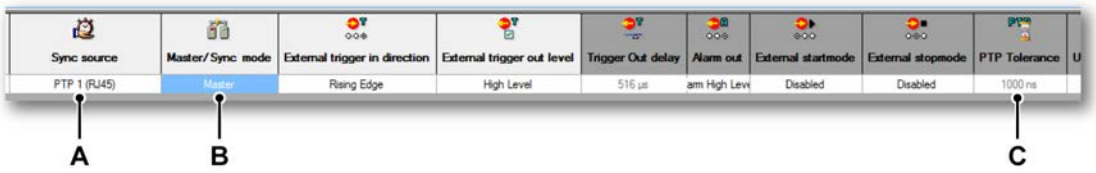


Figure 14.11: Fixed PTP tolerance

A Sync source: PTP (or GPS OTMC 100)

B Master/Sync mode: Master

C PTP Tolerance: fixed 1000 ns

Note ** When selecting IRIG GMR1000 as **Sync source**, this will always fix the **PTP tolerance** to 2000 ns, independent of stand-alone or being MS Master, due to the nature of the IRIG synchronization signal jitter.*

14.3 GPS

14.3.1 Installation

When connecting the GPS antenna to the mainframe, please follow the steps described below.

IMPORTANT

As the GPS antenna is typically placed on a roof or otherwise hard to access position, it is highly recommended to connect the GPS antenna to the PoE injector and plug the injector into mains. Please refer to the LED overview to verify that the GPS antenna is properly powered and optionally connect to the web client to verify the GPS antenna is fully operational.

1 Place the GPS antenna in a position with clear view to the sky. For more information, please refer to chapter "GPS antenna placement" on page 351.

1A **Test:** Power the antenna temporarily and verify if satellites can be found using the antenna's web interface.

Note *For this test, the antenna should be connected directly to a PC, not the GEN series mainframe.*

2 Create outdoor/indoor pass through, ensure enough space is available to position the Surge Protector.

Note *Make sure the wall pass through is clean and does not contain sharp edges or objects that may damage the cable.*

3 Place the Optical Ethernet power over Ethernet Injector (PoE) and connect to mains power.
Verify that the power LED is lit.

4 Make sure the section of cable between the Surge Protector and PoE injector that is outside of the wall is as short as possible.

Note *Make sure the fiber optic cables do not break or get damaged when connecting.*

WARNING

It is highly recommended that the Surge Protector grounding is lightning proof.

5 Connect the cable from the PoE injector to the GEN series mainframe PTP enabled fiber optical Ethernet port.

6 After finishing these steps the G002B option is fully installed and operational. Please refer to for an overview of the installed option.

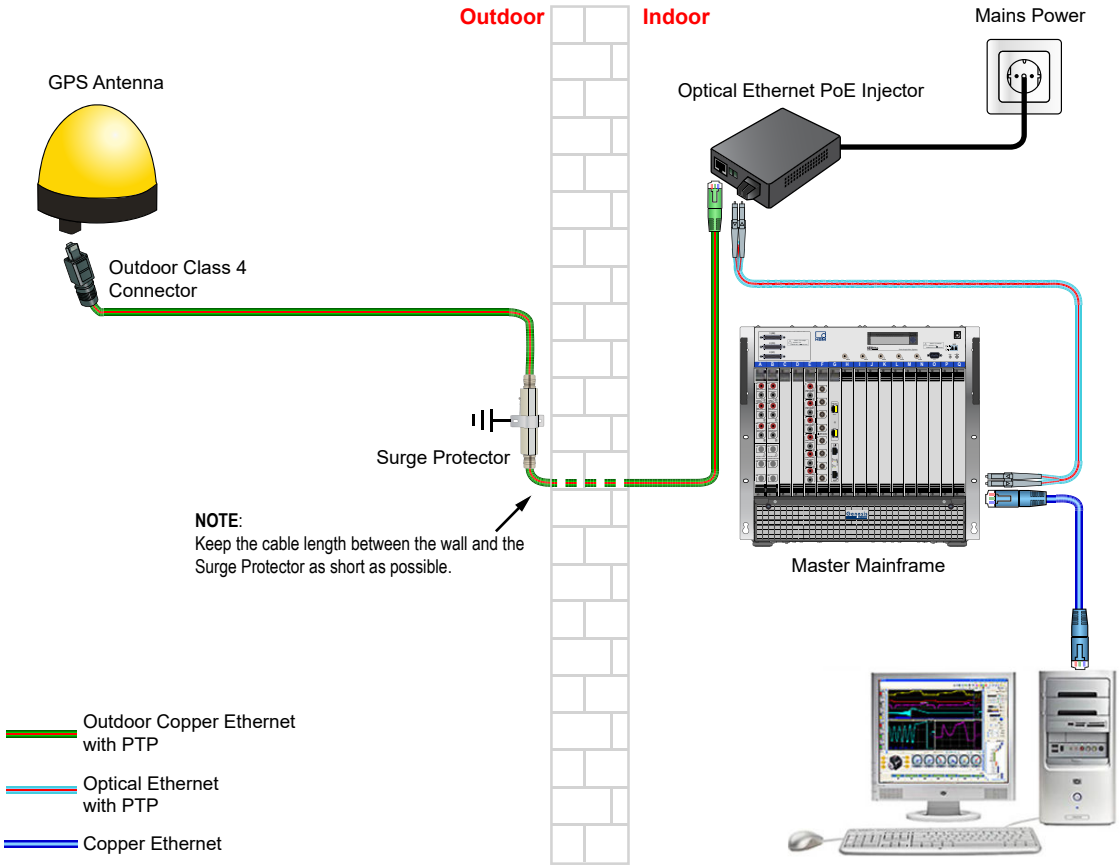


Figure 14.12: Block diagram GPS time synchronization

14.3.2 Using the GPS antenna

The antenna used in G002B uses GPS as a time source and acts as a PTP master clock for the rest of the system (see Figure 14.13).

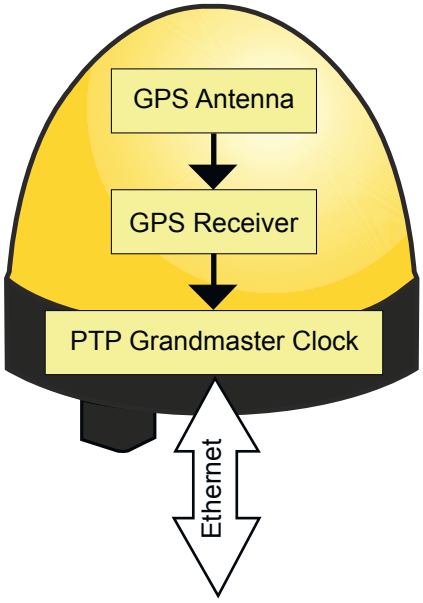


Figure 14.13: GPS antenna architecture

Note *This means that most references in the system setup are **PTP** related, and not **GPS** related.*

Perception setup

To perform time synchronized data acquisition using GEN series mainframes and the G002B option it is necessary to further setup the system. This section explains how to accomplish that using the **HBM Perception Data Acquisition** software.

Note *This section assumes you are familiar with basic operations in Perception such as connecting to data acquisition hardware and changing settings.*

Note *G002B requires usage of Perception version 7.00 or higher.*

1 Start Perception

2 Connect to the mainframe.

3 Open the settings sheet and select advanced settings:

3a In the main menu select **Settings**.

3b In the Settings menu select **Show Settings ►**.

3c In the submenu select:

- **Basic:** this will show only the relevant settings
- **Advanced:** this will show all settings

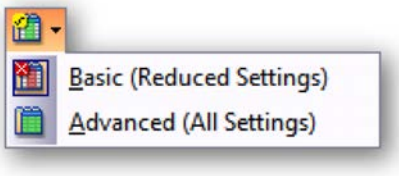


Figure 14.14: Perception settings sheet options

4 In the **Sync source** column select the required PTP option.

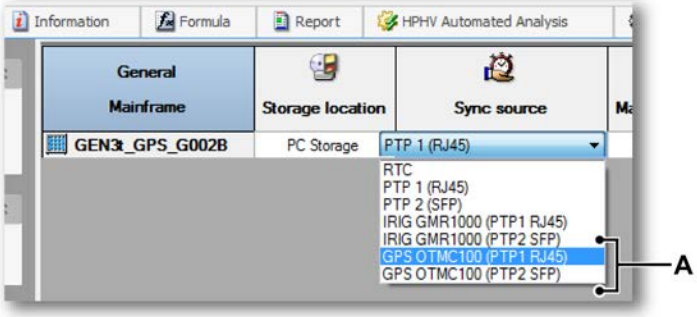


Figure 14.15: Sync source selection

A **GPS OTMC 100 (PTP1 RJ45)** and **GPS OTMC 100 (PTP2 SFP** options

Change the synchronization source to **GPS OTM C100 (PTP2 SFP)**.

Note *G002B setup: Using the fiber optic Ethernet connection provides maximum system safety against lightning impact,in this case select GPS OTMC 100 (PTP2 SFP).*
If a standard RJ45 Ethernet cable is used, select GPS OTMC 100 (PTP1 RJ45).

5 The acquisition system tries to find and synchronize to the PTP signal. The system status goes through the following states:

- No signal
- Out of synchronization
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

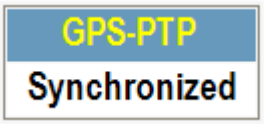


Figure 14.16: GPS-PTP status - Synchronized

6 The GPS antenna acts as a highly accurate PTP master in the network, therefore enable **Use Accurate Master** to ensure that a warning appears if another another PTP node becomes the master in the network (see Figure 14.17).

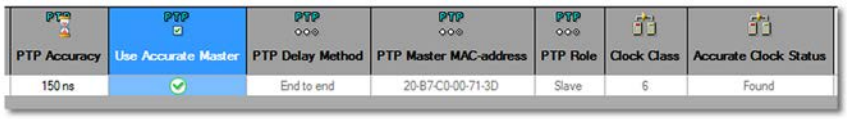


Figure 14.17: PTP - Use Accurate Master

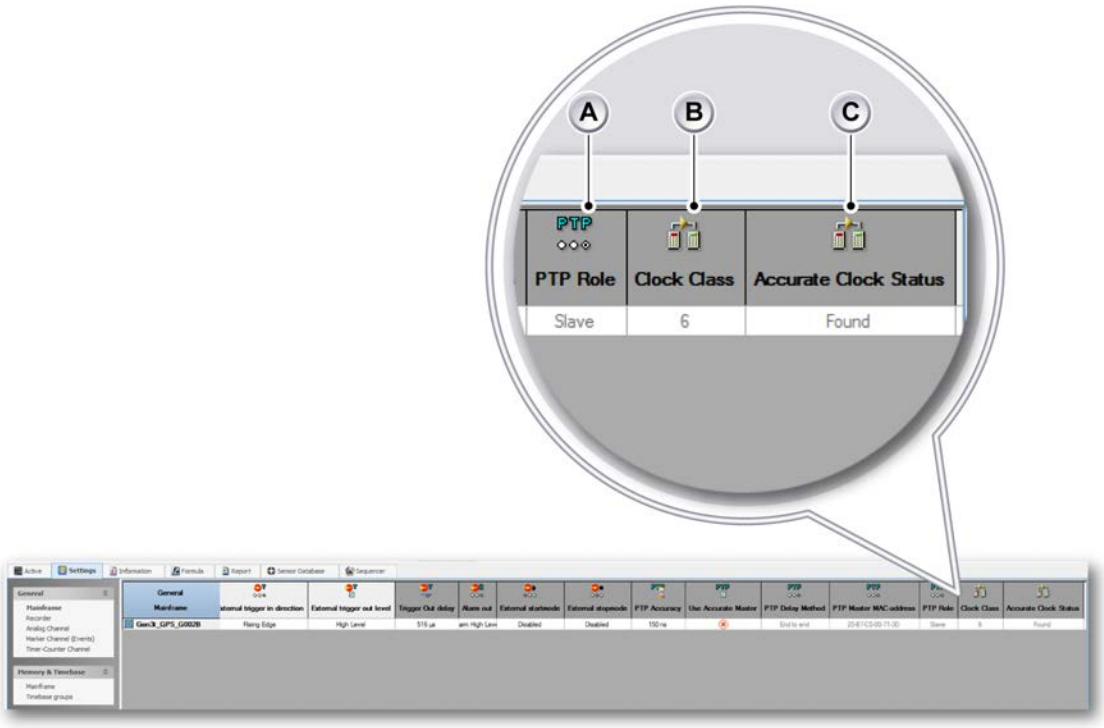


Figure 14.18: PTP synchronization status

Please verify the following settings:

A **PTP Role:** Slave

B **Clock Class:** 6

C **Accurate Clock Status:** Found

Verify setup and installation
Once the setup is complete there are several steps that can be taken to verify if the setup was successful.

Status information
The overall system time base information is displayed in the status window. This will give a system wide overview showing the most imprecise time source from all connected mainframes.

Note *As all mainframes are expected to be on PTP, the status should show PTP, and should have the default colors blue and white (see Figure 14.19).*

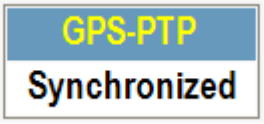


Figure 14.19: GPS-PTP status - Synchronized

Note *In case the status shown is orange / red a problem has occurred, please refer to the “Troubleshooting” chapter (on page 354) for detailed information.*

System topology
An overview can be found in the system topology overview. The system topology will show the information per connected mainframe.

1 In the menu bar choose **Help ▸ System Topology** (see Figure 14.20).

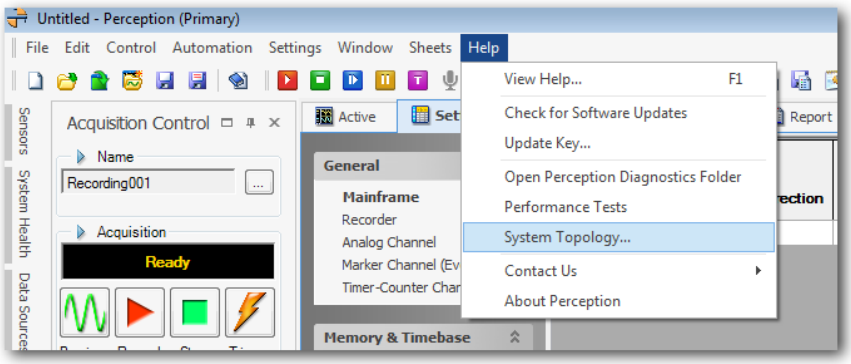


Figure 14.20: System Topology Help

2 The **System Topology** overview opens (see Figure 14.21):

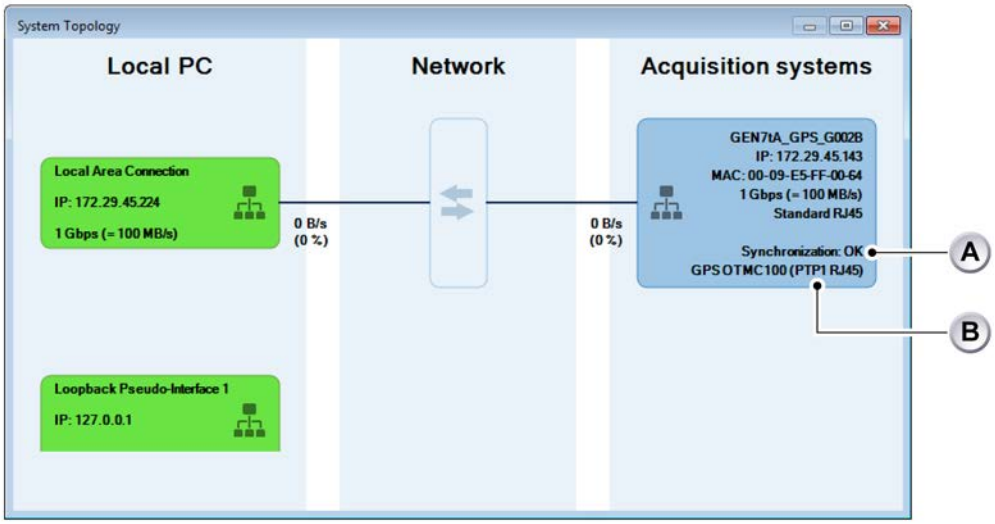


Figure 14.21: System Topology

In **System Topology** overview, please verify the following information:

A States that **Synchronization** is OK

B States that **GPS OTMC 100** is connected as selected (**PTP1 RJ45** for RJ45 connection as shown in Figure 14.21, **PTP2 SFP** if you are using the optical Ethernet connection).

Note *Network peripherals such as switches and routers are not visualized within the network topology overview.*

Recording information

When a recording is created using PTP time synchronization, the PTP master clock information is available in the recorded information in the Yt display in Perception (see Figure 14.22).

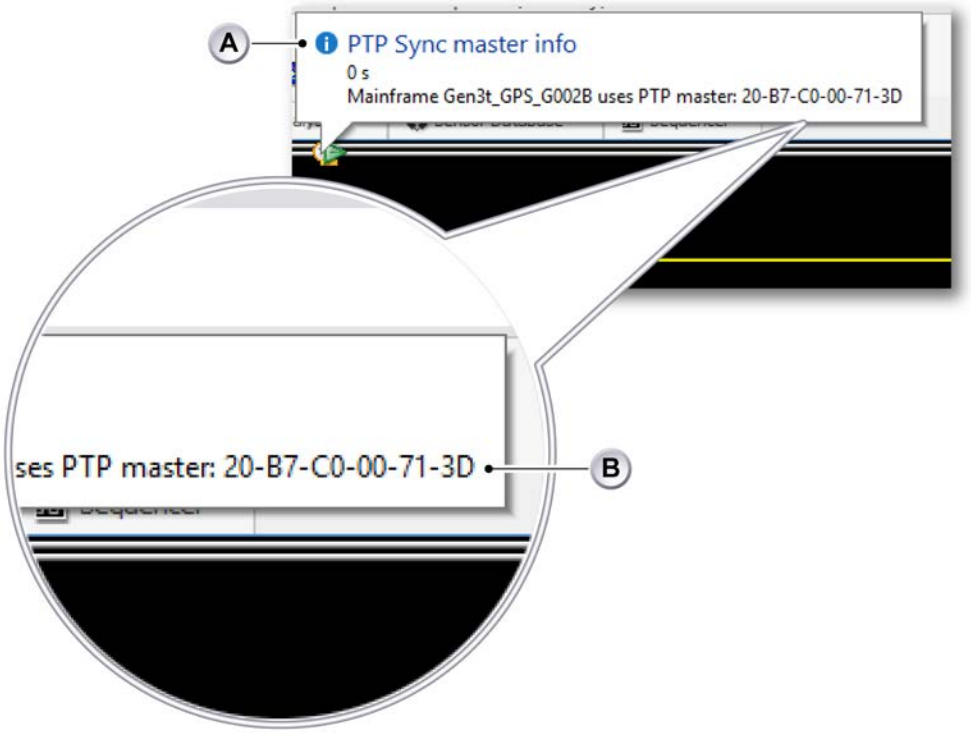


Figure 14.22: PTP synchronization master information

A PTP master clock information

B PTP master MAC adress

Note *Please refer to the chapter "Trouble-shooting guide for G002B" on page 354 in case this information is not shown or is not correct.*

Complex setups

- G002B: GPS Receiver with Master/Sync connected Sync mainframes (see Figure 14.23)
- G002B: GPS receiver with tethered mainframes plus QuantumX (see Figure 14.29)

Complex setup: G002B: GPS Receiver with Master/Sync connected Sync mainframes

It is possible to create synchronized recordings between multiple GEN series mainframes using a single GPS antenna. This section explains how to setup this configuration and what the benefits and limitations are.

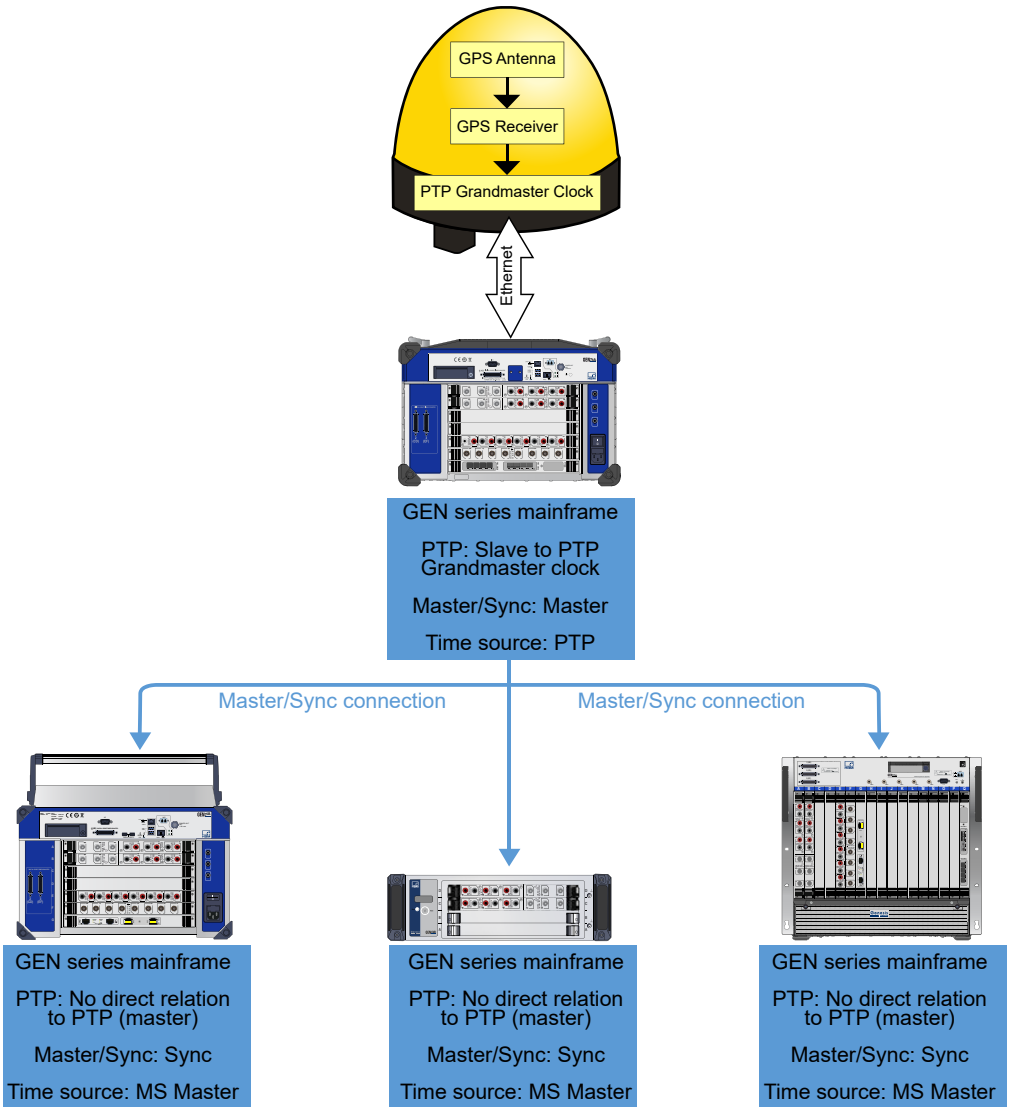


Figure 14.23: GPS Receiver with Master/Sync connected Sync mainframes

Installation

1 Connect the Master mainframe to the G002B GPS antenna and verify if it is operating correctly as explained in the earlier chapters.

2 Connect the Master/Sync optical cables between the Master mainframe and the Sync mainframes (For more information, please refer to "Connecting the Master/Sync connector" on page 149).

3 Set the Master/Sync mode to Master for the mainframe connected to the GPS (see Figure 14.24).

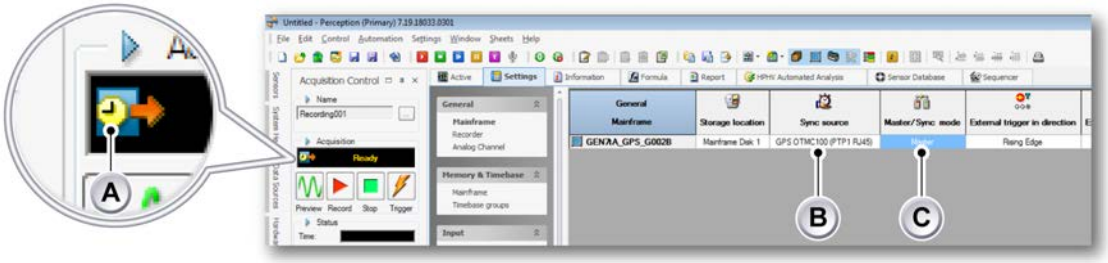


Figure 14.24: Settings for Master/Sync mode to Master in Perception

A This icon indicates that the mainframe is the Master in the Master/Sync setup.

B The sync source is set to GPS OTMC 100 during the G002B setup.

C This indicates the role in the Master/Sync setup, should be Master.

4 Set the Master/Sync mode to Sync for the mainframes connected to the Master mainframe. It will go through these stages:

- **No master** (see Figure 14.25)
- **Searching for master** (see Figure 14.26)
- **Master detected** (see Figure 14.27)

No master

Figure 14.25: Status - No master detected

A This icon indicates that there is currently no Master found on the Master/Sync bus.

B The Sync source is not relevant for the Sync mainframes; the time source is the Master in the Master/Sync mode.

C This indicates the role in the Master/Sync setup, should be Sync.

Searching for Master

Figure 14.26: Status - Searching for Master

A After a short period, the icon **(A)** starts blinking. This indicates that the Sync system is searching for a Master mainframe on the Master/Sync bus.

Master detected

Figure 14.27: Status - Master detected

A Once the Master is found, the icon **(A)** will change indicating the Master is now the time source. In case no Master is detected it will go back to the **No Master** mode.

(For more details of Master/Sync operation in the Perception software, please see "Setting the Master/Sync operating modes" on page 151).

Note *In case of multiple Sync mainframes, the worst-case status will be shown. So, if one of the Sync mainframes is not properly connected,* ***No Master*** *will be reported.*

Conditions and constraints
Additional GEN series hardware is required to synchronize more than two mainframes. For more information, please refer to "Master/Sync connector" on page 145.

Note *It is only possible to synchronize GEN series mainframes through the Master/Sync bus. No support for QuantumX modules or other data acquisition hardware.*

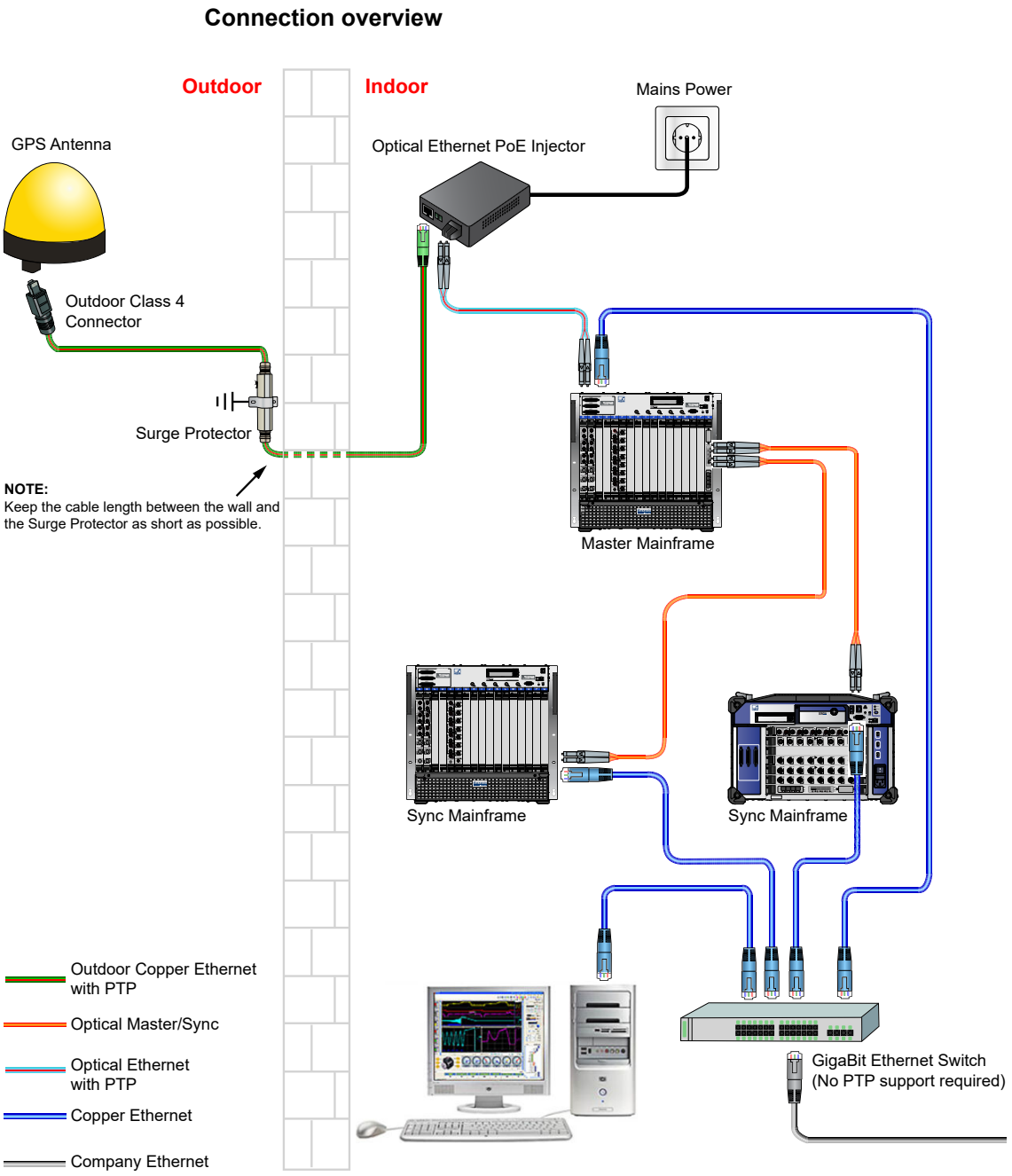


Figure 14.28: GPS setup for tethered mainframe with Master/Sync connected Sync mainframes

Complex setup: G002B: GPS receiver with tethered mainframes plus QuantumX

When using other data acquisition hardware besides GEN series mainframes, it is not possible to connect everything through the Master/Sync mechanism. In this case, using PTP allows multiple mainframes to synchronize against a single GPS antenna.

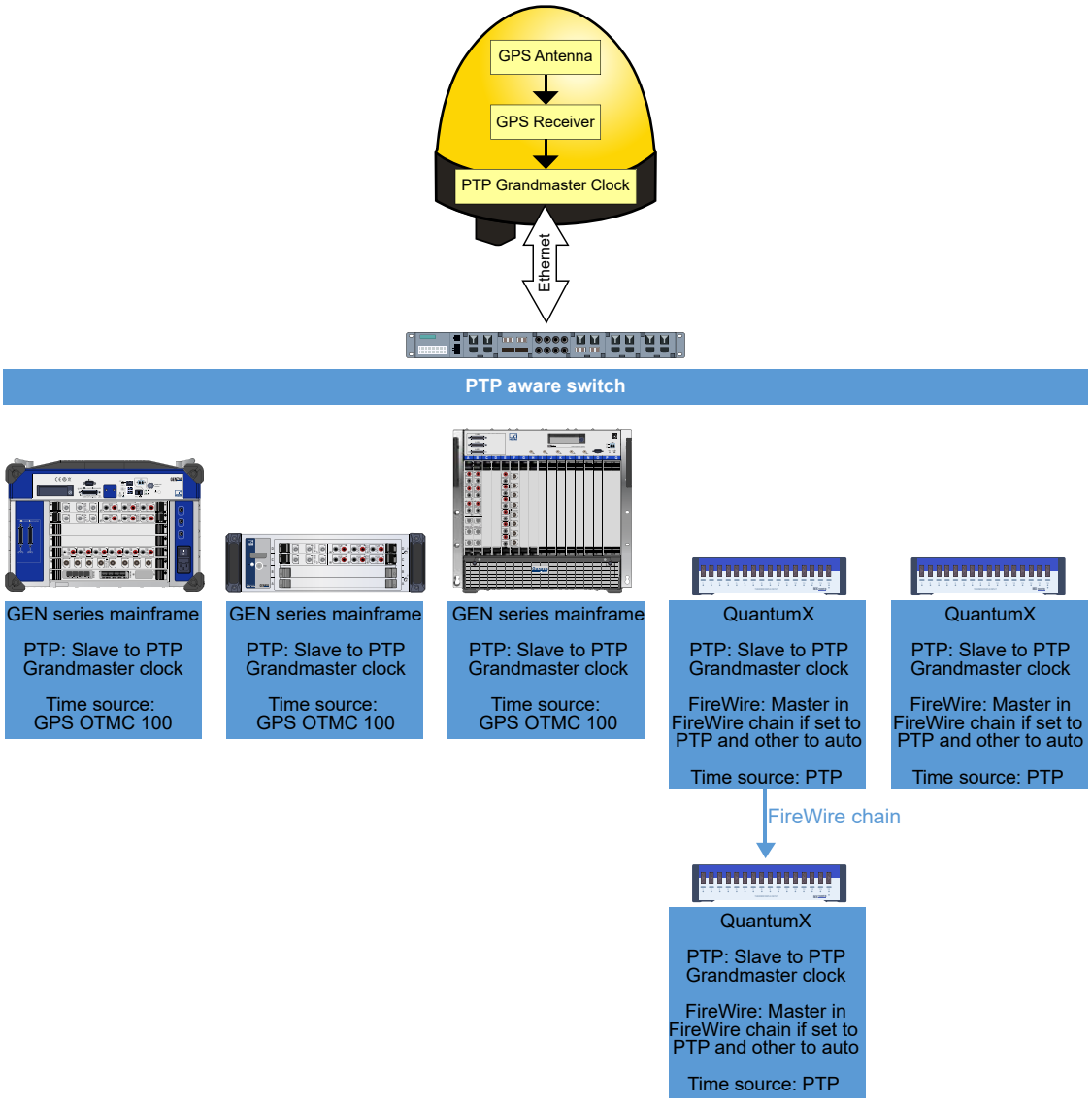


Figure 14.29: GPS receiver with tethered mainframes plus QuantumX

Installation

When connecting the GPS antenna to the mainframe, please follow the steps described below.

IMPORTANT

As the GPS antenna is typically placed on a roof or otherwise hard to access position, it is highly recommended to connect the GPS antenna to the PoE injector and plug the injector into mains. Please refer to the LED overview to verify that the GPS antenna is properly powered and optionally connect to the web client to verify the GPS antenna is fully operational.

1 Place the GPS antenna in a position with clear view to the sky. For more information, please refer to chapter "GPS antenna placement" on page 351.

1A **Test:** Power the antenna temporarily and verify if satellites can be found using the antenna's web interface.

Note *For this test, the antenna should be connected directly to a PC, not the GEN series mainframe.*

2 Create outdoor/indoor pass through, ensure enough space is available to position the Surge Protector.

Note *For this test, the antenna should be connected directly to a PC, not the GEN series mainframe.*

Note *Make sure the wall pass through is clean and does not contain sharp edges or objects that may damage the cable.*

3 Place the Optical Ethernet power over Ethernet Injector (PoE) and connect to mains power.
Verify that the power LED is lit.

4 Make sure the section of cable between the Surge Protector and PoE injector that is outside of the wall is as short as possible.

Note *Make sure the fiber optic cables do not break or get damaged when connecting.*

WARNING

It is highly recommended that the Surge Protector grounding is lightning proof.

5 Connect the cable from the PoE injector to the PTP switch.

6 Connect the cable between the mainframe RJ45 PTP aware connector and the PTP switch. Repeat this step for all mainframes that need to synchronize to the GPS antenna.

7 After finishing these steps the G002B option is fully installed and operational (see also Figure 14.30).

Connection overview

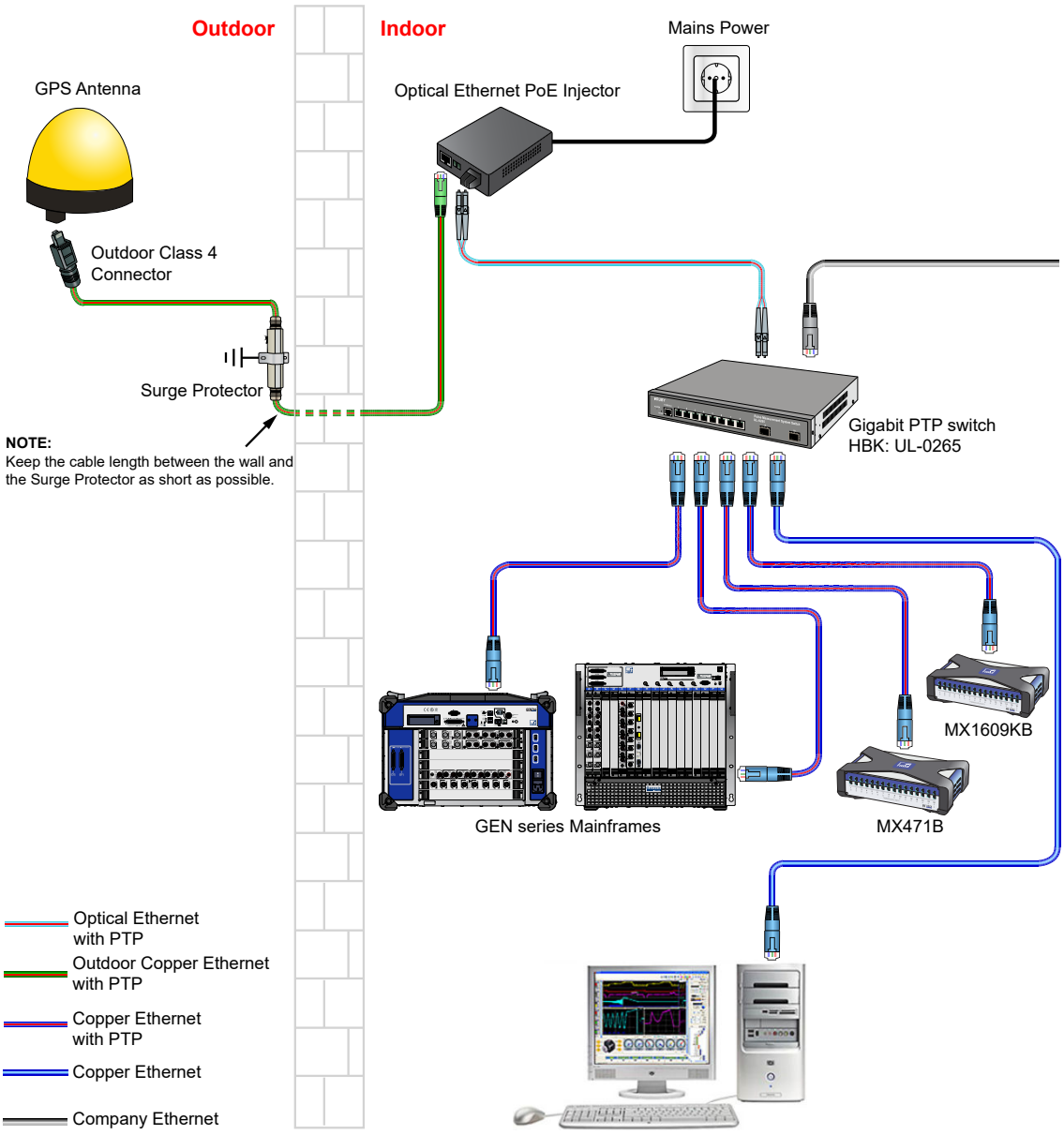


Figure 14.30: GPS setup for tethered mainframes and QuantumX

For more information about QuantumX and GEN series mainframes, please refer to chapter "Synchronizing GEN series and QuantumX using PTP" on page 464.

14.3.3 Setup comparison

Synchronization characteristic	G002B directly to mainframe	G002B with Master/Sync connected mainframes	G002B with Tethered mainframes
Accuracy	150 ns to UTC	150 ns to UTC	150 ns to UTC
Geographical distribution	Worldwide	Limited to the Master/Sync range	Limited to the PTP network range
Scalability	Unlimited	Up to 128 mainframes No QuantumX	Depends on the PTP network setup. Supports QuantumX **Note** *Can be combined with Master/Sync to extend scalability*
Complexity	Low	Medium Requires Master/ Sync setup	High Requires correct setup of PTP network
Electrical safety	Highest Built-in Surge Protector(1) and use of fiber optical connection. No link between mainframes	High Built-in Surge Protector(1) and use of fiber optical connection.	Depends on PTP network
Cost	High Each mainframe requires a PTP master	Low One Master Output card needed for every four Sync mainframes	Medium PTP network setup
Reliability	High No SPOF (Single Point of Failure)	Medium 2 x SPOF G002B antenna Master mainframe	Unknown 1x known SPOF G002B antenna + PTP aware network

(1) **Note** *Surge Protector grounding must be lightning safe.*

14.3.4 GPS antenna placement

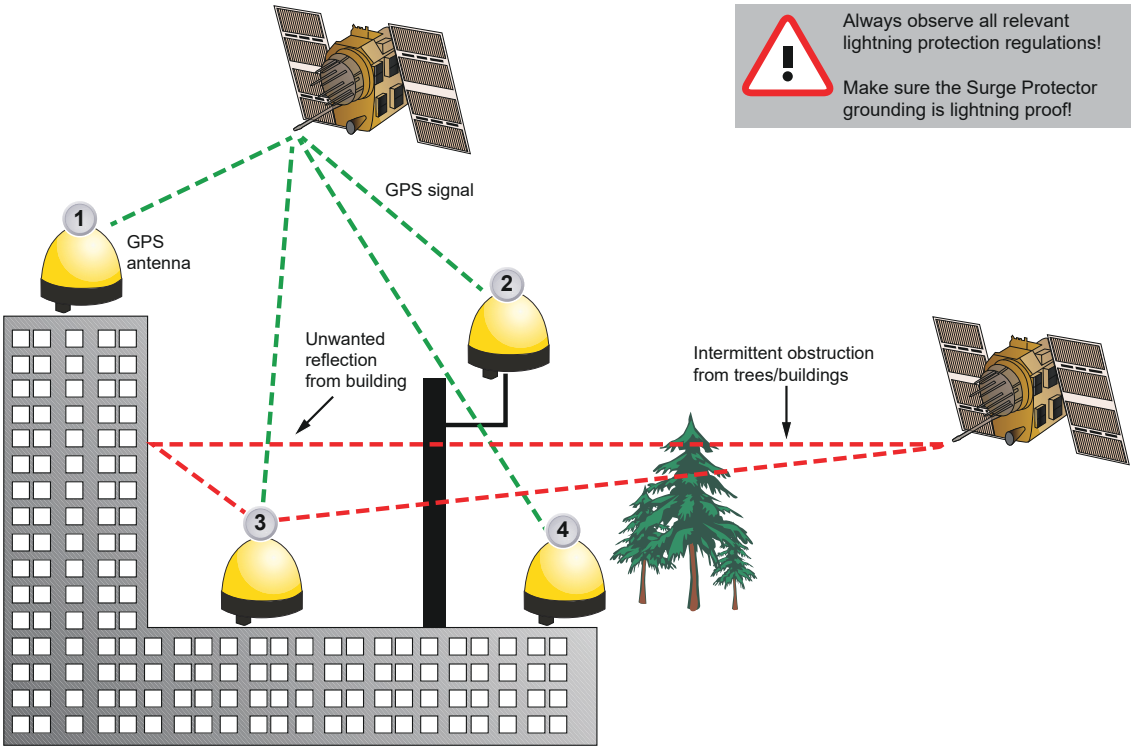


Figure 14.31: Recommended GPS antenna positions

BEST mounting position with best possible reception of GPS signals.
This mounting position provides direct view to the sky. The view is not hindered by any objects and the GPS signals are not influenced by any reflections.

POSSIBLE mounting position on pole providing sufficient reception of GPS signals under most conditions. This mounting position provides direct view to the sky in a range nearly 180°. The view is only partly hindered and there is negligible danger of reflections that could influence the GPS signals.

BAD mounting position. Do not use!
This mounting position provides direct view to the sky for a range only 90° Half the sky is blocked by the taller part of the building and the reception of GPS signals will be considerably influenced by reflections. The *OTMC 100* will not work properly!

NOT RECOMMENDED mounting position. Only use if no other mounting position is available.
This mounting position provides direct view to the sky for a range more than 90° but much less than 180°. The view to the left is hindered by the taller part of the building and there is an increased danger of reflections that could influence the GPS signals.

Note *Mount the OTMC 100 in an upright position with the protective cap to the top only (see Figure 14.32)!*

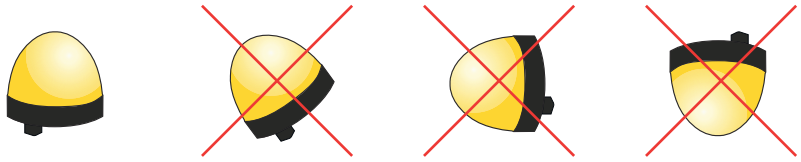


Figure 14.32: GPS antenna mounting positions

2 **Optional:** Install lightning impact protection rod near antenna.

Note *Repeat the test described in chapter "Installation" on page 332 (Step **1A**) to ensure the lightning impact rod does not obstruct satellite detection.*

14.3.5 GPS antenna lightning protection

WARNING

It is highly recommended to apply lightning protection such as a lightning rod to the placement of the GPS antenna (see Figure 14.33).

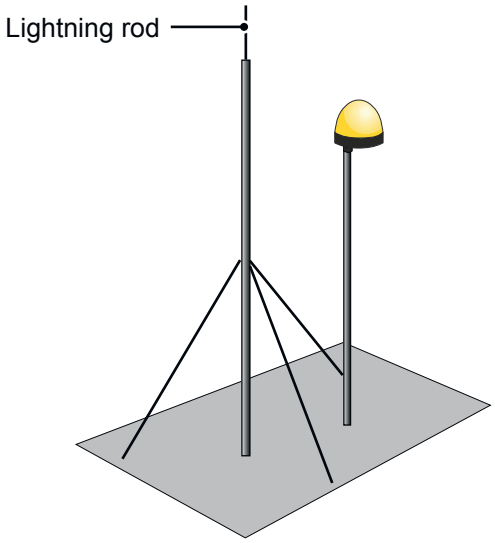


Figure 14.33: GPS antenna with applied lightning protection

14.3.6 Trouble-shooting guide for G002B

The chapter "GPS OTMC 100 Trouble-shooting" on page 432 gives some hints on what to check if the OTMC 100 does not work as expected. It will first explain how to use Perception to determine if there is a problem and then offer help on diagnosing and solving the issue.

14.4 IRIG

14.4.1 System overview

G001B: Direct connection setup

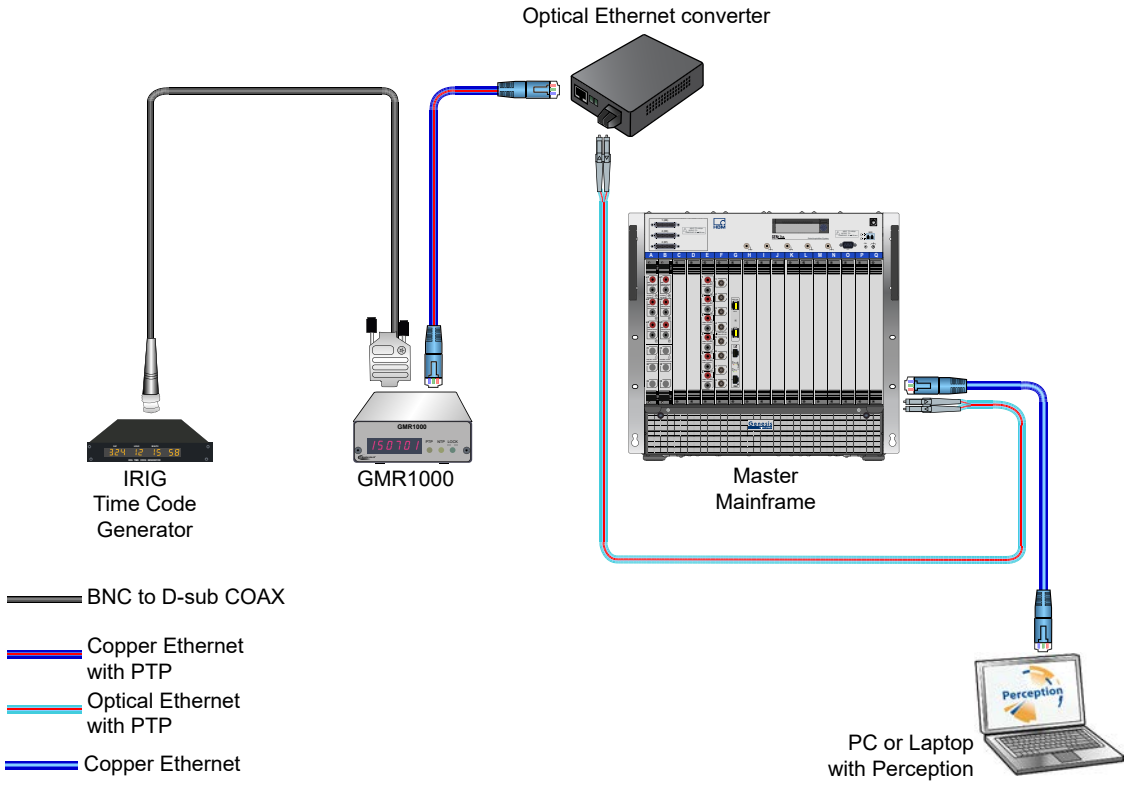


Figure 14.34: Block diagram IRIG synchronization

G001B: Direct connection setup with optical Ethernet

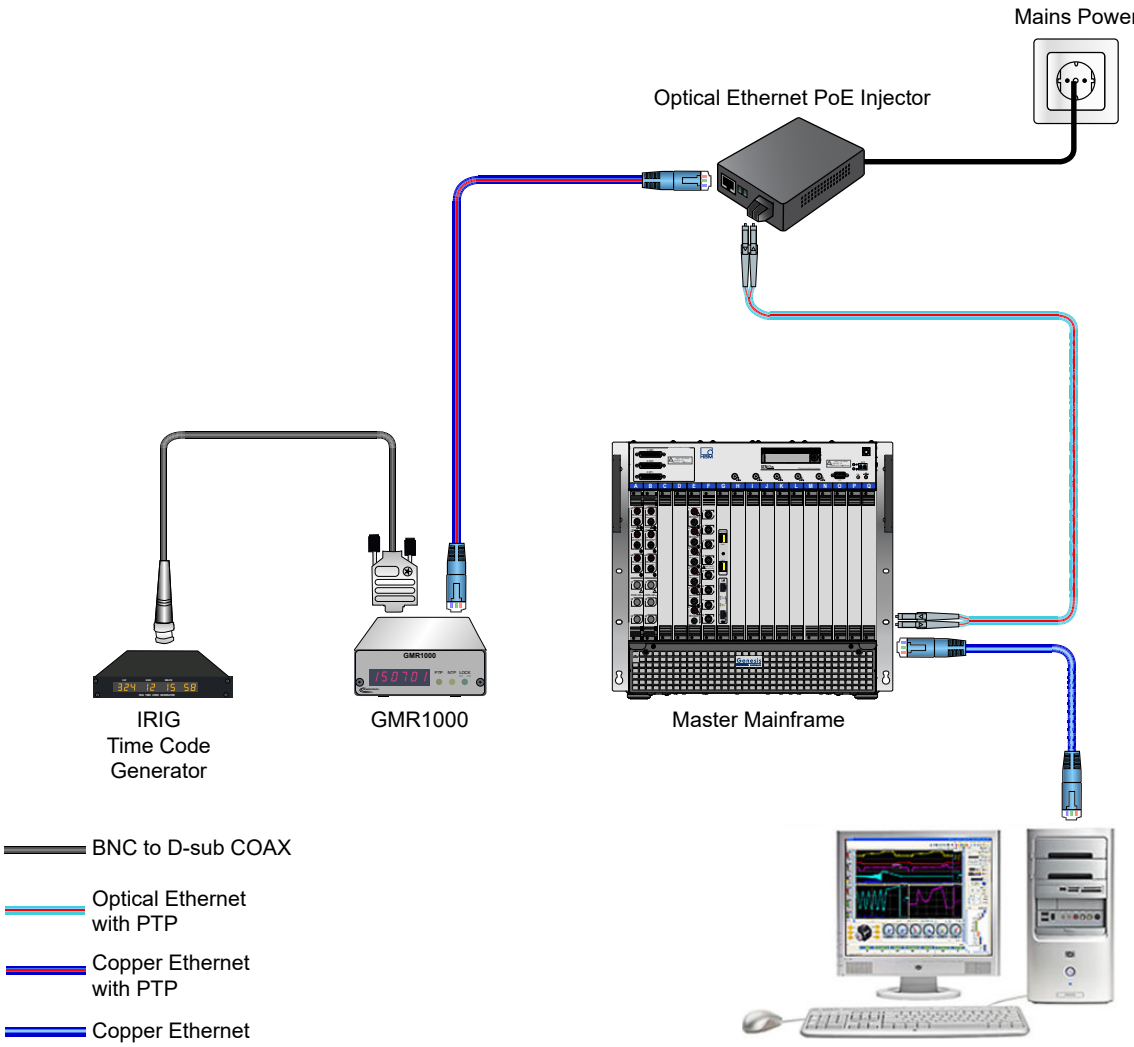


Figure 14.35: Block diagram IRIG synchronization

Note *Use optical Ethernet when there is a large distance between the GMR1000 and the mainframe.*

G001B: IRIG to PTP with tethered mainframes plus QuantumX

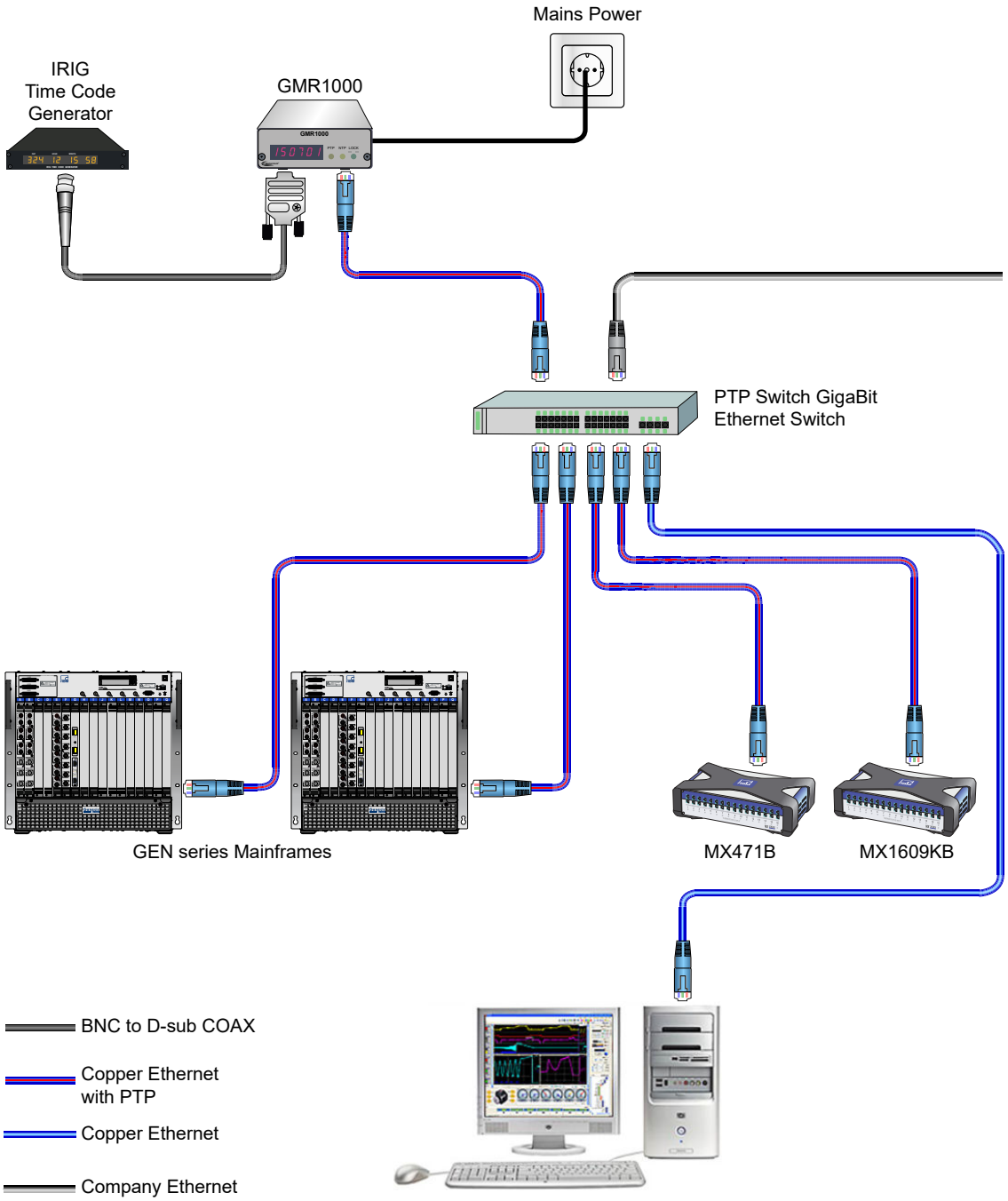


Figure 14.36: IRIG setup for tethered mainframes and QuantumX

14.4.2 Installation

When connecting the G001B option, please follow the steps described below.

1 Connect GMR1000 to power socket using the correct power adapter.

Figure 14.37: GMR1000

A Display information

B LOCK led

The **LOCK** led should light up, stay lit and after a while start to blink. After a while the red digits should start displaying information.

2 Connect the IRIG source to the GMR1000. After a few seconds, the **LOCK** led should blink green.

3 Connect the GMR1000 to the mainframe via Ethernet.

3a G001B: Direct connection setup.

- Connect the GMR1000 to mainframe PTP port 1 (RJ45) using a standard Ethernet cable.

3b G001B: Direct connection setup with optical Ethernet.

- Connect the mainframe PTP port 2 (SFP) to the media converter using the fiber cable.
- Connect the GMR1000 to the media converter using a standard Ethernet cable.

3C G001B: IRIG to PTP with tethered mainframes plus QuantumX.

- Connect the GEN series mainframe to the PTP aware switch using the port of choice PTP 1 (RJ45) or PTP 2 (SFP).
- Connect the GMR1000 to the PTP aware switch.

Note *The choice of mainframe PTP port impacts the later selection of Sync Source. Please match the selection to the actual selection here for proper operation.*

14.4.3 Using the GMR1000 module

The GMR1000 unit takes the IRIG signal as time source input and acts as a PTP master clock for the rest of the system (see Figure 14.38).

Figure 14.38: G001B architecture

Note *This means that most references in the system setup are **PTP** related, and not **IRIG** related.*

Perception setup

To perform time synchronized data acquisition using GEN series mainframes and the G001B option it is necessary to further setup the system. This section explains how to accomplish that using the **HBM Perception Data Acquisition** software.

Note *This section assumes you are familiar with basic operations in Perception such as connecting to data acquisition hardware and changing settings.*

Note *G001B requires usage of Perception version 7.20 or higher.*

1 Start Perception

2 Connect to the mainframe.

3 Open the settings sheet and select advanced settings:

3a In the main menu select **Settings**.

3b In the Settings menu select **Show Settings ►**.

3c In the submenu select:

- **Basic:** this will show only the relevant settings
- **Advanced:** this will show all settings

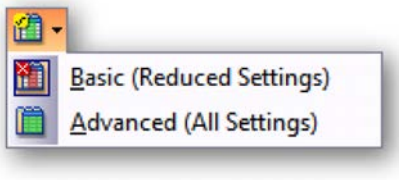


Figure 14.39: Perception settings sheet options

4 In the **Sync source** column select the required IRIG option.

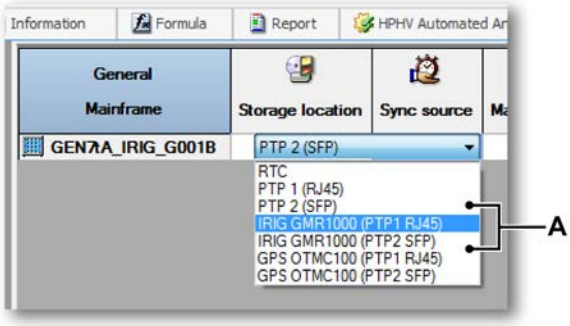


Figure 14.40: PTP selection

A **IRIG GMR1000 (PTP1 RJ45)** and **IRIG GMR1000 (PTP2 SFP)** options

Change the synchronization source to **IRIG GMR1000 (PTP1 RJ45)**.

5 The acquisition system tries to find and synchronize to the PTP signal. The system status goes through the following states:

- No signal
- Out of synchronization
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

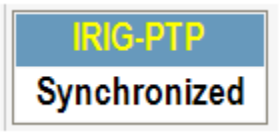


Figure 14.41: IRIG-PTP status - Synchronized

6 The GMR1000 does not act as a highly accurate PTP master in the network, therefore disable **Use Accurate Master** (see Figure 14.42).

Note *If **Use Accurate Master** is enabled and the GMR1000 becomes the PTP master, Perception will show a warning because the GMR1000 is not a clock class 7 or better PTP master.*

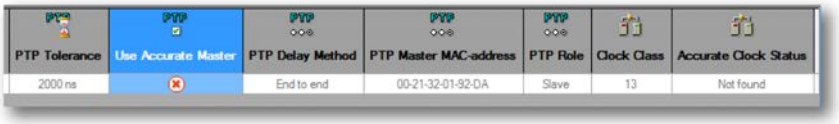


Figure 14.42: PTP - Use Accurate Master

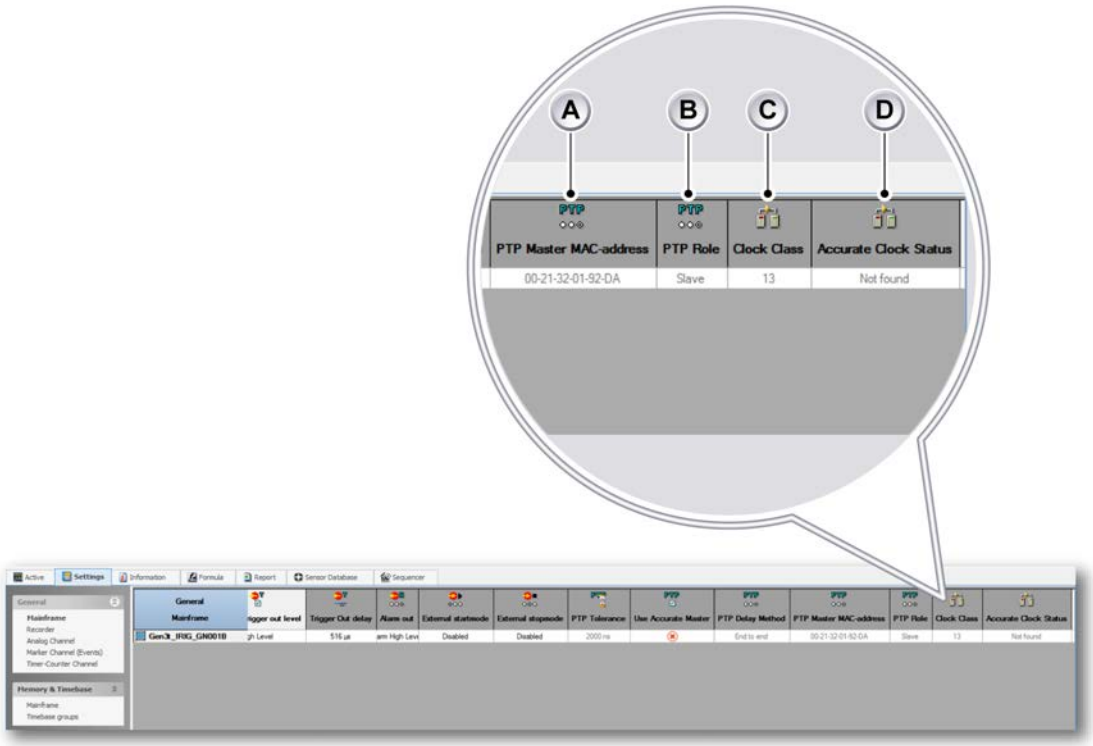


Figure 14.43: PTP synchronization status

Please verify the following settings:

A **PTP Master MAC-address:** Address of the GMR1000

B **PTP Role:** Slave

C **Clock Class:** 13

D **Accurate Clock Status:** Not found

Verify setup and installation

Once the setup is complete there are several steps that can be taken to verify if the setup was successful.

Status information

The overall system time base information is displayed in the status window. This will give a system wide overview showing the most imprecise time source from all connected mainframes.

Note *As all mainframes are expected to be on PTP, the status should show PTP, and should have the default colors blue and white (see figure below).*

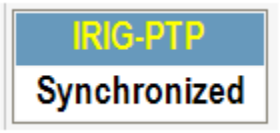


Figure 14.44: IRIG-PTP status - Synchronized

Note *In case the status shown is orange / red a problem has occurred, please refer to the “Troubleshooting” chapter (on page 366) for detailed information.*

System topology

An overview can be found in the system topology overview. The system topology will show the information per connected mainframe.

1 In the menu bar choose **Help ▸ System Topology** (see Figure 14.45).

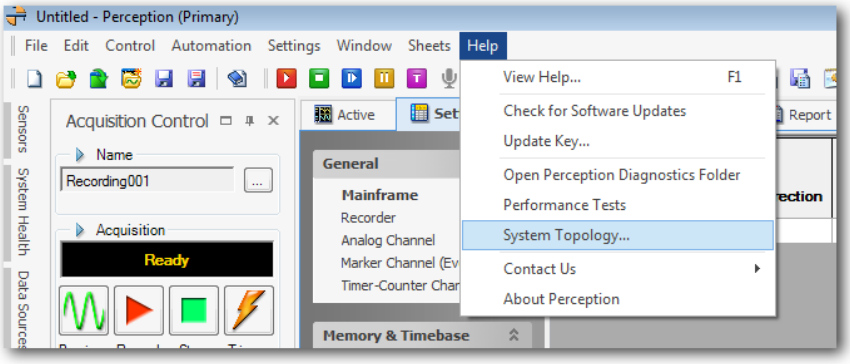


Figure 14.45: System Topology Help

2 The **System Topology** overview opens (see Figure 14.46):

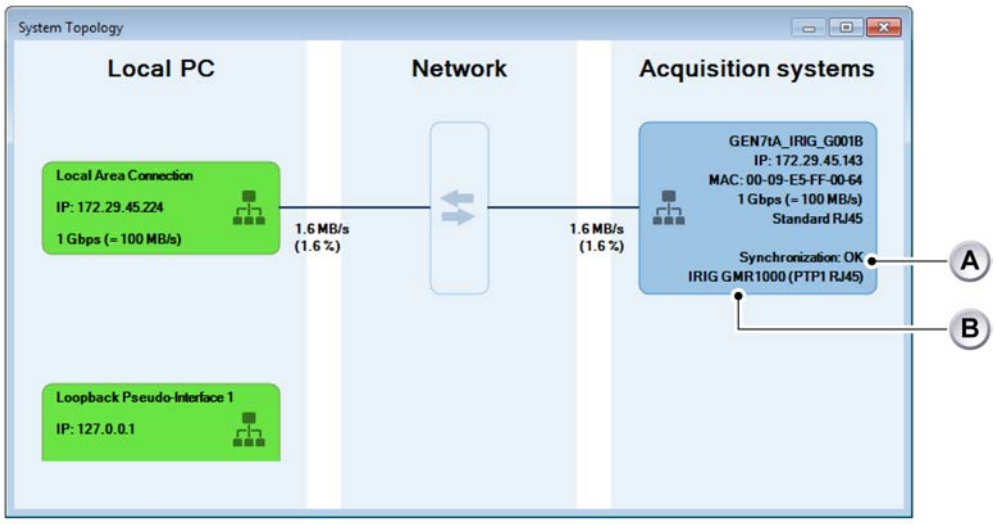


Figure 14.46: System Topology

In **System Topology** overview, please verify the following information:

A States that **Synchronization** is OK

B States that **IRIG GMR1000** is connected as selected (**PTP1 RJ45** for RJ45 connection as shown in Figure 14.46, **PTP2 SFP** if you are using the optical Ethernet).

Note *Network peripherals such as switches and routers are not visualized within the network topology overview.*

Recording information

When a recording is created using PTP time synchronization, the PTP master clock information is available in the recorded information in the Yt display in Perception (see Figure 14.47).

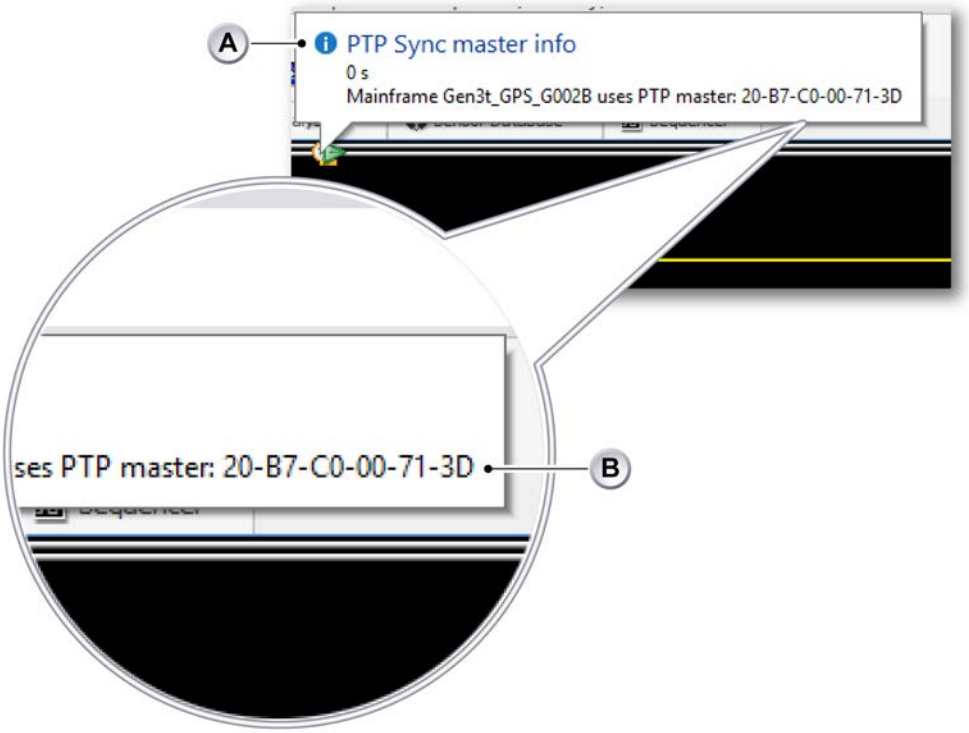


Figure 14.47: PTP synchronization master information

A PTP master clock information

B PTP master MAC adress

Note *Please refer to the chapter "Trouble-shooting guide for G001B" on page 366 in case this information is not shown or is not correct.*

14.4.4 Trouble-shooting guide for G001B

The chapter "IRIG GMR1000 Trouble-shooting" on page 407 gives some hints on what to check if the GMR1000 does not work as expected. It will first explain how to use Perception to determine if there is a problem and then offer help on diagnosing and solving the issue.

15 Understanding Inputs and Usage of Probes

15.1 GEN series inputs

Note *Every manufacturer uses different names for similar or even identical types of inputs. Some of the terminology used is described in this section.*

Balanced Vs Unbalanced
A balanced input describes an input stage where both input terminals exhibit the same electrical behavior, such as resistance and capacitance. Unbalanced electrical input properties are different.

Symmetrical Vs Unsymmetrical
Symmetrical (similar to **balanced**) describes the input properties; if both input terminals are built up using the same component in a mirrored way, they are **symmetrical** (this will result in a **balanced input**).

Differential
A differential amplifier is a type of electronic amplifier that multiplies the difference between two inputs by a constant factor.
A differential amplifier is often treated as an isolated amplifier, which is incorrect.

Single-ended
A single-ended amplifier is a type of electronic amplifier that has the negative input connected to (measurement) ground.

Note *A differential amplifier can be turned into a single-ended one by connecting the negative input to ground.*

Isolated
An isolated amplifier is a type of electronic amplifier where both inputs are isolated from (earth) ground or which has infinite resistance to ground.

Note *Isolation can be combined with any of the amplifier variations mentioned above.*

15.1.1 Single-ended input

A single-ended input is not isolated and uses unbalanced inputs.

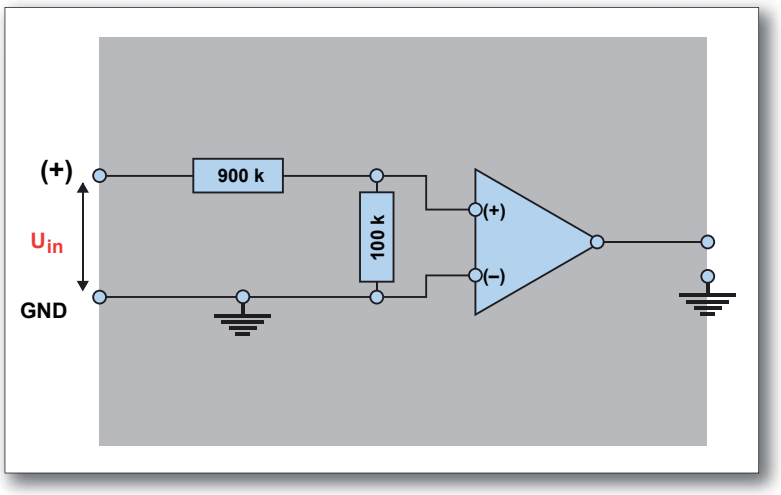


Figure 15.1: Single-ended amplifier

- One input is connected to ground
- Resistance / Capacitance from each terminal to ground is different
- Amplifier is typically found in oscilloscopes
  - Also used in GEN DAQ Basic amp, Liberty 8ch DC amp
  - Often identified by the use of a single METAL BNC connector per channel
- Can be used with standard passive probes (as with oscilloscopes)

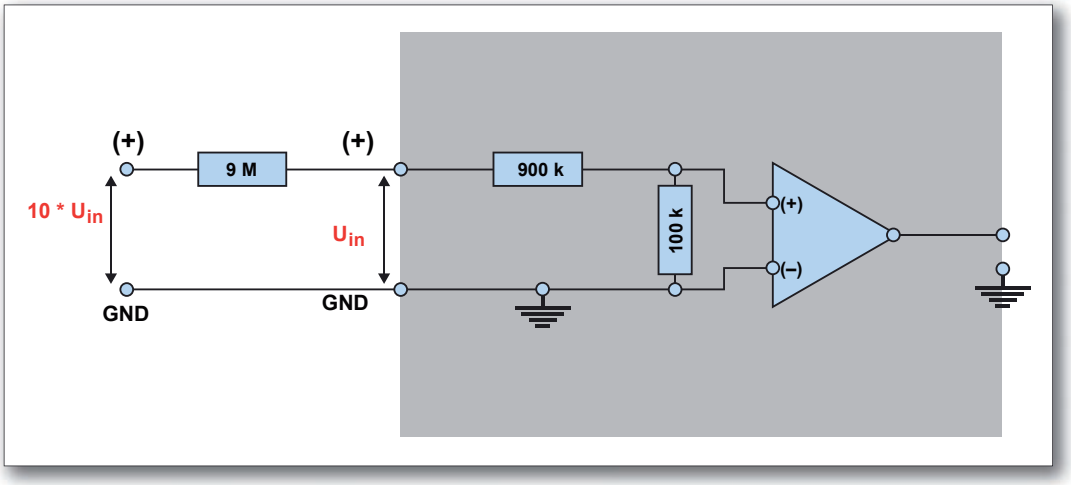


Figure 15.2: Single-ended amplifier with passive probe

- An inline resistor acts as a voltage divider using the input resistance of the amplifier
- The amplifier itself measures only $\mathbf{U_{in}}$; the **total** input range is $\mathbf{10 * U_{in}}$
- This can be done with any oscilloscope or the GEN DAQ Basic Amp
  - Oscilloscope probes are typically only +/- 2% to +/- 5% accurate
- The probes used need compensation. The compensation range needs to match the input amplifier's capacitance range.

15.1.2 Balanced differential input

A balanced differential input is not isolated and uses balanced inputs.

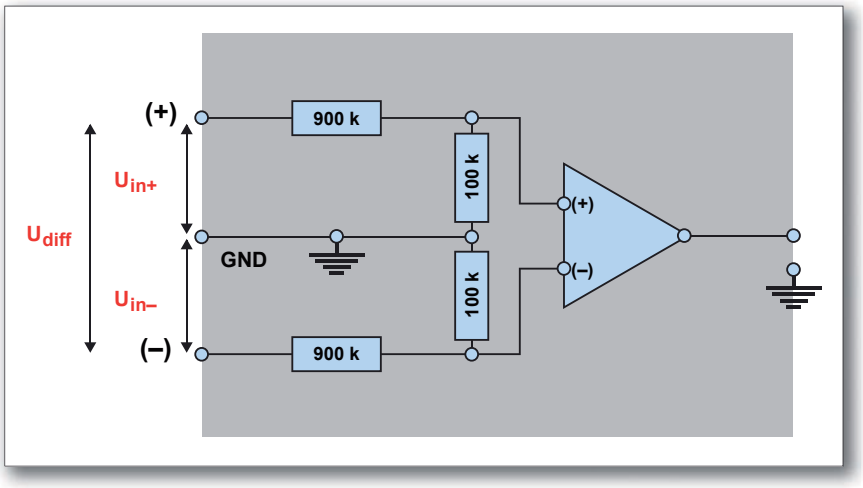


Figure 15.3: Balanced differential amplifier

- Resistance / Capacitance from each terminal to ground is identical
- There is NO ISOLATION
  - Used in some of the GEN DAQ acquisition cards
  - Often identified by the use of two METAL BNC connectors per channel
- Can be used with matched pair of probes only
  - Works with the same limitations as single probes, but is more tricky due to the necessary **balance** between probes
- The probes used need compensation. The compensation range needs to match the input amplifier's capacitance range

15.1.3 Isolated single-ended or Isolated unbalanced differential input

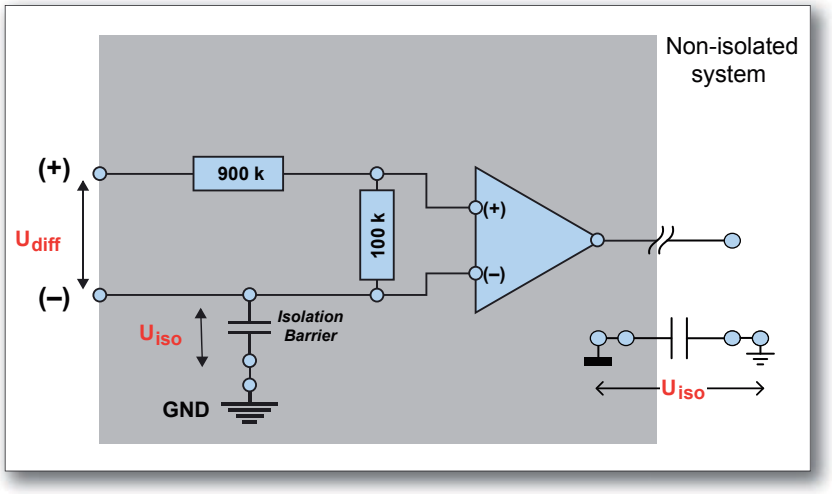


Figure 15.4: Isolated single-ended or Isolated unbalanced differential amplifier

- Also referred to as **unbalanced**, **isolated** or **unbalanced differential** amplifier
- None of the inputs are connected to ground for safety and to avoid ground loops
- Typically used in isolated DAQ systems
  - Often identified by the use of a single PLASTIC (isolated) BNC connector
  - Used in GEN DAQ ISOLATED Basic amp
- Can perform *DIFFERENTIAL MEASUREMENTS with different limitations and options, compared to a differential grounded amplifier*.

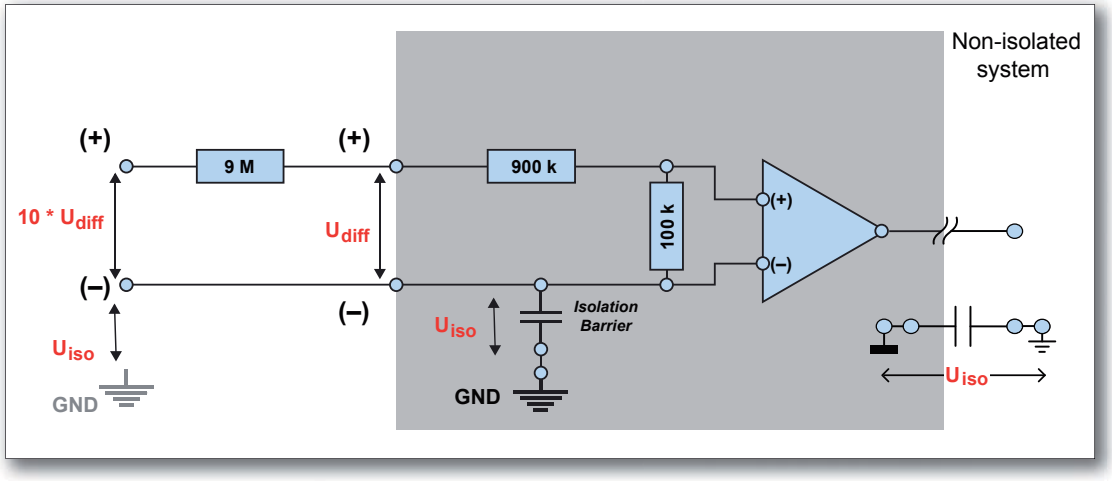


Figure 15.5: Isolated single-ended or Isolated unbalanced differential amplifier with passive probe

- Also referred to as **unbalanced**, **isolated** or **unbalanced differential** amplifier with probe
- None of the inputs are connected to ground
- The positive (system) input accepts ten times the input voltage of the amplifier
- The negative input has NOT CHANGED AT ALL
- The measurement range is increased from + to - inputs,
  BUT the isolation voltage from (-) to ground remains unchanged
  - Example is the GEN DAQ Basic XT Iso card with external Isolated passive probe
- The probes used need compensation. The compensation range needs to match the input amplifier's capacitance range

15.1.4 Isolated balanced differential input

An isolated balanced differential input is isolated and uses balanced inputs. Isolated measurement ground is not often available.

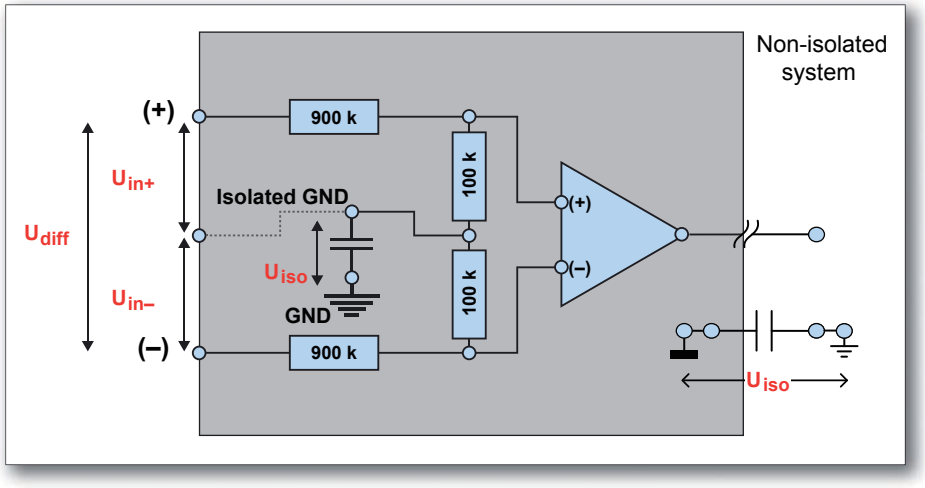


Figure 15.6: Isolated balanced differential amplifier

- Resistance / Capacitance from each terminal to isolated measurement ground is identical
- There is an ISOLATED MEASUREMENT GROUND
  - Used in GEN DAQ Universal amplifier
  - Typically identified by using two or three (isolated) connectors per channel

Note *The isolated ground is not accessible in some designs*

- Cannot be used with probes as there is no ground reference for probes to divide the voltage

Different amplifiers – Pros and Cons

Single-ended (to ground) amplifiers

- Cost effective and small
- High bandwidth
- Easy to use with probes
- Potential ground problems
- No safety problems
- No CMRR and no CMV

Single-ended isolated amplifier – unbalanced differential

- Can perform differential measurements
- Expensive and large
- Difficult to use with probes
- Limited CMRR, best CMV
- Avoids ground loops
- High level of safety

Differential amplifier (with common ground)

- Widely used in DAQ
- Good CMRR, limited CMV
- No (safety) isolation and potential ground loops will remain present

Differential amplifier with isolated common

- Safe
- Expensive and large
- Good CMRR, best CMV
- More difficult to use with probes

15.2 GEN series voltage probe types

HBM offers a variety of probes. Which probe is needed depends on the application and which instrument is being used. It is important to match the compensation of the probe to the instrument.

- **Passive, single-ended voltage probes**
  These probes can be used with single-ended or differential non-isolated amplifiers and increase the input range of the amplifier only in single-ended mode. They typically decrease the overall accuracy of the amplifier.
- **Passive, single-ended isolated voltage probes**
  These probes can be used with single-ended or differential isolated amplifiers and increase the input range of an isolated amplifier only in single-ended mode. They typically decrease the overall accuracy of the amplifier.
  It is important to understand that they increase only the range, not the isolation voltage.
- **Passive, differential matched isolated voltage probes**
  These probes can be used with differential isolated amplifiers and increase the input range of the amplifier in differential mode. They typically decrease the overall accuracy and the CMRR of the amplifier.
  They work with isolated and non-isolated variations of differential amplifiers.
  When used with isolated amplifiers, they increase only the range, not the isolation voltage.
- **Active differential voltage probes**
  These probes are self-contained, differential amplifiers to be used in front of an instrument using any amplifier in single-ended mode.
  The input range and accuracy depend on the type of active differential probe used and have no relation to the amplifier used. They usually operate from batteries; this causes some inconvenience.
- **Current clamps**
  Current clamps function more as transducers than probes, as they convert one physical quantity (current) into another one (usually voltage). They are used to perform non-invasive current measurements. This allows the current in a circuit to be measured without disturbing the circuit.

Note *There are other possibilities to measure current as well (current shunts, or Rogowski coils).*

15.2.1 Passive, single-ended voltage probes

Voltage probes divide a single-ended input signal by a specific factor.

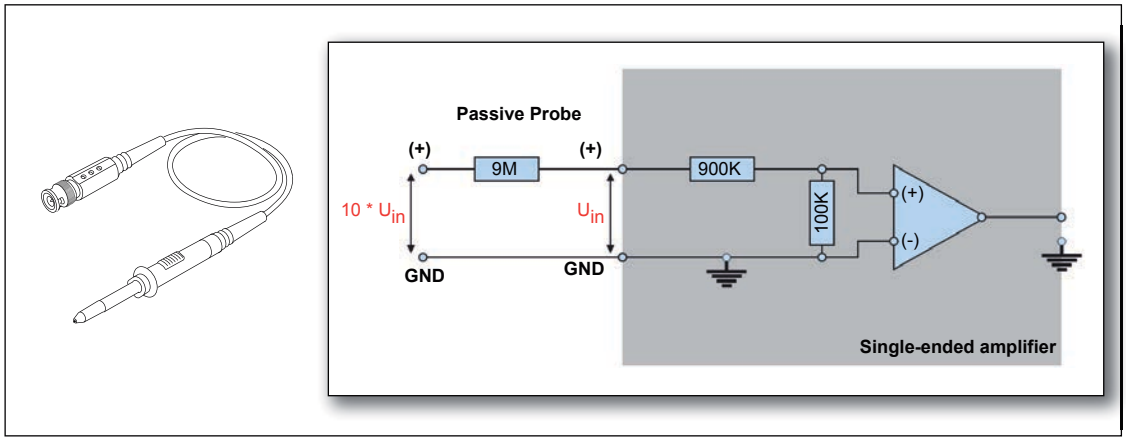


Figure 15.7: Typical example of a voltage probe

Theoretically, voltage probes are simply passive in-line resistors in series with the positive input of a single-ended amplifier. Together with the input resistor of the amplifier, they form a voltage divider so that the voltage in series with the amplifier itself is divided. As there is also a capacitive component in this divider, the input capacitance of the amplifier and the so-called “compensation range” of the probe need to match. Otherwise, signal distortion might occur.

By selecting a higher resistance probe, the divider ratio increases so that large input ranges can be achieved. Voltage probes do not provide or add either isolation or common mode voltage rejection. These probes can only be used in series with single-ended amplifiers.

Voltage probes typically decrease the overall accuracy of the system (caused by the inaccuracy of the input divider ratio formed by the external probe resistance and the internal amplifier resistance).

Table 15.1: Voltage probes overview table

Part number	Capacitive compensation range	Cable length	Divider factor	Bandwidth	Maximum input voltage
1-G901	10 - 25 pF	1.2 m	10 ± 2%	400 MHz	300 V RMS CAT II
1-G903	10 - 50 pF	2 m	100 ± 2%	400 MHz	1 kV RMS CAT II

Table 15.2: Passive, single-ended voltage probe overview

Input card	1-G901	1-G903
GN110/GN111	✓	✓
GN112/GN113	✓	✓
GN310B/GN311B		
GN610B/GN611B		
GN815/GN816		
GN840B/GN1640B		
GN8101B/GN8102B/ GN8103B	✓	✓
GN3210/GN3211	✓	
GENIS-1T/GENIS-1TM	✓	✓

15.2.2 Passive, single-ended isolated voltage probes

Passive, single-ended isolated voltage probes divide an isolated input signal by a specific factor. They are designed in an “isolated way” (like plastic BNCs to prevent users from touching the connection) so they can be used in series with an isolated unbalanced amplifier. They are called “isolated voltage probes”, although the amplifier and not the probe adds the isolation.

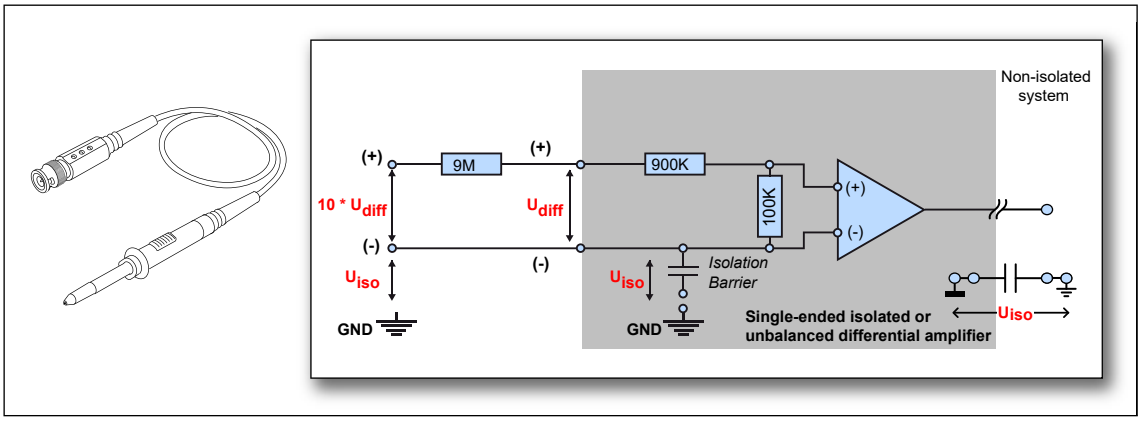


Figure 15.8: Typical example of an isolated voltage probe

Theoretically, voltage probes for isolated amplifiers are simply passive in-line resistors in series with the positive input of an isolated unbalanced amplifier as well.

Together with the input resistor of the amplifier, they form a voltage divider so that the voltage in front of the amplifier itself is divided. As there is also a capacitive component in this divider, the input capacitance of the amplifier and the so-called “compensation range” of the probe need to match. Otherwise, signal distortion might occur.

However, as the division only applies to the positive side of the amplifier input, the input range is increased while the isolation voltage remains the same as without a probe.

These probes can only be used in series with isolated unbalanced amplifiers.

Isolated voltage probes typically decrease the overall accuracy of the system (caused by the inaccuracy of the input divider ratio formed by the external probe resistance and the internal amplifier resistance).

15.2.3 Passive, differential matched isolated voltage probes

Passive, differential matched isolated voltage probes are used in series with differential amplifiers and divide a differential input signal by a specific factor.

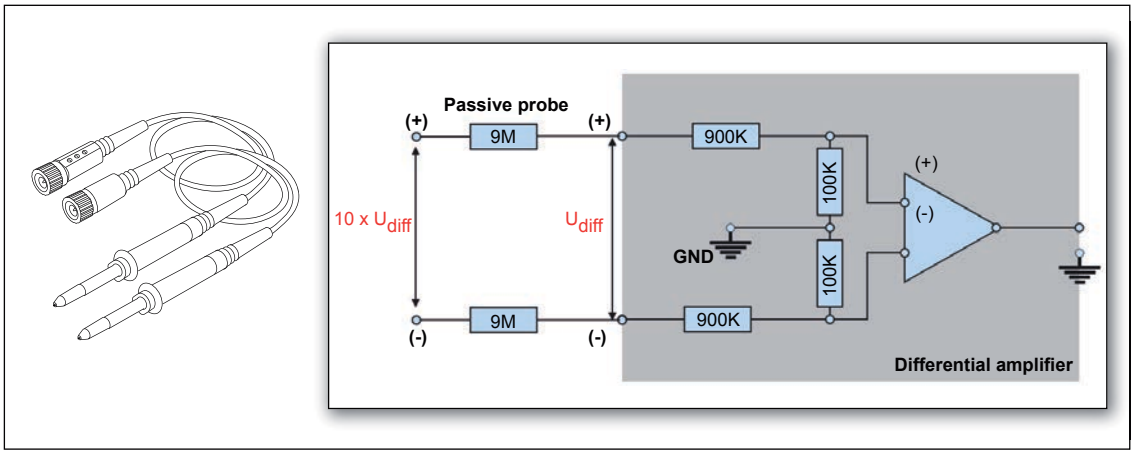


Figure 15.9: Typical example of a passive differential voltage probe

Passive, differential matched isolated voltage probes are – in theory – simply a pair of “normal” voltage probes.

They add passive in-line resistors in series with both the positive and the negative inputs of a differential amplifier. Together with the input resistor of the amplifier, they form a voltage divider on each input side so that the voltage in series with the amplifier itself is divided. As there is also a capacitive component in this divider, the input capacitance of the amplifier and the so-called “compensation range” of the probe need to match.

As two of these probes are used, one with each input terminal, the probes themselves need to “match” as closely as possible. Otherwise, the two input terminals are divided differently. Therefore, the probes are typically manufactured (and sold) in pairs and called “matched”. By selecting higher resistance probes, the divider ratio increases so that large input ranges are possible. Passive, differential matched isolated voltage probes typically decrease the overall accuracy and the CMRR of the system.

15.2.4 Active differential voltage probes

Active differential voltage probes are battery-powered, differential amplifiers in series with any input amplifier in single-ended mode.

Figure 15.10: Typical example of an active differential voltage probe

The achievable input range and accuracy depends on which active differential probe is used. Active differential probes can be used in series with virtually any amplifier, their performance typically is limited. The fact that they are usually battery-powerd may cause some inconvenience, as battery maintenance is required.

Active differential voltage probes typically decrease the overall accuracy of the system. The active output enables the use of the probe with (almost) any type of input.

Table 15.3: Active differential voltage probes

Part number	Capacitive compensation range	Cable length	Divider factor	Bandwidth	Maximum input voltage
1-G909	n/a	0.9 m	20 ± 2%	25 MHz	140 V RMS 140 V DC
			200 ± 2%	25 MHz	1.0 kV RMS 1.4 kV DC

15.3 Probe bandwidth calibration

A probe makes a physical and electrical connection between a test point or signal source and the instrument. Depending on the measurement needs, this connection can be made with something as simple as a length of wire or with something as sophisticated as an active differential probe.

For the purpose of this document, we only describe attenuating probes within two categories: 1X Probes and 10X Probes.

15.3.1 1X Probes

1X probes, also known as 1:1 (one-to-one) probes, simply connect the input of the instrument to the circuit being measured. They are designed for minimum loss and easy connection. Figure 15.11 shows the circuit diagram for an instrument input connected to a circuit under test. The circuit under test is modeled as a voltage source with a series resistor. The 1X probe (or cable) introduces a significant amount of capacitance that appears in parallel with the input of the instrument. A 1X probe may have around 40 to 60 pF of capacitance.

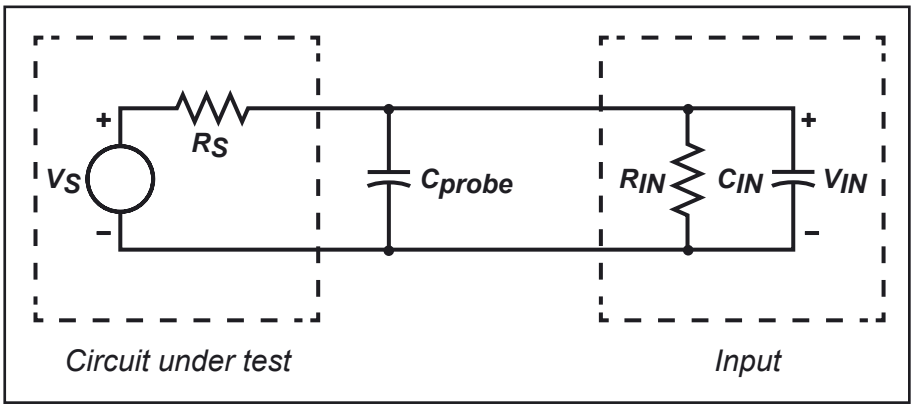


Figure 15.11: Input connection using a 1X probe

The impedance of the circuit and the input impedance of the instrument produce a lowpass filter. For very low frequencies, the capacitor acts as an open circuit and has little or no effect on the measurement. For high frequencies, the capacitor's impedance becomes significant and reduces the voltage detected by the instrument. Figure 15.12 shows this effect in the frequency domain. If the input is a sine wave, the amplitude tends to decrease with increasing frequency and the phase is shifted.

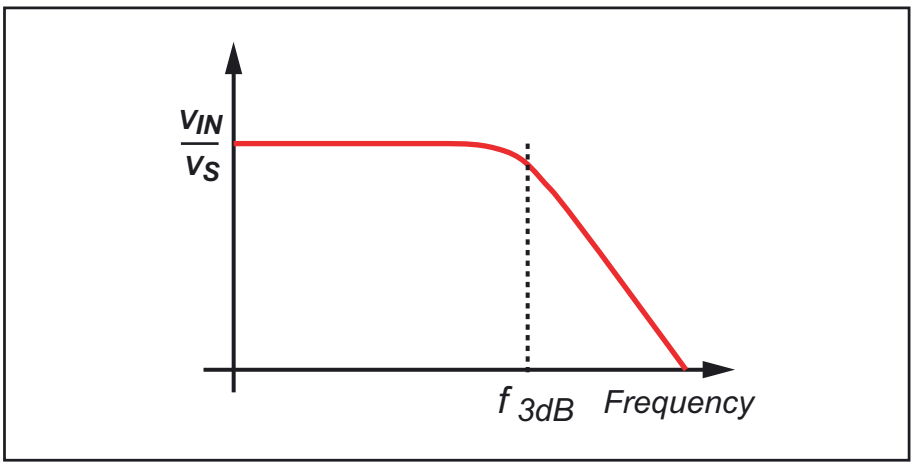


Figure 15.12: Frequency response with 1X probe

Example: Assuming that the voltage source has a 1 MΩ resistance and the 1X probe has a 50 pF capacitance (a 1X probe has no resistance by itself), the universal amplifier input would have a 1 MΩ resistance and a 100 pF capacitance.

This yields a -3dB point at:

(EQ1)

$$f(\text{-}3db) = \frac{1}{2\pi(R_s \| R_{IN})\ (C_{IN}+C_{probe})}$$

= 1 / (6.28 x 500 E+3 x 150 E-12) ≈ 2 kHz

The loading due to the input impedance of the instrument and the probe capacitance is twofold: resistive loading and capacitive loading.

The resistive loading actually reduces the voltage delivered to the instrument:

(EQ2)

$$V_{IN} = V_S\left(\frac{R_{IN}}{R_{IN}+R_S}\right)$$

The effect of the capacitive loading is more complex and results in an exponential response in the voltage:

(EQ3)

$$V_{IN}(t) = V_{MAX}\left[1 - e^{-t/(R_S C_{in\ +\ probe})}\right]$$

15.3.2 10X Probes

10X probes (also called 10:1 probes, divider probes, or attenuating probes) have a resistor and capacitor (in parallel) inserted into the probe.
Figure 15.13 shows the circuit diagram for the 10X probe connected to a high-impedance input of an instrument.

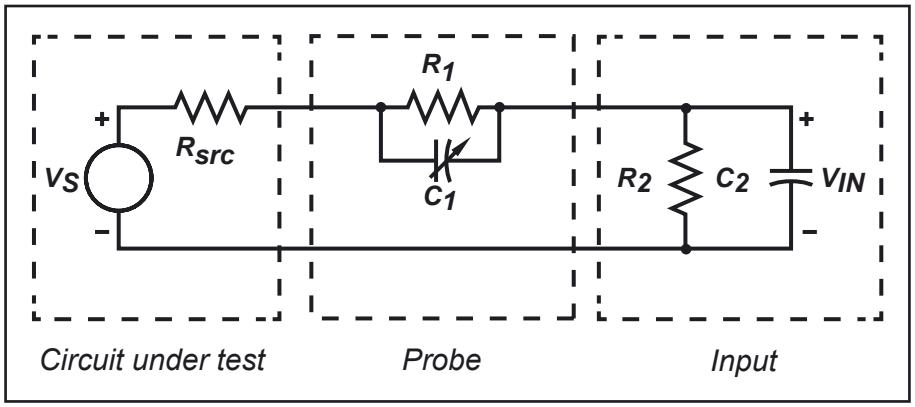


Figure 15.13: Input connection using a 10X probe

Assuming that R_{src} is low compared to R_1 and that $R_1 * C_1 = R_2 * C_2$, then the effect of both capacitors cancel each other out in this circuit. The capacitor is usually adjustable and can be tweaked for a nearly perfect match. In these conditions, the relationship of VS to VIN is:

(EQ 4)

$$V_{IN} = V_S\left(\frac{R_2}{R_1 + R_2}\right)$$

R_2 is the input resistance of the instrument's high input impedance (1 MΩ) and $R_1 = 9 * R_2$. Using the previous equation, this results in:

(EQ 5)

$$V_{IN} = \left(\frac{1}{10}\right)V_S$$

The final result is a probe / instrument input combination that has a much wider bandwidth than the 1X probe due to the effective cancellation of the two capacitors. However, the instrument now measures only one-tenth of the original voltage (hence the name 10X probe). The circuit being measured is affected with a load impedance of $R_1 + R_2 = 10$ MΩ, which is much higher than with the 1X probe.

IMPORTANT

To perform the compensation correctly, both impedances must have the same value, i.e. $R_1 * C_1 = R_2 * C_2$. In practice, $R_1 * C_1$ will never be equal to $R_2 * C_2$, but the values can be approximated. The probe's compensation capacitor is usually adjustable somewhere between 10 pF and 50 pF to compensate for the instrument's input capacitance. Since the Universal Amplifier has a 100 pF capacitance, the compensation cannot be performed correctly with standard probes. Therefore, the probe capacitance must be adapted to this situation. Various probe manufacturers offer the possibility to purchase probes with other compensation ranges on request.

15.3.3 Probes and differential measurements

Connecting the differential amplifier or probe to the signal source is generally a major source of error. To maintain the input match, both paths should be as identical as possible. Any cabling should be the same length for both inputs. If individual probes are used for each signal line, they should be the same model and have the same cable length. When measuring low-frequency signals with large common mode voltages, avoid the use of attenuating probes. At high gains, they simply cannot be used as it is impossible to balance their attenuation precisely. When attenuation is needed for high-voltage or high-frequency applications, special passive probes designed specifically for differential applications should be used. These probes have provisions for precisely trimming the DC attenuation and AC compensation. To get the best performance, a set of probes should be dedicated to each specific amplifier and calibrated with that amplifier using the procedure included with the probes.

15.4 Current shunt measurements

Special care must be taken with shunt measurements. Typical shunt measurements generate signals with an amplitude of only a few volts or even mV. To prevent interference from higher voltage signals (up to 100 V), the following guidelines apply:

- Use only coaxial cables for all measurements.
- If possible, place the instrument as close as possible to the test object to reduce the length of the coax cable.
- Physically separate the low voltage signal lines from the high voltage signal lines as much as possible. Do not combine them. When the high voltage signals include high frequency transients, these will easily cross over to the low voltage signals.

HINT/TIP

The GEN DAQ series instruments typically have a very high bandwidth. Potential higher frequency transients are measured as a result of the high bandwidth. Using other lower bandwidth equipment can not measure these results. Use a filter on the acquisition card to reduce the bandwidth to a physically relevant value.

A Maintenance

A.1 Preventive maintenance

Regularly scheduled HBM preventive maintenance services that include cleaning, adjusting, inspection and calibration will help to:

- Assure that the instrument is available whenever it is needed
- Maintain optimum performance
- Avoid expensive unplanned downtime and repair

Also, regularly scheduled maintenance is a predictable expenditure.

Except for the batteries, the instrument is a maintenance-free product; no preventive maintenance is required.

Inspect the instrument's batteries at least twice a year, but preferably every month. Damaged batteries and batteries with reduced capacity should be replaced to meet the batteries' specified capacity and consequently the instrument's specified run-time using the battery. The main benefit of this inspection will result in reliable use of the instrument.

If the instrument has been stored for four weeks or longer, first inspect the battery before putting the instrument back to use.

How often preventive maintenance needs to be performed depends on your application, workload, and regulatory requirements.

A.2 Preventive drive replacement

When installed in the instrument, the drive is the "data center" of the instrument. It contains all of the programs and recorded data. The CPU may be the "brain" of the system, but the drive is its memory and personality; it is what makes the instrument what it is.

CAUTION

Do not to exceed the drives warranty period.

Contact HBM service for more details.

A.2.1 Hard disk drive

The reliable service life of a typical hard disk drive is around three to five years. Some drives work for a decade or longer, but every year that passes after three years increases the chances of a failure.

If the instrument uses a hard disk drive, HBM therefore advises replacing it at least every two years to prevent loss of data or inactivity of the instrument.

Note *This recommendation is based on 24/7 use of the instrument at full drive write speeds. Reduced use of the instruments drive allows for a longer replacement period.*

A.2.2 Solid State Drive (SSD)

Solid State Drives have no mechanical parts that can fail. However, each block of data on a Solid State Drive can only be erased and written a defined number of times before the data block fails. The Solid State Drive manages this limitation so that drives can last for many years with normal use. Very intensive use of the Solid State Drive to record and store new data will shorten the drive's life expectancy.

The reliable service life of a typical Solid State Drive drive is around three to five years. Some drives work for a decade or longer, but every year that passes after three or so increases the chances of a failure.

If the instrument uses a solid state drive, HBM therefore advises replacing it at least every two years to prevent loss of data or inactivity of the instrument.

Note *This recommendation is based on 24/7 use of the instrument at full drive write speeds. Reduced use of the instruments drive allows for a longer replacement period.*

A.3 Preventive air filter replacement

The GEN17tA is equipped with an air filter to keep unwanted particles from collecting inside the GEN17tA. The air filter needs to be cleaned and replaced regularly, since particles collect in the air filter and can reduce the airflow through the air filter, thus negatively influencing the cooling capacity of the GEN17tA.

WARNING

Do NOT wash the filter, any residual moisture will be blown inside the instrument and can harm the sensitive electronics.

IMPORTANT

In high availability products such as GEN DAQ series systems, equipment maintenance is critical. Filters loaded with dust not only reduce airflow, they can also cause electronics to run inefficiently and promote equipment failure.

There are a number of industry best practices for timely filter maintenance as unique equipment and varying operating conditions preclude a simple, one-size-fits-all answer for equipment maintenance. For clean, controlled, indoor environments such as data centers or offices, filters are often replaced according to a maintenance calendar with all filters replaced three to four times per year.

Specialized equipment and equipment operating in uncontrolled environments often use sensors to define when maintenance should be performed. Temperature, pressure, and airflow sensors are used to determine when equipment is outside of optimal operating parameters and a service alert is triggered. GEN DAQ series system are equipped with temperature sensors and variable FAN speeds. If either the FAN speeds or temperatures are abnormally high immediately replace the air filter.

IMPORTANT

To prevent unexpected failures it is recommended to replace the air filters at least once every year.

A.4 Cleaning

To clean the instrument, disconnect all power sources. Lightly wipe the surfaces with a clean, soft cloth dampened with water.

Insert the new filter and close the GEN17tA air filter section in reversed order.

B Service Information

B.1 General - Service Information

HBM offers comprehensive factory servicing for all HBM Data Acquisition products. Extended warranties for calibration, repair or both are available. Installation, on-site or factory training are also available. Contact the factory or local sales person for more information. For local contact information, visit www.hbm.com/support.

If servicing is needed on the equipment, contact the factory with the model and serial numbers, a description of the problem, and your contact information. A Return Material Authorization (RMA) number will be issued. Attach this number and the accompanying paperwork to the unit.

During the warranty period, the customer pays for shipping to HBM. HBM pays to return the equipment in the same fashion as it was received. Outside of the warranty period, a quote for the shipping costs is issued. A purchase order must be received before work can be performed.

It is recommended that the unit always be shipped in the original shipping container.

For the frequent shipping of some products, HBM offers hard shipping containers specifically designed for frequent transportation.

B.2 Calibration/verification

The GEN series Data Acquisition System is factory calibrated when delivered to the customer. Swapping, replacing or removing the cards may result in minor deviations to the original calibration. HBM recommends that the GEN series system should be tested and, if necessary, calibrated once a year or after any major event that may affect calibration. When in doubt, consult your local supplier.

C Trouble-shooting

C.1 GEN17tA is not detected

E.g.: Ethernet connected mainframe not found on network
If the mainframe is not detected by Perception, follow the steps below to determine the cause of the problem and follow-up measures. Each numbered item in the flowchart (see Figure C.1) is explained in detail later.

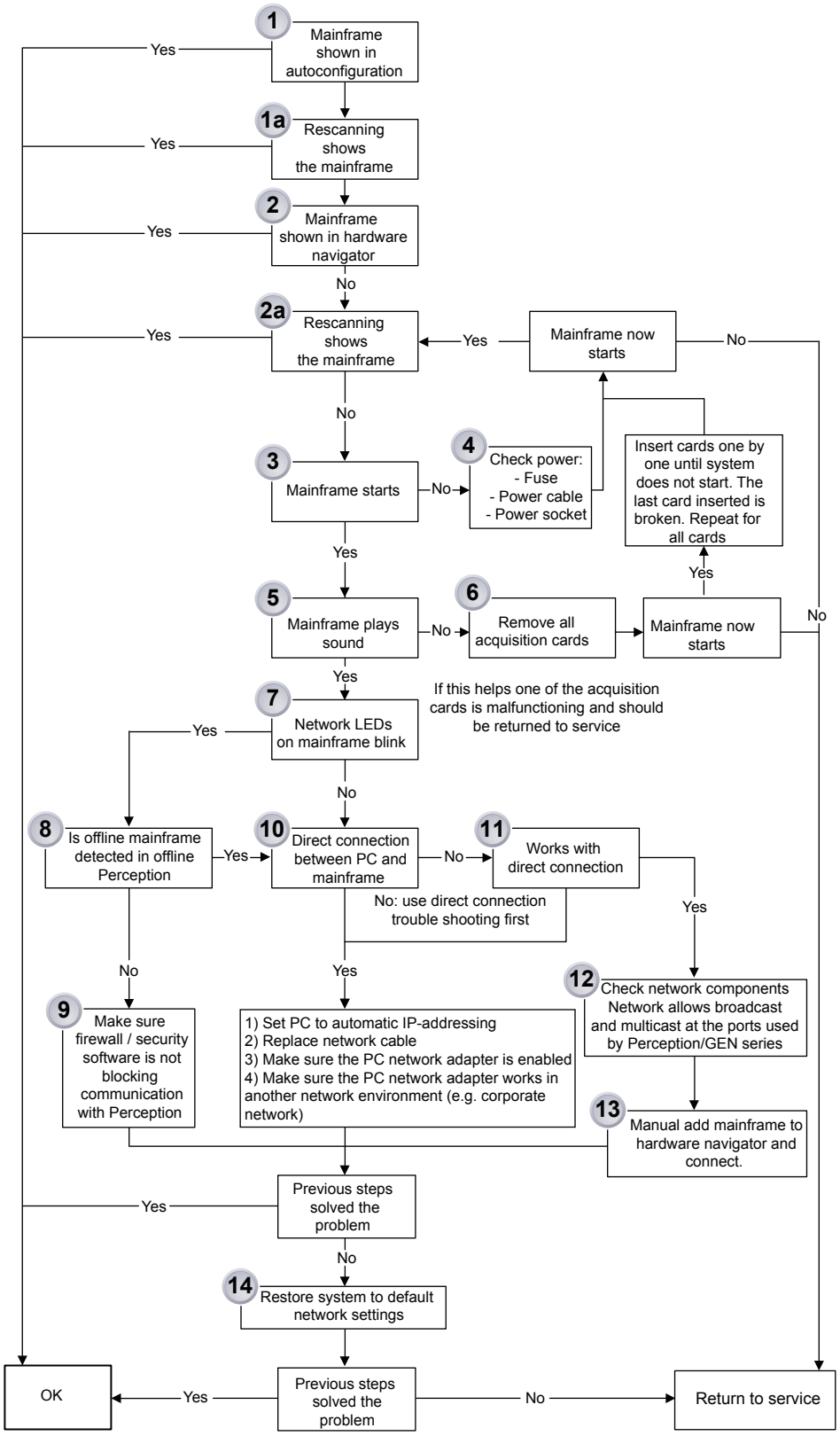


Figure C.1: Mainframe not detected - Error tracking

Detailed description about the numbered items:

1 Mainframe shown in auto-configure mainframe connection dialog.

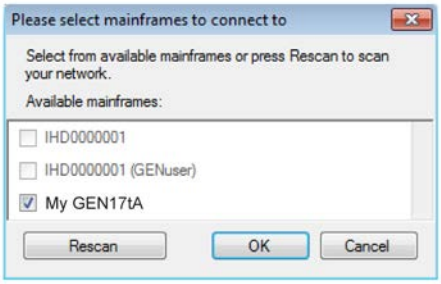


Figure C.2: Mainframe selection dialog

1a Press the **Rescan** button on the dialog above (see Figure C.2) to initiate a new network search for the mainframe. Typically, the mainframe should appear within a few seconds.

2 Mainframe shown in hardware navigator
Perception will show the mainframe in the unused hardware section of the hardware navigator if it detects the mainframe on the network.

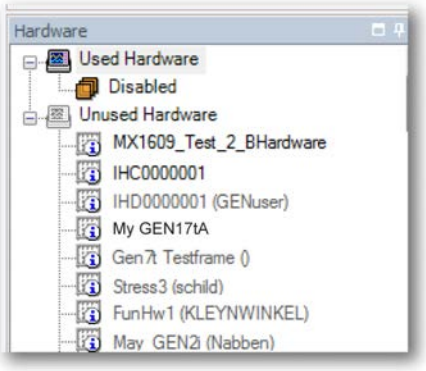


Figure C.3: List of unused hardware

2a If the mainframe is not shown in the list of unused hardware, make sure it is powered on. Use the right click menu on **Unused Hardware** and select **Scan for Mainframes**.

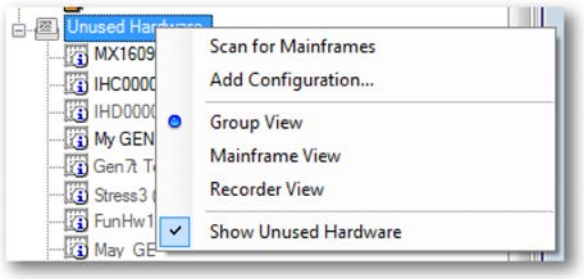


Figure C.4: Unsed hardware context menu

3 To determine if the mainframe starts, turn the unit off and back on. Then observe the following items (may differ depending on the type of mainframe)

a Fans start

b LEDs on mainframe are turned on or blink

4 Check power

a Check 220 V/110 V setting

b Check the power cable

c Make sure the power socket correctly powers another device

d Check fuse

5 If the mainframe is fully booted, it will play a 3-tone confirmation sound.

6 Remove the acquistion cards. For more information, please refer to "Removing and installing input cards" on page 92.

7 On the Interface/Controller module of the mainframe look for the network connectors. For more information, please refer to "Communication and control" on page 142.

8 For more informationon how to start and use the offline setup and configuration manager, please refer to the I2689 Perception User Manual, Appendix C.
Use the example setup installed with Perception for this test to make sure the hardware in the setup is supported and properly configured. The example setup can be found in: “My Documents\My Offline Configuration” and is named “Example.pOfflineConfig”.

9 Contact your system administrator. Make sure Perception is not blocked by anti-virus or network protection software.

10 When troubleshooting connection problems, first make sure that the basic connection is working by connecting the mainframe to the GEN series mainframe directly using only an UTP or SFP cable.

11 If the mainframe is detected in a direct connection setup, there are a number of potential problems in the network that can prevent the mainframe from communicating with Perception. Most likely, one of the network components in the connection from Perception to the mainframe is either incorrectly configured or broken. Ask the network administrator to determine the cause of the problem.

12 Perception/GEN series use a number of multicast and broadcast ports and addresses to allow detection of the mainframe in the network. These ports and addresses should be open for communication in the network. A detailed overview of the ports and addresses used can be found in "Network protocols and ports" on page 143.

13 For more information, please refer to the I2689 Perception User manual: Chapter “Data Sources navigation”, topic “To add an unlisted system”

14 To restore a GEN17tA to its default network settings, follow the steps in chapter "Restore default network settings" on page 91.

C.2 Embedded Software upgrades

When a new version of Perception is installed, the embedded software of the mainframes is automatically updated when Perception connects to the mainframe.

Note *Some upgrades may take more than ten minutes.*

IMPORTANT

Do not power off the mainframe, do not disconnect network cables and do not shut down Perception during an embedded software upgrade.

When the software upgrade process does not complete within 30 minutes, power off the mainframe by keeping the Power-On button pressed for five seconds. Wait for 30 seconds and turn the unit back on.

Wait until the unit has completed the boot process. If the new software version is booted, Perception will connect and start using the mainframe as normal. In rare cases, the upgrade might have failed. This could result in:

- The mainframe using the old software.
- The mainframe using the “minimum mode” software.

In both cases, Perception software will automatically detect an old software version during the connection attempt and will restart the upgrade procedure.

In the very unlikely event that the mainframe does not reboot, turn the unit off again and retry the boot process. If the mainframe keeps failing to boot, contact your HBM service agent for enhanced support.

C.2.1 Boot recovery switch

In the very unlikely event the GEN DAQ mainframe fails to boot correctly and/ or a firmware update is not possible, the mainframes supports a minimum boot mode recovery switch.

IMPORTANT

Use this switch only when instructed by HBM support. The GEN DAQ mainframe normally should boot in the recovery mode automatically whenever the normal boot fails.

When instructed to use the minimum boot mode switch:

1 Power off the mainframe and remove the power cord.
2 Remove all acquisition cards to allow access to the mainframes backplane
See "Removing and installing input cards" on page 92 for more details.
3 Locate the boot mode switch **(A)** on the mainframes backplane.

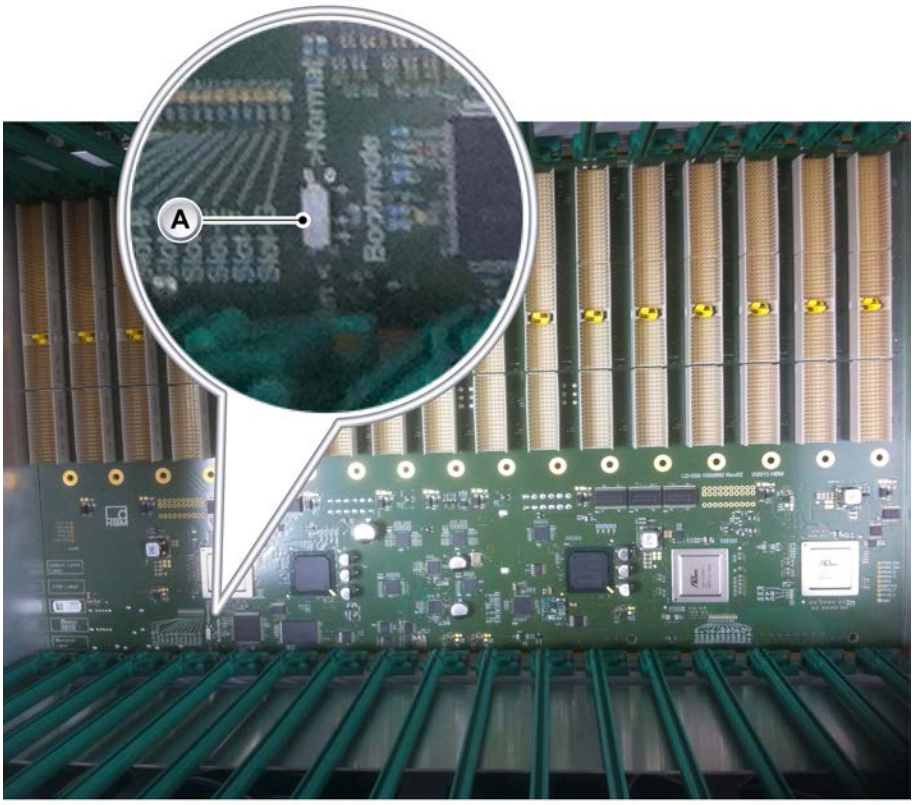


Figure C.5: Location of boot mode recovery switch

Note *Details might look slightly different depending on mainframe version.*

4 To enable the recovery mode, use a pointy object (e.g. screwdriver) and move the lever to the side labeled **Min**.

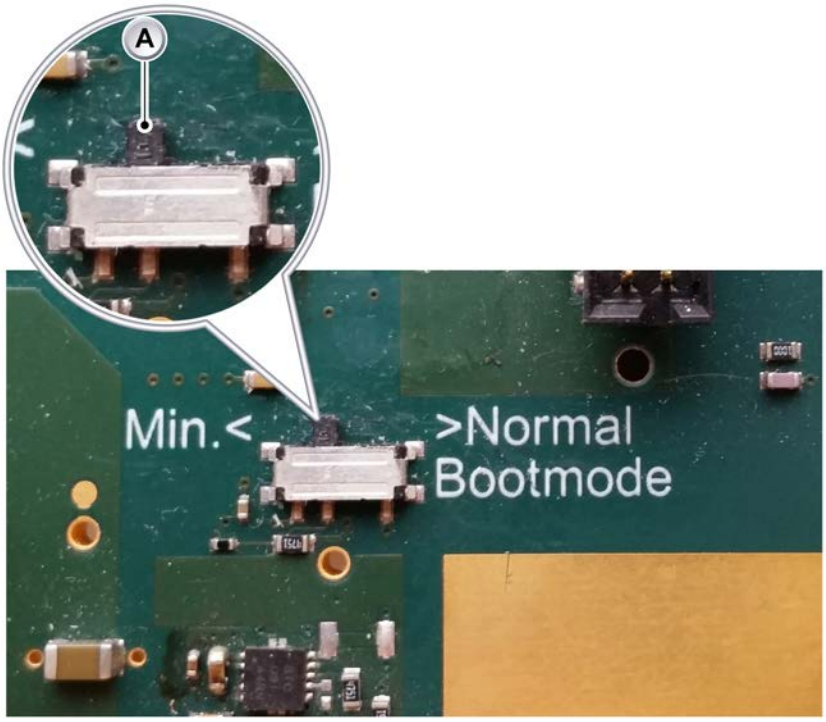


Figure C.6: Lever to switch the boot mode

A Lever

5 Re-insert all acquisition cards.
6 Insert the power cord and power on the mainframe.
7 Use Perception software to perform a firmware upgrade.
8 When Perception completes the mainframe will automatically reboot.
9 When reboot is completed power off the mainframe and remove the power cord.
10 Remove all acquisition cards to allow access to the mainframes backplane.
11 Shift the black lever to the side labeled **Normal**.
12 Re-insert all acquisition cards.
13 Insert the power cord and power on the mainframe.

The GENDAQ mainframe should now work in normal mode.

Note *If the mainframe still fails to work correctly after this recovery process the unit must be send back to HBM service for a repair.*

C.3 Unexpected mainframe shutdown

If the mainframe has shut down unexpectedly, this can have several causes:

- **Power interruption**
  - Check if the mains cable is still firmly connected.
  - Check if other devices on the same mains group have experienced a power interruption.
- **Over-temperature or over-voltage:**
  - If this happens while Perception is connected, a message is shown that tells the reason for the shutdown. Apart from that, a message is shown when connecting the next time, even if Perception was not connected at the time of the shutdown.
  - If the cause was over-temperature, please check the airflow around the mainframe; the mainframe must be able to attract cool air to avoid over-heating.
  - If the cause was over-voltage, please contact HBM service.

C.4 The Master/Sync connection does not synchronize

If this happens, check the following:

- Check whether the Master/Sync mode setting for each mainframe matches the role of that mainframe. There should be one (and only one) Master and one or more Sync mainframe(s).
- Check the optical Master/Sync cables. Both LEDs at the connector should be lit.
- Verify the cable type. The Master/Sync cables should be Multi Mode, 850 nm optical cables.
- Very long cables and optical couplers in the cable degrade the optical signal. For information on how to calculate optical losses, please refer to the chapter "Calculating maximum fiber cable length" on page 479.
- The optical connections should not be damaged and should be free of dust and lint.

C.5 Optical Network (SFP)

If no connection is present on the fiber optic channel, first check the following:

1. Check whether the **cable wavelength** and **SFP module wavelength** are the same.
   Check the wavelength printed on the label of the SFP module with the specification of the cable used.
2. Check whether the communication speed at both ends of the fiber optic connection are the same.
3. Inspect the cable and connectors for any possible faults or breaks that could impede communication.
4. The optical connections should not be damaged and should be free of dust and lint.

C.6 Master/Sync connection verification procedure

To verify the correct operation of the Master/Sync configuration, proceed as follows:

Hardware setup

1. Set up two GEN series mainframes, each with at least one recorder card installed.
2. The system synchronization connector can be used.
3. Connect a TTL level, 1 Hertz signal to the top input in the first recorder card of the master mainframe and to the top input in the first recorder card of the Sync mainframe.
4. Switch on both GEN series mainframes and wait until they have completed the boot process.
5. Using the fiber optic cable, connect any Master/Sync card's connector of the master mainframe to Master/Sync card's top connector, labelled **M/S IN**, of the Sync mainframes using the Master/Sync synchronization connector.
6. Check if both LEDs on both Master/Sync cards are illuminated green. Check the LEDs near the Master/Sync connection connector.

Software setup

1. If it is not already active, start Perception.
2. In the start dialog, select **New blank experiment**.
3. Make sure you are connected to the required mainframes. Use the *Hardware Navigator* to do this.
4. In the **Settings** sheet, go to the **General** group in the task pane and select **Mainframe**. A list of available mainframes is displayed in the settings area.
5. Set the master mainframe operating mode to Master in the **Master/ Sync mode** column.
6. Set the Sync mainframe operating mode to Sync in the **Master/ Sync mode** column.
7. The Sync mainframe will now be synchronized to the master mainframe. The status palette will show a box with the synchronization status of the Master/Sync system. This box is labelled **SYNC**.

8 The synchronization status will first be **Synchronizing** for up to three minutes before becoming **Synchronized**.

Figure C.7: Master/Sync Synchronizing

Figure C.8: Master/Sync Synchronized

9 In the **Settings** sheet, go to the **Trigger** group in the task pane and select **Channel**.

Making a multi-mainframe recording

1 Wait for the “Master/Sync” status to display **Synchronized** before proceeding to the next step.

Figure C.9: Master/Sync Synchronized

2 Press **Run** in the acquisition control panel to start a recording.
3 The signal on the master mainframe will now generate a trigger event. This trigger event will be relayed to the Sync mainframe.
4 The recording will now show the rising edge of the TTL level 1 Hertz signal recorded by the master mainframe and the Sync mainframe.
5 The recordings in both mainframes are started at the same time.
6 All recorded signals will match in time to within ± 150 ns.

If all signals match in time, the recordings were completed successfully.

C.7 CAN Trouble-shooting

USB to CAN FD Converter is not visible	
Situation	• The USB to CAN FD Converter is not visible in the hardware tree • Not possible to select any channel for Publishing to CAN
Cause	• No USB to CAN FD converter is connected to the GEN series mainframe or the converter is connected after it was booted and the mainframe was not restarted.
Solution	**1** Connect a USB to CAN FD Converter to the GEN series mainframe. **2** Reboot the GEN series mainframe **3** Reconnect again to see if the USB to CAN FD Converter is visible in the hardware tree (see Figure 11.53 on page 211) and channels can be selected for Publishing to CAN.

Problems with signal for Publishing to CAN	
Situation	• It is not possible to select a certain signal for Publishing to CAN.
Cause	• Signal has a result type that cannot be published. Only results of RT-FDB formulas with the result type “Scalar” and/or “‘Async”’ can be published on the CAN bus.
Solution	**1** With the use of RT-FDB a CycleDetector together with a Cycle function can be used to create an “Async” result using “Sync” input. **2** This “Async” result can be published on the CAN bus.

CAN bus: data problems	
Situation	• The GEN series mainframe is configured to output signals on the CAN bus, but data is not present, or not present correctly on the CAN bus.
Cause	• The bus is not terminated correctly. • The bus-mode, bitrate(s) and/or endianness does not match the settings of the bus. • Configured CAN message IDs are not unique and used by other devices on the bus.

CAN bus: data problems	
Solution	**1** A high speed CAN bus is normally terminated with 120 Ω at both ends, see Figure C.10. Termination can be done in the cable connector or with a CAN terminator dongle. **2** Select the correct CAN bus settings in the CAN bus setup dialog (see Figure 11.49 on page 206). **3** Change the CAN message ID of the signals that are published by the GEN series mainframe (see Figure 11.47 on page 204) or the CAN message ID of the other device on the bus.

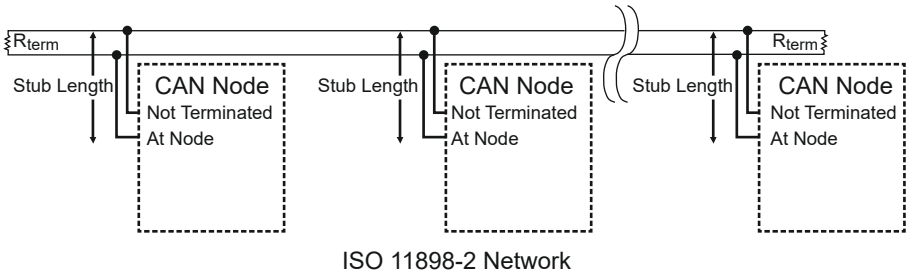


Figure C.10: CAN bus termination

C.8 IRIG GMR1000 Trouble-shooting

HINT/TIP

In case the information in this chapter does not solve the problem, call your local HBM Support group.

Note *The PTP settings used in this document are displayed only in the **Advanced** settings mode of Perception.*

To open the **Advanced** settings do the following:

1. Open the settings sheet
2. In the main menu select **Settings**.
3. In the Settings menu select **Show Settings ►**.
4. In the submenu select:
   - **Basic:** this will show only the relevant settings
   - **Advanced:** this will show all settings

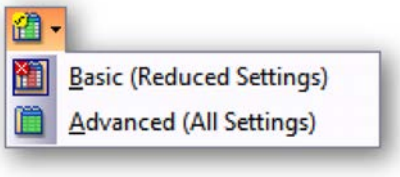


Figure C.11: Perception settings sheet options

How to check synchronization

The synchronization status is displayed in the status window of Perception: When IRIG GMR1000 is selected, the system status goes through the following states:

- No signal
- Out of sync
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

Note *The system status returns an overall status for all connected mainframes. To determine which mainframe(s) is causing problems, please see "Finding the system that is causing the problems" on page 410.*

The state remains at “NO GMR1000”	
Category	**Description**
Cause	This problem is caused because the mainframe is synchronizing to a PTP master other than the GMR1000.
Solution	Check the GMR1000 and network peripherals.
Recording	When starting a recording the mainframes that are in the state “NO GMR1000” try to follow the signal from the PTP grandmaster they did find. The time used in the recording is undetermined. The PTP settings can be used to determine the synchronization source. If the PTP Role is Master, the mainframe has become the master in the PTP network. If the PTP Role is Slave, the PTP Master MAC-address can be used to determine which node in the network is the PTP master. In-depth knowledge of networking is required to obtain this information.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “Coarse”	
Category	**Description**
Cause	A network switch is causing jitter on the PTP timestamps in the network.
Solution	Increase the PTP Accuracy, see chapter "Checking the Perception setup" on page 410
Recording	When starting a recording the mainframes are typically **not** synchronized within the specified accuracy. The samples at the start of the recording are expected to be synchronous within 10 times the specified accuracy, but may drift apart as the recording proceeds depending on the cause of the problem.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

Finding the system that is causing the problems

The status described in the previous section is an overall system status showing the most important status in the system. To verify the synchronization details per mainframe, please refer to the chapter "System topology" on page 363.

Checking the Perception setup

The following settings can all be found in the Perception Settings (see Figure C.12).

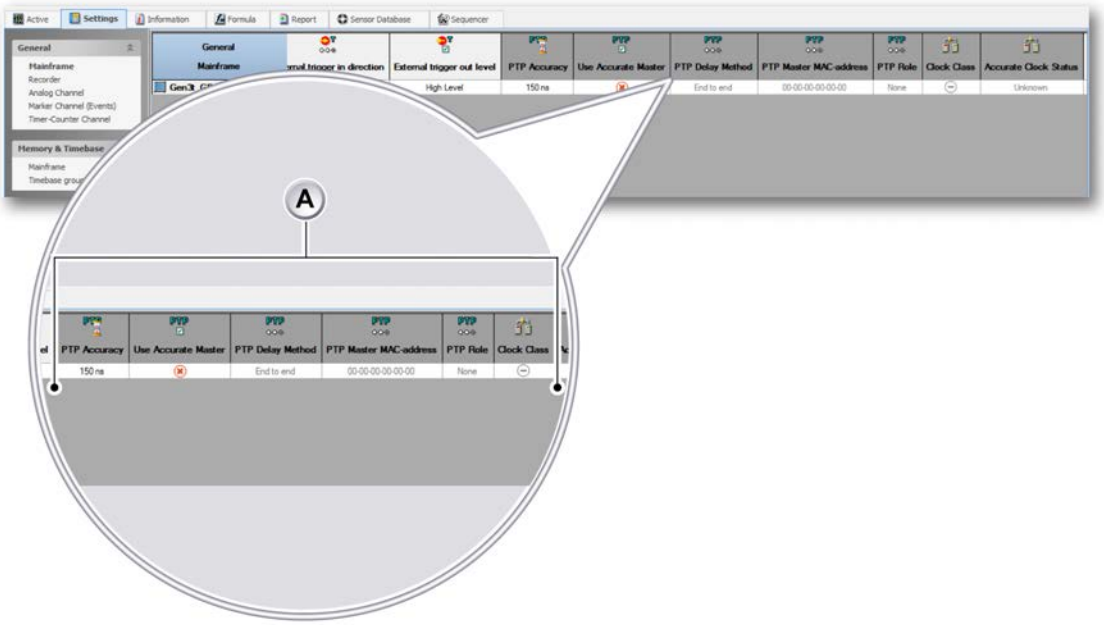


Figure C.12: Perception General Mainframes settings

A PTP related settings in Perception General Mainframes settings

Sync source	
Network port used	**Sync source setting**
RJ45	IRIG GMR1000 (PTP1 RJ45)
Optical 1 Gbit	IRIG GMR1000 (PTP2 SFP)

PTP Accuracy
This is set to a fixed value because of the nature of the IRIG synchronization signal jitter. **Note** *This setting only needs to be changed if a network switch without PTP support is being used and more jitter is acceptable.* **Note** *Interaction between different time synchronization types in complex set-ups may induce a fixed accuracy.*

Use Accurate Master
Ensure that “accurate master”’ setting is disabled.

PTP Role (read-only)
Verify that the PTP Role is slave. If Master is listed in this column, the GEN series mainframe itself is the master rather than the GMR1000.

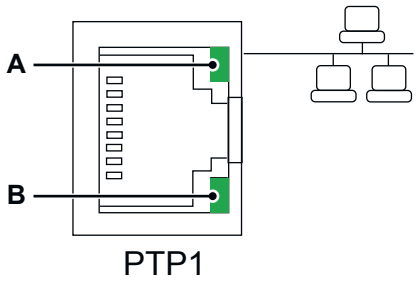
Clock Class
The clock class should be 13 (GPS clock class if the GPS antenna is synchronized).

Note *If the clock class is 14, IRIG is not locked and the GMR1000 runs on its internal clock.*
If the clock class is 52, the GMR1000 was never synchronized.

PTP Master MAC-address
This is the GMR1000 MAC-address, or the boundary clock MAC-address when boundary clocks are used.

Verify the GEN series network port

The following section explains how the LEDs on the ports can be used to diagnose system synchronization problems. The images herein are schematic, for actual port images and positioning of the ports in the system, refer to appendix “PTP Synchronization” on page 455.

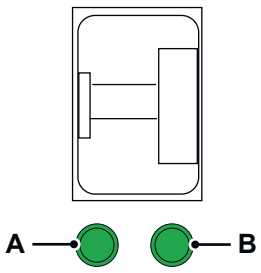


A Activity LED RJ 45 network (blinking)

B Link speed RJ45 network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	**1** Make sure the PoE injector is powered by checking the power LED. **2** Make sure PoE injector IN and OUT are correctly connected. **3** Replace the cables used to verify the cables are not causing the problem.(1)
100 or 10 Mbit/s network connection	ON	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
100 or 10 Mbit/s network connection	Blinking	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
1 Gbit/s network connection	ON	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.
1 Gbit/s network connection	Blinking	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.

(1) **Note** *In case the problem remains unsolved, contact HBM service.*



PTP2

A Activity LED optical network

B Link speed LED optical network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	Refer to the “Verify SFP PoE injector” section (see details on page 415). If no problem is found, swap the SFP with the SFP in the PoE injector and retry. If a problem occurs now it is related to the SFP, contact HBM Service for information on how to replace it. **Note** *In case the problem remains unsolved, contact HBM service.*
100 or 10 Mbit/s network connection	ON	OFF	See section "Optical Network (SFP)" on page 402 for additional checks.
100 or 10 Mbit/s network connection	Blinking	OFF	See section "Optical Network (SFP)" on page 402 for additional checks.
1 Gbit/s network connection	ON	ON	This is expected.
1 Gbit/s network connection	Blinking	ON	This is expected.

Checking the SFP PoE injector

The “PoE injector LEDs trouble-shooting diagram” helps to determine the connection problems (see Figure C.14).

The LED names that are referenced in the diagram can be found on the front of the device (see Figure C.13).

PoE injector LEDs

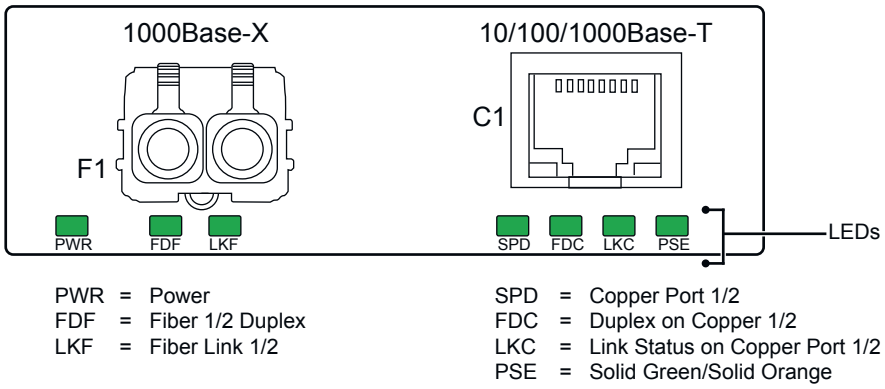


Figure C.13: Power over Ethernet injector LEDs details

Checking the PoE injector LEDs

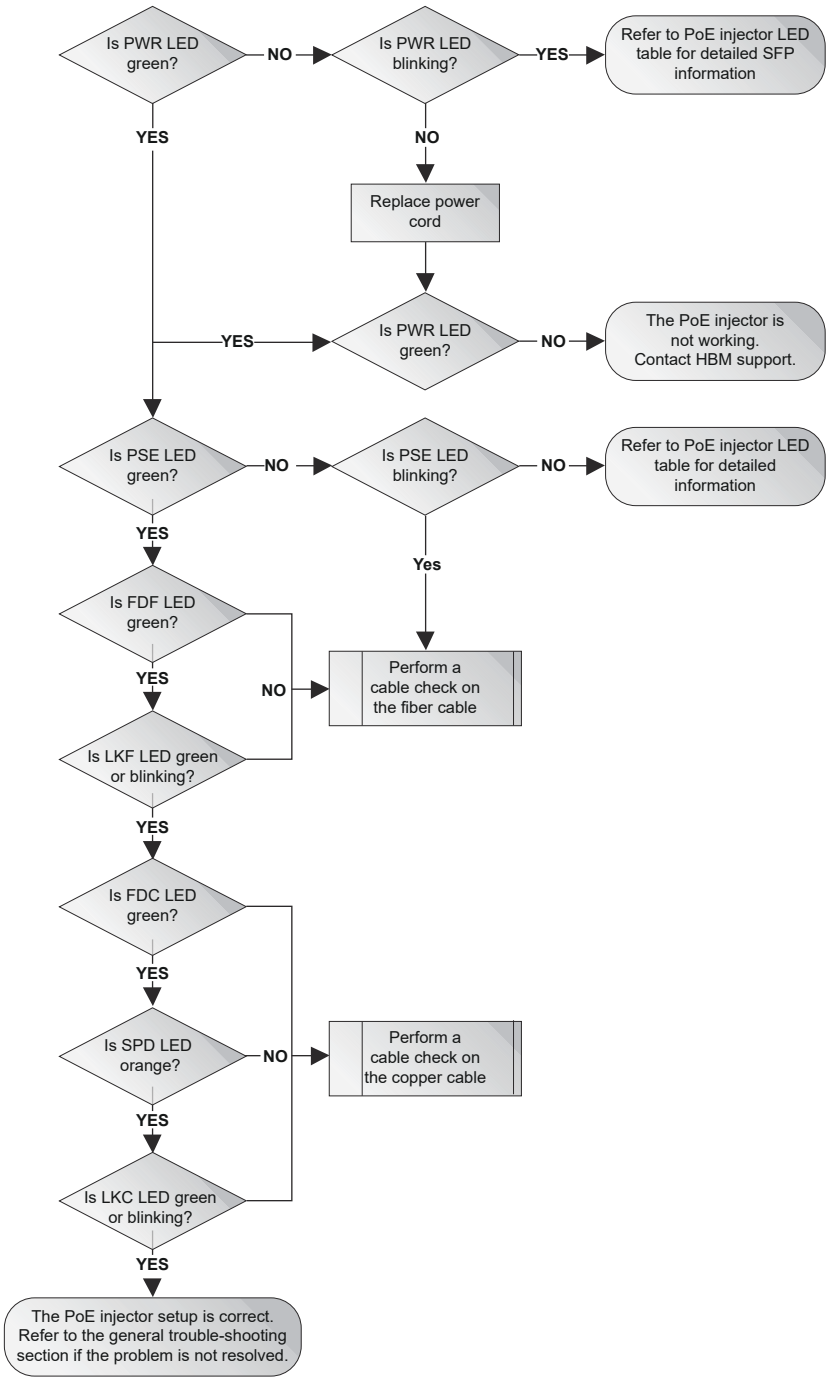


Figure C.14: PoE injector LEDs trouble-shooting diagram

Checking PoE injector cables

When asked to check cables connected to the PoE injector, please use the following workflow to systematically rule out problems related to the network cables (see Figure C.15).

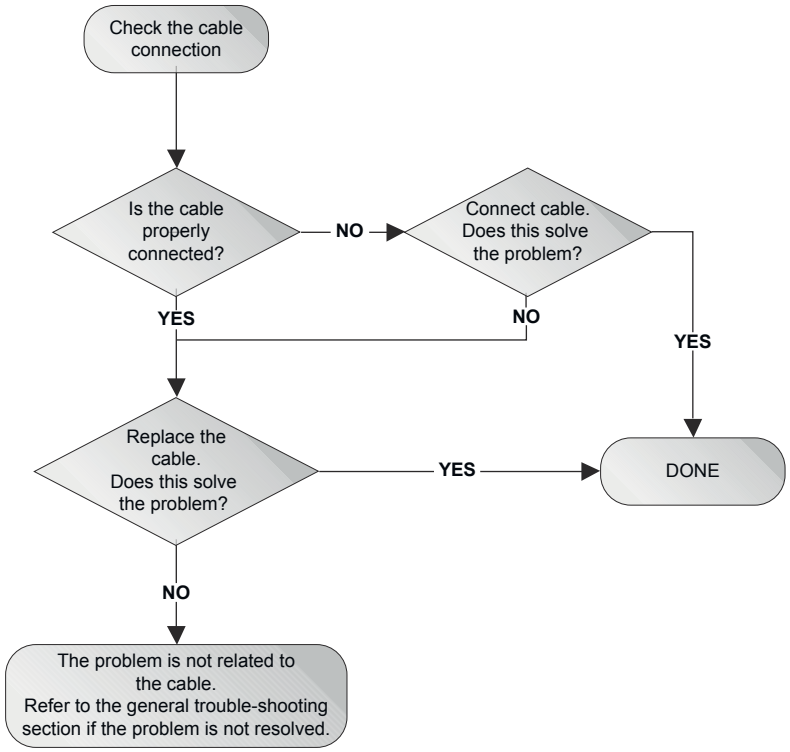


Figure C.15: PoE injector cables trouble-shooting diagram

PoE injector settings

DIP switches can be used to configure settings on the PoE injector. All DIP switches should be in the factory default position. This means that all switches should be in the “up” position (see Figure C.16).

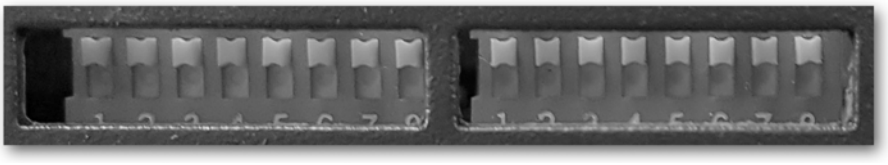


Figure C.16: DIP switches on media converter

PoE injector LED status overview

The following tables give an overview of the LEDs' status for the PoE injector and can be used as reference. This information is an extract from the GPS antenna's manual, please refer to that manual directly for more detailed information.

Status LED

The Perle PoE/PoE +10/100/1000 rate Media convertors have status LEDs located on the front panel of the unit.

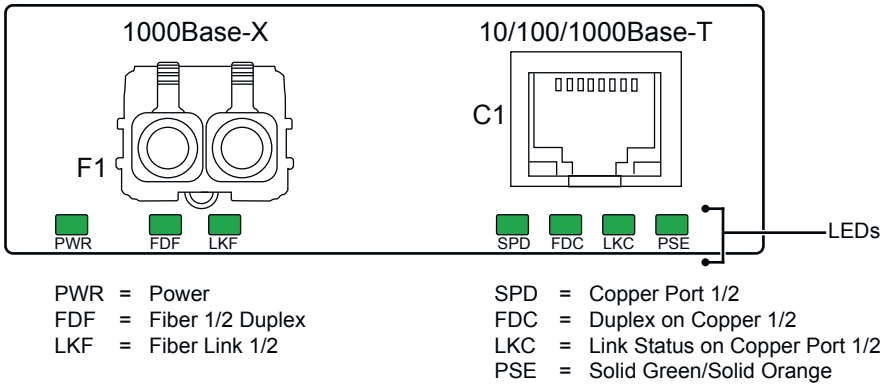


Figure C.17: Power over Ethernet injector LEDs details

Status LED	Activity	Description
PWR	ON	Power is applied to the unit.
	Blinking (slow)	Loopback mode (one or both fiber interfaces are in loopback mode)
	Blinking (fast)	*Power ON* failure. See LED pattern table to determine pattern combination and failure cause*

***LED pattern**				
FDF	LKF	FDC	PSE	
OFF	OFF	ON	ON	SFP incompatible
All other LED patterns				Internal hardware failure

Status LED	Activity	Description
FDF-1/2 (Fiber 1/2 Duplex)	ON	Full Duplex
	OFF	Half Duplex

Status LED	Activity	Description
LKF-1/2 (Status on Fiber Link 1/2)	ON	Fiber Link is present
	OFF	No Fiber Link is present
	Blinking (slow)	Fiber Link appears functional - Fiber Link has been brought down by Smart Link pass-through
	Blinking (fast)	Fiber Link up and receiving data

Status LED	Activity	Description
SPD-(Copper port 1/2)	Green	1000 Mbps
	Orange	100 Mbps
	OFF	10 Mbps (if link is currently established)

Status LED	Activity	Description
FDC-1/2 (Duplex on Copper 1/2)	ON	Full Duplex mode
	OFF	Half Duplex mode

Status LED	Activity	Description
LKC-1/2 (Link status on Copper port 1/2)	ON	Copper link is present
	OFF	No Copper link is present
	Blinking (slow)	Copper link appears functional - Copper link has been brought down by Smart Link pass-through
	Blinking (fast)	Copper link up and receiving data

Status LED	Activity	Description
PSE-1/2	Solid green (Active)	The PSE has successfully detected a compliant PD and is applying power over the UTP
	Solid orange (Inactive)	The PSE is not active. The PSE has been configured to provide power, however ● Compliant is not detected - no power applied ● PSE has turned off power for Reset function
	OFF - (Disabled)	The PSE function is disabled in the configuration
	Error conditions A **blinking red light** is an error condition. The LED light will cycle with a three second stop interval between the error condition code.	
	Red (1 blink)	PD Capacitance too high
	Red (2 blinks)	PD Resistance too low or short circuit
	Red (3 blinks)	PD Resistance too high

Checking the GMR1000

The WinDiscovery tool from Masterclock© has to be installed on the PC, refer to the GMR1000 manual for detailed instructions on how to install and use the software.

1 Start the WinDiscovery tool from Masterclock©, this will show the devices on the network (see Figure C.18).

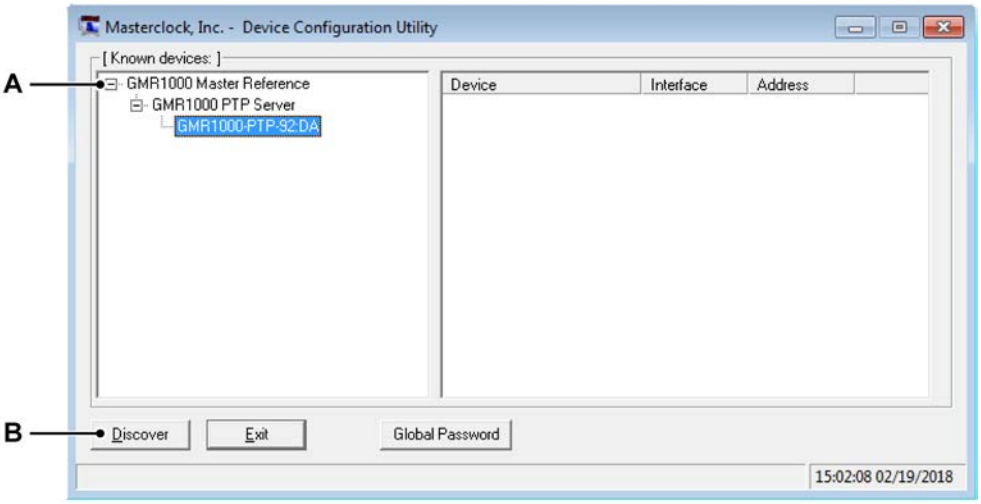


Figure C.18: Device Configuration Utility tool - Detected devices

A List of detected devices

B Discover button

Note *In case no devices are shown, click the **Discover** button. If no devices are discovered, check that the PC running the tool is connected to the GMR1000 via Ethernet.*

1A The first time WinDiscovery is started, Windows® may show the firewall configuration window. Select both options as shown in Figure C.19 and confirm with **Allow access** button.

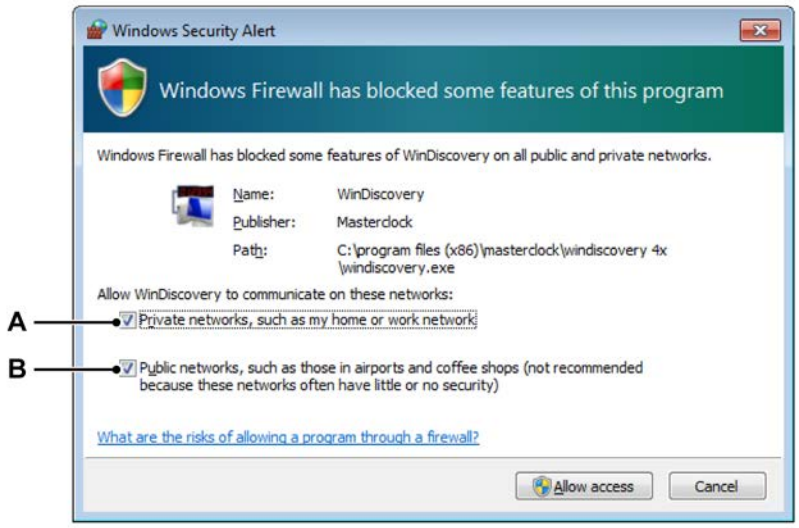


Figure C.19: Windows® Security Alert settings

A Check box for private network(s)

B Check box for public networks

2 Expand the tree in the **Device Configuration Utility** until the specific device is found, which is part of the GMR1000 Master reference -> GMR1000 PTP Server family. Once found, click on the device, this will open the device settings window (see Figure C.20).

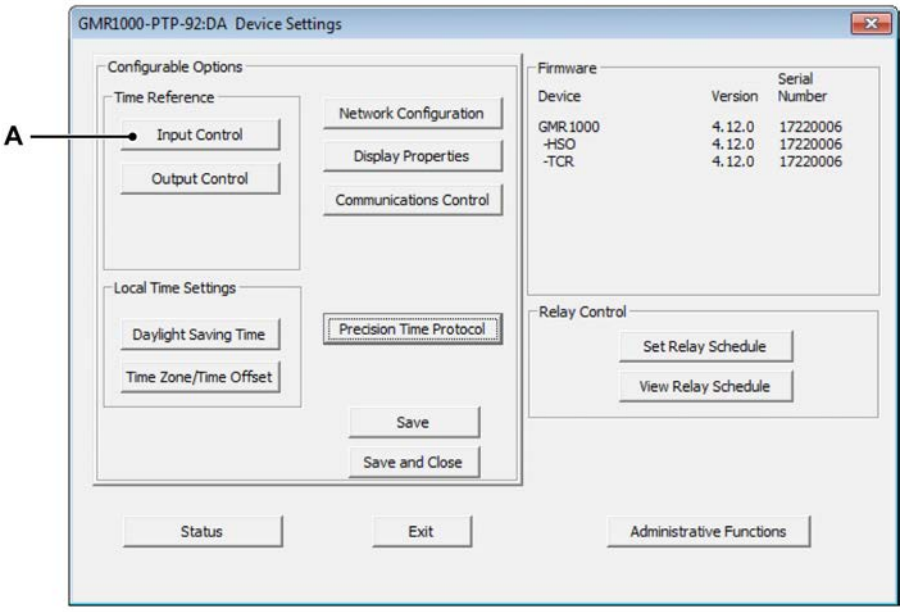


Figure C.20: GMR1000 PTP Device settings

A Input Control

In the device settings, select the **Input Control (A)**.

3 In **Input Control A** dialog, select the **Time Code Reader** button.

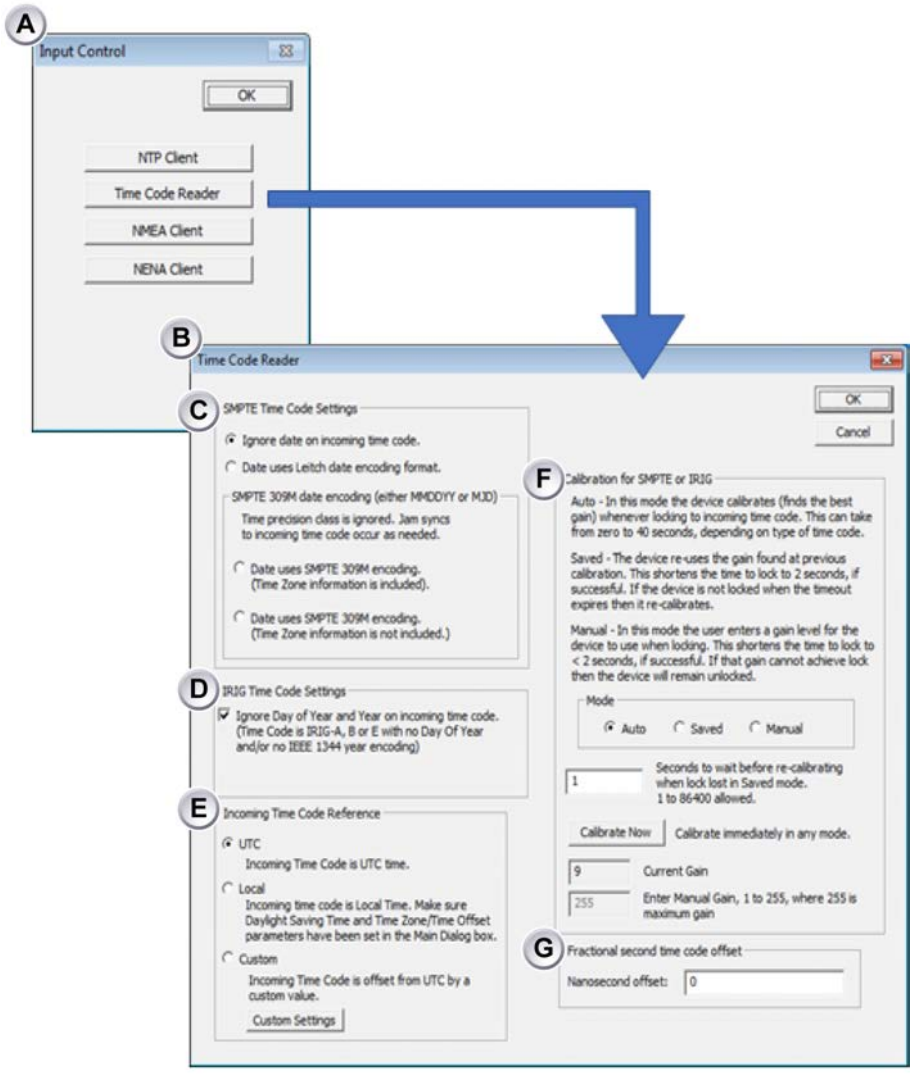


Figure C.21: Input Control - Time Code Reader settings

A **Input Control** dialog

B **Time Code Reader** window

Make sure the settings are set as shown in Figure C.21:

C **SMPTE Time Code Settings:** Select: **Ignore date on incoming time code.** option

D **IRIG Time Code Settings:** Select check box

E **Incoming Time Code Reference:** Select **UTC** option

F **Calibration for SMPTE ot IRIG:** Select **Auto** mode
Seconds to wait before re-calibrating... Set the value to: **1**

G **Fractional second time code offset: Naonosecond offset:** Should be **0**

Close the **Time Code Reader** and **Input Control** windows again.

4 In the GMR1000 PTP device settings window select the **Precision Time Protocol** button.

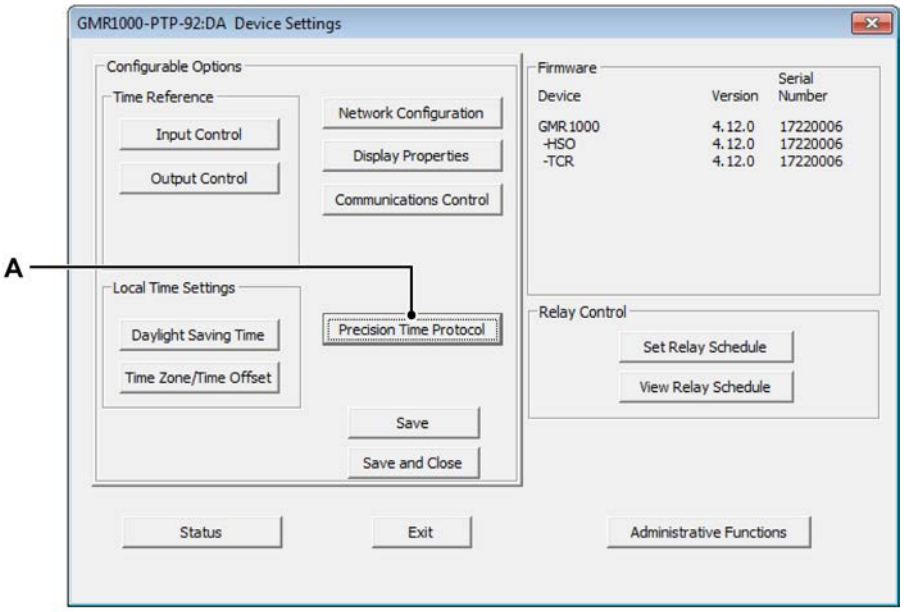


Figure C.22: GMR1000 PTP Device settings

A Precision Time Protocol option

5 In **PTP- Precision Time Protocol** window make sure that the following settings are set:

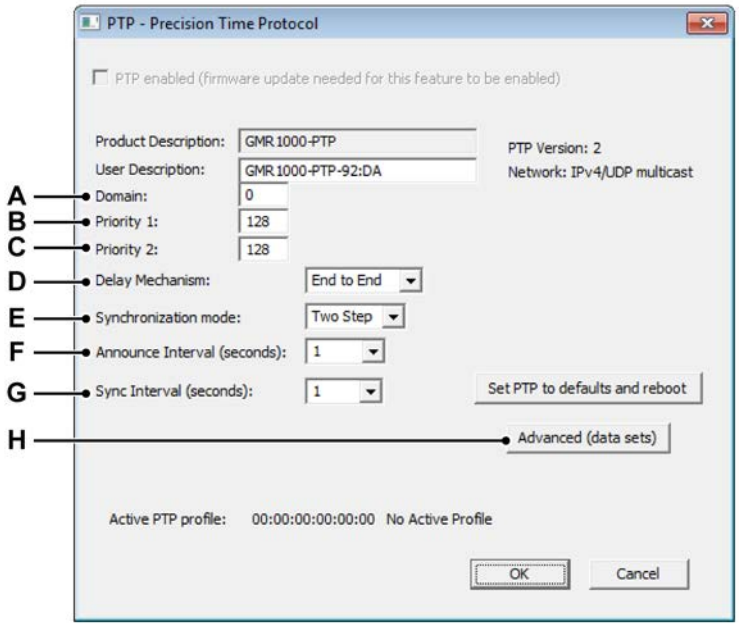


Figure C.23: PTP - Precision Time Protocol

A	**Domain:**	Set the value to "0"
B	**Priority 1:**	Set the value to “128”
C	**Priority 2:**	Set the value to “128”
D	**Delay Mechanism:**	End-to-End
E	**Synchronization mode:**	Two Step
F	**Announce Interval (seconds):**	Set the value to “1”
G	**Sync Interval (seconds):**	Set the value to “1”

6 Click the **Advanced (data sets) button (H)** in PTP - Precision Time Protocol window (see Figure C.23) to open the **PTP Avanced** settings (see Figure C.24).
In **PTP Advanced** window make sure the followings settings are set:

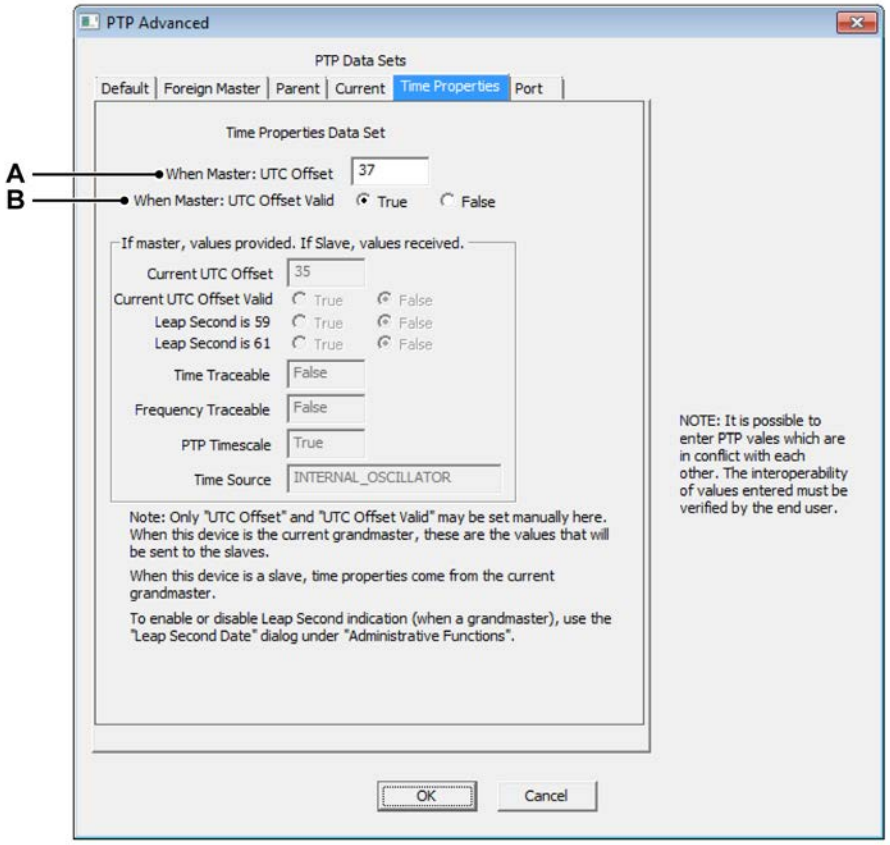


Figure C.24: PTP Advanced - PTP Data Sets/Time Properties settings

Note *UTC Offset to TAI may differ, please enter the value that is currently correct.*

A	**When Master: UTC Offset**	Set the value to “37”
B	**When Master: UTC Offset Valid**	Select the option “True”

7 Finally, close the Advanced (data sets) and PTP - Precision Time Protocol windows. This will bring back the GMR1000 PTP device settings window (see Figure C.25).

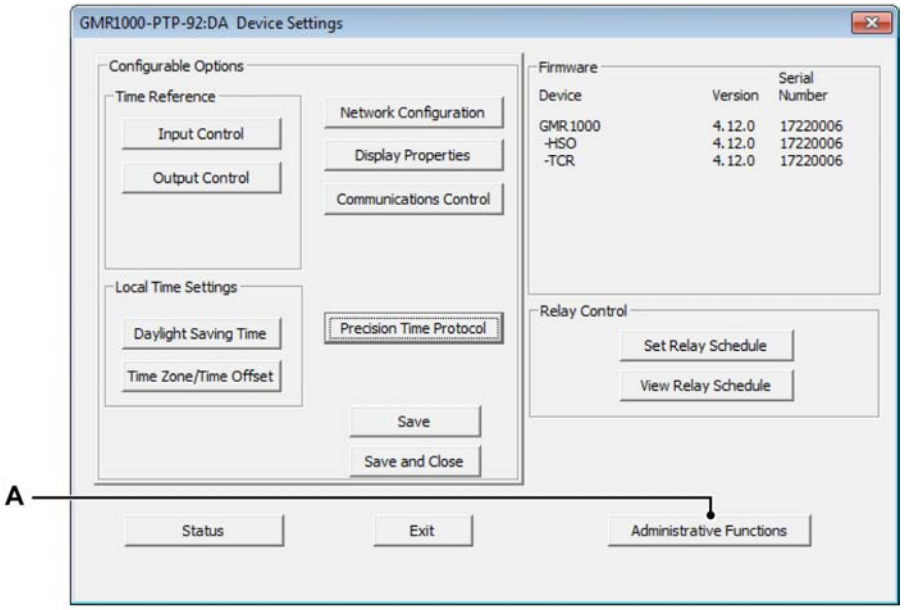


Figure C.25: GMR1000 PTP Device settings

A Administrative Functions

8 As the IRIG signal contains no date, this needs to be entered manually. Open the **Administrative Functions** dialog with the **Administrative Functions (A)** button (see Figure C.25).

9 Edit the date by clicking on the **Set Time/Date** button in the **Administrative Functions** dialog (see Figure C.26).

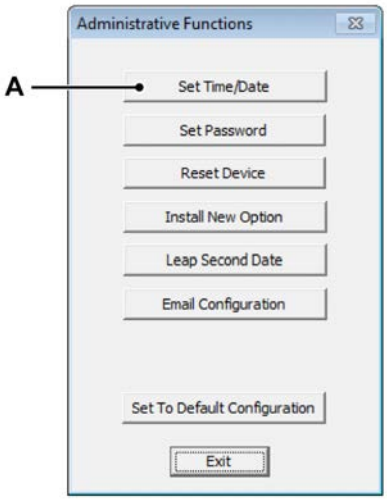


Figure C.26: Administrative Functions - GMR1000

A Set Time/Date option

10 A message will be shown (see Figure C.27).

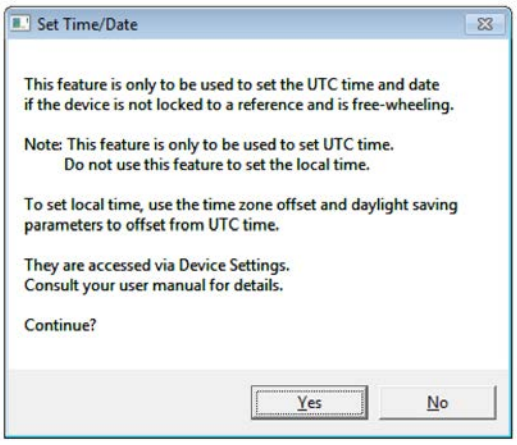


Figure C.27: Set Time/Date

Confirm with **Yes**

11 Now the **Set Time and Date** window is shown (see Figure C.28).

Note *Depending on the PC's settings, the **UTC Time and Date from the PC clock** or the **Custom** option button has to be clicked.*

If the PC's clock is set correctly select the **UTC Time and Date from the PC clock** option button (see Figure C.28).

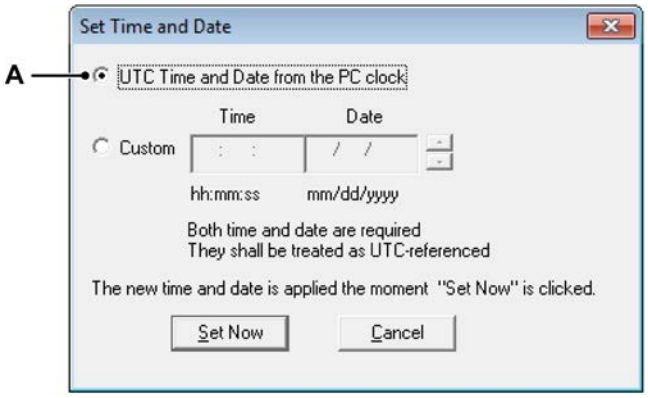


Figure C.28: UTC Time and Date from the PC clock

A UTC Time and Date from the PC clock option

Otherwise select the **custom** time option button (see Figure C.29).

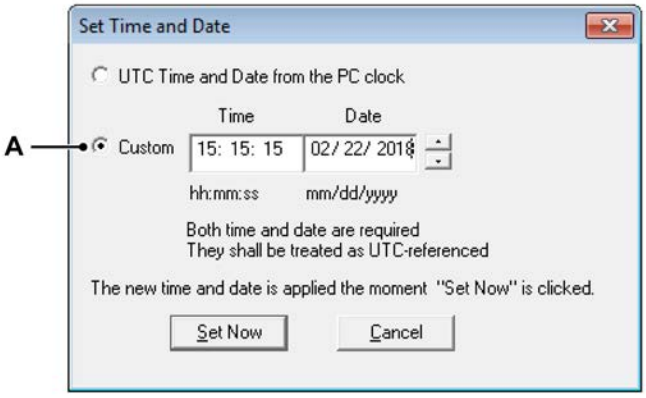


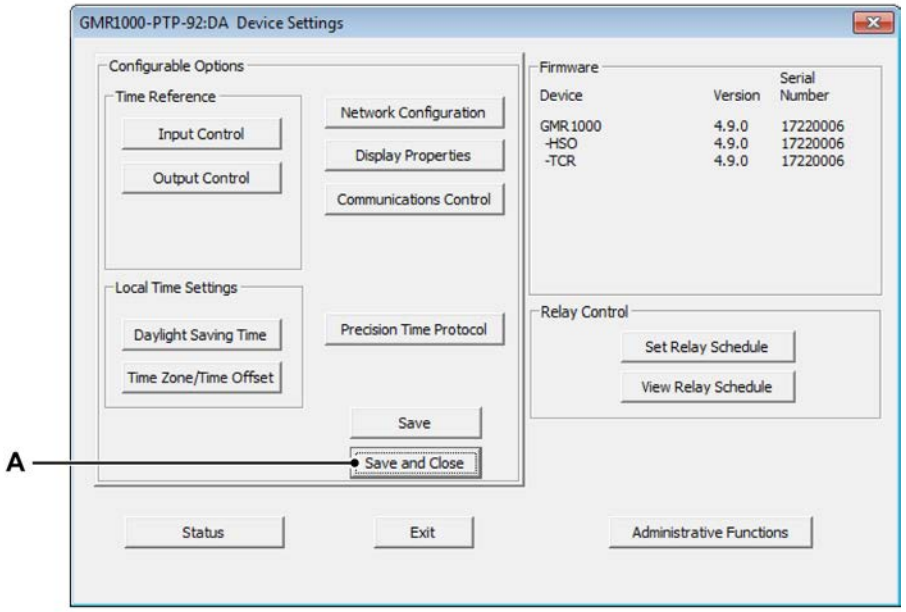
Figure C.29: Setting the time to a custom value

A UTC Time and Date - Custom

Note *Enter any time as this will be overridden later by the IRIG source, but make sure the date entered is the correct date!*

Confirm the changes with **Set Now**.

12 Select the **Save and Close (A)** button to confirm the changes. After a few seconds, the GRM1000 will take over the time from the IRIG source again.



A Save and Close

C.9 GPS OTMC 100 Trouble-shooting

HINT/TIP

In case the information in this chapter does not solve the problem, call your local HBM Support group.

Note *The PTP settings used in this document are displayed only in the **Advanced** settings mode of Perception.*

To open the **Advanced** settings do the following:

1. Open the settings sheet
2. In the main menu select **Settings**.
3. In the Settings menu select **Show Settings ►**.
4. In the submenu select:
   - **Basic:** this will show only the relevant settings
   - **Advanced:** this will show all settings

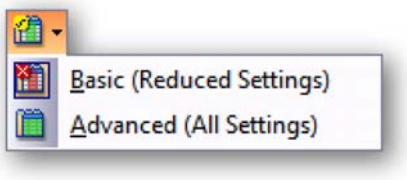


Figure C.30: Perception settings sheet options

How to check synchronization

The synchronization status is displayed in the status window of Perception: When PTP is selected, the system status goes through the following states:

- No signal
- Out of sync
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

Note *The system status returns an overall status for all connected mainframes. To determine which mainframe(s) is causing problems, please see “Finding the system that is causing the problems” on page 436.*

Note *Please be aware that GPS synchronization may take a long time. Do not use this troubleshooting guide in case you have not waited for at least the specified synchronization time.*

The state remains at “No signal”	
Category	**Description**
Cause	The mainframe cannot find the GPS antenna.
Solution	Check these components: **1** Perception setup (see "Checking the Perception setup" on page 436) **2** GEN series network port (see "Verify the GEN series network port" on page 438) **3** PoE injector (see "Checking the SFP PoE injector" on page 441) **4** Verify that the GPS antenna is operational and functioning (see "Checking the GPS antenna" on page 447).
Recording	When starting a recording the mainframes that are in the state “no signal” run on their internal clock (RTC) and the recording is not synchronized.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “Out of sync”	
Category	**Description**
Cause	This problem can be caused by a faulty GPS antenna or malfunctioning network peripherals.

The state remains at “Out of sync”	
Category	**Description**
Solution	Check the GPS antenna and network peripherals.
Recording	When starting a recording the mainframes that are in the state “out of sync” try to follow the signal from the GPS antenna, the recording is most likely **not** synchronized. The time used in the recording is undetermined.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “NO OTMC 100”	
Category	**Description**
Cause	This problem is caused because the mainframe is synchronizing to a PTP master other than the OTMC 100.
Solution	Check the GPS antenna and network peripherals.
Recording	When starting a recording the mainframes that are in the state “NO OTMC 100” try to follow the signal from the PTP grandmaster they did find. The time used in the recording is undetermined. The PTP settings can be used to determine the synchronization source. If the PTP Role is Master, the mainframe has become the master in the PTP network. If the PTP Role is Slave, the PTP Master MAC-address can be used to determine which node in the network is the PTP master. In-depth knowledge of networking is required to obtain this information.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “Coarse”	
Category	**Description**
Cause	A network switch is causing jitter on the PTP timestamps in the network.
Solution	Increase the PTP Accuracy, see chapter "Checking the Perception setup" on page 436.

The state remains at “Coarse”	
Category	**Description**
Recording	When starting a recording the mainframes are typically **not** synchronized within the specified accuracy. The samples at the start of the recording are expected to be synchronous within 10 times the specified accuracy, but may drift apart as the recording proceeds depending on the cause of the problem.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

Use accurate master is set, status is orange	
Category	**Description**
Cause	The mainframe is synchronized to a PTP master that has a clock class worse than 7.
Solution 1	GPS antenna is not found, the mainframe has become PTP master. Treat this the same as “No signal”.
Solution 2	Wait for approximately five minutes, the GPS antenna may still be evaluating its clock class.
Recording (different non- accurate masters)	Each mainframe operates synchronized to its master, data in the recording maybe shifted.
Recording (single non-accurate master)	The data of all mainframes are typically synchronized to the PTP master; however, some systems may apply additional sanity checks and adjust sample times when these checks fail. **Note** *This setup requires any additional network peripherals to be PTP aware.*

Finding the system that is causing the problems

The status described in the previous section is an overall system status showing the most important status in the system. To verify the synchronization details per mainframe, please refer to the chapter "System topology" on page 338.

Checking the Perception setup

The following settings can all be found in the Perception Settings (see Figure C.31).

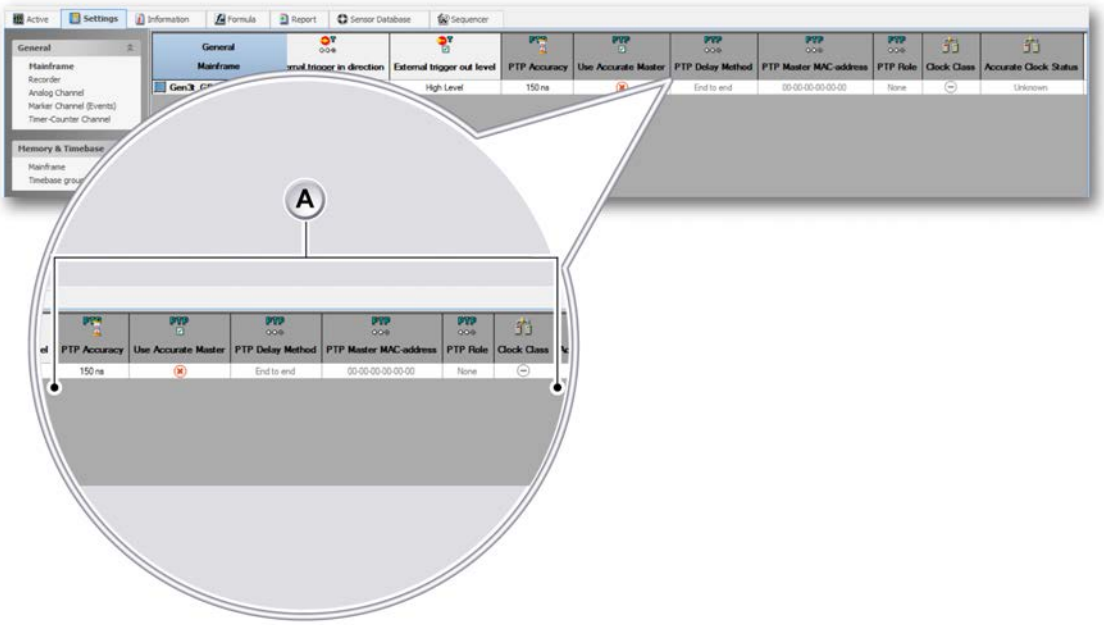


Figure C.31: Perception General Mainframes settings

A PTP related settings in Perception General Mainframes settings

Sync source	
Network port used	**Sync source setting**
RJ45	GPS OTMC 100 (PTP1 RJ45)
Optical 1 Gbit	GPS OTMC 100 (PTP2 SFP)

PTP Accuracy
This should typically be set to 150 ns for best accuracy. **Note** *This setting only needs to be changed if a network switch without PTP support is being used and more jitter is acceptable.* **Note** *Interaction between different time synchronization types in complex set-ups may induce a fixed accuracy.*

Use Accurate Master
Ensure that “accurate master”’ setting is enabled.

PTP Role (read-only)
Verify that the PTP Role is slave. If Master is listed in this column, the GEN series mainframe itself is the master rather than the GPS antenna.

Clock Class
The clock class should be 6 (GPS clock class if the GPS antenna is synchronized).

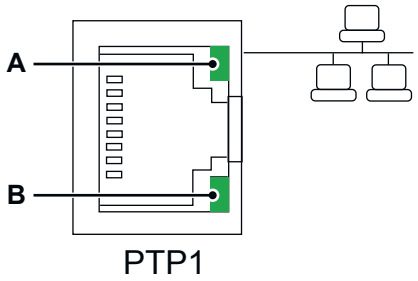
Note *If the clock class is 7, the GPS antenna is currently not locked and runs on its internal clock.*
If the clock class is 52, the GPS antenna was never synchronized.

PTP Master MAC-address
This is the GPS antenna MAC-address, or the boundary clock MAC-address when boundary clocks are used.

Verify the GEN series network port

The following section explains how the LEDs on the ports can be used to diagnose system synchronization problems. The images herein are schematic, for actual port images and positioning of the ports in the system, refer to appendix “PTP Synchronization” on page 455.

PTP1 RJ45 network connection



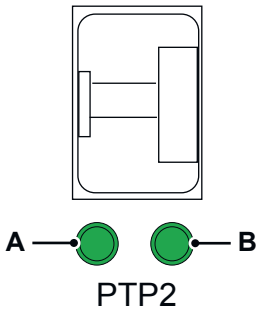
A Activity LED RJ 45 network (blinking)

B Link speed RJ45 network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	**1** Make sure the PoE injector is powered by checking the power LED. **2** Make sure PoE injector IN and OUT are correctly connected. **3** Replace the cables used to verify the cables are not causing the problem.(1)
100 or 10 Mbit/s network connection	ON	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
100 or 10 Mbit/s network connection	Blinking	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
1 Gbit/s network connection	ON	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.
1 Gbit/s network connection	Blinking	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.

(1) **Note** *In case the problem remains unsolved, contact HBM service.*

PTP2 Optical 1 Gbit network connection



A Activity LED optical network

B Link speed LED optical network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	Refer to the “Verify SFP PoE injector” section (see details on page 441). If no problem is found, swap the SFP with the SFP in the PoE injector and retry. If a problem occurs now it is related to the SFP, contact HBM Service for information on how to replace it. **Note** *In case the problem remains unsolved, contact HBM service.*
100 or 10 Mbit/s network connection	ON	OFF	See section "Optical Network (SFP)" on page 402 for additional checks.
100 or 10 Mbit/s network connection	Blinking	OFF	See section "Optical Network (SFP)" on page 402 for additional checks.
1 Gbit/s network connection	ON	ON	This is expected.
1 Gbit/s network connection	Blinking	ON	This is expected.

Checking the SFP PoE injector

The “PoE injector LEDs trouble-shooting diagram” helps to determine the connection problems (see Figure C.33).
The LED names that are referenced in the diagram can be found on the front of the device (see Figure C.32).

PoE injector LEDs

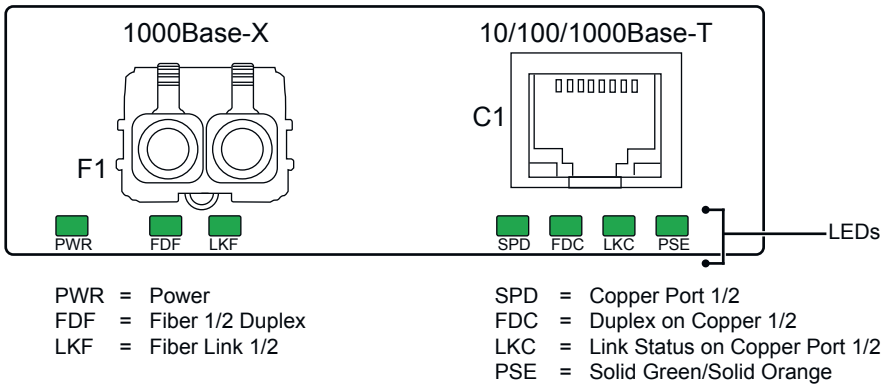


Figure C.32: Power over Ethernet injector LEDs details

Checking the PoE injector LEDs

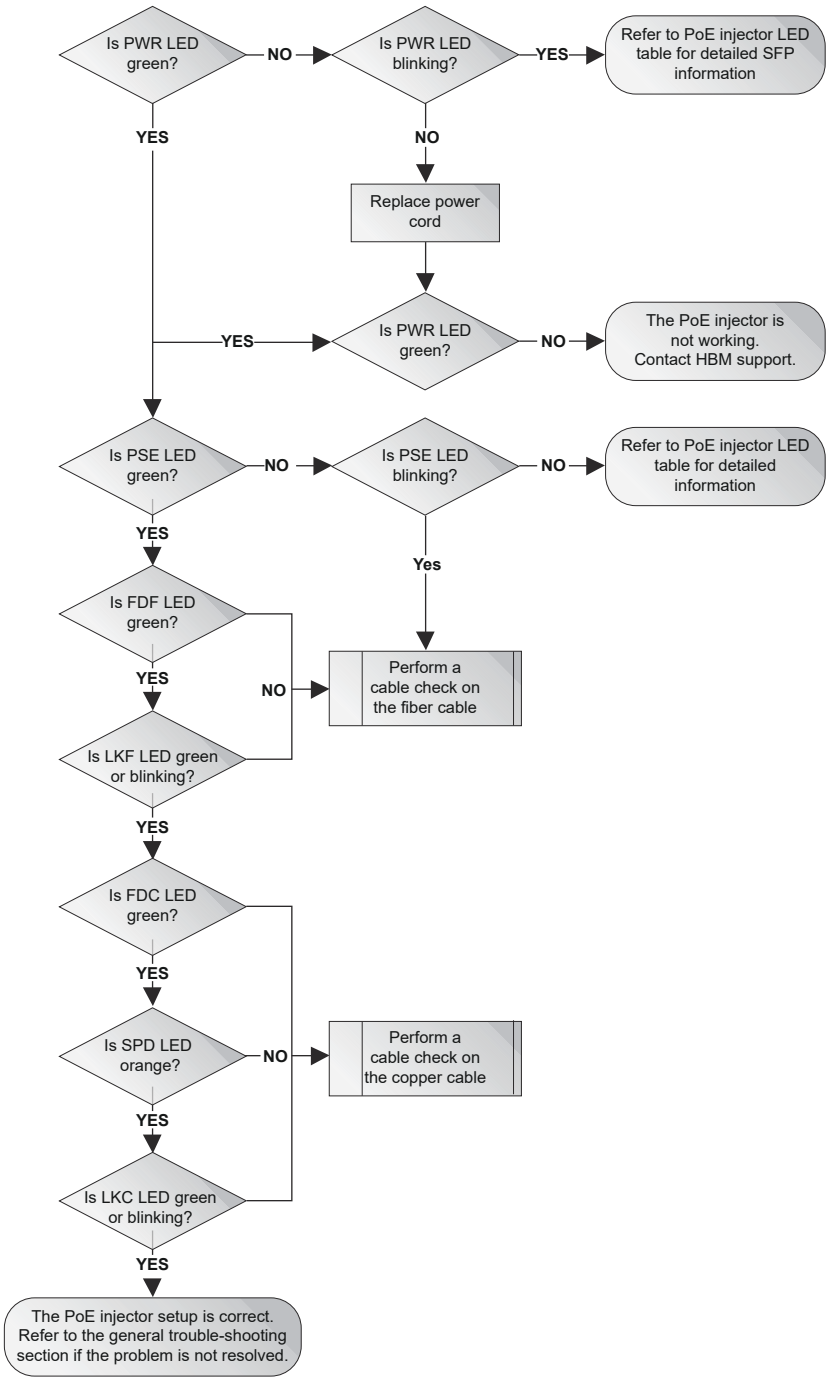


Figure C.33: PoE injector LEDs trouble-shooting diagram

Checking PoE injector cables

When asked to check cables connected to the PoE injector, please use the following workflow to systematically rule out problems related to the network cables (see Figure C.34).

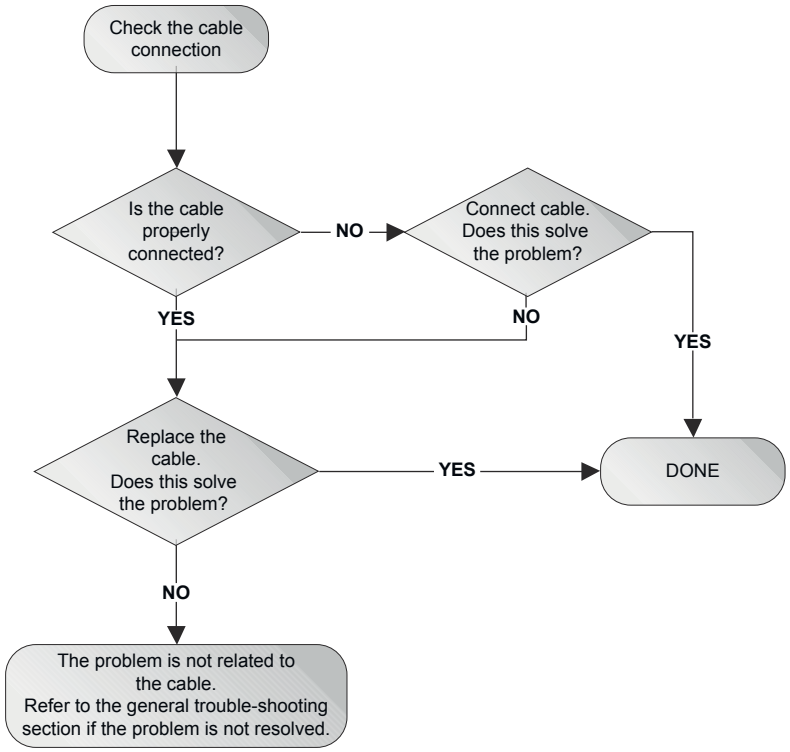


Figure C.34: PoE injector cables trouble-shooting diagram

PoE injector settings

DIP switches can be used to configure settings on the PoE injector. All DIP switches should be in the factory default position. This means that all switches should be in the “up” position (see Figure C.35).

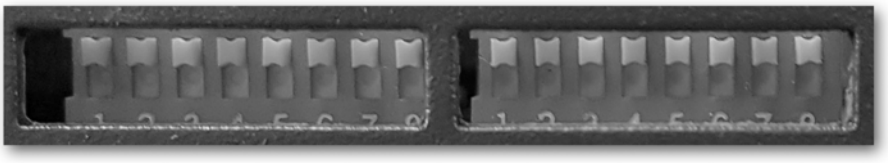


Figure C.35: DIP switches on media converter

PoE injector LED status overview

The following tables give an overview of the LEDs' status for the PoE injector and can be used as reference. This information is an extract from the GPS antenna's manual, please refer to that manual directly for more detailed information.

Status LED

The Perle PoE/PoE +10/100/1000 rate Media convertors have status LEDs located on the front panel of the unit.

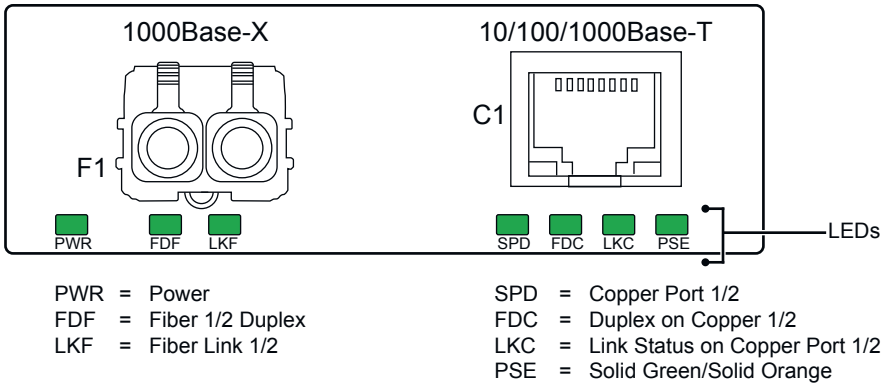


Figure C.36: Power over Ethernet injector LEDs details

Status LED	Activity	Description
PWR	ON	Power is applied to the unit.
	Blinking (slow)	Loopback mode (one or both fiber interfaces are in loopback mode)
	Blinking (fast)	*Power ON* failure. See LED pattern table to determine pattern combination and failure cause*

***LED pattern**				
FDF	LKF	FDC	PSE	
OFF	OFF	ON	ON	SFP incompatible
All other LED patterns				Internal hardware failure

Status LED	Activity	Description
FDF-1/2 (Fiber 1/2 Duplex)	ON	Full Duplex
	OFF	Half Duplex

Status LED	Activity	Description
LKF-1/2 (Status on Fiber Link 1/2)	ON	Fiber Link is present
	OFF	No Fiber Link is present
	Blinking (slow)	Fiber Link appears functional - Fiber Link has been brought down by Smart Link pass-through
	Blinking (fast)	Fiber Link up and receiving data

Status LED	Activity	Description
SPD-(Copper port 1/2)	Green	1000 Mbps
	Orange	100 Mbps
	OFF	10 Mbps (if link is currently established)

Status LED	Activity	Description
FDC-1/2 (Duplex on Copper 1/2)	ON	Full Duplex mode
	OFF	Half Duplex mode

Status LED	Activity	Description
LKC-1/2 (Link status on Copper port 1/2)	ON	Copper link is present
	OFF	No Copper link is present
	Blinking (slow)	Copper link appears functional - Copper link has been brought down by Smart Link pass-through
	Blinking (fast)	Copper link up and receiving data

Status LED	Activity	Description
PSE-1/2	Solid green (Active)	The PSE has successfully detected a compliant PD and is applying power over the UTP
	Solid orange (Inactive)	The PSE is not active. The PSE has been configured to provide power, however ● Compliant is not detected - no power applied ● PSE has turned off power for Reset function
	OFF - (Disabled)	The PSE function is disabled in the configuration
	Error conditions A **blinking red light** is an error condition. The LED light will cycle with a three second stop interval between the error condition code.	
	Red (1 blink)	PD Capacitance too high
	Red (2 blinks)	PD Resistance too low or short circuit
	Red (3 blinks)	PD Resistance too high

Checking the GPS antenna

The status of the antenna can be checked by the LED under the antenna.

LED status	Description
Green	OK
Red	Antenna is booting
OFF	Antenna has no power
Blinking	Antenna internal problem, please refer to the GPS antenna manual for detailed information.

Using a direct connection to the PC, the status and configuration of the antenna can be viewed in more detail.

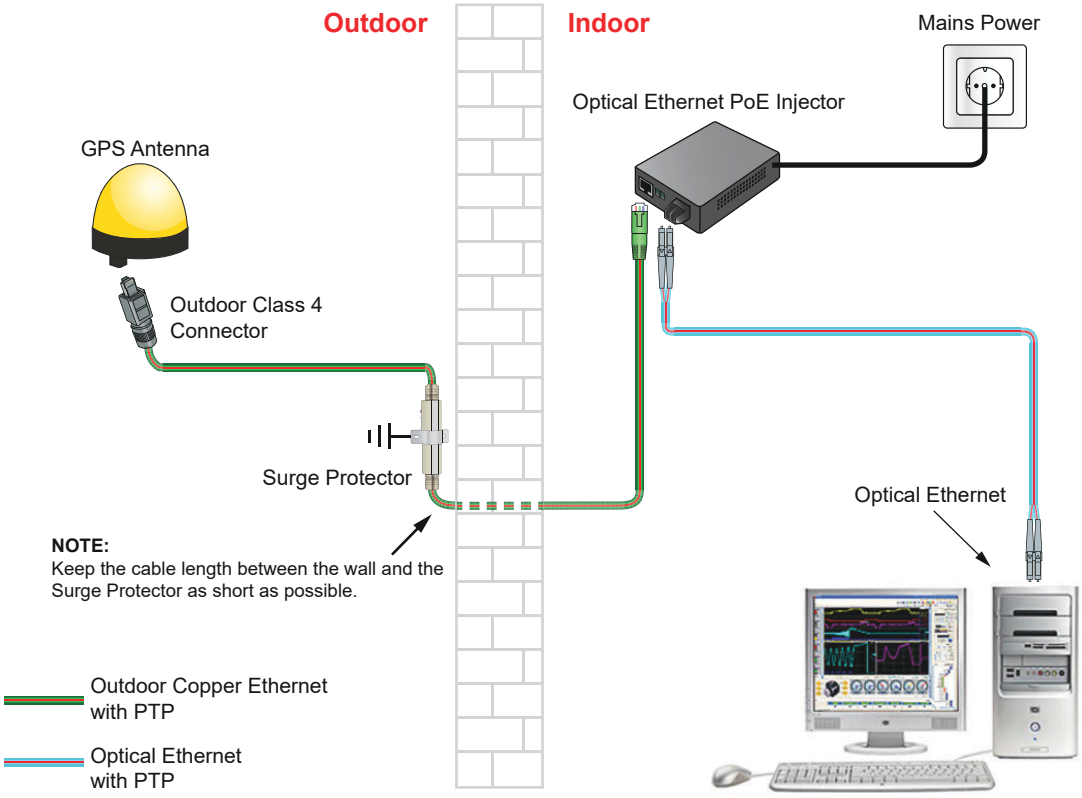


Figure C.37: GPS antenna - PC connection (example)

Note *Use an RJ45 to RJ45 PoE injector to make a direct connection to a PC if the PC does not contain an optical network port.*

The Omnicron® device browser (for the OTMC GPS antenna) has to be installed on the PC, refer to the GPS antenna manual for detailed instructions on how to install and use the software.

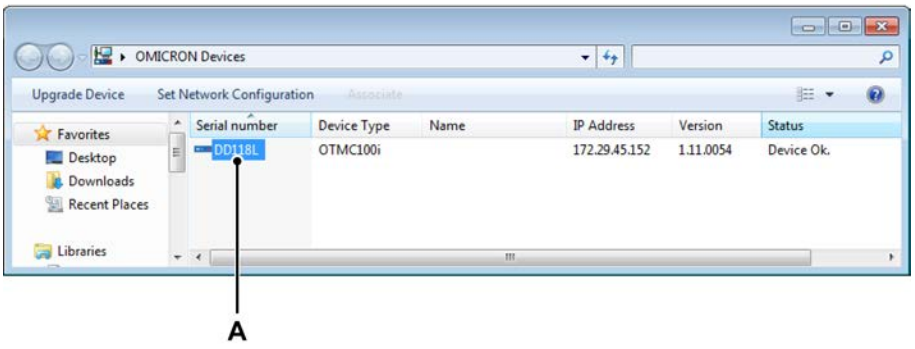


Figure C.38: Omnicron® device browser

A Omnicron® GPS antenna OTMC 100*i*

Right-click on the device to open the web browser (see Figure C.39).

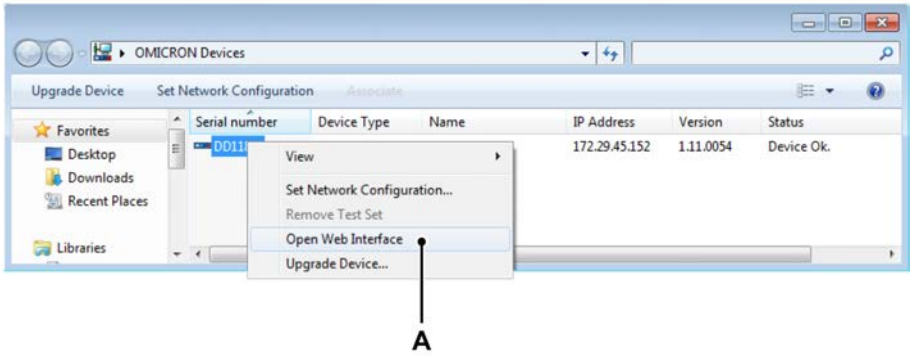


Figure C.39: Opening Omnicon® web interface

A Web inferface configuration for GPS antenna

The details of the **Web Interface** are explained in the next section.

Verify the PTP Master MAC-address

In **Overview** ► **Network** option, the MAC address is shown (see Figure C.40).

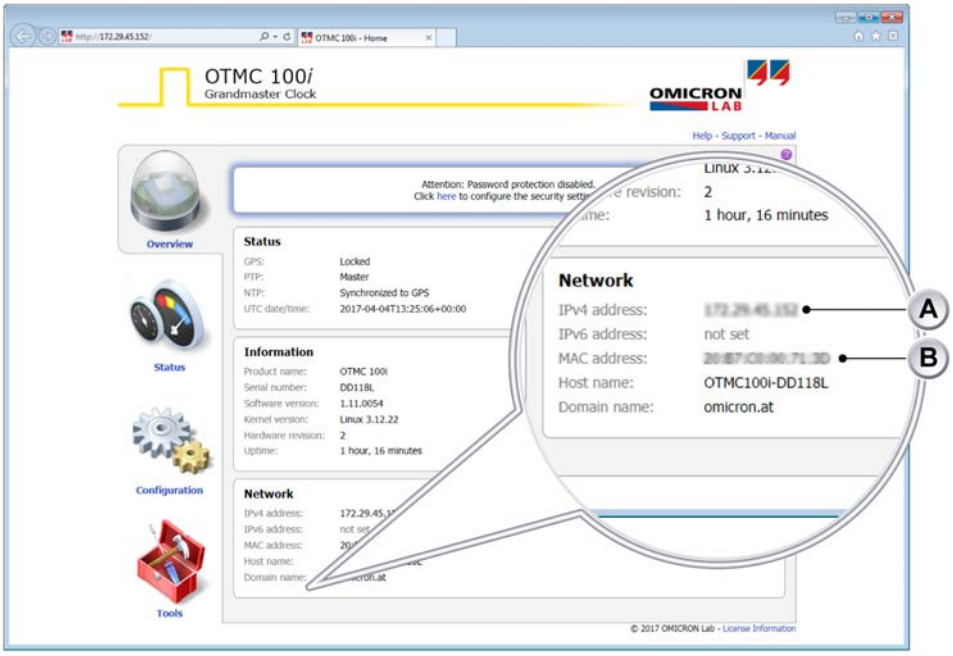


Figure C.40: OTMC 100 MAC/IP address

A IP address

B MAC address

Verify the usable GPS antenna satellite reception

In **Status ► GPS** option, a minimum of six satellites is recommended for proper PTP operation (see Figure C.41).

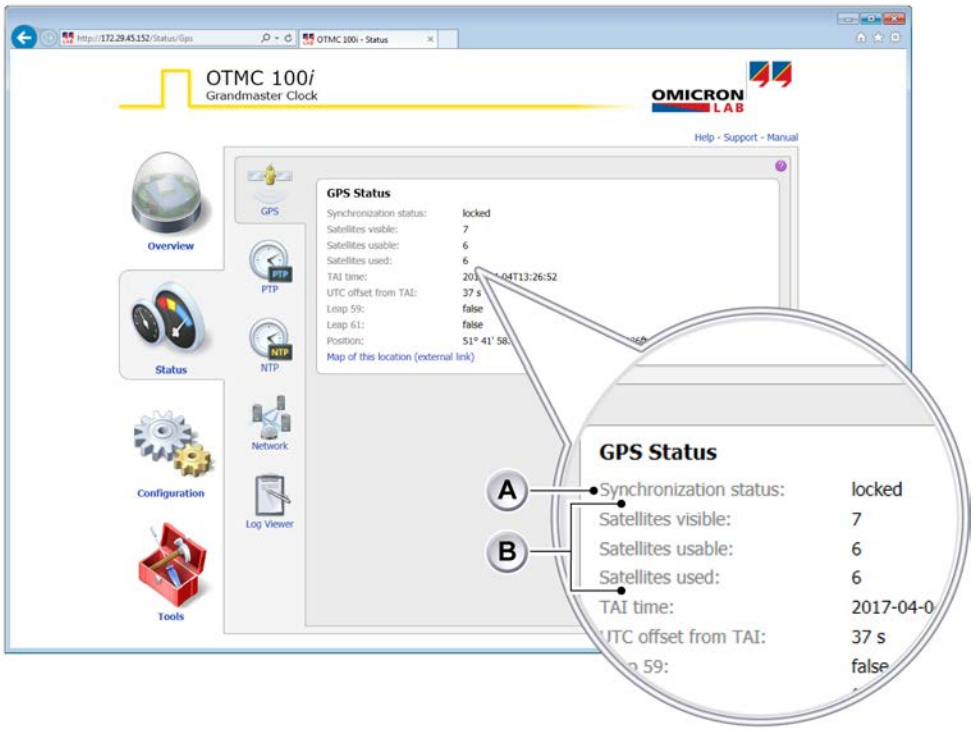


Figure C.41: OTMC 100 GPS status information

A GPS/Synchronization status

B GPS status of satellites

PTP Settings

The antenna should work with Perception using the factory default settings, however it is possible to change the PTP settings. An overview of the actual PTP settings can be found in the PTP options (see Figure C.42).

In **Status ► PTP** option, the settings should match the values shown in the image below (see Figure C.42) for the **Port** and **Default** sections. The only exceptions are **Profile ID** and **Clock identify** as these may vary per antenna and their value does not affect the PTP protocol operation.

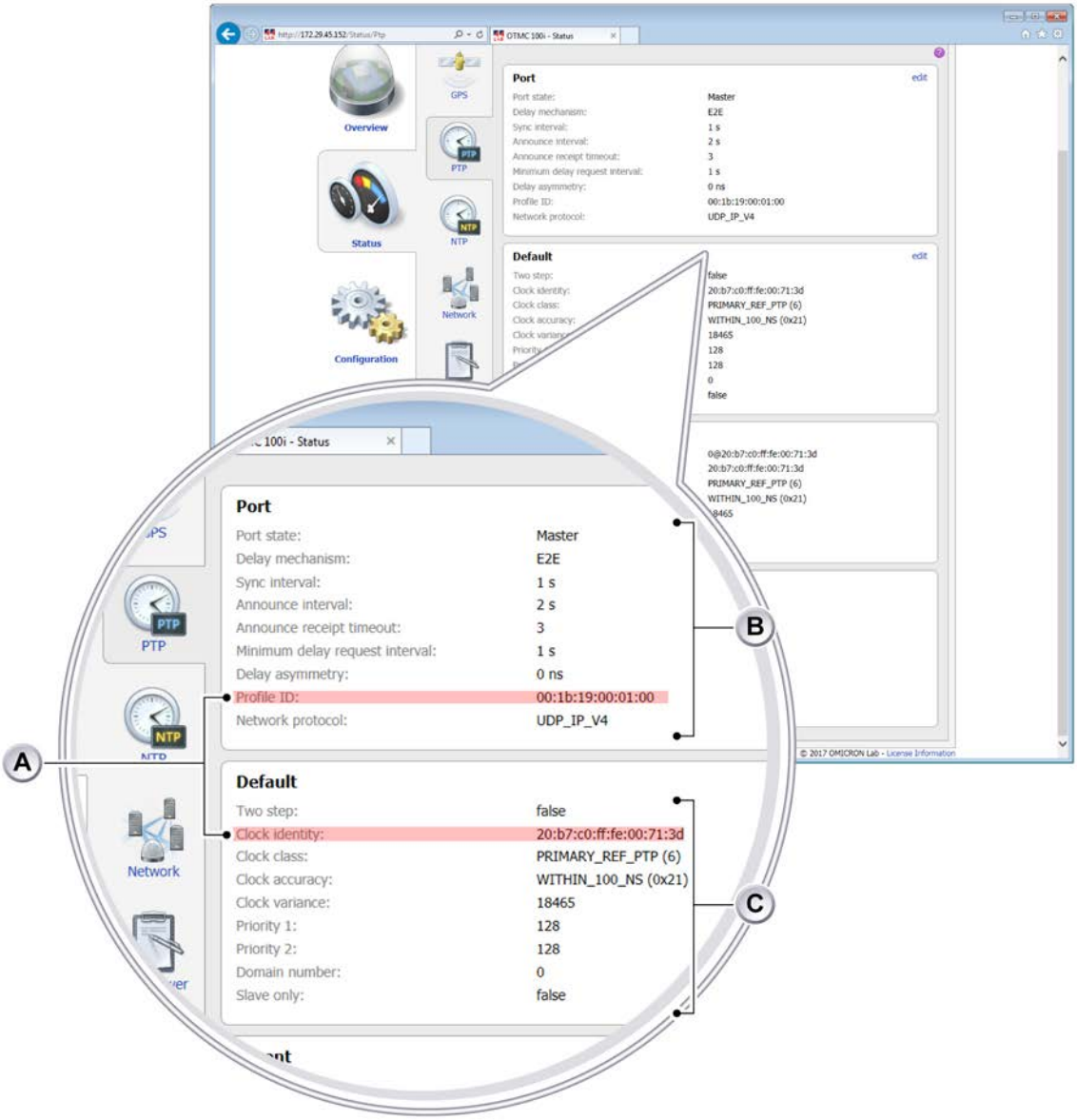


Figure C.42: OTMC 100 PTP status information

A **Port**: **Profile ID** may vary per antenna.
Default: **Clock identify** may vary per antenna.

B **Port**: Standard settings for PTP.

C **Default**: Standard settings for PTP.

Network settings

In **Configuration ► Network** option, make sure that **Precision Time Protocol (PTP)** is enabled (see Figure C.43).

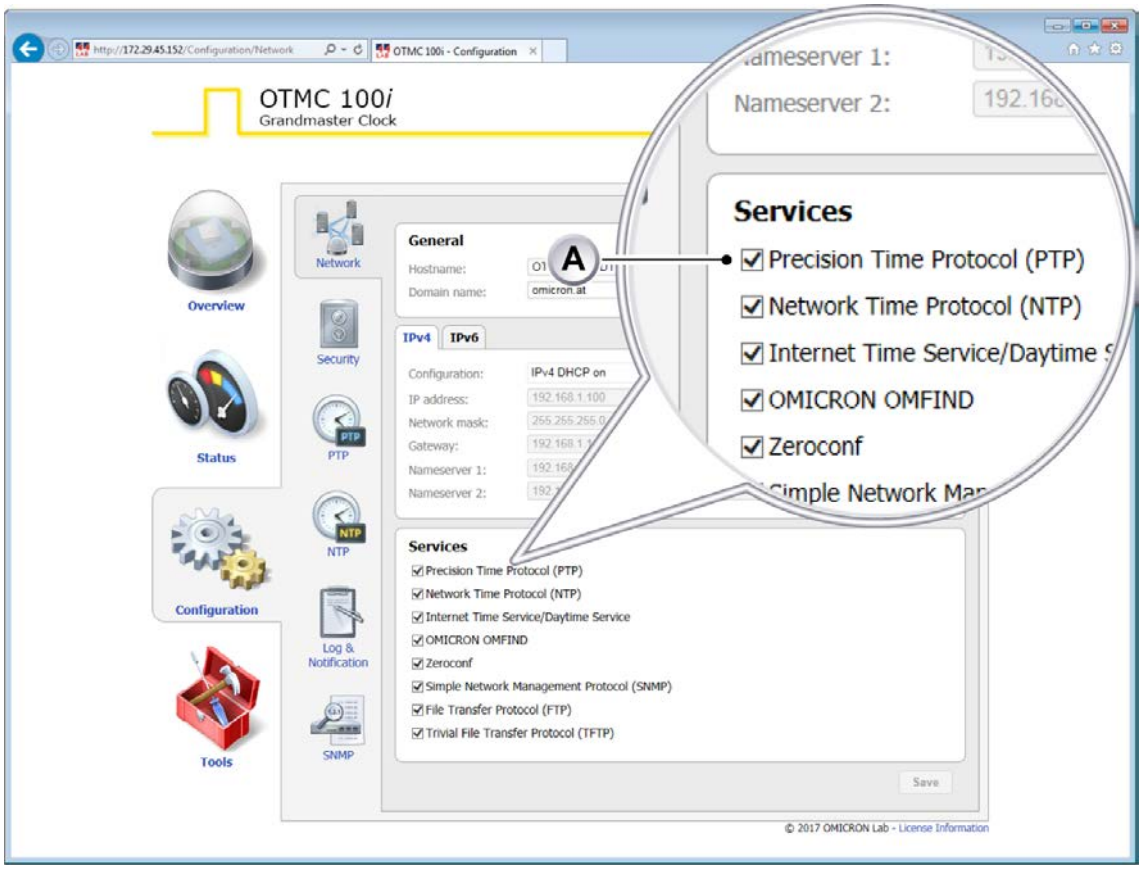


Figure C.43: OTMC 100 Network status information

A Precision Time Protocol (PTP)

Other

For more detailed GPS antenna related troubleshooting, use of the web interface and resetting the antenna to its factory defaults, please refer to the manual delivered with the GPS antenna.

D Frequently Asked Questions

D.1 Overview

Question:	Answer:
Can **Trigger Arm** be used in a multi mainframe setup using Master/Sync connection?	Yes, **Trigger Arm** can be used in a multi mainframe setup using Master/Sync connection when the arm signal is provided to all mainframes like the TTL signal External Event In or the CAN bus. Trigger Arm uses the qualifier lines to allow triggering or not. Master/Sync setup shares the qualifier and trigger lines over the multi Mainframes. In case one mainframe isn't being armed the whole multi Mainframe setup cannot trigger due to the qualifier state.

Question:	Answer:
Is there a difference in **External Trigger Out delay** from a calculated (RT-FDB) channel and input channel trigger detector?	Yes, **External Trigger Out delay** from a calculated channel will always have a delay of 100 ms. The External Trigger Out delay from an input channel is user selectable between 10 µs and 516 µs.

E Rack Mount Instructions

E.1 Mount GEN17tA in a 19-inch rack

A 19-inch rack is a standardized (EIA 310-D, IEC 60297 and DIN 41494 SC48D) system for mounting various electronic units in a rack, 19-inches (482.6 mm) wide. Equipment designed to be placed in a rack is described as rack-mount or a rack-mounted system.

The GEN17tA by itself can directly be mounted into a 19-inch rack.

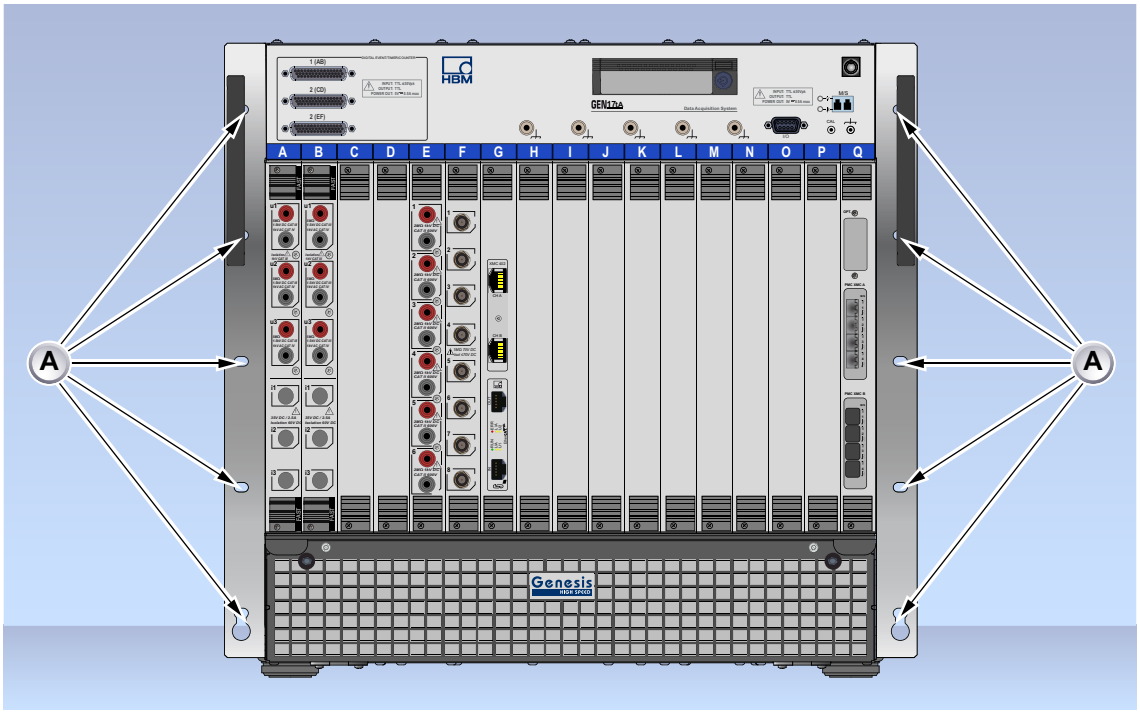


Figure E.1: 19 inch mounting holes

A Mounting holes

If required, the rubber feet under the device can be removed. Please see chapter "Feet" on page 96 on how to remove the feet.

F PTP synchronization

F.1 Mainframe PTP connections

Note *GEN DAQ mainframes support two 1 Gigabit PTP ports. However, these ports can not be used as a bridge.*

Note *GEN DAQ mainframes do not forward PTP information (or any other message/ data) from one port to the other port.*

F.1.1 GEN7i

Figure F.1: GEN7i PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.1.2 GEN7iA

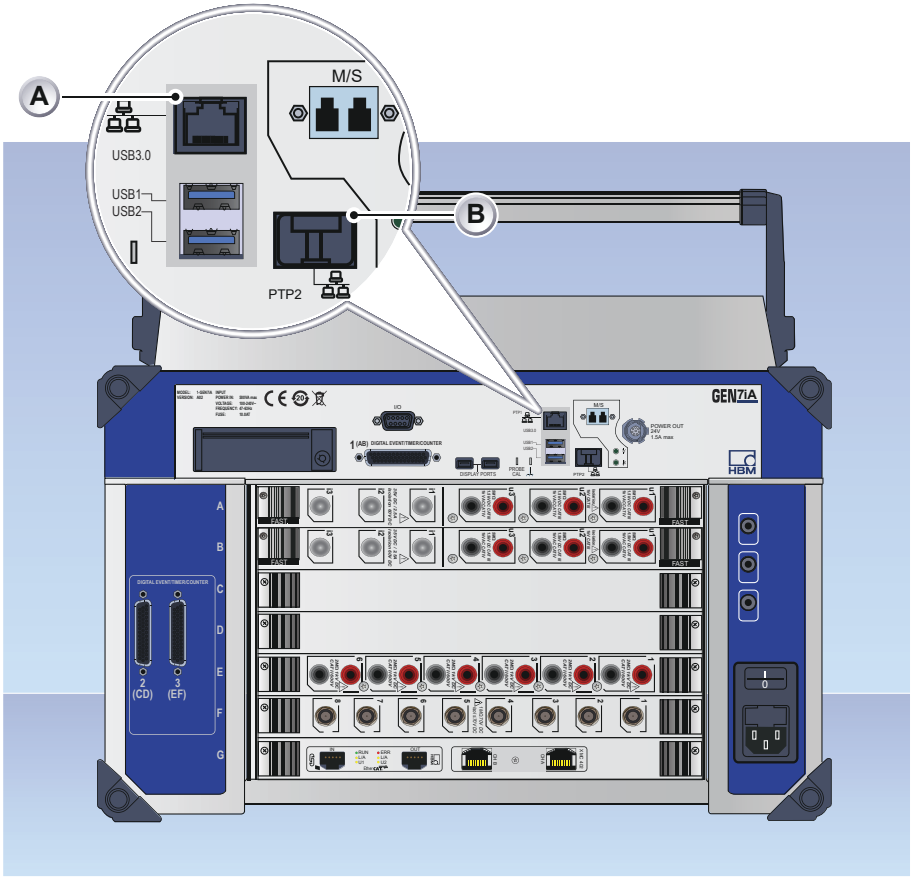


Figure F.2: GEN7iA PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.1.3 GEN7tA

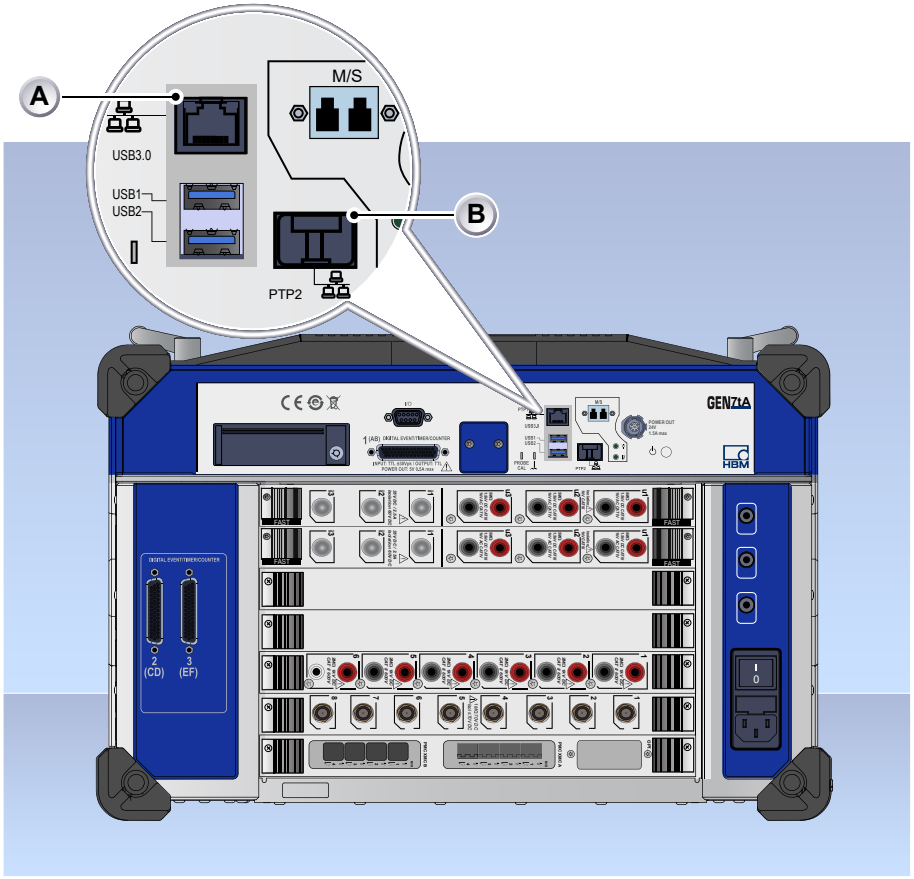


Figure F.3: GEN7tA PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.1.4 GEN2tB

Figure F.4: GEN2tB PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.1.5 GEN4tB

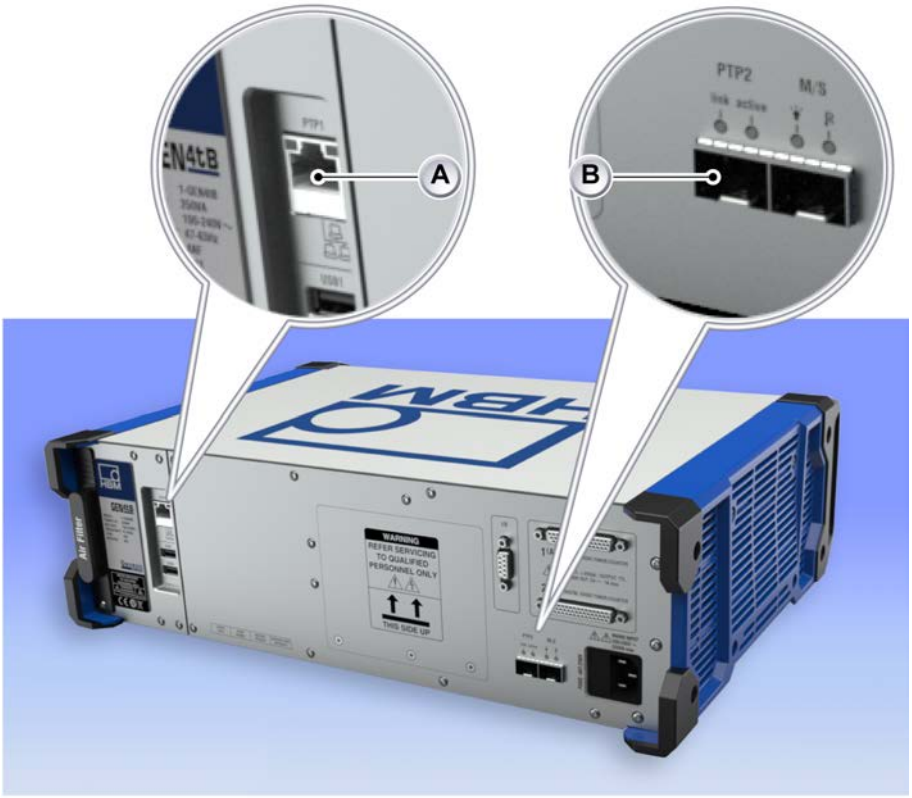


Figure F.5: GEN4tB PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.1.6 GEN3i

Figure F.6: GEN3i PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.1.7 GEN3iA

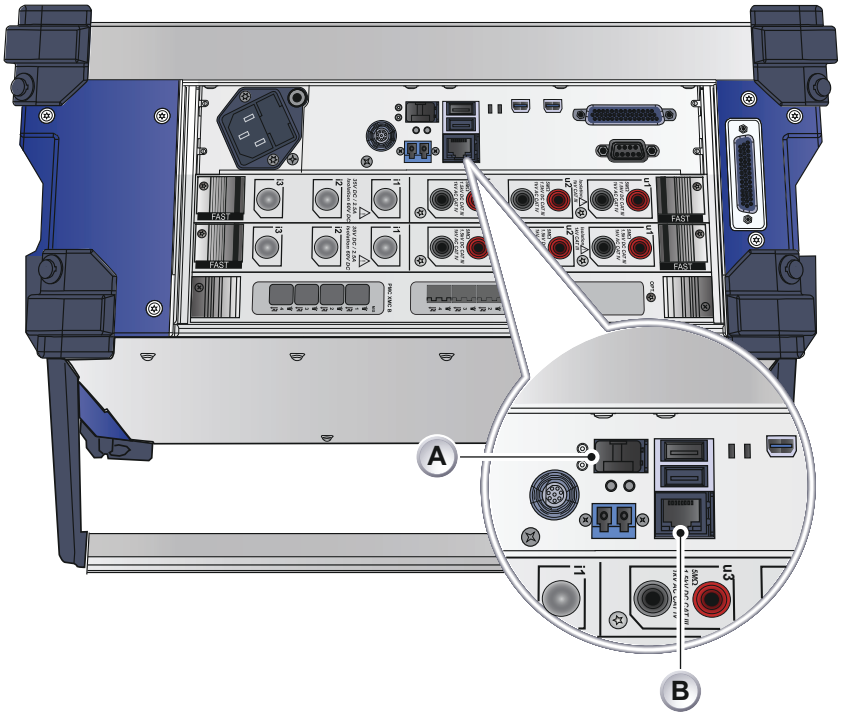


Figure F.7: GEN3iA PTP enabled ports

A PTP enabled network optical SFP slot (SFP module is optional)

B PTP enabled network RJ45

F.1.8 GEN17tA

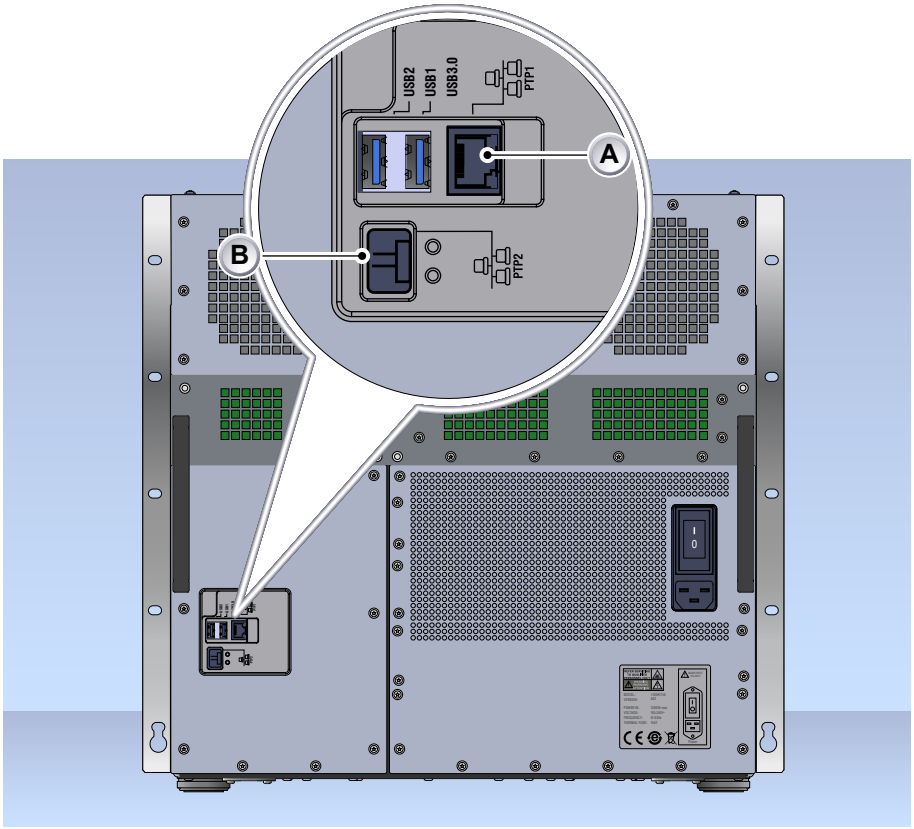


Figure F.8: GEN17tA PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

F.2 Perception settings

Set "Sync Source“ to PTP1 (RJ45) **or** to PTP2 (optical):

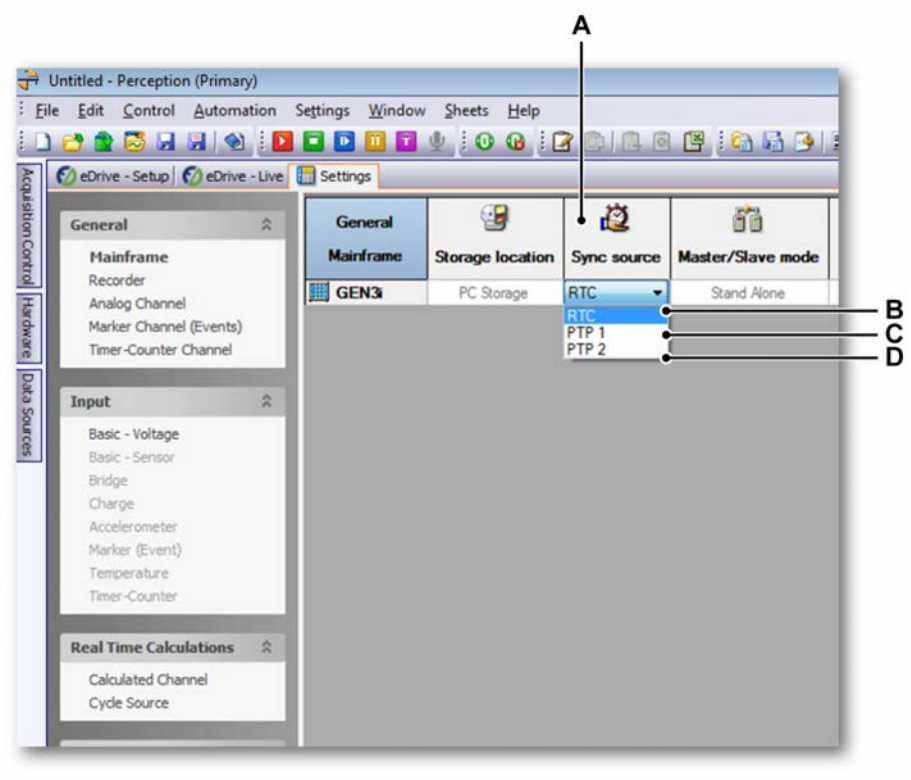


Figure F.9: Perception - Sync source option (PTP 1) or (PTP 2)

A Sync source option

B RTC

C PTP 1

D PTP 2

F.3 Synchronizing GEN series and QuantumX using PTP

F.3.1 GEN3i/GEN3iA/GEN7i/GEN7iA with single QuantumX "B" version module

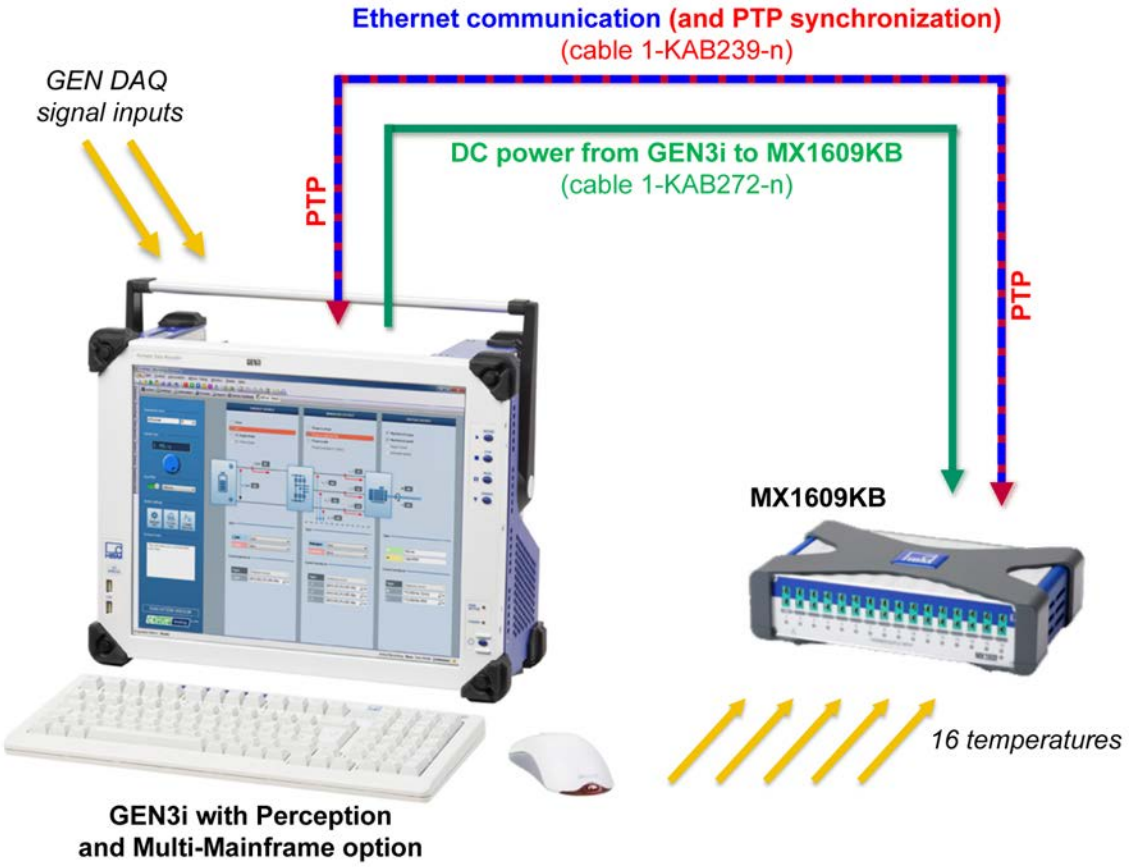


Figure F.10: GEN3i with single MX1609KB/MX1609TB - Overview

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i/GEN7iA.*

Note *Setup only shows MX1609KB, MX471B (CAN) could also be used.*

F.3.2 GEN3i/GEN3iA/GEN7i/GEN7iA with single SomatXR "B" version module

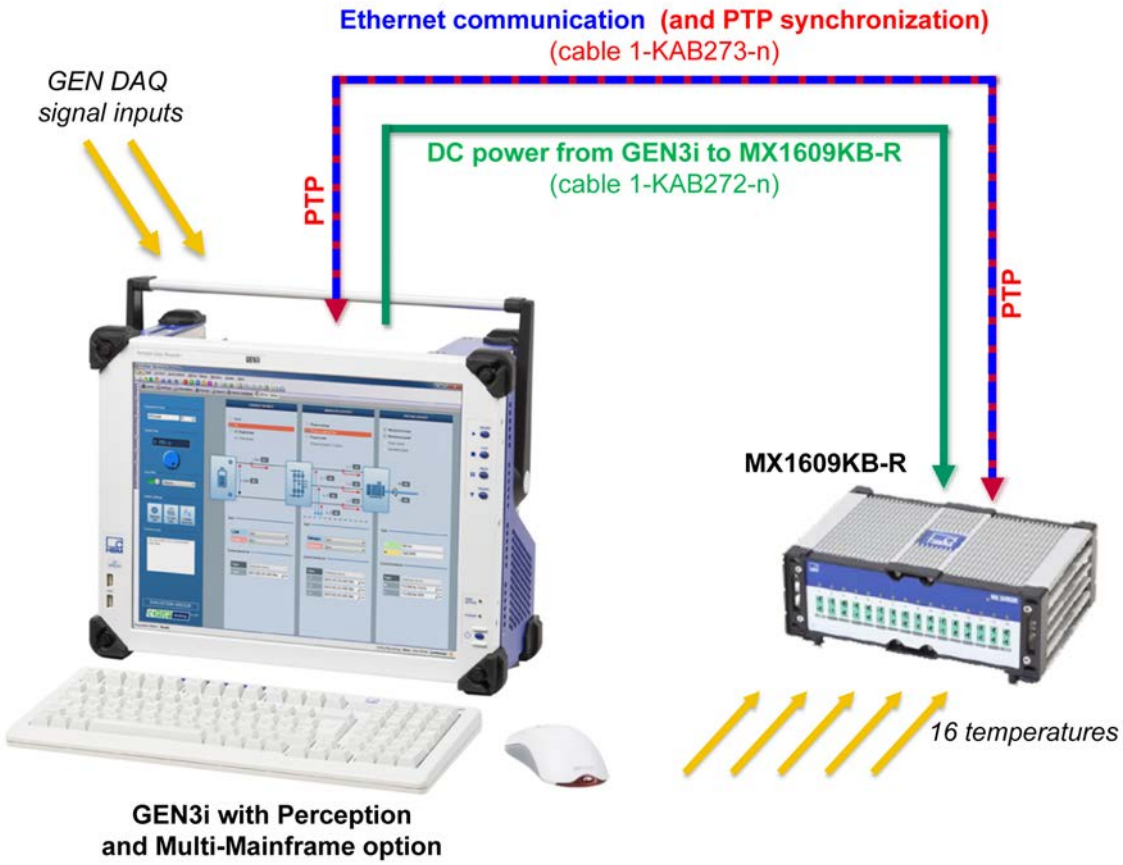


Figure F.11: GEN3i with single Somat^{XR} MX1609KB-R - Overview

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i/GEN7iA.*

F.3.3 GEN3i/GEN3iA/GEN7i/GEN7iA with up to three QuantumX "B" version modules

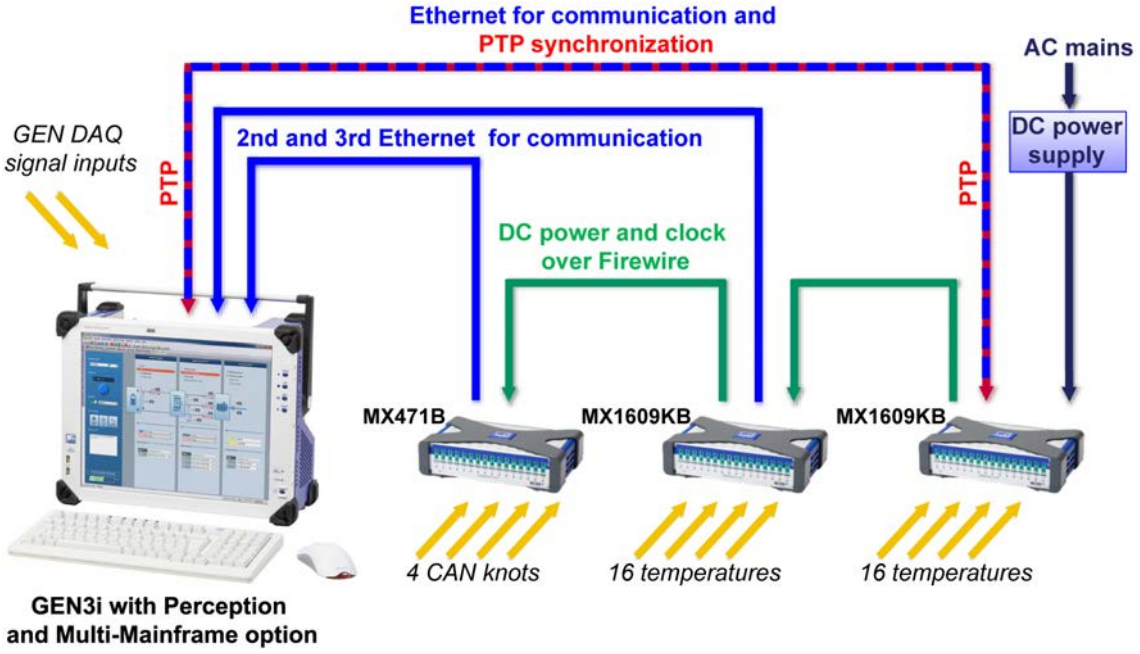


Figure F.12: GEN3i with a mix of three QuantumX "B" version modules

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i/GEN7iA.*

Note **** All** modules must be "B" versions; one module must set to "clock master" and connected to the GEN3i PTP Ethernet.*

HINT/TIP

This setup uses multiple network ports on the GEN3i PC section.
Use fixed IP address setup with different base IP address and non-overlapping IP-ranges (Combination of base IP address and net mask) for each of the GEN3i network ports to make sure the setup always works.

Example setup:	
GEN3i network 1:	192.168.1.10 mask 255.255.255.0
GEN3i network 2:	192.168.2.10 mask 255.255.255.0
GEN3i network 3:	192.168.3.10 mask 255.255.255.0
QuantumX module 1:	192.168.1.11 mask 255.255.255.0
QuantumX module 2:	192.168.2.11 mask 255.255.255.0
QuantumX module 3:	192.168.3.11 mask 255.255.255.0

Background network details

If the network ports are configured for DHCP setup, each of the connections using the APIPA protocol to find a free IP address. As none of the network ports are linked together the APIPA protocol does not detect the address used any of the network devices in this setup. At random all QuantumX systems might end up with exactly the same network IP address. If this happens the systems are not uniquely addressable anymore and the communication fails.

F.3.4 GEN3i/GEN3iA/GEN7i/GEN7iA with standard network switch and four or more of QuantumX "B" version modules

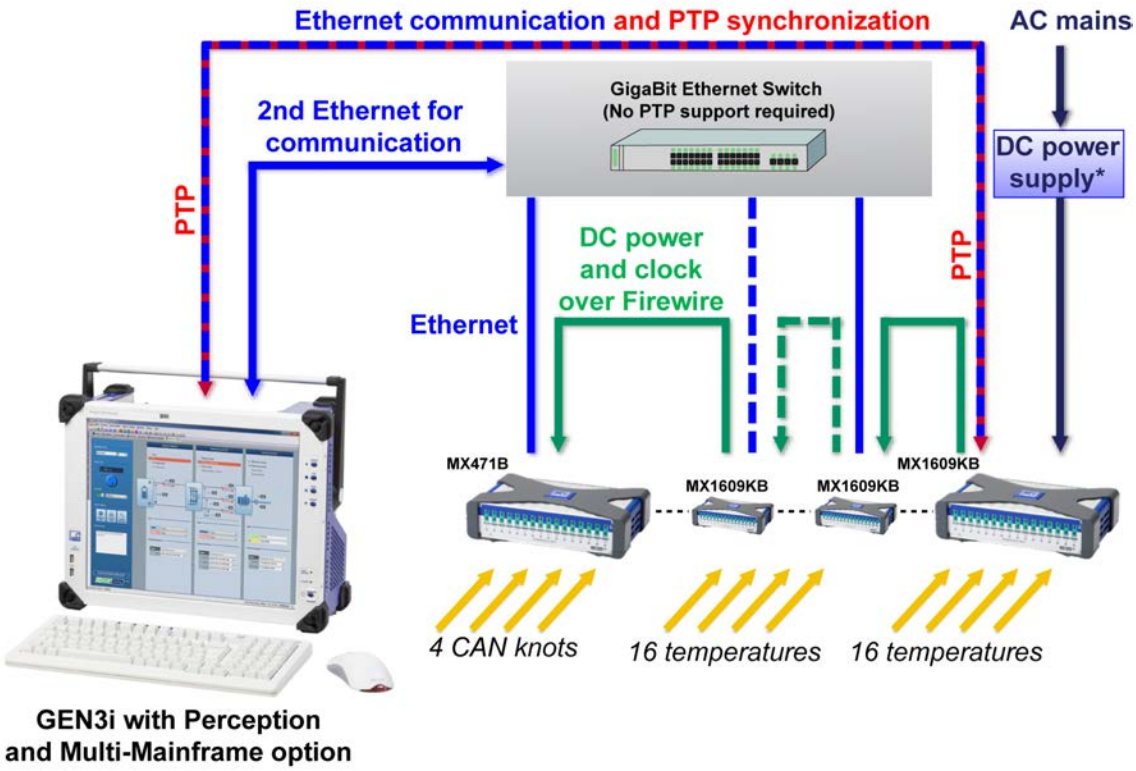


Figure F.13: GEN3i with multiple QuantumX "B" version modules

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i/GEN7iA.*

Note ** Multiple QuantumX modules requires more than one power supply; see QuantumX documentation.*

Note *** **All** modules must be "B" versions; one module must set to "clock master" and connected to the GEN3i PTP Ethernet.*

HINT/TIP

This setup uses two network ports on the GEN3i PC section.
Use fixed IP address setup with different base IP address and non-overlapping IP-ranges (Combination of base IP address and net mask) for each of the GEN3i network ports to make sure the setup always works.

Example setup:	
GEN3i network 1:	192.168.1.10 mask 255.255.255.0
GEN3i network 2:	192.168.2.10 mask 255.255.255.0
QuantumX module 1:	192.168.1.11 mask 255.255.255.0
QuantumX module 2:	192.168.2.11 mask 255.255.255.0

Background network details
If the network ports are configured for DHCP setup, each of the connections using the APIPA protocol to find a free IP address. As the two network ports are not linked together the APIPA protocol on the PTP port does not detect the address used any of the network devices on the second network port. At random the PTP QuantumX system might end up with exactly the same network IP address as any of the other QuantumX systems. If this happens the two systems sharing the same IP address are not uniquely addressable anymore and the communication fails.

F.3.5 GEN3i/GEN3iA/GEN7i/GEN7iA with PTP network switch and four or more of QuantumX "B" version modules

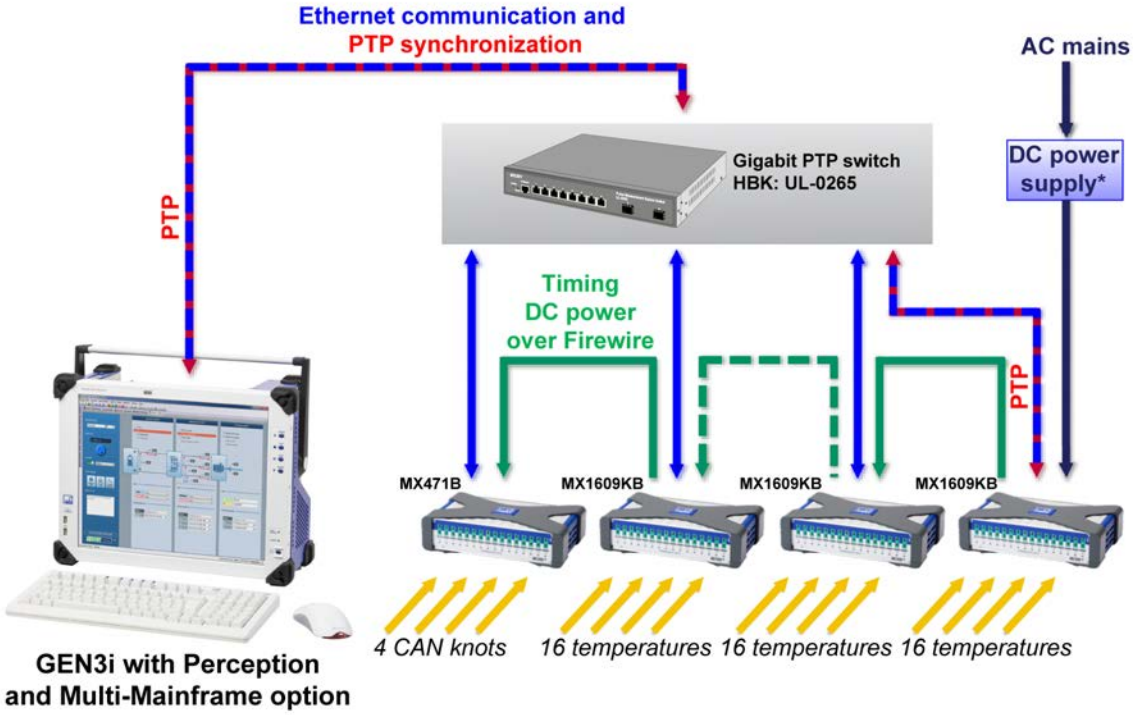


Figure F.14: GEN3i with multiple MX1609KB/MX1609TB - Using PTP switch

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i/GEN7iA.*

Note ** Multiple QuantumX modules requires more than one power supply; see QuantumX documentation.*

HINT/TIP

This setup is preferred as it doesn't require any manual network setup. However it does require a PTP switch.

HINT/TIP

Perception V6.72 allows the PTP synchronization within the GEN series mainframes to be reduce to lower accuracies. With the lower sample rates used within the QuantumX this might be very acceptable within your application. Normal switches without PTP support can then be used without PTP synchronization error reports.

F.3.6 GEN7tA/GEN17tA with single QuantumX "B" version module

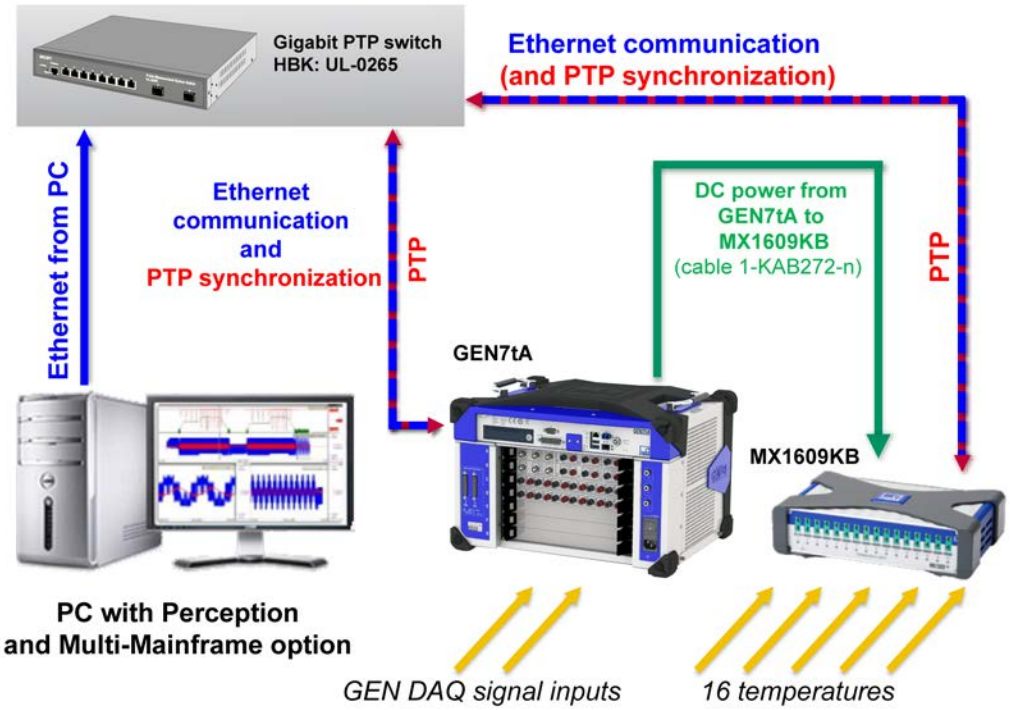


Figure F.15: GEN7tA with single QuantumX "B" version module

Note *Setup only shows GEN7tA. GEN7tA can be replaced by GEN17tA.*

F.3.7 GEN7tA with multiple QuantumX "B" version modules

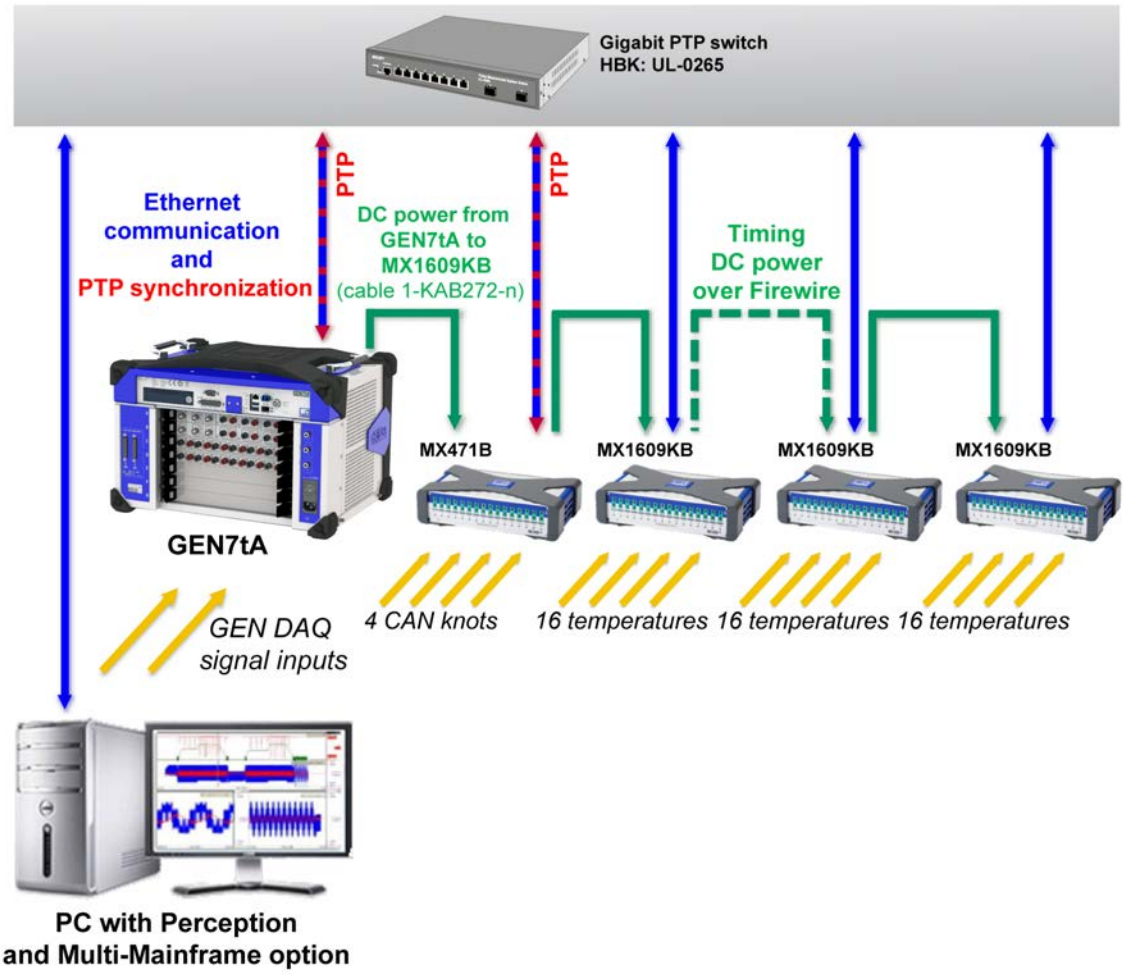


Figure F.16: GEN7tA with multiple MX1609KB/MX1609TB - Using PTP switch

Note *Setup only shows GEN7tA. GEN7tA can be replaced by GEN17tA.*

Note ***** *Multiple QuantumX modules requires more than one power supply; see QuantumX documentation.*

F.3.8 Genesis and QuantumX Setup using IRIG-to-PTP Bridge

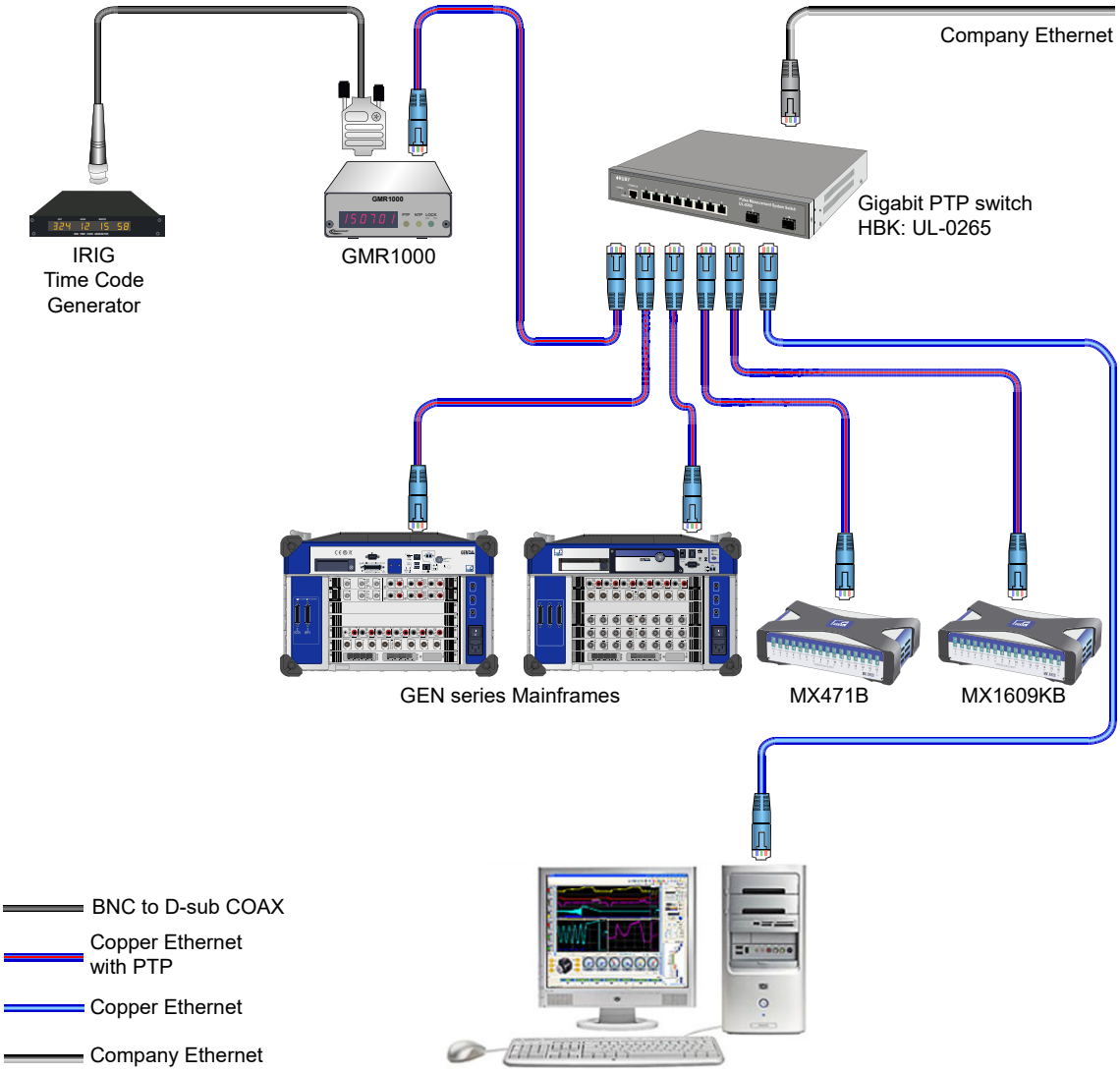


Figure F.17: IRIG setup for tethered mainframes and QuantumX

Note *GEN7tA can be replaced by any mainframe*

Settings in Perception

- Use the RJ45 connector for PTP support **(PTP 1)**.

F.3.9 Genesis and QuantumX setup using GPS-to-PTP bridge

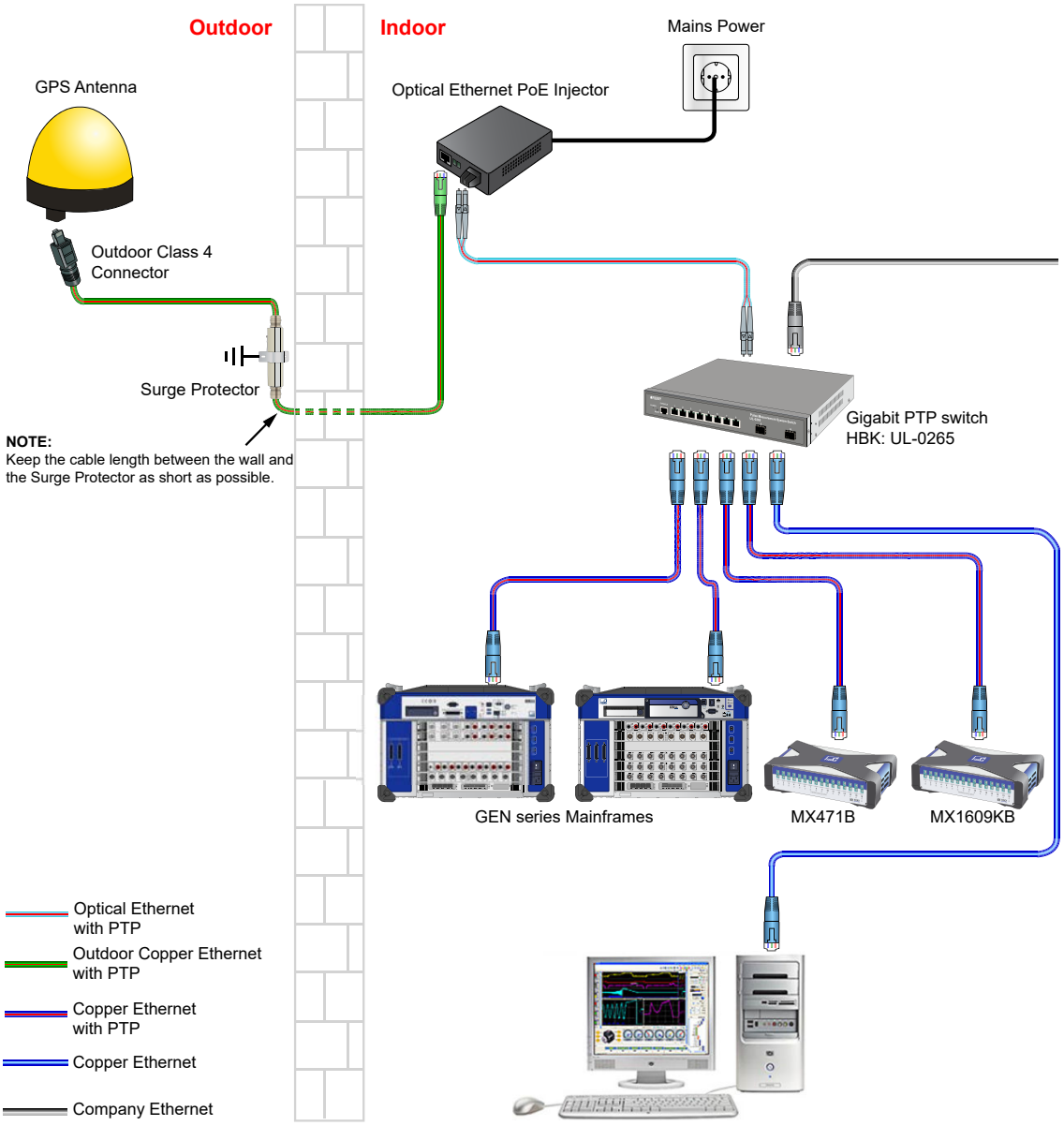


Figure F.18: GPS setup for tethered mainframes and QuantumX

F.3.10 Genesis using GPS-to-PTP bridge with Master/Sync Connected Systems

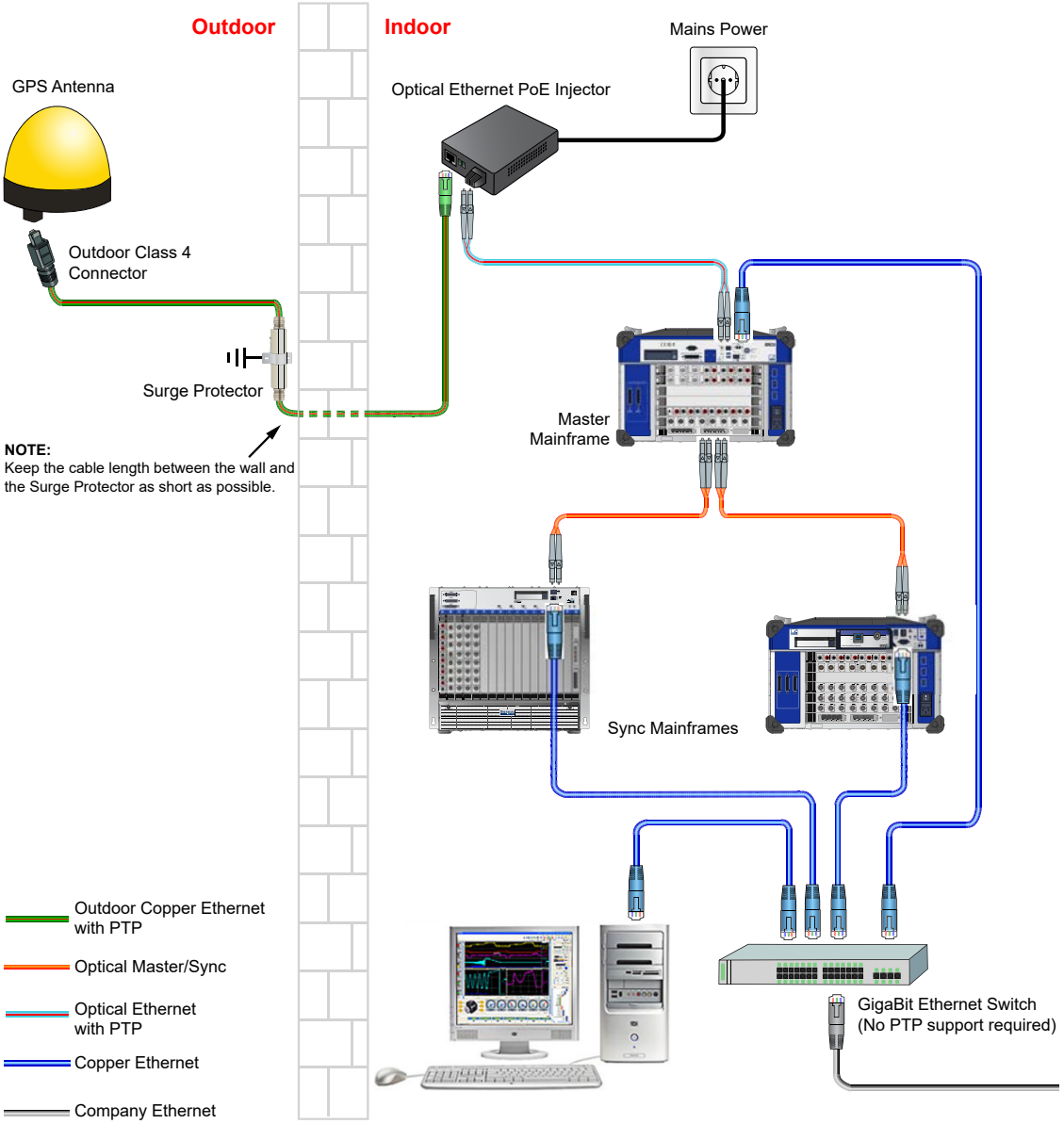


Figure F.19: GPS setup for tethered mainframe with Master/Sync connected Sync mainframes

F.3.11 PTP Grandmasters

IRIG or GPS to PTP bridge

- Successfully tested Symmetricom SyncServer® S350
- Equivalent model Symmetricom Xli GPS receiver (Model 1510-713)

Figure F.20: Symmetricom Xli GPS receiver

For more information please refer to: www.microsemi.com/

GPS to PTP Bridge

Successfully tested OTMC 100i Grand Master Clock.

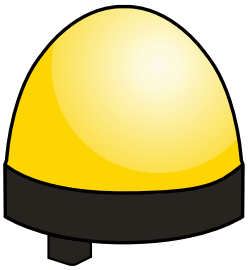


Figure F.21: OTMC 100i

For more information, please refer to: www.omicron-lab.com/

IRIG to PTP bridge

Successfully tested GMR1000 Master Clock.

Figure F.22: GMR1000

For more information, please refer to:
www.masterclock.com/products/master-clocks/gmr1000

F.3.12 HBK UL-0265 gigabit PTP switch

The HBK UL-0265 gigabit PTP switch has been successful tested with GEN DAQ and QuantumX systems.

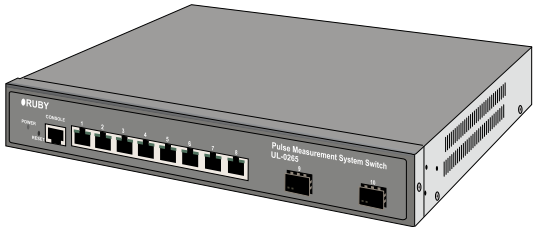


Figure F.23: HBK UL-0265 gigabit PTP switch

F.3.13 Siemens Scalance XR234-12M PTP switch

Successfully tested Siemens scalance xr324-12m

Figure F.24: Siemens scalance xr324-12m

For more information, please refer to the Siemens Scalance XR234-12M product page:
support.industry.siemens.com/cs/pd/515156?pdti=pi&dl=en&lc=en-NO

F.3.14 PTP configuration errors

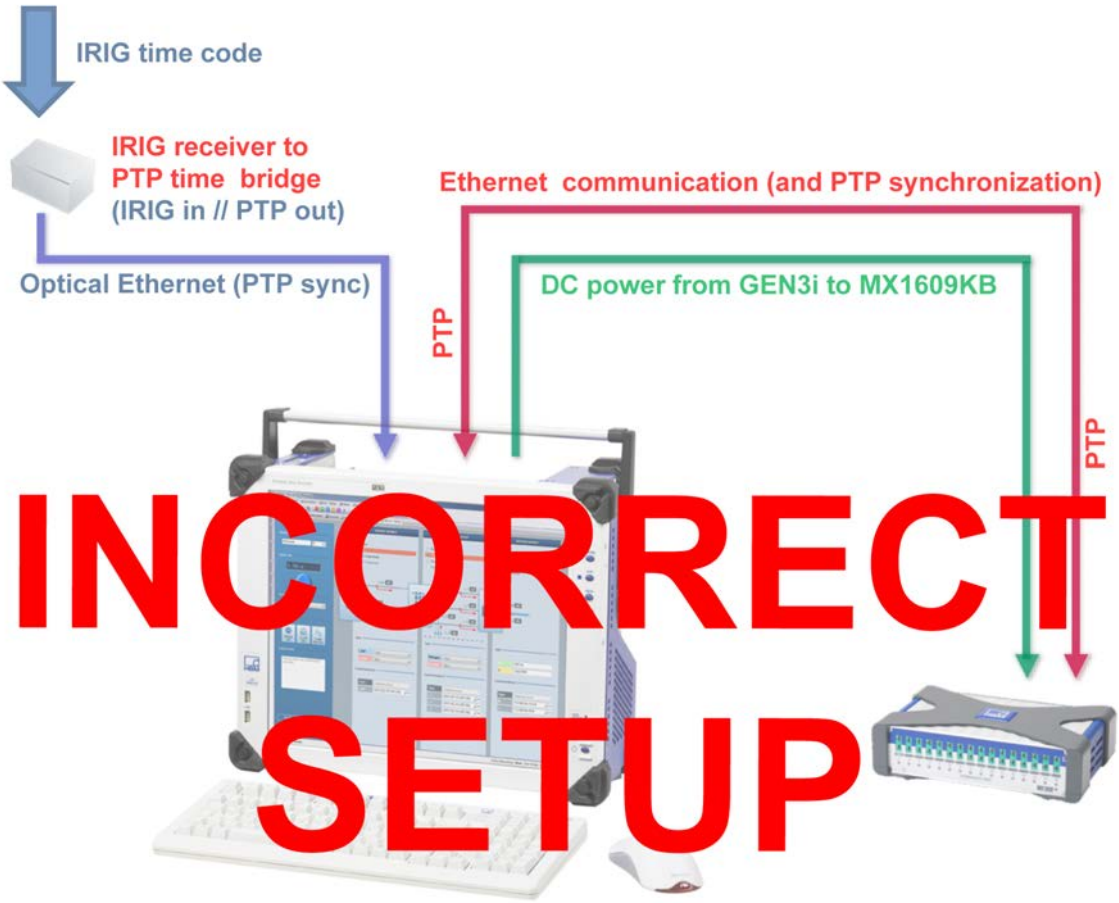


Figure F.25: Example of incorrect PTP usage

This is not possible!

- Set "Sync Source“ to PTP1 (RJ45) **or** to PTP2 (optical)
- Both at the same time is not possible: we don’t “bridge” PTP1 to PTP2

G Application Specific Usage

G.1 Calculating maximum fiber cable length

Maximum optical fiber length is determined by two major factors: optical loss and bandwidth limit. These types of optical fiber performance and quality are defined in the ISO standard ISO/IEC 11801.

OMx/OCx = ISO/ IEC 11801 standard (optical fiber type)	For wave-length	Optical power budget	Cable loss	Coupler loss. ANSI/TIA/ EIA-568-A	BW Length limit
OM1 = Multi Mode 62.5/125 µm	850 nm	8 dB	-3.5 dB/km	-0.75 dB	200 MHz*km
OM2 = Multi Mode 50/125 µm	850 nm	8 dB	-3.5 dB/km	-0.75 dB	500 MHz*km
OM3 = Multi Mode 50/125 µm laser optimized fiber	850 nm	8 dB	-3.5 dB/km	-0.75 dB	2000 MHz*km
OM4 = Multi Mode 50/125 µm laser optimized fiber	850 nm	8 dB	-3.5 dB/km	-0.75 dB	4700 MHz*km
OS1 = Single Mode 9/125 µm	1310 nm	10 dB	-1 dB/km	-0.75 dB	N/A
OS2 = Single Mode 9/125 µm	1310 nm	10 dB	-0.4 dB/km	-0.75 dB	N/A

Note *Table shows worst-case specifications.*

Standard GHS systems use VCSEL 850 nm optical transmitters/receivers; they have an optical power budget of 8 dB. Calculating the maximum length of optical cable can be done in the following manner:

Optical budget GHS system 850 nm	:	8 dB
Maximum fiber cable length	:	$L_{optical}$ (km)
Fiber cable loss	:	-3.5 dB/km
Number of couplers	:	c
Coupler loss	:	-0.75 dB
Safety margin for aging and repair	:	-3 dB

$$L_{optical} = -\frac{8dB + (c * -0.75dB) + (-3\,dB)}{-3.5dB}\ (km)$$

This formula also applies to Single Mode systems

For example, if two couplers are used in the cable, c = 2, the maximum length would be $L_{optical}$ = 1 km

The second limiting factor for cable length is fiber cable bandwidth.
Bandwidth limit is caused by light pulse dispersion in the optical fiber; this only affects Multi Mode fiber systems.
This limit is the product of the GHS system's maximum signaling speed and the defined fiber cable bandwidth.

GHS signaling speed over optical fiber	:	1000 MHz
OM class defined bandwidth	:	BW
Maximum fiber cable length	:	L_{BW} (km)

$$L_{BW} = \frac{BW}{1000MHz}\ (km)$$

For example, if an OM2-type cable is used, the maximum length will be L_{BW} = 0.5 km

The maximum optical fiber length that can be used in a setup is the shortest outcome of $L_{optical}$ or L_{BW}

If the two examples above are followed, the optical fiber length must be limited to L_{BW} = 0.5 km

G.2 Wake-on-LAN support (WOL)

Several of the GEN series mainframes support Wake-on-LAN features (WOL). WOL is only supported on copper or optical networks. WOL is not supported by wireless networks.

At the time of this manual's release, the following mainframes support WOL:

- GEN2tB
- GEN3i
- GEN3iA
- GEN3t
- GEN4tB
- GEN7i
- GEN7iA
- GEN7tA
- GEN17tA

WOL can turn the GEN series mainframe on from the “S5”' power state when power is connected to the mainframe and the power switch at the net entry is switched to the “1” or “on” position. In this state, the power can be turned on by sending a “magic packet” to one of the mainframe's wired network ports. The magic packet must contain the MAC or Physical address of the connected network port.

Generating a magic packet can be done with third party tools or custom-built applications. Search the internet using “Wake-on-LAN” and several freeware tools show up. HBM is not responsible for any of the (freeware) tools found using this search method.

WARNING

Whenever a mainframe is powered off by using a forced power down (keeping the standby button pressed for five seconds), the WOL feature is disabled. Always allow the system to power down normally to enable the WOL feature.

HINT/TIP

When a mainframe's power is interrupted externally, re-applying power to the mainframe immediately starts the mainframe (no WOL magic packet is required).

WAN (Wide Area Network) support

As the name WOL indicates (Wake-on-LAN), there is no direct support outside the boundaries of your LAN (Local Area Network). A LAN typically ends as soon as routers or layer 3 switches are used to transfer network data from point A to point B. Routers are typically used to access the internet. Layer 3 switches are typically used to control network traffic within larger facilities to avoid unwanted network traffic on different segments within the network.

- Without using routers or layer 3 switches, magic packets can be sent within a LAN without problems.
- When your company uses layer 3 switches, your IT department might need to help you set up their layer 3 switches to allow WOL magic packets to reach your remote GEN series system.
- Sending the magic packets for WOL from a location outside the LAN (WAN setup) may require a VPN connection to the target LAN or special settings to the LAN internet router.

For additional information on Wake-on-LAN, please refer to:
en.wikipedia.org/wiki/Wake-on-LAN

G.2.1 Locating GEN3i, GEN3iA, GEN7i and GEN7iA MAC/Physical address

For **GEN3i**, **GEN3iA**, **GEN7i** and **GEN7iA**, the MAC/Physical address can be found in Windows® in the following manner:

1. Connect the required network port.
2. Go to Windows® **Network and Sharing Center**. Select **Local Area Connection (A)**.

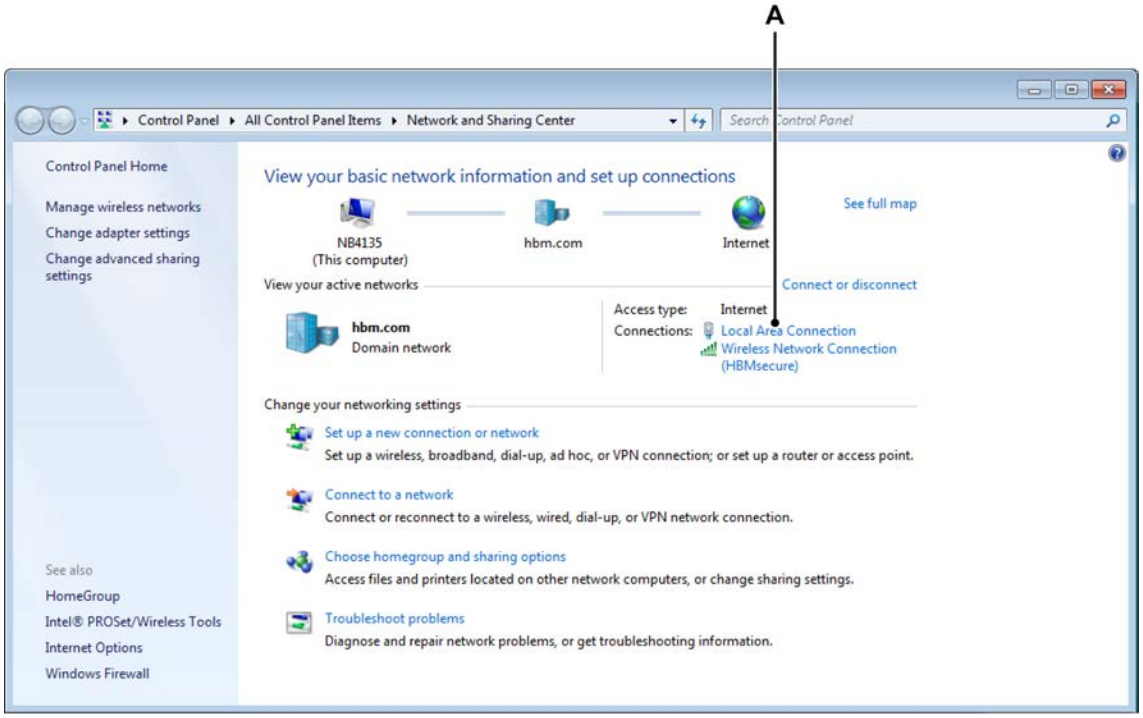


Figure G.1: Network and Sharing Center

A Local Area Connection

3 The **Local Area Connection Status** dialog opens. Select **Details**.

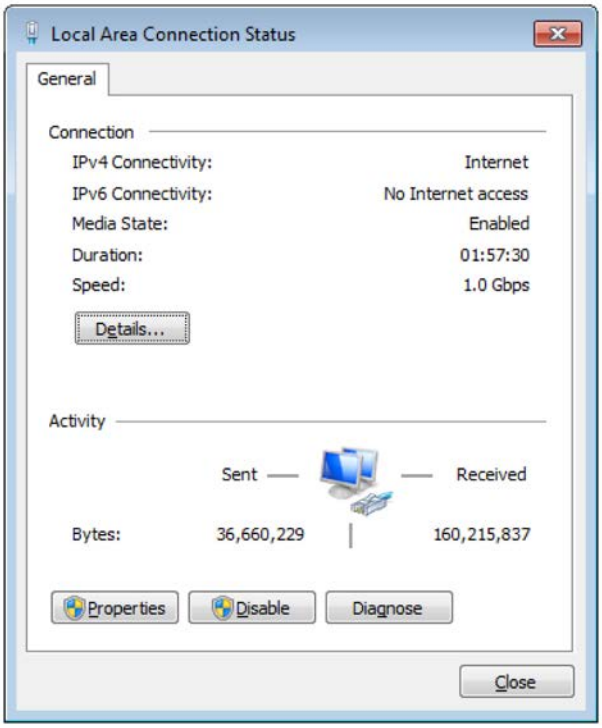


Figure G.2: Local Area Connection Status

4 The **Network Connection Details** dialog opens.

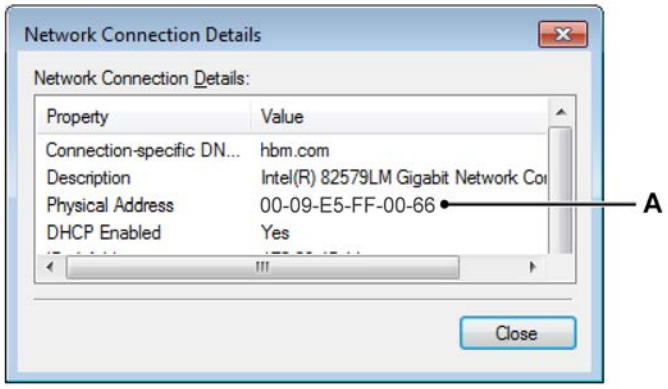


Figure G.3: Network Connection Details

A MAC/Physical address

The MAC/Physical address of the selected network connection is displayed in the **Network Connection Details** dialog as a twelve character string.

G.2.2 Locating GEN3t, GEN7tA and GEN17tA MAC/Physical address

For **GEN7tA** and **GEN17tA**, the MAC/Physical address can be found in Perception in the following manner:

1 Start the Perception software

2 Connect to either GEN7tA or GEN17tA.

3 Enable the **Properties Window** (see Figure G.5); this can be found in the Perception “Windows” menu.

4 Open the **Hardware** window. Select the target mainframe **(A)**. Right click on the mouse to open the context menu. Select **Mainframe view (B)**.

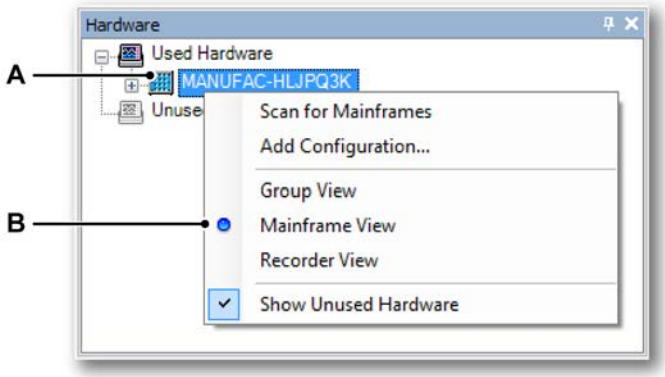


Figure G.4: Hardware window in Perception

A Target mainframe

B Mainframe view

5 The MAC/Physical address of the selected network connection is displayed in the **Properties window** as a twelve character string.

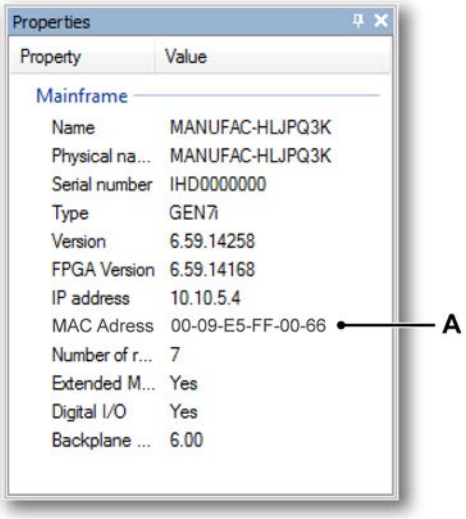


Figure G.5: Properties window in Perception

A MAC/Physical address

G.3 Configuring an encoder with direction and reset

Pins and Connectors:

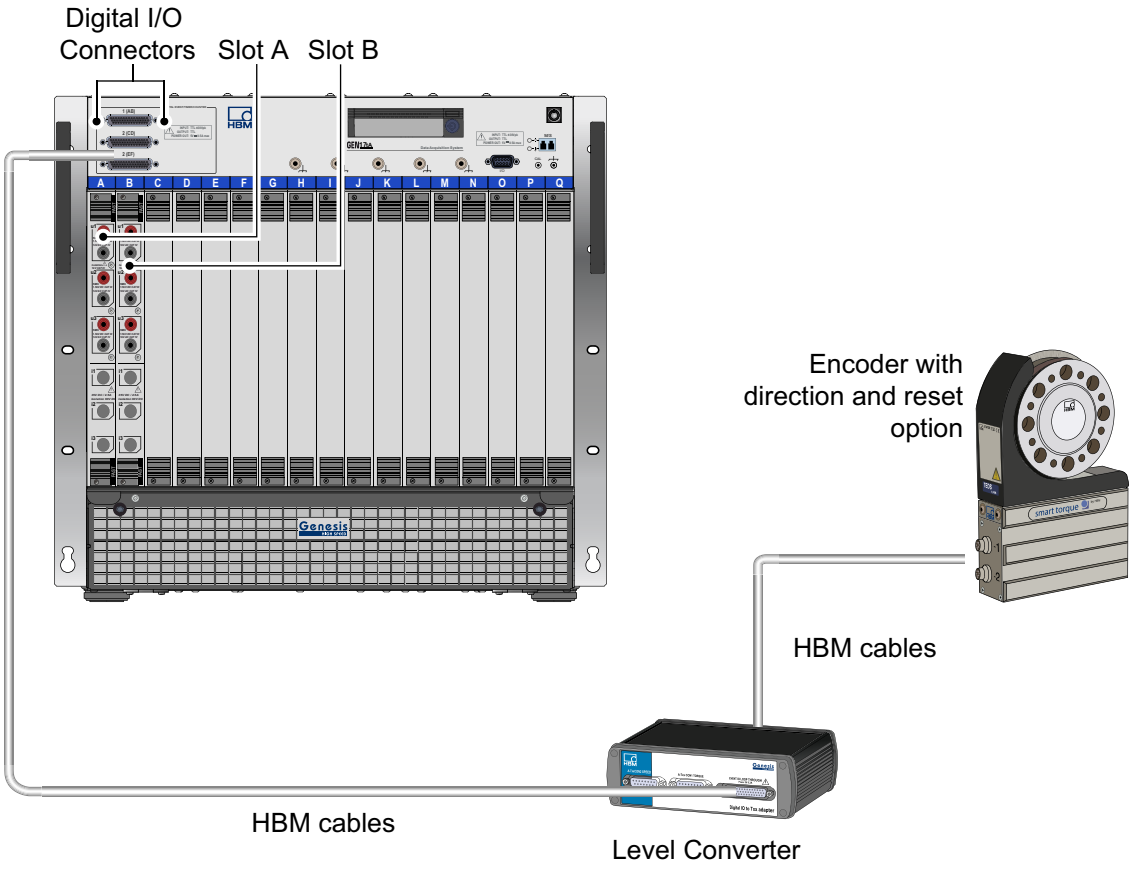


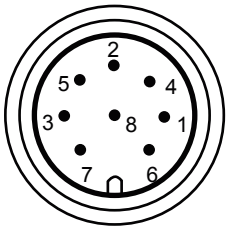
Figure G.6: Connecting Encoders with reset and direction options to a GEN17tA

The following descriptions shows how to configure the encoder:

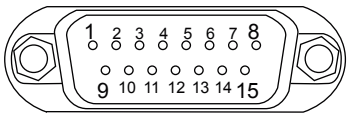
- Pins and connectors from encoder to level converter (see chapter "From encoder to level converter" on page 488)
- Pins and connectors from level converter to digital I/O connector on the mainframe (see chapter "From level converter to Digital I/O connector on the mainframe" on page 490)

G.3.1 From encoder to level converter

The Level converter 1-G070-2 offers the possibility to connect two speed connectors to two different encoders. In this example, the B-TxxCON2 Speed connector of the Level Converter is used. HBM cables 1-KAB149-6 and 1-KAB163-6 are designed to be used with the Level Converter. KAB149 is compatible with the Torque interface connector; KAB163 is compatible with the Speed/RPM interface connector.



Top view



T12 speed	Txx adapter speed

Plug pin	**Assignment**	**TXX adapter Speed**
1	Rotational speed measurement signal (pulse string, 5 V; 0°)	Pin 12
2	Reference signal (1 pulse/revolution, 5 V)	Pin 2
3	Rotational speed measurement signal (pulse string, 5 V; 90° phase shifted)	Pin 15
4	Reference signal (1 pulse/revolution, 5 V)	Pin 3
5	Not in use	
6	Rotational speed measurement signal (pulse string, 5 V; 0°)	Pin 13
7	Rotational speed measurement signal (pulse string, 5 V; 90° phase shifted)	Pin 14
8	Operating voltage zero	Pin 8
	Shielding connected to housing ground	

The signal from the encoder has the following characteristics:

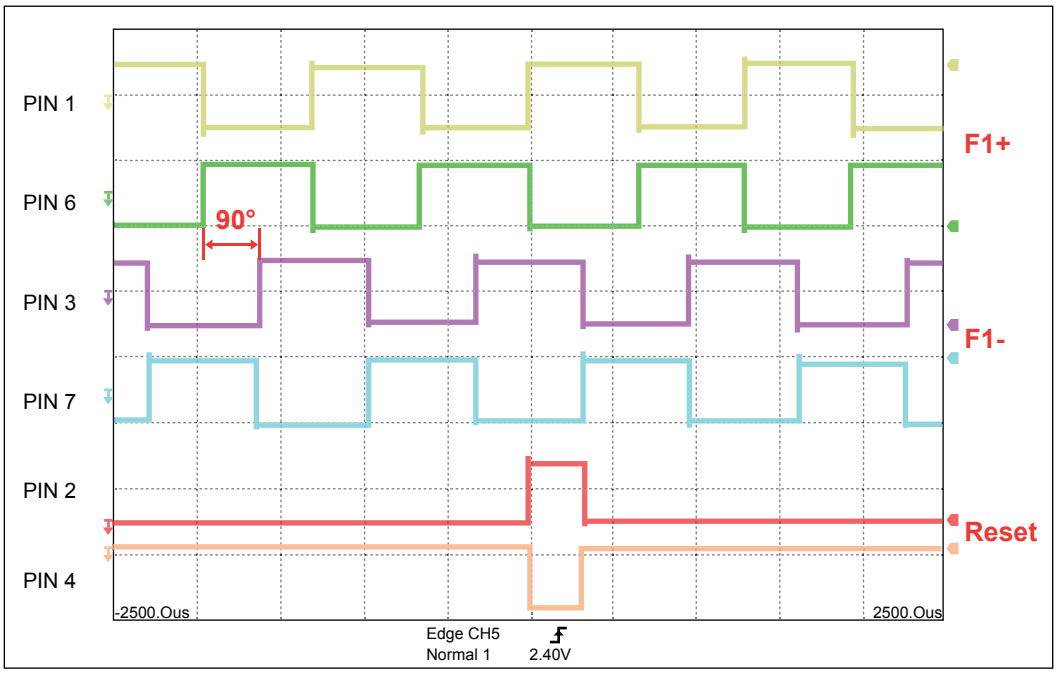


Figure G.7: Rotational speed signals at level converter

G.3.2 From level converter to Digital I/O connector on the mainframe

This cable is included with the level converter (1-G070-2).

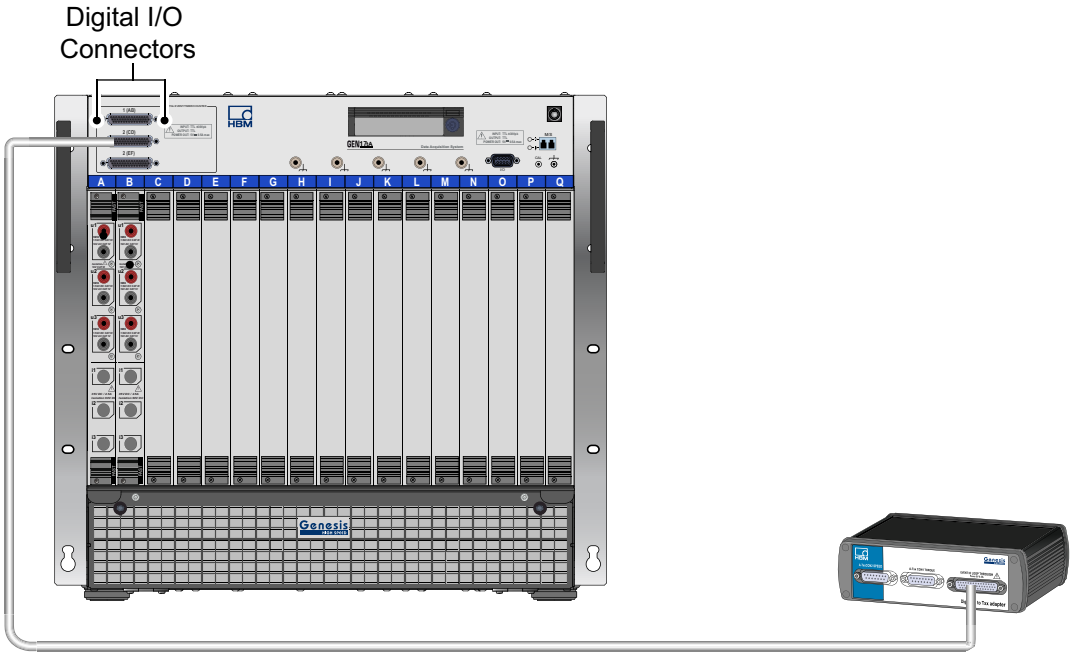
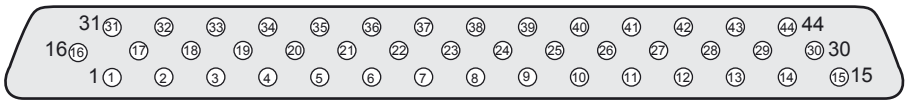


Figure G.8: Connecting a GEN17tA from level converter to a digital I/O connector

G.3.3 Activate Digital I/O channels with Perception

In order to activate the Digital I/O channels, including the counter/timer channels, a module that supports the Digital I/O connector must be installed. Not all input modules in the GEN series family support the Digital I/O connector. In this example, the two 1kV modules which activate four counter timer channels (two counter channels per module) are used.

The Timer/Counter channels that are active depend on which pins of the Digital I/O connector are used:



A
- **PIN 1 - Event Input 1A & Reset Timer/Counter 2A**
- **PIN 2 - Event Input 2A & Direction Timer/Counter 2A**
- **PIN 3 - Event Input 3A & Clock Timer/Counter 2A**
- PIN 4 - Event Input 4A
- PIN 5 - Event Input 5A
- PIN 6 - Event Input 6A
- PIN 7 - Event Input 7A
- PIN 8 - Event Input 8A
- PIN 9 - Event Input 9A

B
- **PIN 10 - Event Input 10A & Reset Timer/Counter 1A**
- **PIN 11 - Event Input 11A & Direction Timer/Counter 1A**
- **PIN 12 - Event Input 12A & Clock Timer/Counter 1A**

C
- **PIN 13 - Event Input 1B & Reset Timer/Counter 2B**
- **PIN 14 - Event Input 2B & Direction Timer/Counter 2B**
- **PIN 15 - Event Input 3B & Clock Timer/Counter 2B**
- PIN 16 - Event Input 4B
- PIN 17 - Event Input 5B
- PIN 18 - Event Input 6B
- PIN 19 - Event Input 7B
- PIN 20 - Event Input 8B
- PIN 21 - Event Input 9B

D
- **PIN 22 - Event Input 10B & Reset Timer/Counter 1B**
- **PIN 23 - Event Input 11B & Direction Timer/Counter 1B**
- **PIN 24 - Event Input 12B & Clock Timer/Counter 1B**
- PIN 25 - Event Input 13B
- PIN 26 - Event Input 14B
- PIN 27 - Ground
- PIN 28 - Ground
- PIN 29 - Ground
- PIN 30 - Ground
- PIN 31 - Event Input 15B & External Stop B
- PIN 32 - Event Input 16B & External Start B
- PIN 33 - Event Input 13A
- PIN 34 - Event Input 14A
- PIN 35 - Event Input 15A & External Stop A
- PIN 36 - Event Input 16A & External Start A
- PIN 37 - Event Output 2B
- PIN 38 - Event Output 1B
- PIN 39 - Event Output 2A
- PIN 40 - Event Output 1A
- PIN 41 - Ground
- PIN 42 - Ground
- PIN 43 - +5 V Power
- PIN 44 - +5 V Power

For connectors supporting slot C/D and E/F replace A with C & E and B with D & F

Figure G.9: Pin diagram for Digital Event/Timer/Counter connector

A Card A-Txx CON2 Speed Channel A9

B Card A-Channel A8

C Card B-Txx CON2 Speed Channel B9

D Card A-Channel B8

In this example (see Figure G.9), Recorder A and Recorder B are 1kV modules (six channels each). The event channels supported by the module are assigned the next available channel number after the analog channels. In this case, that is Channel 7; for Recorder B, the event channels are assigned channel names of Ev B7-01 to Ev B7-16.

The two counter timer channels supported by Recorder B are Channel B8 (Timer/Counter2A, see Figure G.9) and Channel B9 (Time/Counter2A, see Figure G.9). In Perception, the channels are named Ch B8 and Ch B9 (see Figure G.10).

For this example, connect one B-Txx CON2 Speed and wire it to the Ch B9 counter (Pins 13, 14, 15 on the digital input connector).

Note *Perception allows you to view each of the inputs individually as an event channel in addition to seeing the counter result.*

The reset signal is Ev B7_01, the input F1- is Ev B7_02 and the input F1+ is Ev B7_03. If you only need to view the Timer/Counter result and have no interest in the individual signals, do not activate the event channels. This will decrease the size of the final data file by not recording channels that are not needed.

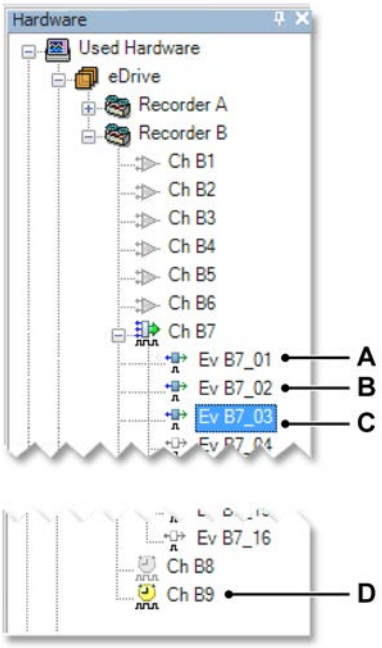


Figure G.10: Channels in Perception

A Reset

B F1-

C F1+

D B-Txx CON2 Speed

To activate Channel 8 or Channel 9 in Perception

1 Change the resolution of Recorder B to **18 bit**

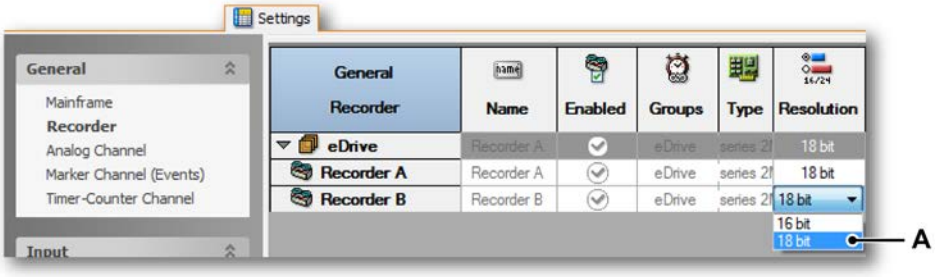


Figure G.11: Activating Channel 8 or Channel 9 in Perception

A Recorder B with 18 bit resolution

2 Configure the B-Txx CON2 in Ch B9 (Perception):

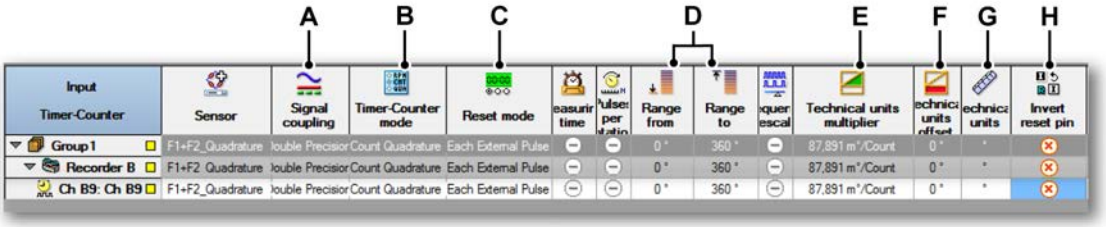


Figure G.12: Configuration of the B-Txx CON2 connector in Perception

A **Signal coupling mode** In quadrature mode, the counter supports three ways of tracking the quadrature states defined by the signal coupling.

- Single precision
- Double precision
- Quad precision

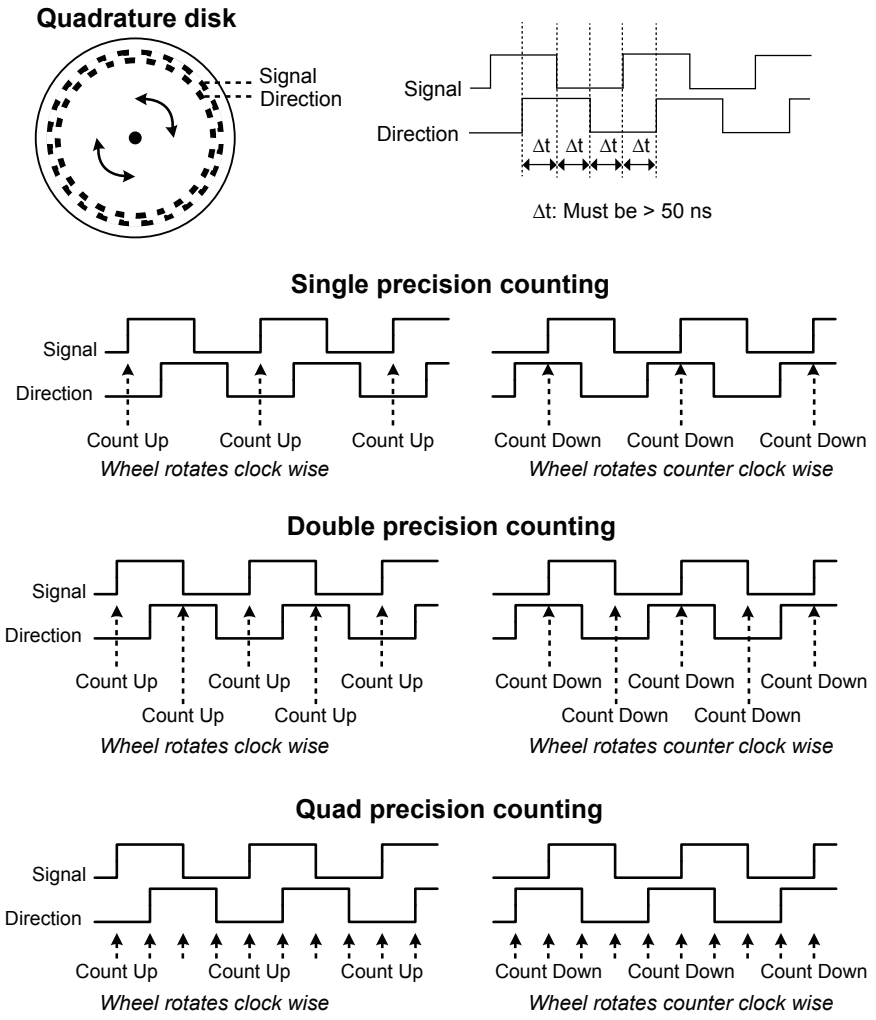


Figure G.13: Signal coupling/precision modes

- In **single precision**, the counter only increments/decrements on the rising edge of the signal input. This is the default traditional quadrature count mode.
- In **double precision**, the counter increments/decrements on both the rising and falling edge of the signal input. As a result, smaller rotations can already be detected. For every full rotation the counter counts double the values compared to the single precision signal coupling mode.
- In **quad precision**, the counter increments/decrements on every rising and falling edge of both the signal and direction input. As a result, even smaller rotations can already be detected. For every full rotation the counter counts quadruple values compared to the single precision signal coupling mode.

Unless other requirements do not allow the quad precision mode to be selected, using this mode is strongly advised due to it higher accuracy.

B **Timer Counter mode:** Count Quadrature -> counters monitor the transition of the four different states the signal can be in.

C **Reset Mode:** Each External Pulse -> resets the counter every time we receive a pulse in Reset input.

D **Range from/to** 0 to 360°

E **Technical units multiplier: 87.891** m°/Count
This setting assumes the use of an encoder with **4096** pulses/rotation
1024 pulses [from encoder] x 4 transitions [quad precision selected].

F **Technical units offset:** 0°

G **Technical units:** ° (degrees)

H **Invert reset pin:** Deactivated* -> A High Level of Reset input is needed to reset the counter to 0.

Note ***** *The counter works ONLY when the reset input is set to Low. After you reset the counter with a High Level, you need to return the reset level to Low to continue the measurement. In other words, your reset signal needs to be a really short impulse in order to minimize the amount of time that the counter is not counting.*

3 Another possibility is to configure the counter channel using the Perception Sensor Database:

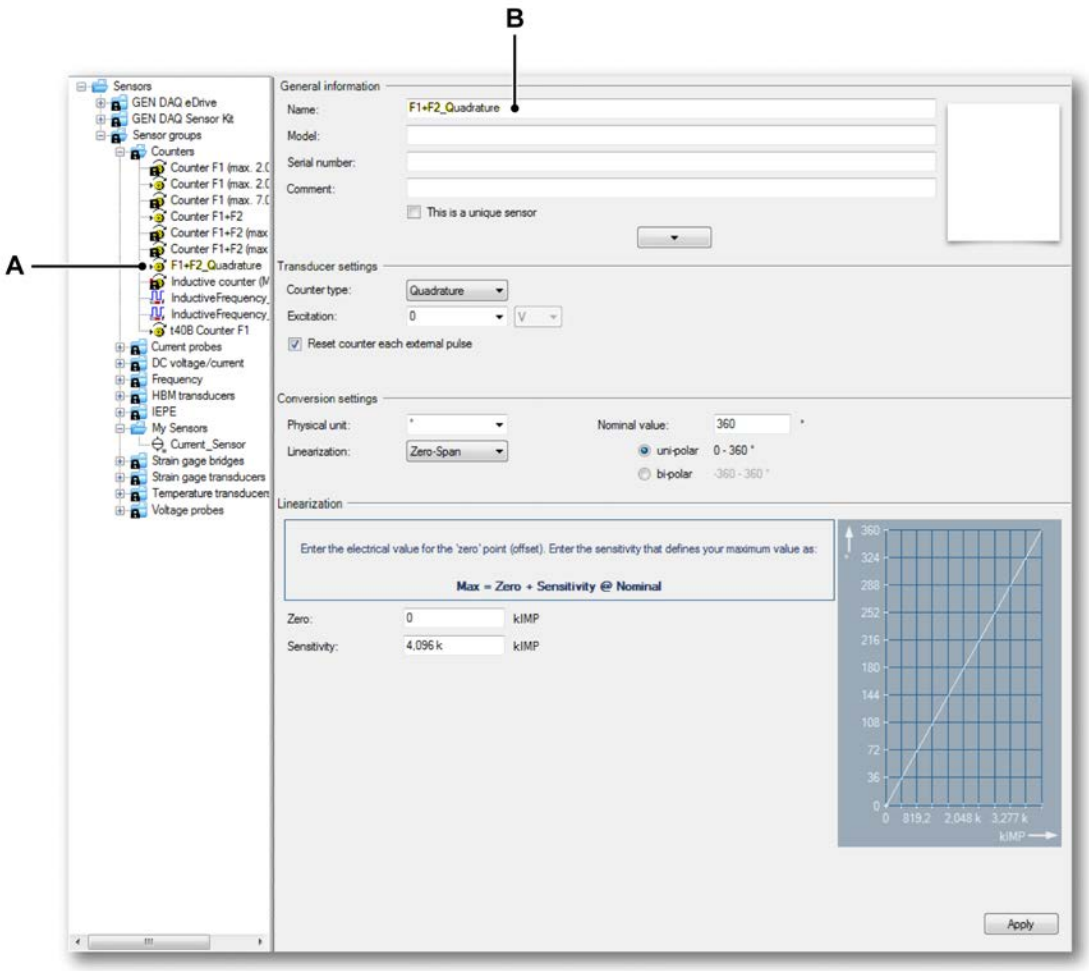


Figure G.14: Perception Sensor Database (Configuring the counters channel)

A Sensor goups/Counters: F1 + F2 Quadrature

B General information/Name: F1 + F2 Quadrature

Assign the sensor **F1+F2_Quadrature** sensor to Channel Ch B9.

Note *Disable the **Invert reset pin** option manually. All other settings are set correctly after the sensor has been selected.*

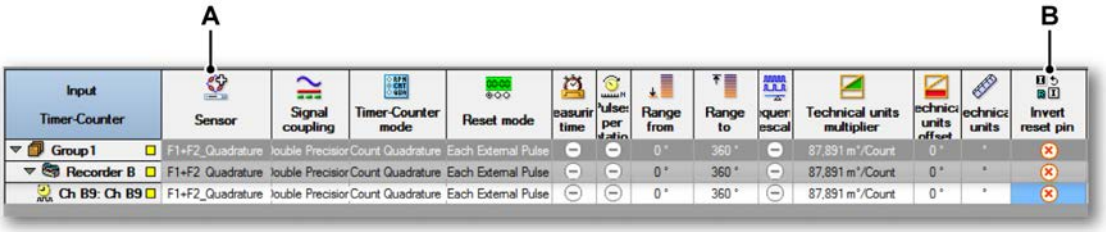


Figure G.15: Configuration of the B-Txx CON2 connector in Perception

A Sensor

B Invert reset pin

The settings of the the frequencies **F1+**, **F1-**, reset and the counter signal on **ChB9** are displayed in the following window (see Figure G.16)

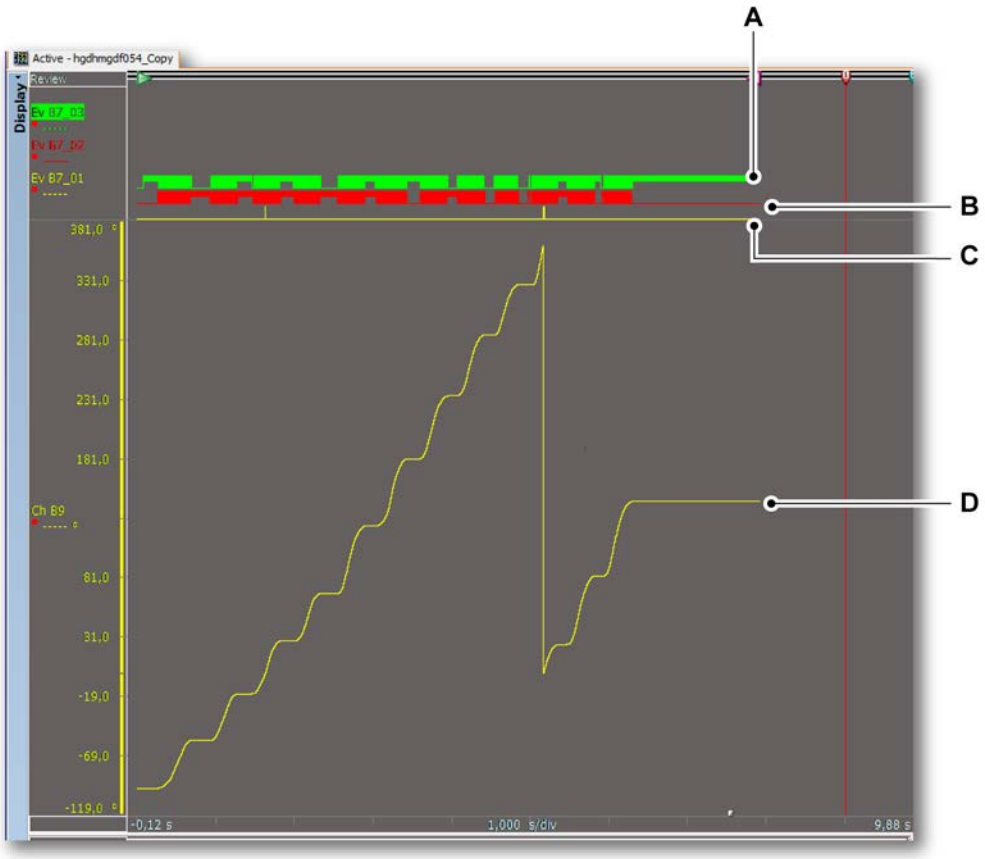


Figure G.16: F1+, F1- , Reset Angular variation (Perception)

A F1+

B F1-

C Reset

D Angular variation

H Disk Storage Technology

H.1 Most used RAID modes

RAID (Redundant Array of Independent Disks) is a technology that is used to increase the performance and/or reliability of data storage. A RAID system consists of two or more disks working as a single logical unit for the purposes of data redundancy or performance improvement. These disks can be solid state or hard disks. There are different RAID levels, each optimized for a specific situation. Some companies come up with their own unique implementations.

HINT/TIP

Sometimes disks in a RAID system are defined as JBOD, which stands for “Just a Bunch Of Disks”. This means that those disks do not use a specific RAID level and act as stand-alone disks. This is often done for drives that contain swap files or temporary data.

WARNING

RAID is no substitute for back-up!
All RAID levels offer protection from a single drive failure, except RAID 0. For complete security, back-up of the data from a RAID system is always required.

- The back-up will come in handy if two or more drives fail simultaneously because of a power spike.
- It is a safeguard if the storage system is lost/fails all together.
- Back-ups can be kept off-site at a different location in case of a natural disaster or fire destroying your workplace.

The most popular RAID levels are:

- RAID 0 – Striping (see "RAID 0 – Striping" on page 501)
- RAID 1 – Mirroring (see "RAID 1 – Mirroring" on page 502)
- RAID 5 – Striping with distributed parity check (see "RAID 5 – Striping with parity" on page 503)
- RAID 10 – Combining RAID 0 & RAID 1 (see "RAID level 10 – Combining RAID 0 & RAID 1" on page 504)

	RAID 0	RAID 1	RAID 5	RAID 10
Minimum no. of disks required	2	2	3	4
Required no. of disks to extend array	1	N/A	1	2
Maximum volume size	Sum of Disks	One disk size	Sum Of Disks -1	Sum of Disks /2
Redundant storage	0%	100%	1 parity disk/ array	100%
Approximate storage speed	Sum of disks	No. of Disks/2	No. of Disks - 1	No. of Disks/2
Supported loss of disks	0	1	1	1

H.1.1 RAID 0 – Striping

In a **RAID 0** system, storage is split into blocks that are written split across all the drives in the array. Using more disks in one RAID 0 system offers higher storage rates. The performance also depends on the RAID controller used.

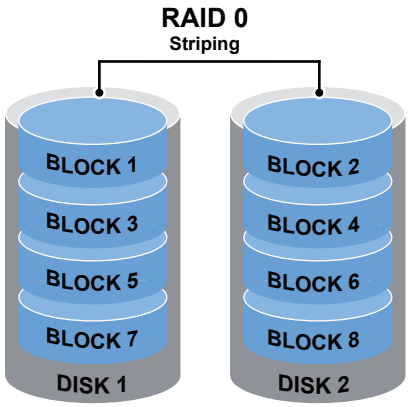


Figure H.1: RAID 0 – Striping

Advantages

- Great performance, both in read and write operations.
- All storage capacity is used; there is no disk overhead.
- Volume size grows with every extra disk added.
- The technology is easy to implement.

Disadvantages

- Not fault-tolerant. If one disk fails, all data is lost.

WARNING

RAID 0 systems should not be used on mission-critical systems.

H.1.2 RAID 1 – Mirroring

In a **RAID 1** system, data is stored twice by writing to both a (set of) data disk(s) and a (set of) mirror disk(s). If one disk fails, the controller uses either the data disk or the mirror disk for data recovery and continues operation. You can only use two disks for a RAID 1 array.

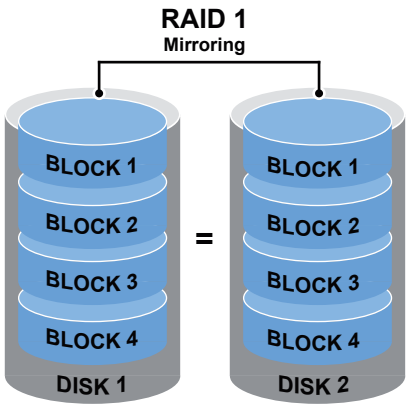


Figure H.2: RAID 1 – Mirroring

Advantages

- Offers excellent read speed and a write speed that is comparable to that of a single disk.
- If a disk fails and is replaced by a new disk, data does not have to be rebuilt; it just has to be copied to the replacement disk.
- RAID 1 is very simple technology.

Disadvantages

- Volume size limited to one disk
- Ineffective storage capacity; only half of the total disk capacity is available.

H.1.3 RAID 5 – Striping with parity

RAID 5 arrays require at least three disks. Data blocks are subdivided (striped) and written to two (or more) drives. Parity for the stored data blocks is calculated and stored on an additional drive. Parity is not stored on a dedicated drive but spread across all the drives in the array. Since parity is used, a stripe set can withstand a single disk failure without losing data. Although RAID 5 can be achieved in software, a hardware controller is recommended to support the parity calculations in hardware. Extra cache memory is often used on these controllers to improve the write performance. RAID 5 is a good all-round system that combines efficient storage with excellent security and decent performance.

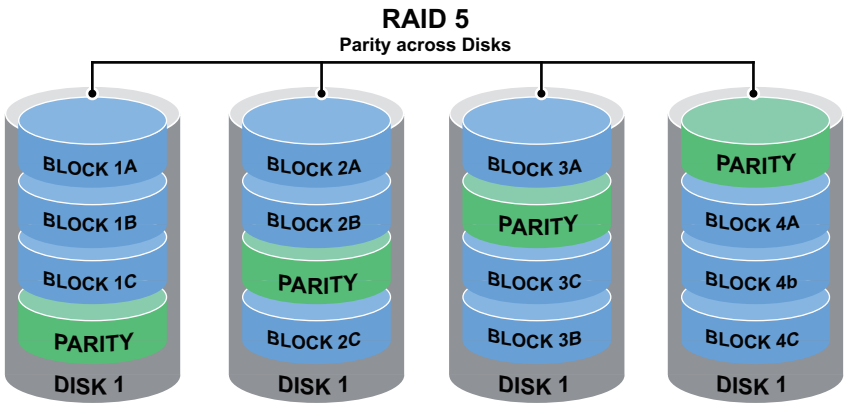


Figure H.3: RAID 5 – Striping with parity

Advantages

- Read data transactions are very fast while write data transaction are somewhat slower (due to the parity that has to be calculated).

Disadvantages

- Disk failures have an effect on throughput, although this is still acceptable.
- Complex technology requiring hardware support to efficiently calculate parity.

H.1.4 RAID level 10 – Combining RAID 0 & RAID 1

RAID 10 combines RAID 0 and RAID 1 in one single system. It provides security by mirroring all data on a secondary set of disks (Disk 2 and 4 in the drawing below) while using striping across each set of disks to speed up data transfers.

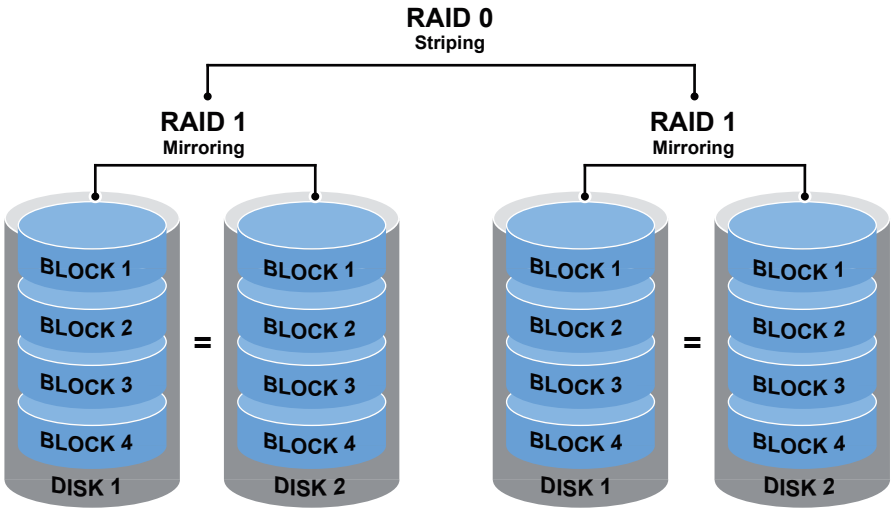


Figure H.4: RAID level 10 – Combining RAID 0 & RAID 1

Advantages

- Great performance, both in read and write operations.
- If a disk fails and is replaced by a new disk, data does not have to be rebuilt; it just has to be copied to the replacement disk.
- The technology is easy to implement. No parity calculations are required.
- Volume size is not limited to one disk.

Disadvantages

- Ineffective storage capacity, only half of the total disk capacity is available.

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