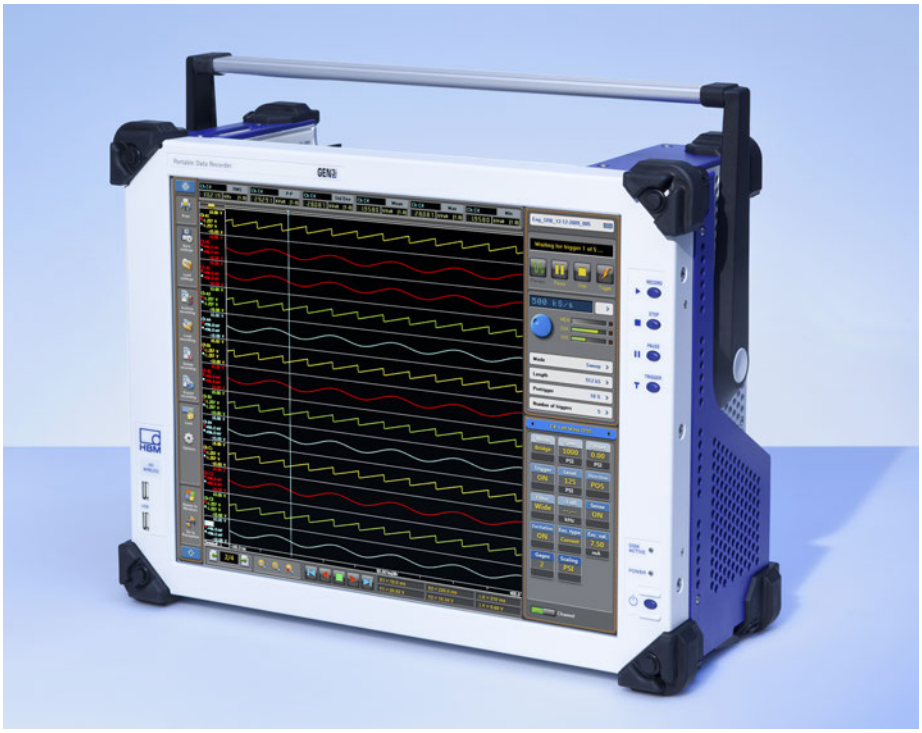
Genesis HIGH SPEED

User Manual

English



Portable Data Recorder

GEN3i

A03763_04_E00_00 HBM: public

HBM

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References made to the Perception software are for version 6.72 or higher

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StatStream® is a registered trademark of HBM in the European Union and a trademark in other countries.

StatStream® is patented in the US, Patent No. 7,868,886; patent pending in other countries.

Legal statement
This product uses GNU General Public Licensed (GPL) software, the source code is available at:
www.hbm.com/highspeed

For more information please refer to the following website:
www.gnu.org

Table of Contents

1 About this manual

1.1 Symbols used in this manual

The following symbols are used throughout this manual to indicate warnings and cautions.

WARNING

Indicates a potentially hazardous situation which, if not avoided, could result in death or serious injury.

WARNING

Indicates an electrical shock hazard which, if not avoided, could result in death or serious injury.

CAUTION

Indicates a potentially hazardous situation which, if not avoided, could result in minor or moderate injury; or alerts against unsafe practices; or alerts against actions which could damage the product or result in a loss of data.

CAUTION

The ESD susceptibility symbol indicates that handling or use of an item may result in damage from ESD if proper precautions are not taken.

HINT/TIP

The info icon indicates sections which provide additional information about the product. This information is not essential for correct operation of the instrument, but provides knowledge to make better use of the instrument.

1.2 Manual conventions

When the wording “Click Start ...” is used, this refers to the Windows® Start button. Compared to Windows® XP, Windows® Vista and Windows® 7, the Start Menu has undergone some significant changes. The taskbar icon is no longer labeled "Start" and is now simply the pearl icon (of the window-frame in an orb).

For clarity and convenience, these conventions are used throughout this manual:

- **Menu names** from the display appear in bold, blue lettering.
- **Settings** within a menu appear in bold, red lettering.
- **Front panel controls** and **control names** appear in bold, black lettering.

2 Safety Messages

2.1 Introduction

IMPORTANT

Read this section before using this product!

This instrument is mains powered and protective ground connections are required (unless otherwise specified for certain parts).

This manual contains information and warnings that must be observed to keep the instrument safe. The instrument should not be used when environmental conditions exceed the instrument's specifications (e.g. damp, high humidity) or if the unit is damaged.

For the correct and safe use of this instrument, it is essential that both operating and service personnel follow generally accepted safety procedures in addition to the safety precautions specified in this manual.

Whenever it is likely that safety protection has been impaired, the instrument must be made inoperative and secured against any unintended operation. Qualified maintenance or repair personnel should be informed. Safety protection is likely to be impaired if, for example, the instrument shows visible damage or fails to operate normally.

Appropriate use
This instrument and the connected transducers may be used only for measurement and directly related control tasks. Any other use is not appropriate. To ensure safe operation, the instrument may only be used as specified in this user manual.

- The covers protect the user from live parts and should only be removed by suitably qualified personnel for maintenance and repair purposes.
- The instrument must not be operated with the covers removed.
- This instrument must not be used in life support roles.
- There are no user serviceable parts inside the instrument.

It is also essential to follow the respective legal and safety regulations for specific applications during use. The same applies to the use of accessories. Additional safety precautions must be taken in setups where malfunctions could cause major damage, loss of data or even personal injury.
Some examples of precautions are: mechanical interlocking, error signaling, limit value switches, etc.

Maintenance and cleaning
The instrument is a maintenance-free product. However, please note the following information about cleaning the housing:

- Before cleaning, disconnect the instrument completely.
- Clean the housing with a soft, slightly damp (not wet!) cloth. Never use solvents, since these could damage the display or the labeling on the front panel.
- When cleaning, ensure that no liquid gets into the housing or connections.

General dangers, failing to follow the safety instructions
This instrument is a state-of-the-art device and as such is fail-safe. Using this instrument may be hazardous if it has been installed incorrectly and is operated by untrained personnel. Any person assigned to install, maintain or repair the unit or to put the unit into operation must have first read and understood the user manual, particularly the technical safety instructions.

Residual risks
This instrument's scope of supply and performance covers only a small area of measurement technology. In addition, equipment planners, installers and operators should plan, implement and respond to the safety engineering considerations of measurement technology in such a way as to minimize any residual risks. Prevailing regulations must be complied with at all times. The residual risks of the measurement technology must be referenced.

Conversions and modifications
Neither the design nor the safety features of this instrument may be modified without our express prior written agreement. Any modification shall exclude all liability on our part for any resultant damage. In particular, any repair or soldering work on cards (replacement of components) is prohibited. When exchanging complete units, use only original parts from HBM. The unit is delivered from the factory with a fixed hardware and/or software configuration. Changes should only be made within the possibilities documented in this manual.

Qualified personnel
People entrusted with the installation, fitting, operation of the instrument and putting the unit into service must have the appropriate qualifications. The instrument may only be installed and used by qualified personnel, in strict accordance with the specifications and the safety rules and regulations. This includes people who meet at least one of the three following qualification levels:

- Project personnel: Have a working knowledge of the safety concepts of automation and test and measurement technology.
- Automation plant or test and measurement operating personnel: Have been instructed on how to handle the equipment and are familiar with the operation of the cards and technologies described in this documentation.
- Commissioning engineers or service engineers: Have successfully completed the training on how to repair the automation systems. They are also authorized to activate, to ground and to label circuits and equipment in accordance with engineering safety standards. It is essential that the legal and safety requirements for the product and any accessories are complied with during use.

2.2 FCC and general

The first WARNING note below is required by the FCC (Federal Communications Commission) and relates only to the interference potential of this equipment. This message is a direct quotation.

WARNING

The equipment generates, uses, and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, may cause interference to radio communications. As temporarily permitted by regulation, it has not been tested for compliance with the limits for Class A computing devices pursuant to Subpart B or Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

2.3 Grounding

The instrument must be used with a protective ground connection via the protective ground conductor of the supply cable. The protective ground conductor is connected to the instrument before the line and neutral connections are made when the supply connection is made. If the final connection to the supply is made elsewhere, ensure that the ground connection is made before line and neutral connections are made.

WARNING

Any interruption of the ground connection, inside or outside the instrument, is likely to make the instrument dangerous. Intentional interruption is prohibited.

For protection against electric shock, all external circuits or equipment need a safe insulation. Therefore, peripheral equipment must not be connected to the system with a power supply without the SELV (Separated Extra Low Voltage) rating unless explicitly mentioned.

Signal connections to the instrument should be connected after the ground connection is made and disconnected before the ground connection is removed, i.e. the supply lead must be connected whenever signal leads are connected.

WARNING

For safety, it is essential that the protective ground connector of the instrument is used whenever voltages greater than 33 V RMS, 46.7 V PEAK or 70 V DC (IEC 61010-1:2010) are connected. This is to prevent the instrument's case becoming live in the event of a protective ground interruption, which could occur if the supply connector is accidentally disconnected from the instrument.

The primary purpose of protective grounding is to provide adequate protection against electric shock that could cause death or injury to personnel while working on de-energized equipment. This is accomplished by grounding and bonding to limit the body contact or exposure to voltages at the work-site to a safe value if the equipment were to be accidentally energized from any source of hazardous energy. The greatest source of hazardous energy in most cases is direct energizing of the equipment from a power-system or source.

WARNING

If connection to a protective ground is not possible for any reason, then please refer to the international safety standard EN 50191:2000

2.3.1 Mains power cord

WARNING

Do not use the equipment with damaged cords and/or cables. Replace a damaged cord and/or cable immediately.

2.4 Instrument symbols

A variety of symbols can be found in the system. Below is a list of symbols and their meaning.

This symbol is used to denote the measurement ground connection. This point is not a protective ground connection.

This symbol is used to denote a protective ground connection.

This symbol is used to denote a frame or chassis ground connection. This point is not a protective ground connection.

Where caution is required, this symbol refers to the user manual for further information.

This symbol warns that high voltages are present close to this symbol.

This symbol shows that the switch is a power switch. When pressed, the instrument state toggles between the operating and power-off mode. When the system is in power-off mode, all electronics are disconnected from the power, except for a small circuit used to detect the switch state.

2.5 Protection and isolation

2.5.1 Measurement categories

- The international standards for test equipment safety are IEC 61010-1 and the IEC 61010-2-030.
- IEC 61010-1 defines three overvoltage categories (CAT II, CAT III, and CAT IV) for the power supply of an instrument.
- IEC 61010-2-030 defines three measurement categories (CAT II, CAT III, and CAT IV) for an instrument's input measurements which can be directly connected to mains supply.
- All measurement inputs which are not specified to be connected to the mains power have no CAT rating and are referred to as O (like Others).

Categories in accordance with IEC 61010-2-030:2010
Electrical equipment, specifically measurement tools, can be assigned into four categories in accordance with IEC 61010-2-030:2010. These measurement categories are indicated by the terms O (previously CAT I), CAT II, CAT III and CAT IV. Originally, these categories were used to indicate the overvoltage or surge voltage that was likely to occur and could be sustained by the equipment. Currently, the category indicates the amount of energy that can be released if a short circuit occurs. A higher category number indicates a higher energy level that can occur and can be sustained by the equipment.

O (Other) (previously referred to as **CAT I**): This category is for measurements not directly connected to a mains supply. Measurements for this category are signal levels, regulated low voltage circuits or protected secondary circuits. For this category, there are no defined standard overvoltage or surge impulse levels.

CAT II: This category is for measurements directly connected to a low voltage mains supply. Measurements for this category are mains sockets in household applications or portable tools. This category expects a minimum of three levels of overcurrent protection between the transformer and connection point of the measurement. (See Figure 2.1).

CAT III: This category is for measurements directly connected to the distribution part of a low voltage mains installation. Measurements for this category are circuit breakers, wiring, junction boxes, etc. This category expects a minimum of two levels of overcurrent protection between the transformer and connection point of the measurement. (See Figure 2.1).

CAT IV: This category is for measurements directly connected to the source of a low voltage mains installation. Measurements for this category are overcurrent protection devices, ripple control units, etc. This category expects that there is a minimum of one level of overcurrent protection between the transformer and connection point of the measurement circuit. (See Figure 2.1).

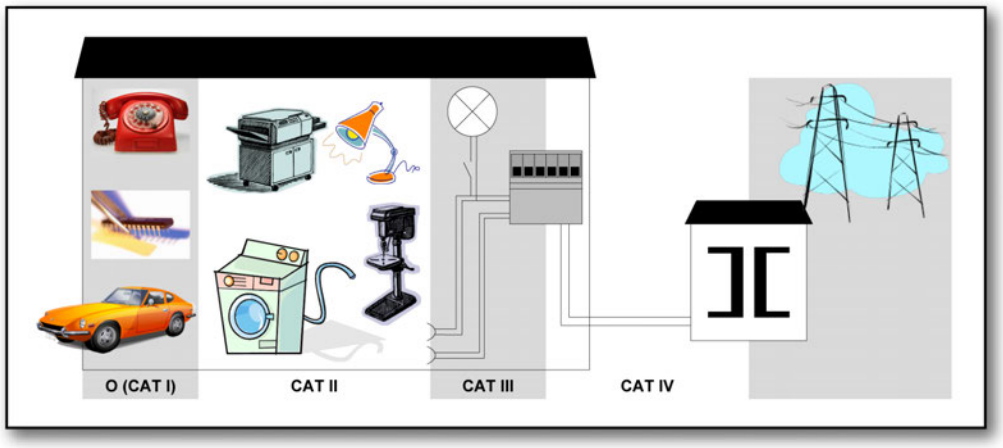


Figure 2.1: Category indication in accordance with IEC 61010-2-030:2010

Example: A measurement device is specified as 600 V CAT II, maximum input voltage 1000 V DC.

Table 2.1: Insulation test voltages in accordance with IEC 61010-2-030:2010

Nominal Voltage (V RMS or V DC)	IEC 61010-2-030:2010					
	5 sec. AC test (V RMS)			Impulse test (V)		
	CAT II	CAT III	CAT IV	CAT II	CAT III	CAT IV
≤ 150	840	1390	2210	1550	2500	4000
> 150 ≤ 300	1390	2210	3310	2500	4000	6000
> 300 ≤ 600	2210	3310	4260	4000	6000	8000
> 600 ≤ 1 000	3310	4260	6600	6000	8000	12000

Using the table above, it can be concluded that this specification informs the user that the device passed the insulation tests; 5 sec at 2210 V RMS and impulse 4000 V. The maximum operating input voltage is 1000 V DC. This device is to be used to measure CAT II circuitry up to 600 V.

WARNING

Measurement inputs of this instrument should not be used to measure high-energy signals of measurement categories CAT II, CAT III or CAT IV (IEC 61010-2-030:2010) (e.g. mains measurements) , unless specifically stated for the specific input.

2.5.2 Basic insulation versus reinforced

For reference, the basic insulation and supplementary insulation and the reinforced insulation test values for CAT II can be found below.

Table 2.2: Test voltages for the testing electric strength of solid insulation in measuring circuits in measurement category II (IEC 61010-2-030:2010)

Nominal voltage line to neutral AC RMS or DC of MAINS being measured. (V)	Test voltage			
	5 s AC test V AC RMS		Impulse test V peak	
	Basic insulation and supplementary insulation	Reinforced insulation	Basic insulation and supplementary insulation	Reinforced insulation
≤ 150	840	1390	1550	2500
> 150 ≤ 300	1390	2210	2500	4000
> 300 ≤ 600	2210	3510	4000	6400
> 600 ≤ 1000	3310	5400	6000	9600

Several means of protection can be used to protect a user from hazardous voltages. As can be seen below, basic insulation and supplementary insulation is one mean of protection, but reinforced isolation is also a means of protection. The test voltages are different for each mean of protection, as can be found in the table above.

Additional means of protection for single fault conditions
Accessible parts shall be prevented from becoming HAZARDOUS LIVE IN SINGLE FAULT CONDITION. The primary means of protection (see Figure 2.2) shall be supplemented by one of **A**, **B**, **C** or **D**. Alternatively, one of the single means of protection **E** or **F** shall be used. See Figure 2.2.

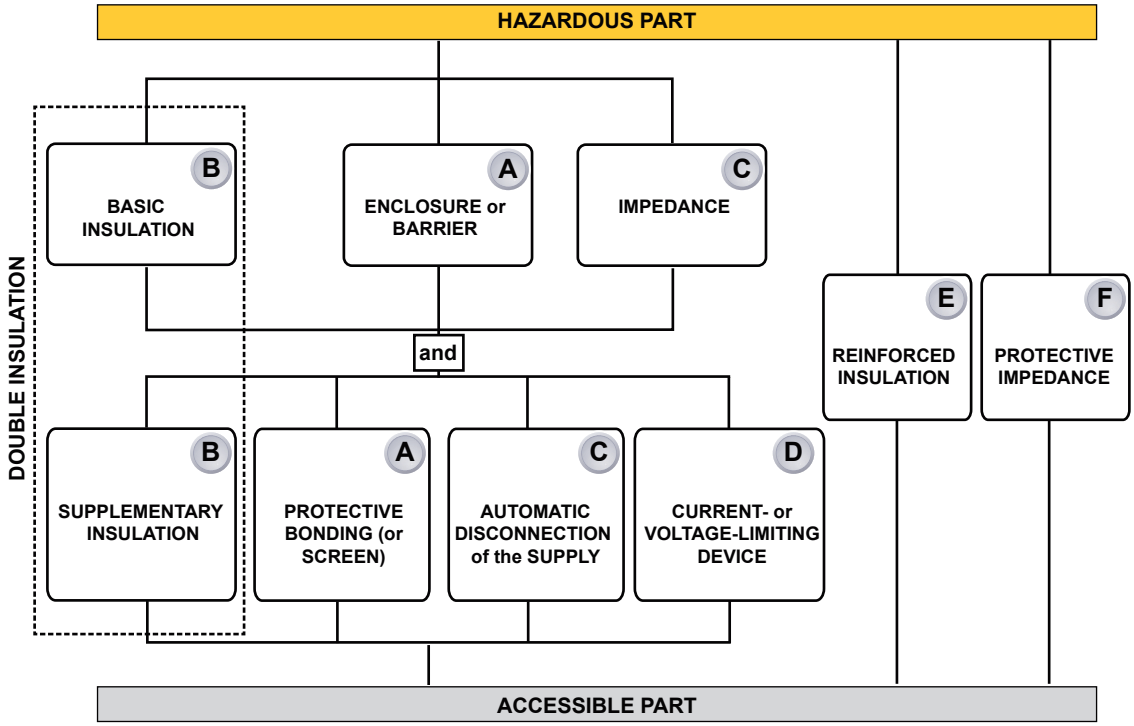


Figure 2.2: Acceptable arrangement of protective means against electric shock

Example: A measurement device is specified as 600 V CAT II reinforced insulation, with a maximum input voltage 1000 V DC.
Using the information above, it can be concluded that this specification informs the user that the measurement device is tested on input to chassis ground for five seconds at 3510 V RMS and impulse 6400 V. The maximum operating input voltage is 1000 V DC. This device is to be used to measure CAT II circuitry up to 600 V.

2.5.3 Protection

WARNING

ELECTRICAL SHOCK HAZARD!
Any interruption of the protective conductor inside or outside the apparatus is likely to make the apparatus dangerous. Intentional interruption is prohibited.
When the apparatus is connected to its supply, terminals may be live, and the opening of covers for removal of parts is likely to expose live parts.

Whenever it is likely that the protection has been impaired, the apparatus must be made inoperative and be secured against any unintended operation.

The protection is likely to be impaired if, for example, the apparatus shows visible damage or has been subjected to severe transport stresses.

It is the responsibility of the user to ensure the safety of any accessories used with the equipment, such as probes.

Proper use of this device depends on careful reading of all instructions and labels.

If the instrument is used in a manner not specified by HBM, the protection provided by the instrument can be impaired.

WARNING

This instrument must not be operated in explosive atmospheres.

WARNING

This instrument and related accessories are not designed for biomedical experimentation on humans or animals and should not be directly connected to human or animal subjects or used for patient monitoring.

2.5.4 Overvoltage/current protection

All signal inputs are protected against overloads and transients. Exceeding the limits stated in the specifications, particularly when connected to potentially high-energy sources, can cause severe damage that is not covered by the manufacturer's warranty.

WARNING

Do not remove covers. Refer to qualified individuals for servicing.

The covers protect the user from live parts and should only be removed by suitably qualified personnel for maintenance and repair purposes.

The instrument must not be operated with the covers removed.

There are no user serviceable parts inside.

2.5.5 Isolation

CAUTION

For input channels with plastic BNCs (galvanically isolated from the chassis), the input conductors including the BNC shell may carry hazardous voltages. Only appropriate insulated BNC connectors should be used.

It is the responsibility of the user to ensure the safety of any accessories used with the instrument, such as probes.

CAUTION

Even low voltage inputs may contain high voltage fast transients (spikes), which could damage the input. For this reason it is not safe, for instance, to make direct connections to an AC line supply, unless specifically stated otherwise for the specific input.

2.6 Environment

The instrument should be operated in a clean, dry environment with an ambient temperature as specified in the data sheets.

The instrument is specified for use in a Pollution Degree II environment, which is normally non-conductive with temporary light condensation, but it must not be operated while condensation is present. It should not be used in more hostile, dusty or wet conditions, as specified in the Pollution Degree II environment.

Humidity should be between 0% and 80%. When moving the device from a cold to a warm environment, the device has to be left off for a period of 30 minutes to avoid short circuits as a result of condensation.

Note *Direct sunlight, radiators and other heat sources should be taken into account when assessing the ambient temperature.*

If the instrument has a fan installed, leave space around the equipment for unrestricted ventilation.

Do not store the equipment in hot areas. High temperatures can shorten the life of electronic devices and damage batteries.

Do not store the equipment in cold areas. Before the equipment warms up to its normal operating temperature, moisture can form inside the equipment, which may damage the equipment's electronic circuits.

Do not drop, knock or shake the equipment. Rough handling can break internal electronics and/or PCBs.

Do not use harsh chemicals, cleaning solvents or strong detergents to clean the instrument. To clean the instrument, disconnect all power sources and clean the housing with a soft, slightly damped (not wet!) cloth.

It is the responsibility of the user to ensure the safety of any accessories used with the instrument, such as probes.

2.7 Laser Safety

Some of the GEN series cards or systems use lasers. All laser products used are classified as a **Class 1 laser product**. The lasers do not emit hazardous light but it is recommended to avoid direct exposure to the beam.

WARNING

Intrabeam viewing of the laser product may produce dazzling visual effects, particularly in low ambient light. Lasers of any wavelength with sufficient output power can cause injury.

The built-in laser complies with laser product standards set by government agencies for Class 1 laser products:

The GEN series products are certified as Class 1 Laser Products and comply with US FDA regulations. These are certified by TÜV and CSA to meet the Class 1 eye safety requirements of EN (IEC) 60825 and the electrical safety requirements of EN (IEC) 60950. The devices are for use only under the specifications and ratings specified in the manual and data sheets.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

2.8 Manual handling of loads

The Manual Handling of Loads Directive 90/269/EEC from the European Community lays down the minimum health and safety requirements for the manual handling of loads where there is a risk particularly of back injury to workers.

Before lifting or carrying a heavy object, the following questions should be asked:

- Can one person lift this load safely, or do two people need to lift the load?
- How far will the load have to be carried?
- Is the path clear of clutter, cords, slippery areas, overhangs, stairs, curbs or uneven surfaces?
- Will closed doors that need to be opened be encountered?
- Once the load is lifted, will it block the carrier's view?
- Can the load be broken down into smaller parts?
- Should the carrier wear gloves to get a better grip and to protect hands?

Contact the "Occupational Health and Safety" organization, or equivalent, in your country for more information.

The GEN3i weighs approximately 12 kg with three acquisition cards plugged in (9 kg without acquisition cards)

2.9 International safety warnings

Dansk

SIKKERHEDSADVARSEL
Dette instrument skal anvendes med en sikkerhedsjordforbindelse, som er tilsluttet via lysnetkablets beskyttelsesjordledning eller via en sikkerhedsjordklemme, hvis instrumentet er forsynet hermed. Hvis sikkerhedsjordforbindelsen afbrydes, inden i eller uden for instrumentet, kan instrumentet udgøre en farekilde. Sikkerhedsjordforbindelsen må ikke afbrydes. Der skal desuden tilsluttet en signaljordforbindelse, hvis et indgangssignal overstiger 33 V RMS, 46,7 V PEAK eller 70 V DC (IEC 61010-1:2010).

Dækslerne må ikke fjernes.

Afbryd dette instrument eller dets strømforsyning fra lysnettet ved at fjerne IEC-stikket. Instrumentets vekselstrømsafbryder er kun beregnet til funktionelle formål. Den er ikke beregnet eller egnet til at afbryde instrumentet fra lysnettet.

Hvis målingerne et omfattet af EN 50110-1 og EN 50110-2, skal alle kort med en driftsspænding på mere end 50 V AC RMS eller 120 V DC tilsluttes af en kvalificeret tekniker eller en elektriker, og arbejdet skal kontrolleres af en kvalificeret tekniker. (En kvalificeret tekniker er en person, som i kraft af sin specialuddannelse, sin viden og erfaring samt sit kendskab til relevante bestemmelser kan vurdere omfanget af det arbejde, de skal udføre, og afdække de potentielle risici, og som er blevet udpeget som kvalificeret tekniker af deres arbejdsgiver).

Nederlands

VEILIGHEIDSWAARSCHUWING
Dit instrument mag uitsluitend worden gebruikt als een beschermde massa (aarde) is aangesloten via de beschermde massageleider van de voedingskabel, of indien het instrument daarvan is voorzien via de veiligheids-massa-aansluiting. Als de beschermde massa, binnen of buiten het instrument, wordt onderbroken, dan kan dat hierdoor uitermate gevaarlijk worden. Het opzettelijk onderbreken van de massa is verboden. Indien er een signaal wordt aangeboden van meer dan 33 V RMS, 46.7 Vpeak of 70 V DC (IEC 61010-1:2010) dient eveneens een signaalaarding aangesloten te zijn.

De deksels mogen nooit worden verwijderd.

Om dit instrument los te koppelen of van het stroom af te halen, dient de IEC-aansluiting er uit te worden getrokken. De wisselstroom-voedingsschakelaar op dit instrument is uitsluitend bestemd voor functionele doeleinden. Het is niet bedoeld of geschikt als een ontkoppelingsapparaat.

Voor metingen die binnen de EN 50110-1 en EN 50110-2 vallen: let op dat alle panelen met bedrijfsspanningen van meer dan 50 V AC RMS of 120 V DC alleen door een gekwalificeerde technicus mogen worden aangesloten of door een persoon die is opgeleid in de elektrotechniek en onder toezicht van een gekwalificeerde technicus staat. (Gekwalificeerde technici zijn personen, die op basis van hun specialistische opleiding, kennis en ervaring als ook hun kennis van de betreffende voorzieningen, in staat zijn om het werk dat aan hen is toevertrouwd te beoordelen en mogelijke gevaren te ontdekken en door hun werkgever zijn aangewezen als gekwalificeerde technici.)

Suomi

TURVAOHJEITA

Tätä laitetta käytettäessä sen tulee olla suojamaadoitettu joko verkkojohdon suojajohtimen tai erillisen suojamaadoitusliitännän kautta, mikäli laitteeseen on sellainen asennettu. Suojamaadoituksen katkaiseminen laitteen sisä- tai ulkopuolelta tekevät siitä vaarallisen. Tahallinen katkaisu on kiellettyä. Lisäksi signaalimaa on oltava kytkettynä, jos jokin tulosignaali ylittää tehollisarvon 33 V, huippuarvon 46,7 V tai 70 V DC (IEC 61010-1:2010).

Älä poista suojakansia.

Katkaise laitteen tai sen virtalähteen käyttöjännite irrottamalla IEC-liitin. Laitteen verkkokytkimellä on ainoastaan toiminnallinen tarkoitus. Sitä ei ole tarkoitettu, eikä se sovellu laitteen erottamiseen käyttöjännitteestä.

Mittauksissa, jotka kuuluvat EN 50110-1- ja EN 50110-2-standardien soveltamisalaan, huomaa, että kortit, jotka toimivat tehollisarvojännitteellä yli 50 V AC tai 120 V DC, saa kytkeä vain pätevä asentaja tai sähköteknisen koulutuksen saanut henkilö pätevän asentajan valvonnassa. (Pätevät asentajat ovat henkilöitä, jotka erikoiskoulutuksensa, tietojensa ja kokemuksensa sekä asiaan kuuluvien määräysten tuntemuksensa ansiosta pystyvät arvioimaan heille annettuja töitä ja havaitsemaan mahdolliset vaarat ja jotka heidän työnantajansa on nimennyt ammattitaitoisiksi asentajiksi).

Français

ATTENTION - DANGER!
Lorsqu'il est en fonctionnement, cet instrument doit impérativement être mis à la masse par le conducteur de terre du câble d'alimentation ou, si l'instrument en comporte une, par la borne de terre. Il peut être dangereux en cas de coupure du circuit de terre, que ce soit à l'intérieur ou à l'extérieur de l'instrument. Il est formellement interdit de couper intentionnellement le circuit de terre. De plus, une masse signal doit être connectée si l'un des signaux d'entrée, quel qu'il soit, dépasse 33 V RMS (valeur efficace), 46,7 V PEAK (valeur de crête) ou 70 V DC (courant continu) (CEI 61010-1:2010).

Ne pas déposer les panneaux de protection.

Pour déconnecter cet instrument ou son alimentation de l'alimentation secteur, débrancher le cordon d'alimentation (CEI). L'interrupteur d'alimentation secteur sur cet instrument est purement fonctionnel. Il ne s'agit pas d'un dispositif de coupure du courant, et n'est pas conçu pour cette fonction.

Pour les mesures entrant dans le champ d'application des normes EN 50110-1 et EN 50110-2, veuillez noter que tous les panneaux avec des tensions de service supérieures à 50 V AC RMS (tension efficace) ou 120 V DC (courant continu) ne peuvent être connectés que par un technicien qualifié ou une personne formée en ingénierie électrique et supervisée par un technicien qualifié. (Les techniciens qualifiés sont des personnes qui, du fait de leur formation, leurs connaissances et leur expérience spécialisées ainsi que leur connaissance des dispositions réglementaires appropriées, sont capables d'évaluer le travail qui leur est confié et détecter les risques possibles, et qui ont été désignées comme techniciens qualifiés par leur employeur).

Deutsch

WARNHINWEIS!
Dieses Gerät muss mit einer Schutzerde betrieben werden, die über den Schutzleiter des Speisekabels oder über die Erdungsklemme des Gerätes (falls vorhanden) anzuschließen ist. Bei einer Unterbrechung der Schutzerde außerhalb oder innerhalb des Gerätes kann eine Gefahr am Gerät entstehen. Eine beabsichtigte Unterbrechung ist nicht zulässig. Achtung! Bei Signalspannungen über 33 V Effektivwert, 46,7 V Spitzenwert oder 70 V Gleichspannung (IEC 61010-1:2010) muss die Signalmasse angeschlossen sein.

Die Schutzabdeckung nicht entfernen.

Zum Trennen des Gerätes oder seiner Spannungsversorgung von der Wechselstromversorgung den IEC-Stecker abziehen. Der Wechselstromversorgungs-Schalter dient bei diesem Gerät nur für Funktionszwecke. Er ist nicht als Trennvorrichtung bestimmt bzw. geeignet.

Für Messungen gemäß EN 50110-1 und EN 50110-2 bitte berücksichtigen, dass alle Platinen mit Betriebsspannungen über 50 V AC RMS oder 120 V DC nur durch einen qualifizierten Elektriker oder einer elektrotechnisch unterwiesenen Person unter Aufsicht eines qualifizierten Technikers durchgeführt werden dürfen. (Qualifizierte Techniker sind aufgrund ihrer fachlichen Ausbildung, Kenntnisse und Erfahrungen sowie Kenntnis der einschlägigen Bestimmungen in der Lage, die ihnen anvertrauten Arbeiten zu beurteilen und mögliche Risiken zu erkennen, sowie Personen, die durch ihren Arbeitgeber zu qualifizierten Technikern ernannt worden sind).

Italiano

AVVISO DI SICUREZZA
Questo strumento deve esser utilizzato con un collegamento protettivo di messa a terra tramite il filo di messa a terra del cavo di alimentazione o tramite il terminale di messa a terra in sicurezza, nel caso in cui lo strumento ne sia dotato. Qualsiasi interruzione della messa a terra di protezione, sia all'interno che all'esterno dello strumento, lo renderà pericoloso. È vietata qualsiasi interruzione causata intenzionalmente. Inoltre, la connessione di terra deve essere collegata se ad uno qualsiasi degli ingressi viene applicato un segnale superiore a 33 V RMS, 46,7 V di picco o 70 V c.c. (IEC 61010-1:2010).

Non aprire lo strumento.

Per disinnestare questo strumento o l'alimentazione dalla corrente alternata, scollegare il connettore IEC. L'interruttore dell'alimentazione a corrente alternata di questo strumento viene fornito esclusivamente per scopi operativi e non viene inteso, né è adatto, per essere utilizzato come dispositivo di disinnesto.

Si noti che per le misurazioni che rientrano nell'ambito di applicazione delle norme EN 50110-1 ed EN 50110-2, tutte le schede con tensioni di esercizio superiori a 50 V c.a. RMS o 120 V c.c. possono essere collegate esclusivamente da un tecnico qualificato o da una persona in possesso di una formazione specifica nel campo dell'ingegneria elettrica sotto la supervisione di un tecnico qualificato. (Per tecnico qualificato si intende una persona che, in virtù della propria formazione , preparazione ed esperienza specialistica, nonché conoscenza delle disposizioni di settore, è in grado di valutare il lavoro che gli viene assegnato e di individuare possibili rischi, oltre ad essere stato nominato tecnico qualificato dal proprio datore di lavoro).

Norsk

ADVARSEL!
Dette instrument må betjenes med beskyttelsesjord tilkoblet via beskyttelsesjordlederen til tilførselskabelen eller via beskyttelsesjordklemmen, hvis instrumentet er utstyrt med en slik. Ethvert brudd i beskyttelsesjorden inni eller utenpå instrumentet kan føre til at instrumentet blir farlig. Tiltenkt brudd er tillatt. I tillegg må en signaljord tilkobles hvis et inngangssignal overskrider 33 V RMS, 46,7 V PEAK eller 70 V DC (IEC 61010-1:2010).

Ikke fjern dekslene.

For å koble dette instrumentet eller dets strømforsyning fra AC-tilførselen, trekker du ut IEC-kontakten. AC-tilførselsbryteren på dette instrumentet er kun for funksjonelle formål. Den er ikke beregnet for, eller egnet til frakoblingsenhet.

For målinger som faller innenfor EN 50110-1 og EN 50110-2 må man være oppmerksom på at alle kort med arbeidsspenninger over 50 V AC RMS eller 120 V DC kun kan kobles til av en kvalifisert tekniker eller elektriker og overvåket av en kvalifisert tekniker. (Kvalifiserte teknikere er personer som på grunn av sin spesialistopplæring, kunnskap og erfaring, samt sin kunnskap om relevante bestemmelser, er i stand til å gå inn i arbeidet som de har fått i oppdrag å utføre og detektere mulige farer, og som er blitt utnevnt som kvalifiserte teknikere av sin arbeidsgiver.

Português

AVISO DE SEGURANÇA
Este instrumento deve funcionar com uma terra de proteção conectada através do condutor da terra de proteção do cabo de alimentação ou, caso o instrumento esteja equipado com um, através do terminal da terra de proteção. Qualquer interrupção da terra de proteção, no interior ou no exterior do instrumento, poderá tornar o instrumento perigoso. A interrupção intencional é proibida. Além disso, deve ser conectado um sinal de terra se qualquer sinal de entrada exceder 33 V RMS, 46,7 V PICO ou 70 V CC (IEC 61010-1:2010).

Não retirar as tampas.

Para desconectar este instrumento ou a respetiva fonte de alimentação da alimentação CA, retire o conector IEC da ficha. Neste instrumento, o interruptor de alimentação CA é fornecido apenas para fins funcionais. Não se destina a, nem é adequado para, ser utilizado como dispositivo de desconexão.

Para medições abrangidas pelas normas EN 50110-1 e EN 50110-2, tenha em atenção que todos os quadros com tensões de funcionamento superiores a 50 V CA RMS ou 120 V CC apenas poderão ser conectados por um técnico qualificado ou por alguém com formação em engenharia elétrica e supervisionados por um técnico qualificado. (Técnicos qualificados são pessoas que, devido à sua formação especializada, ao conhecimento e à experiência, bem como ao seu conhecimento das disposições relevantes, são capazes de avaliar o trabalho que lhes é confiado e detetar possíveis riscos e são pessoas que foram nomeadas técnicos qualificados pelo seu empregador.)

Português (Brasil)

AVISO DE SEGURANÇA
Este instrumento deve ser operado com um terra de proteção conectado por meio do condutor do terra de proteção do cabo de alimentação ou, se o instrumento estiver equipado com um, por meio do terminal de aterramento de segurança. Qualquer interrupção do terra de proteção, no interior ou no exterior do instrumento, poderá tornar o instrumento perigoso. A interrupção intencional é proibida. Além disso, deve ser conectado um sinal de terra se qualquer sinal de entrada exceder um máximo de 33 V RMS, 46,7 V PICO ou 70 V CC (IEC 61010-1:2010).

Não retirar as tampas.

Para desconectar este instrumento ou a fonte de alimentação dele da alimentação CA, desconecte o conector IEC. Neste instrumento, o interruptor de alimentação CA é fornecido somente para fins funcionais. Não se destina a, nem é adequado para, ser usado como dispositivo de desconexão.

Para medições no escopo das normas EN 50110-1 e EN 50110-2, note que todos os quadros com tensões de funcionamento superiores a 50 V CA RMS ou 120 V CC poderão somente ser conectados por um técnico qualificado ou por alguém com formação em engenharia elétrica e supervisionados por um técnico qualificado. (Os técnicos qualificados são pessoas que, devido à sua formação acadêmica, conhecimento e experiência, bem como ao seu conhecimento das provisões relevantes, são capazes de avaliar o trabalho que lhes é confiado e detectar possíveis riscos e são pessoas que foram nomeadas técnicos qualificados por seu empregador.)

Español

ADVERTENCIA SOBRE SEGURIDAD
Este instrumento debe utilizarse conectado a tierra a través del conductor de puesta a tierra del cable de alimentación o de la borna de seguridad, si dicho instrumento estuviera equipado con ella. Cualquier interrupción de esta puesta a tierra, dentro o fuera del instrumento, hará que el manejo del mismo resulte peligroso. Queda terminantemente prohibido dejar en circuito abierto dicha puesta a tierra. Además, debe conectarse una señal de tierra si cualquier señal de entrada sobrepasa los 33 V eficaces, los 46,7 V de PICO o los 70 V de CC (IEC 61010-1:2010).

No quite las tapas.

Para desconectar este instrumento o su fuente de alimentación de la CA, desenchufe el conector IEC. El interruptor de entrada de CA (encendido) se incluye solo para fines funcionales. No está pensado para utilizarse como medio de desconexión, ni tampoco es adecuado para ello.

En cuanto a las mediciones que se clasifiquen bajo el alcance de las normas EN 50110-1 y EN 50110-2, tenga en cuenta que los cuadros con tensión de funcionamiento por encima de los 50 V de CA eficaces o los 120 V de CC solo puede conectarlos un técnico cualificado o una persona con formación en ingeniería eléctrica y supervisada por un técnico cualificado. (Los técnicos cualificados son personas que, debido a su formación especializada, conocimientos y experiencia, así como por su conocimiento de los suministros pertinentes, son capaces de evaluar el trabajo encomendado y detectar posibles riesgos, al igual que personas nombradas como técnicos cualificados por la empresa contratadora).

Svenska

SÄKERHETSVARNING
Detta instrument måste användas med jordad anslutning via strömkabelns ledare eller, om sådan finns, via en isolerad jordterminal. Avbrott i den isolerande jordningen inuti eller utanför strömgivaren kan göra strömgivaren farlig. Avsiktligt avbrott är förbjudet. Dessutom måste en signaljordning anslutas om någon ingångssignal överskrider 33 V RMS, 46.7 V PEAK eller 70 V DC (IEC 61010-1:2010).

Ta inte bort höljet.

Dra ut IEC-kontakten för att koppla loss instrumentet eller dess strömkälla från strömförsörjningen. Brytaren för växelströmförsörjningen på detta instrument är endast avsedd för funktionella syften. Den är inte avsedd eller lämplig som frånkopplingsenhet.

För mått inom intervallen som anges i EN 50110-1 och EN 50110-2, observera att alla kort med arbetsspänning över 50 V AC RMS eller 120 V DC kan endast anslutas av en kvalificerad tekniker eller en person som är utbildad i elteknik och övervakas av en kvalificerad tekniker. (Kvalificerade tekniker är personer som på grund av sin specialistutbildning, kunskap och erfarenhet liksom sin kunskap om relevanta enheter kan utvärdera arbetet som tilldelas dem och göra kvalificerade riskbedömningar samt utses av sina arbetsgivare till kvalificerade tekniker).

English

SAFETY WARNING

This instrument must be operated with a protective ground (earth) connection via the protective ground conductor of the supply cable or, if the instrument is fitted with one, via the protective ground terminal. Any interruption of the protective ground, inside or outside the instrument, is likely to make the instrument dangerous. Intentional interruption is prohibited. In addition, a signal ground must be connected if any input signal exceeds 33 V RMS, 46.7 V PEAK or 70 V DC (IEC 61010-1:2010).

Do not remove the covers.

To disconnect this instrument or its power-supply from the AC supply, unplug the IEC connector. The AC supply switch on this instrument is provided for functional purposes only. It is not intended, or suitable, as a disconnecting device.

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that all cards with working voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience as well as their knowledge of the relevant provisions are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

日本語

安全上の警告
本機器の操作は、電源ケーブルの保護接地線で接地（アース）を施した上で行ってください。また、安全接地用端子が存在する場合は、これを経由して本機器を接地してください。機器の内部または外部にある保護接地線が遮断されると、機器が危険な状態に陥る可能性があります。故意に保護接地線を遮断することを禁止します。また、入力信号が33V RMS、ピーク時に46.7V RMS、または70V DCを超える場合は、信号接地線を接続してください（IEC 61010-1:2010）。

カバーは取り外さないでください。

本機器またはその電源供給をAC電源供給から遮断するには、IECコネクターを抜きます。本機器のAC電源スイッチは、機能上の目的のためだけに提供しています。したがって、機器の主電源遮断用として意図されていないか、適応していません。

EN 50110-1とEN 50110-2の適用範囲に該当する測定を行う際、使用電圧が50 V AC RMSまたは120 V DCを超えるすべての基板の接続作業は、適正な資格を持つ技術者が、または電気工学の訓練を受けた者が適正な資格を持つ技術者の監督の下、行わなければなりませんのでご注意ください。(適正な資格を有する技術者とは、専門技術者に向けた訓練を受け、知識と経験を有し、該当する規定についても熟知しているため、委託された作業の内容を評価し、存在する可能性のあるリスクを特定することができ、雇用主により適正な資格を有する技術者として任命されている者を指します。)

中文

安全警告

该仪器必须通过电源电缆的保护接地线连接到保护接地（接地），如果该仪器已配备了安全接地端子，则通过该端子接地。断开仪器内外的任何保护接地可能使设备存在危险。严禁有意断开。此外，若任何输入信号高于 33 V RMS, 46.7 V 峰或 70 V DC，则必须将信号接地 (IEC 61010-1:2010)。

不要取下保护盖。

要将此设备或其电源断开交流电源，请拔下 IEC 接头。仪器上的交流电源开关仅用于功能性目的。而不是用于或适用于断开设备。

对于 EN 50110-1 和 EN 50110-2 中的测量，请注意：所有工作电压高于 50 V AC RMS 或 120 V DC 的板卡只能由合格的技术人员或在由受过电气工程培训的人员在合格技术人员的监督下进行连接。（合格技术人员指的是其专业培训、知识和经验以及相关规定的指示能够胜任委托给他们的工作并能检查出可能风险的人，这些人会被其雇主指定为合格技术人员）

РУССКИЙ

ПРЕДУПРЕЖДЕНИЕ
Для эксплуатации данного прибора необходимо использовать защитное заземление, подключенное через проводник заземления кабеля питания или через терминал защитного заземления, если прибор оснащен таковым. В случае прерывания защитного заземления (внутри или снаружи прибора) прибор может стать травмоопасным. Преднамеренное прерывание заземления запрещено. Кроме того, необходимо подключить сигнальное заземление, если напряжение входного сигнала превышает 33 В среднеквадр. знач., 46,7 В пиков. знач. или 70 В пост. тока (IEC 61010-1:2010).

Не снимать крышки.

Для отключения данного прибора или его блока питания от сети переменного тока отсоедините разъем IEC. Переключатель питания переменного тока данного прибора предусмотрен только для функциональных целей и не должен использоваться в качестве устройства отключения.

Для проведения измерений в соответствии со стандартами EN 50110-1 и EN 50110-2 следует учесть, что подключение всех плат, рабочее напряжение которых превышает 50 В перемен. тока среднеквадр. знач. или 120 В пост. тока, может выполнять только квалифицированный технический персонал или сотрудники, прошедшие курс обучения по электротехнике, под наблюдением квалифицированного персонала. (Квалифицированным техническим персоналом считаются сотрудники, которые после специальной подготовки, получения требуемых знаний и опыта, а также знакомые с основными процедурами, способны оценить доверенную им работу, определив возможные риски. При этом назначение на должность квалифицированного технического работника осуществляет работодатель.)

안전 경고

안전 경고
본 장비는 반드시 보안용 접지(접지)가 전원 공급 장치 케이블의 보안용 접지 도체를 통해 연결된 상태에서 작동해야 하며, 접지가 장착된 경우에는 보안용 접지 터미널을 통해 작동해야 합니다. 장비 내부 혹은 외부적으로 접지 방해 요인이 있는 경우 사용자에게 위험할 수 있습니다. 고의적인 방해는 금지됩니다. 또한, 입력 신호가 **33 V RMS, 46.7 V** 피크 또는 **70 V DC(IEC 61010-1:2010)**를 초과하는 경우 신호 접지를 연결해야 합니다.

덮개를 제거하지 마십시오.

AC 공급 전원으로부터 이 기기 또는 전원 공급 장치를 분리하려면 **IEC** 커넥터를 뽑으십시오. 본 장비의 **AC** 전원 공급 스위치를 장비 작동 외에 다른 용도로 사용하지 마십시오. 본 스위치는 단절 용도로 설계되지 않았으며, 이에 적합하지도 않습니다.

EN 50110-1 및 **EN 50110-2** 범위에 속한 측정값의 경우, **50 V AC RMS** 또는 **120 V DC** 를 초과하는 작동 전압의 모든 보드는 검증된 전문 기사 또는 전기 공학 교육을 받고 검증된 전문 기사의 감독을 받는 사람만이 연결할 수 있습니다. (검증된 전문 기사는 전문가 교육, 지식 및 경험뿐만 아니라 관련 규정의 지식을 보유하고 있어 그들에게 위임된 작업을 수행하고 가능한 위험을 탐지할 수 있으며 고용주가 자격을 갖춘 기술자로 지명한 사람입니다.)

2.10 Operation of electrical installations

Working on, with, or near electrical installations implies certain dangers. These electrical installations are designed for the generation, transmission, conversion, distribution and use of electrical power. Some of these electrical installations are permanent and fixed, such as a distribution installation in a factory or office complex, others are temporary, such as on construction sites, and others are mobile or capable of being moved either while energized or while neither energized nor charged.

The European Standard EN 50110-1 sets out the requirements for the safe operation of and work activity on, with, or near these electrical installations. The requirements apply to all operational, working and maintenance procedures. The European Standard EN 50110-2 is a set of normative annexes (one per country) which specify either the present safety requirements or give the national supplements to these minimum requirements at the time when this European Standard was prepared.

WARNING

High voltage and qualified personnel

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that working with voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience, as well as their knowledge of the relevant provisions, are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

3 Normative Documents and Declarations

3.1 Electrical

3.1.1 Electrostatic Discharge (ESD)

When handling disconnected devices, electrostatic discharge (ESD) can cause damage if discharged into or near sensitive components on the device. Take steps to avoid such an occurrence.

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN series system, its connections or a plug-in card.

Description of ESD

Static electricity is an electrical charge caused by the buildup of excess electrons on the surface of a material. To most people, static electricity and ESD are nothing more than annoyances. For example, after walking over a carpet while scuffing your feet, building up electrons on your body, you may get a shock - the discharge event - when you touch a metal doorknob. This little shock discharges the built-up static electricity.

ESD-susceptible equipment

Even a small amount of ESD can harm circuitry, so when working with electronic devices, take measures to help protect the electronic devices, including the GEN3i Portable data recorder, from ESD harm. Although HBM has built protections against ESD into its products, ESD exists and, unless neutralized, could build up to levels that could harm the equipment. Any electronic device that contains an external entry point for plugging in anything from cables to acquisition cards is susceptible to entry of ESD.

Precautions against ESD

Any built-up static electricity should be discharged from the user and the electronic devices before touching an electronic device, before connecting one device to another, or replacing acquisition cards. This can be done in many ways, including the following:

- Grounding oneself by touching a metal surface that is at earth ground. For example, if the computer has a metal case and is plugged into a standard three-prong grounded outlet, touching the case should discharge the ESD on the body.
- Increasing the relative humidity of the environment.
- Installing ESD-specific prevention items, such as grounding mats and wrist straps.

While appropriate precautions to discharge static electricity should always be taken, the user may want to take extra precautions to protect the electronic equipment against ESD if ESD events are observed in the present environment.

The use of wrist straps
Use an ESD wrist strap whenever you open a chassis, particularly when you will be handling circuit cards and components. In order to work properly, the wrist strap must make good contact at both ends (with the user's skin at one end, and with the chassis at the other).

WARNING

The wrist strap is intended for static control only. It will not reduce or increase your risk of receiving an electric shock from electrical equipment. Follow the same precautions you would use without a wrist strap.

WARNING

Wrist straps should only ever be used in situations where no direct power is connected to the circuit or system being handled.

3.1.2 Electromagnetic Compatibility (EMC)

EMC stands for Electromagnetic Compatibility. The overall intention is that electronic equipment must be able to co-exist with other electronic equipment in its immediate vicinity and that the electronic equipment does not emit large amounts of electromagnetic energy. Thus, there are two distinct requirements for electromagnetic compatibility: emission and immunity.

This instrument generates, accepts and can radiate radio frequency energy and, if not installed and used in accordance with the operator manual, may cause harmful interference to other equipment. However, there is no guarantee that interference will not occur in a particular installation.

Immunity test: All immunity tests are done with the failure criterion being a change of the current transducer's control settings. Any of these tests may produce a spurious trigger. Measurements are not valid during and immediately after the immunity tests.

Whether the instrument causes interference to other equipment can be determined by turning the instrument on and off. If this instrument does cause minor harmful interference to other equipment, the user is encouraged to try reducing the interference by one or more of the following measures:

- Re-orient or relocate the affected equipment.
- Increase the distance between the instrument and the affected equipment.
- Re-orient or relocate interface cables.
- Connect the instrument to an outlet on a different supply circuit to the affected equipment.

Electrical supply cables, interface cables and probes should be kept as short as practical, preferably a maximum of 1 m. Interface cables should be screened and interface cables longer than 3 m are not acceptable in terms of interference port immunity.

WARNING

An electrical frequency of approximately 270 kHz or equipment working with an electrical frequency of approximately 270 kHz can interrupt the stability of the GEN3i touch screen. Under these conditions, the touch screen may become erratic or unusable. If such interference occurs, please contact your local supplier for more details.

WARNING

During mains immunity testing, some of the USB ports combined with other parts, such as keyboards, failed during the disturbance bursts and the drivers needed to restart to resume the operation. Whenever you experience this malfunction, using a ferrite coil on the USB cable will resolve the problem. (See Figure 3.1)

Figure 3.1: Ferrite coil

3.2 Environment

3.2.1 WEEE - Waste Electrical and Electronic Equipment

Since February 2003, European Union legislation stating that EU members now restrict the use of hazardous substances in electrical and electric equipment (Directive 2002/95/EC) and promotes the collection and recycling of such electrical equipment (Directive 2002/96/EC) has been in force.

Statutory waste disposal mark

The electrical and electronic devices that bear this symbol are subject to the European waste electrical and electronic equipment directive 2002/96/EC. The symbol indicates that the device must not be disposed of as household garbage.

In accordance with national and local environmental protection and material recovery and recycling regulations, old devices that can no longer be used must be disposed of separately and not with normal household garbage. For more information about waste disposal, please contact local authorities or the dealer from whom the product was purchased. As waste disposal regulations may differ from country to country within the EU, please contact the supplier about waste disposal regulations if necessary.

Packaging

The original packaging of HBM devices is made from recyclable material and can be sent for recycling. For ecological reasons, empty packaging should not be returned to us.

Environmental protection

The product will comply with general hazardous substances limits for at least 20 years, and will be ecologically safe to use during this period, as well as recyclable. This is documented by the 20 years symbol on the system as statutory mark of compliance with emission limits in electronic equipment supplied to China.

3.3 CE Declaration of conformity

For information about the CE Declaration of conformity, please refer to www.hbm.com/highspeed.

3.4 FCC Class A Notice

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1 This device may not cause harmful interference.
2 This device must accept any interference received, including interference that may cause undesired operation.

Note *This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy, and if it is not installed and used in accordance with the instruction manual, it may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.*

IMPORTANT

Any modifications made to this device that are not approved by HBM may void the authority granted to the user by the FCC to operate this equipment.

4 Batteries

4.1 General

The GEN3i has internal batteries. They are used by the system to keep the time and date, even when the system is powered down. When the system starts to loose track of the time and date, these batteries need to be replaced.

Battery lifetime

A battery's lifetime depends on how it is handled. High temperature, super-fast charging and harsh discharges are conditions that harm batteries. Repeated full discharge cycles also stress the battery.

Precautions and warnings when using batteries

- Use the battery only for its intended purpose.
- Do not take batteries apart or modify them. The batteries must not be damaged, crushed, pierced or exposed to high temperatures. If a battery is handled inappropriately, it could be a risk of combustion or explosion.
- Do not leave the batteries in hot or cold places, as you will reduce the capacity and lifetime of the batteries. Always try to keep batteries at room temperature. A system with hot or cold batteries may not work temporarily, even if the batteries are fully charged.
- Do not short-circuit the battery. Accidental short-circuit can occur when a metallic object causes a direct connection between the + (plus) and - (minus) terminals of the battery, for example when a spare battery is carried in a pocket or bag. Short-circuiting the terminals may damage the battery or the object that causes the short-circuiting.

WARNING

Use HBM approved batteries only.

WARNING

If leaked battery fluid comes into contact with your eyes, immediately flush out your eyes with water and consult a doctor, as it may result in blindness or other injury. If leaked battery fluid comes in contact with your body or hands, wash thoroughly with water.
If leaked battery fluid comes into contact with the instrument, carefully wipe the instrument, avoiding direct contact with your hands.

4.2 Removal and replacement

WARNING

ELECTRICAL SHOCK HAZARD! Remove all cables before proceeding.

There are two CR2032 batteries located inside in a GEN3i, one in the backplane (see Figure 4.1) and one in the Battery CPU section (see Figure 4.2). To access the batteries for removal or replacement, the acquisition cards need to be removed from the GEN3i. For instructions on how to remove an acquisition card, please refer to chapter "Removing and installing input cards" on page 99.

CAUTION

All GEN series mainframes are factory-calibrated as delivered to the customer. Swapping, replacing or removing cards may result in minor deviations to the original calibration. Make sure that the input cards are reinstalled in the exact same slot that they were removed from to avoid changes to the calibration results.

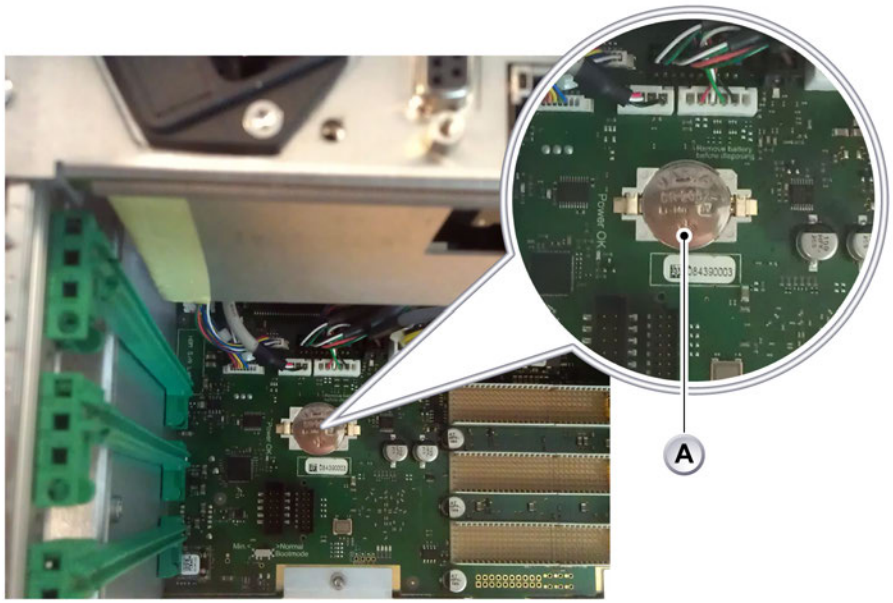


Figure 4.1: Battery backplane

A Battery in the backplane

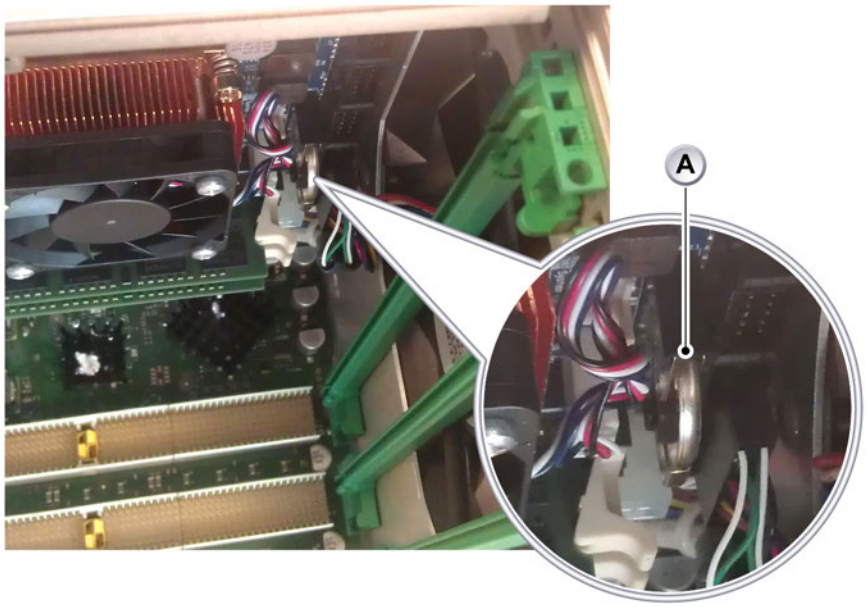


Figure 4.2: Battery PC section

A Battery in the PC section

4.2.1 Remove/replace the battery from the backplane

1 Power off the GEN3i system and remove the power input cable.

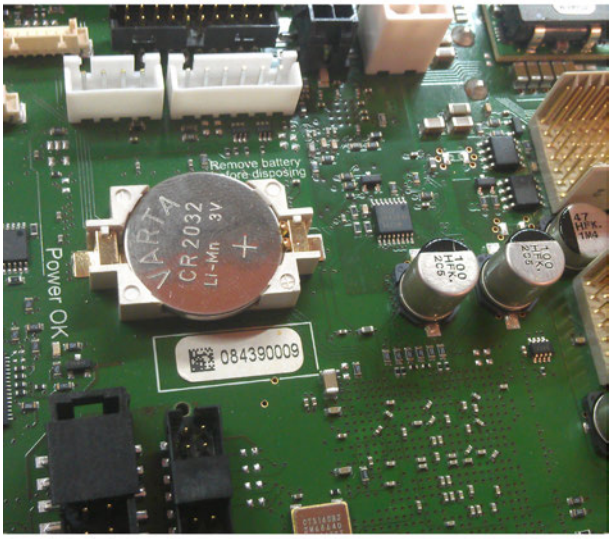


Figure 4.3: Battery - Backplane section

2 Disconnect all cables to the acquisition cards.

3 Remove acquisition cards/blind panels from the GEN3i.
4 To remove the battery, simply pull it out with two fingers.

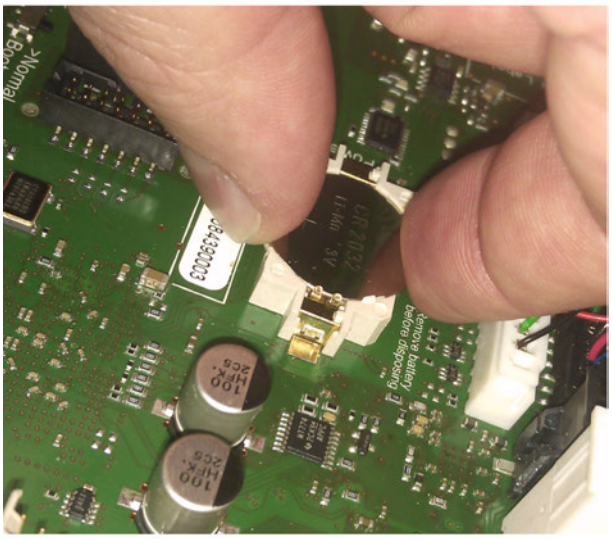


Figure 4.4: Remove battery from the backplane

5 To place the battery on the backplane, place it on the battery holder.

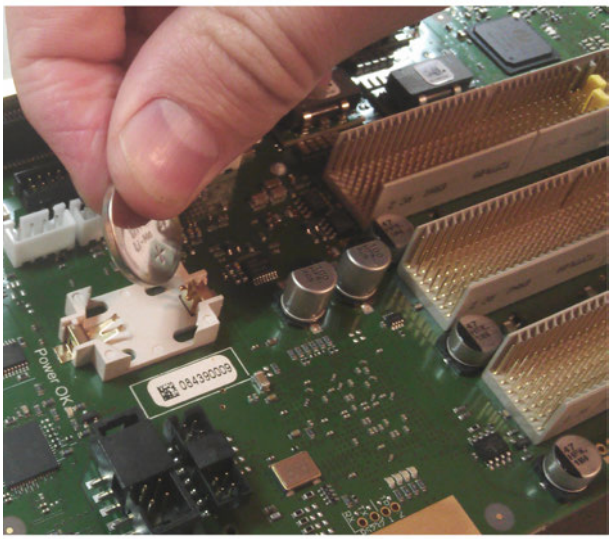


Figure 4.5: Place the battery on the holder (backplane)

6 Push the battery until the lid clicks back into position.

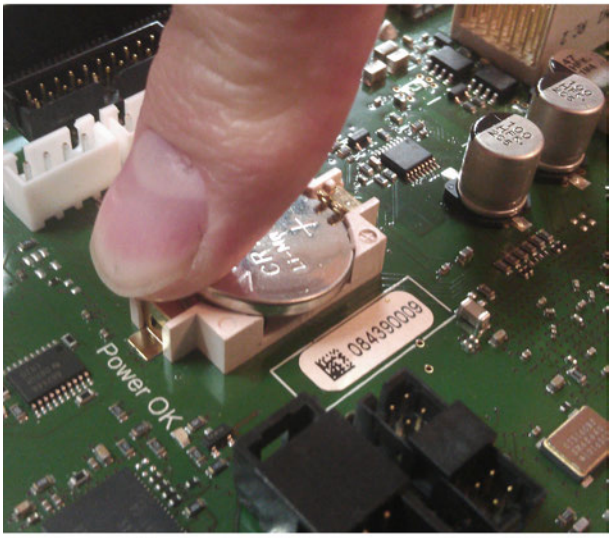


Figure 4.6: Battery almost in its final position (backplane)

4.2.2 Remove/replace the battery from the PC section

1 Power off the GEN3i system and remove the power input cable.

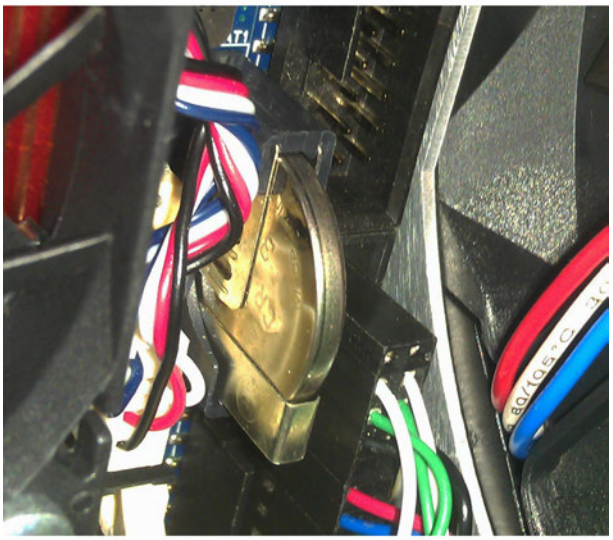


Figure 4.7: Battery - PC section

2 Disconnect all cables to the acquisition cards.
3 Remove acquisition cards/blind panels from the GEN3i.

4 To remove the battery, push the metal lid to the left and pull the battery out of the holder.

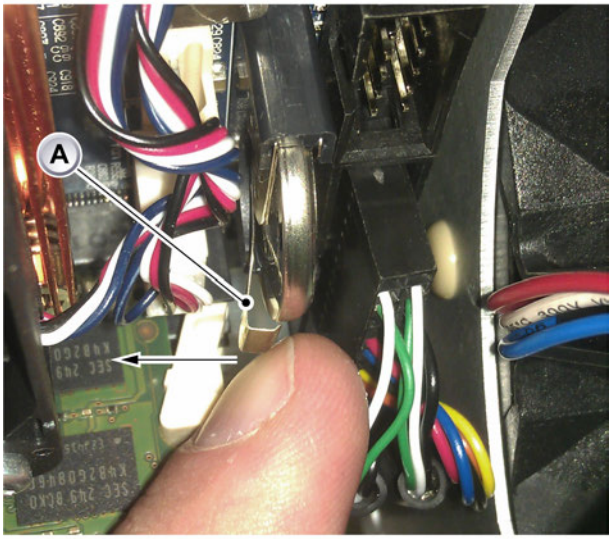


Figure 4.8: Remove battery (PC section)

A Metal lid

5 To place the battery in the CPU section, place it on the battery holder.

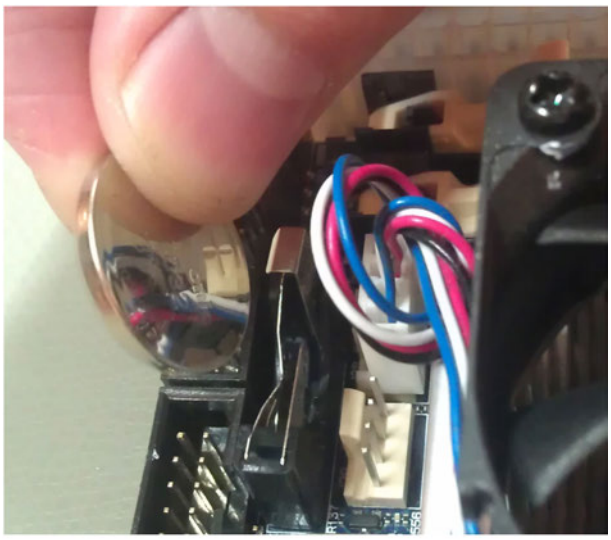


Figure 4.9: Place the battery on the holder (PC section)

Note *Place the new battery in the same direction as the original battery was placed.*

6 Push the battery until the lid clicks back into position.

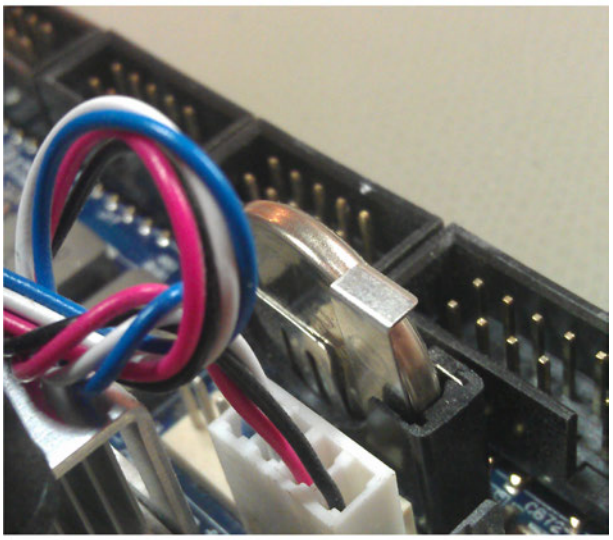


Figure 4.10: Battery in final position (PC section)

7 Install all removed input cards in the exact same sequence as you removed them to avoid changes in calibration results.

4.3 Recharging

The GEN3i does not use rechargeable batteries. When batteries are depleted, dispose of the batteries.

4.4 Disposal

Dispose of used batteries only in accordance with local chemical waste regulations. Always recycle.

WARNING

Do not dispose of batteries in a fire.

For more information about waste disposal, please contact the local authorities or the dealer from whom the product was purchased.
As waste disposal regulations may differ from country to country within the EU, please contact the supplier about waste disposal regulations if necessary.

5 Mains Power

5.1 Power and frequency requirements

To connect or disconnect the instrument from the AC supply, plug or unplug the IEC connector from the instrument or external power supply. The instrument should be positioned to allow access to the AC connector. The front power switch on the instrument is not a disconnecting device. When the instrument is connected some power will be consumed.
For more information, please refer to chapter "Connecting power" on page 72.

The GEN3i uses up to 250 VA and operates from line voltages between 100 V AC and 240 V AC at 47-63 Hz. The power connection of the GEN3i is a standard IEC 320 EN 60320 C14, 2-pole, 3-wire (male) appliance inlet, designed for 250 V at 10 A. Access to the AC supply fuses can only be made if the AC supply connector is removed. For more information, please refer to chapter "Fuse requirements and protection" on page 74.

CAUTION

Do not position the GEN3i in a way that makes it difficult to remove the power input cable.

The GEN3i must be connected to ground by the conductor of the supply cable. This is to ensure that all electromagnetic Compatibility (EMC) requirements are met.

5.2 Connecting power

The power inlet and the protective ground connection are located at the top of the GEN3i system. A mains power cord that is in accordance with the destination country's standards is shipped with the unit. For more information on power consumption, please refer to chapter "Mains Power" on page 71.

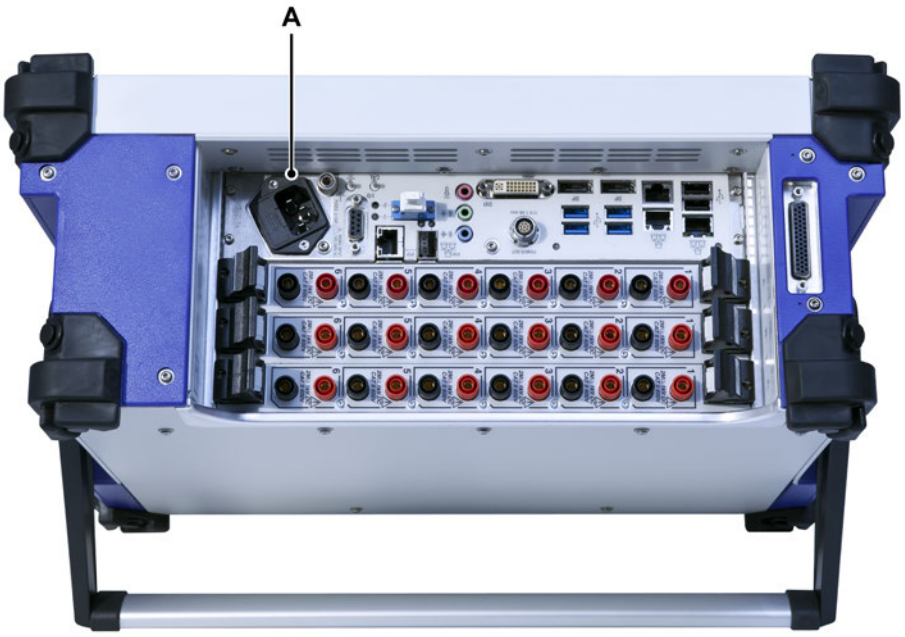


Figure 5.1: GEN3i Portable Data Recorder

A Power inlet

The power inlet connects/disconnects the main power from the GEN3i. To disconnect the GEN3i from the AC supply completely, unplug the IEC connector from the instrument.
Plugging in the unit will not switch on the GEN3i instrument. Use the standby button on the front panel for this purpose; see "Front panel control" on page 119.

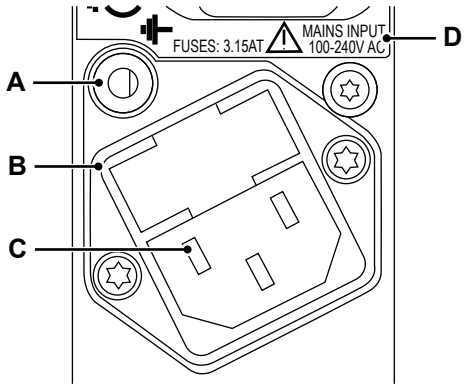


Figure 5.2: Power inlet

A Protective ground
B Fuses, 2 times of 3.15 A each
C Power Inlet
D Voltage rating

HINT/TIP

After an unexpected power loss the instrument will automatically return to the last power state when power is restored.

5.3 Fuse requirements and protection

GEN3i is equipped with replaceable fuses. The fuse positioning stated in this manual and on the GEN3i must be followed. Additionally for the UK, a fuse should be fitted in the line supply plug.

WARNING

Any interruption of the protective conductor inside or outside the apparatus is likely to make the apparatus dangerous. Intentional interruption is prohibited.

When the apparatus is connected to its supply, terminals may be live, and opening covers to remove parts is likely to expose live parts.

Whenever it is likely that the protection has been impaired, make the apparatus inoperative and secure it against any unintended operation.
For example, if the apparatus shows visible damage or has been subjected to severe transport stresses, the protection is likely to be impaired.

It is the responsibility of the user to ensure the safety of any accessories used with the equipment, such as probes.

WARNING

Connect a protective ground wire as an additional safety measure to prevent electric shock or damage to GEN3i.

Using this device properly depends on the user reading all instructions and labels carefully.

If the instrument is used in a manner not specified by HBM, the protection provided by the instrument can be impaired.

5.4 Fuse replacement

To gain access to the fuses, proceed as follows:

1. Power off the system and remove the power cord. This will enable access to the groove on the fuse holder.
2. Using a pocket screwdriver, insert the screwdriver in the slot under the fuse door and gently lift the door. When unlatched, pull out the fuse door.

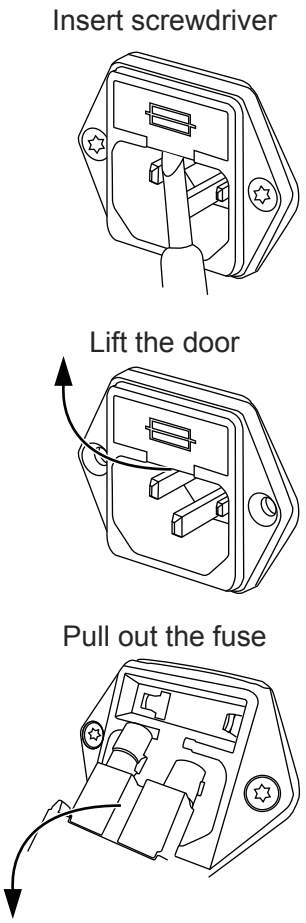


Figure 5.3: Access to fuses

WARNING

Replace both fuses with new ones that have the correct type and rating, as indicated on GEN3i and in this manual, at the same time.

The fuse holder is equipped with two identical fuses.

To replace the fuses, proceed as follows:

1 Remove the fuses from their fixture and insert new fuses of 3.15 A (slow) each.
2 When done, re-insert the fuse holder and push it into position.

6 Introduction

6.1 Introducing GEN3i

Welcome! You have made the right choice; your GEN3i Portable Data Recorder is one of the most sophisticated and powerful systems on the marketplace and demonstrates the high quality HBM has to offer. GEN3i is an all-in-one, field-ready, feature-packed unit.

Figure 6.1: Using GEN3i

Some of the main features include:

- Combines a data recorder and transient recorder system
- Transient RAM up to 100 MegaSamples per channel in parallel
- Isolated and non-isolated channels with high-fidelity signal conditioning
- Unlimited recording size and duration
- Built-in PC with sophisticated interface and analysis software
- A variety of data storage capabilities
- High-resolution, 17", TFT, SXGA touch screen display
- Portable and rugged

Data archiving is a challenging task when doing data acquisition. GEN3i offers a variety of storage and archiving options. Internally GEN3i is equipped with a 480 GB solid state Hard Drive. The instrument can be connected to a network using built-in wired and wireless interfaces. Standard USB (4 x USB2 and 4 x USB3) interfaces can be used for any kind of data storage device.

When it comes to usability, a fully touch-optimized Instrument Panel GUI offers a working environment that allows you to achieve your goals with effectiveness, efficiency and satisfaction.

This Instrument Panel provides one-touch access to the features most commonly used for everyday work.

Note *Not all hardware features described in this manual are available via the Instrument Panel.*

For sophisticated or more exotic features, you can use Perception software that is accessible from the Instrument Panel via a single touch.

6.2 Mainframe overview

There are several different GEN series mainframes available:

Model	Slots	Design	Comments
GEN2tB	2	Portable	Tethered, portable data recording solution, best suited for low channel count applications. Option for 19" rack mount available.
GEN3i	3	Portable	An integrated all-in-one portable data recording solution suitable for field use. Best suited for lower channel count or medium computing power applications.
GEN3t	3	Portable/Rack	Tethered, portable data recording solution, best suited for lower channel count applications. Option for 19" rack mount available.
GEN7i	7	Mobile	An integrated all-in-one mobile data recording solution suitable for field use. Best suited for medium channel count or high computing power applications. Option for 19" rack mount available.
GEN7tA	7	Mobile/Rack	Tethered mobile data recording solution, best suited for medium channel count applications. Option for 19" rack mount available.
GEN17tA	17	Rack	Tethered 19" rack mounted mainframe. Best suited for higher channel count applications.

All mainframes share many of the GEN series features. Besides the listed differences in the table above, other differences are: mechanical form factor, power consumption, integrated PC or tethered PC use, etc. For technical details, please refer to the individual mainframe data sheets.

6.2.1 Mainframe feature comparison

Mainframe	Standard streaming (cPCI backplane)	Fast Streaming (PCI-e backplane)	Option carrier card	Direct NAS storage (using iSCSI)	EtherCAT® support
1-GEN2i-2, 1-GEN5i-2, 1-GEN7T-2, 1-GEN16T-2	*Yes*	*No*	*No*	*No*	*No*
Exceptions 1-GEN7T-2 and 1-GEN16T-2 with IM2	*Yes*	*No*	*No*	*Yes*	*No*
1-GEN3I, 1-GEN3IA, 1-GEN7I and GEN7IA	Yes	Yes	Yes	No	No
1-GEN2TB	No	Yes	Yes	Yes	No
1-GEN3T, 1-GEN7TA and 1-GEN17TA	Yes	Yes	Yes	Yes	Yes

Note *Grey columns are end-of-life systems.*

Master/Slave support	Synchronization connector (also Slave input)	Extended Master/Slave	Master/Slave card	Master output card (Master/Slave card version 2)
1-GEN2I-2, 1-GEN5I-2, 1-GEN7T-2 and 1-GEN16T-2	*No*	*No*	*Yes*	*No*
Exception 1-GEN2I-2 with IM2	*Yes*	*No*	*Yes*	*No*
1-GEN3I, 1-GEN3IA, 1-GEN7I, GEN7IA, 1-GEN2TB, 1-GEN3T, 1-GEN7TA and 1-GEN17TA	Yes	Yes	No	Yes

Note *Grey columns are end-of-life systems.*

IRIG/GPS and Ethernet PTP synchronization	IRIG and IRIG/GPS synchronization	1 Gbit Ethernet (RJ45, electrical) PTP synchronization	1 Gbit Ethernet (SFP, optical) PTP synchronization	10 Gbit Ethernet (RJ45, electrical) without PTP synchronization	10 Gbit Ethernet (SFP, optical) without PTP synchronization
1-GEN2I-2, 1-GEN5I-2, 1-GEN7T-2 and 1-GEN16T-2	*Yes*	*No*	*No*	*No*	*No*
Exceptions 1-GEN7T-2 and 1-GEN16T-2 with IM2	*Yes*	*No*	*No*	*Yes*	*No*
1-GEN3I, 1-GEN3IA, 1-GEN7I, GEN7IA, 1-GEN2TB, 1-GEN3T, 1-GEN7TA and 1-GEN17TA	Yes	Yes	Yes	No	No

Note *Grey columns are end-of-life systems.*

6.3 Hardware

The acquisition section of the GEN3i is based on the successful and proven GEN series Data Acquisition System.

In GEN3i the same concepts are used.

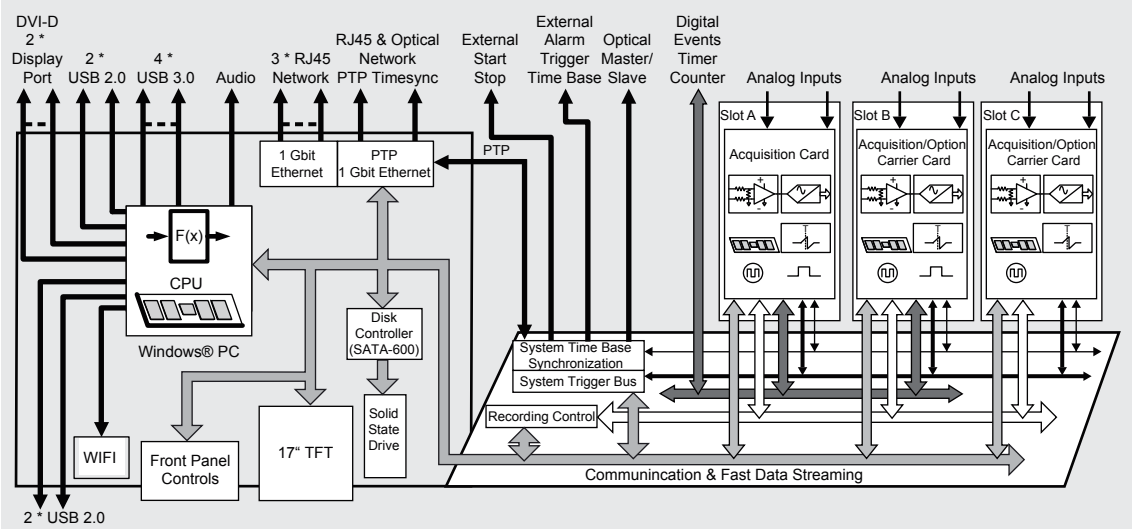


Figure 6.2: Block Diagram GEN3i Portable Recorder

6.3.1 PCI-e/CPCI backplane

GEN3i uses a combined PCI-e/CPCI backplane. The PCI-e (Peripheral Component Interconnect Express) backplane can transfer data at very high speeds to ensure the highest system throughput. The CPCI (Compact Peripheral Component Interconnect) backplane can transfer data at high speeds to ensure a high system throughput. The combined backplane supports backward compatibility to support any GEN series acquisition cards and allows new acquisition cards to use the faster PCI-e transfer speeds.

HINT/TIP

The CPCI backplane is the standard data storage bus. All acquisition cards introduced to market before 2014 support only this backplane. The maximum aggregate streaming rate for these acquisition cards is 200 MB/s.

Check the detailed specifications of the individual acquisition cards to see whether it uses the fast data storage bus of the GEN3i if aggregate streaming rates above 200 MB/s are required.

6.3.2 Input cards

GEN3i can accept up to three input cards. Each input card includes one or more digitizers, a powerful CPU or DSP for filtering, intelligent triggering, and acquisition management. For more information on the various cards, please refer to chapter "Available input cards" on page 191.

Note *Before changing or removing input cards, always check the warranty information. Changing input cards will void the tight calibration of the input card. Wider tolerances have to be considered when exchanging input cards. See individual specification of input cards used in appendix A “Specifications” on page 378.*

6.3.3 Master/Slave support

The GEN3i system has a built-in Master/Slave synchronization connector. This connector supports the GEN series Master/Slave extended synchronization protocols and is fully backward compatible with the basic synchronization protocols. The single synchronization connector allows for the direct connection of one Slave to the GEN3i or the GEN3i to be a Slave within any Master/Slave multi mainframe setup.

6.3.4 Thermal protection

Every GEN series mainframe supports a feature called Thermal Shutdown. For this, the mainframe and acquisition cards have built-in digital thermal sensors to measure local temperatures. The GEN series embedded software reads these values every minute and monitors the system's internal temperature for overheating.

Automatic user warnings are initiated using the following diagram (see Figure 6.3).

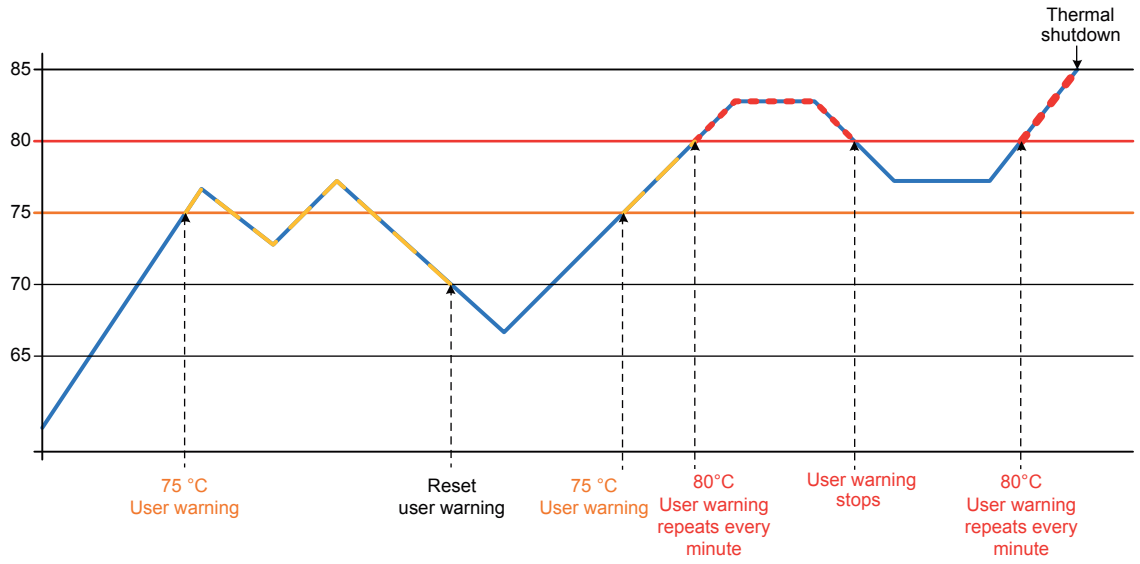


Figure 6.3: Thermal protection - Automatic user warnings

- As soon as one of the internal thermocouples measures a temperature above +75 °C for the first time, a single user warning is initiated. As long as the highest temperature measured is above +70 °C and below +80 °C, no additional user warnings are initiated.
- If the internal temperature drops below +70 °C after reaching +75 °C, the system assumes that the user has performed an action, to reduce internal temperatures. If the internal temperature reaches +75 °C again, the system assumes that there is a new thermal problem and a new user warning is initiated.
- If the internal temperature keeps rising and reaches +80 °C, the system assumes that a critical zone has been reached. User warnings will be sent every minute for as long as the measured temperatures are above +80 °C. If the temperature drops below +80 °C, the warnings sent at minute intervals stop. If the temperature rises above +80 °C again, user warnings are initiated every minute again.
- If the internal temperature were to keep rising and then reaches +85 °C, an automatic thermal system shutdown user warning is initiated, the automatic thermal shutdown event is logged in the systems error log and the system will shut down.

At next power-on of the GEN series system, the automatic thermal shutdown event will be presented to the user again and can be found in the error diagnostics of the mainframe.

6.4 Acquisition

GEN3i is a multi-channel Portable data recorder. It provides real-time data for waveform and meter displays. It allows unlimited recording duration and file size at a high streaming rate. Statistics are performed in real-time. Its extreme performance signal conditioning includes both Bessel and Butterworth anti-alias filters to provide excellent response.

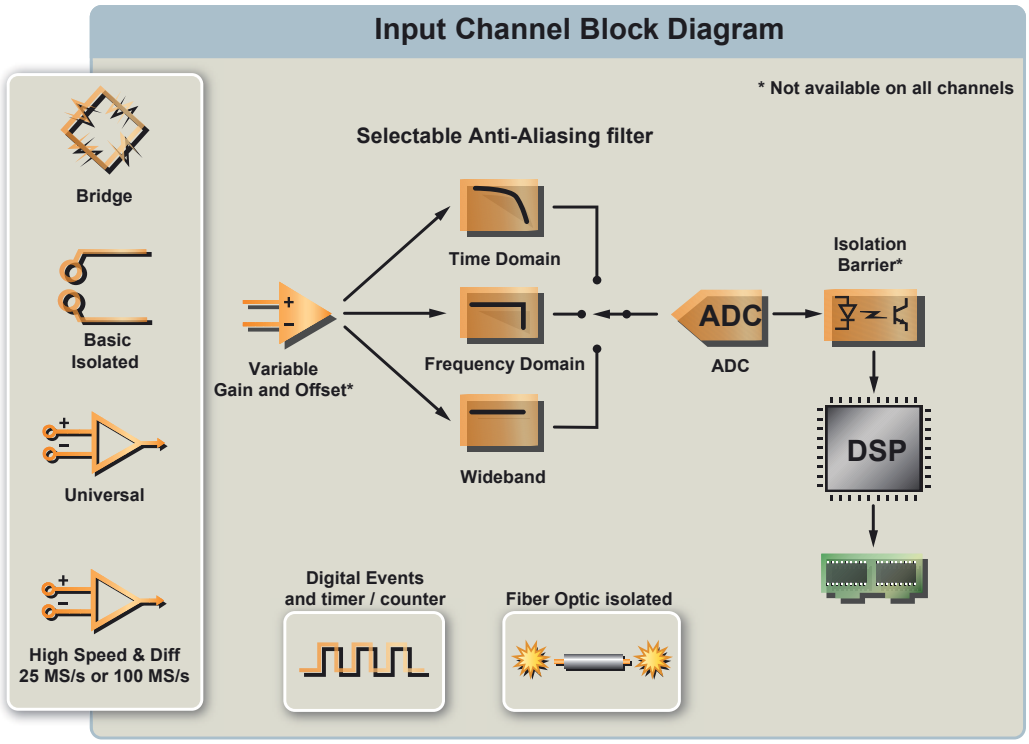


Figure 6.4: Input channel block diagram

It also functions as a transient recorder with a hardware trigger on all channels with hysteresis, delay and logic features. Transient memory is huge and can capture minutes of data on all channels. Segmented sweeps are displayed with no dead time and the recorder has a wide analog bandwidth.

6.4.1 StatStream®

Most PC-based DAQ systems can easily acquire megabytes of data. But even the most powerful PC is poorly equipped to display and process files of megabytes or gigabytes. In fact, most DAQ systems fail to display over 99% of live data! The exclusive StatStream® technology accelerates all aspects of a measurement task with dedicated hardware and firmware.

While recording, StatStream® pre-processes a display summary at the full resolution of a PC monitor. Even a single transient point on any channel is accurately displayed.

In addition, StatStream® continuously calculates parameter values on blocks of data. Vital statistics are available at every moment, including warnings if any channel goes off scale. The Perception software offers a variety of meters to display these on-line parameters.

When reviewing stored files, the embedded StatStream® data enables an accurate, detailed overview of any size file in seconds. Unlike competitive systems, the GEN3i has no need to inspect gigabytes of information just to display the last kilobyte. While zooming in, more detail is displayed while always maintaining the highest visible resolution.

6.5 Signal conditioning

GEN3i supports common analog sensors with the highest performance signal conditioning available. All inputs are sampled simultaneously for exact time correlation.

Plug-and-play hardware discovery with scalability to any number of channels. Perception software can group and outline similar amplifiers for one-click settings. Extensive diagnostics gives the confidence of correctly wired and working sensors before any test.

6.6 Data storage

In addition to mega samples of on-board RAM, record data directly to the GEN3i hard drive, or USB device. In addition you can archive your data on a USB stick, or to a network server over the Gigabit Ethernet. GEN3i always stores to on-board high-speed RAM. Recorded data is then automatically stored at the GEN3i defined storage location at maximum speed.
Storing data to the built-in GEN3i SSD allows data storage at 200 MB/s. In continuous mode, a full drive recording can be made at 200 MB/s. In circular recording, the GEN3i can monitor signals at 200 MB/s forever and will stop only when triggered by a user pre-defined event. The entire SSD can then be used as pre-trigger recording.

Recorded files are standard Perception files with the PNRF extension (Perception Native Recording File).

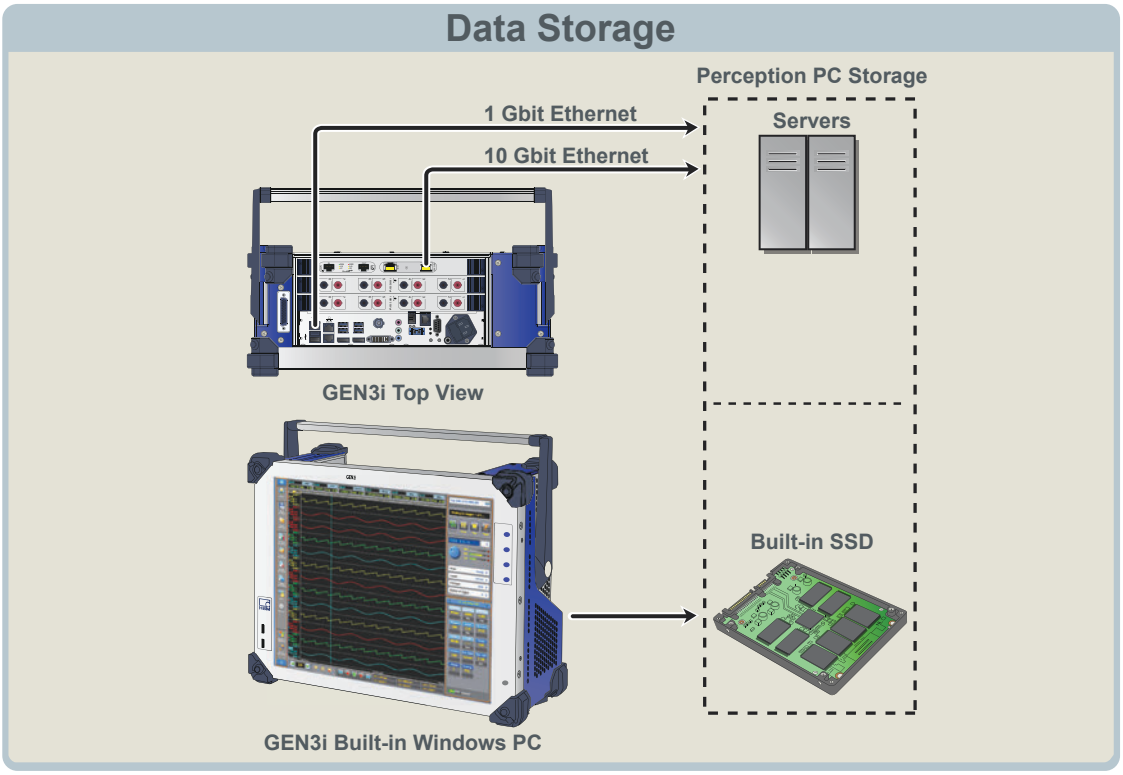


Figure 6.5: Data storage options

6.7 PC Section

GEN3i has a built-in industrial PC. This PC provides all the standard features that you would expect from an industrial grade quality PC.

Features include:

- Intel® Core™ i5 processor (3rd generation) (1)
- Ivy Bridge M chipset (x77)
- Microsoft® 64 bit Windows® 10 Operating System (2)
- 8 GB DDR3 RAM
- 480 GB SSD SATA 6 (Solid State Drive)
- On-board graphics engine with video out (dual monitor support)
- Full audio and internal speaker
- 4 USB 2.0 and 4 USB 3.0 ports
- 4 wired (RJ45) and 1 Optical (SFP) Gigabit Ethernet connector, PTP support for timing synchronization between 1 fixed RJ45 and 1 Optical (SFP) of these ports.
- Wireless LAN support in accordance with IEEE 802.11 b/g/n standards, up to 300 Mbit/s

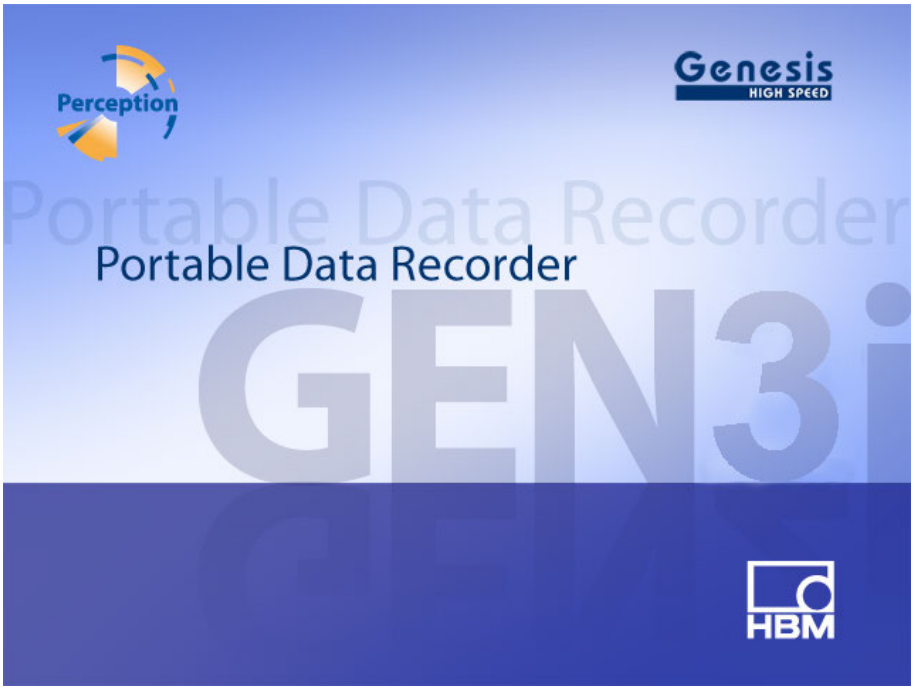
(1) Intel® and Intel® Core™ are trademarks of Intel Corporation in the U.S. and/or other countries.

(2) Microsoft, Encarta, MSN, and Windows are either registered trademarks or trademarks of Microsoft Corporation in the United States and/or other countries.

For full details on GEN3i, please refer to the specification section ("B3762-6.0 en (GEN3i Portable Data Recorder)" on page 378) of this manual.

6.8 Perception Software

Perception Software is installed on your GEN3i for control, analysis, archiving and reporting.



The GEN3i has two modes of operation. During operation, you can choose between these two modes.

Primary mode:

- Instrument Panel - for daily use

Secondary mode:

- Standard Perception - For post-processing

The Instrument Panel is the dedicated touch screen software interface which has been specifically designed for GEN3i as the normal mode of operation. However, you can switch to Standard Perception for on-board post-processing at any time.

- When in the Instrument Panel, click the Perception icon in the lower left-hand corner of the toolbar to switch to Perception.

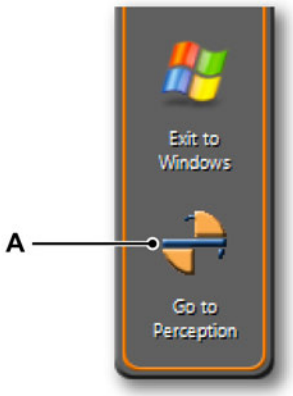


Figure 6.6: Toolbar

A Go to perception

- When in Perception, navigate to the menu item **File**, select **Switch to Instrument Panel** and confirm the action to switch to the Instrument Panel.

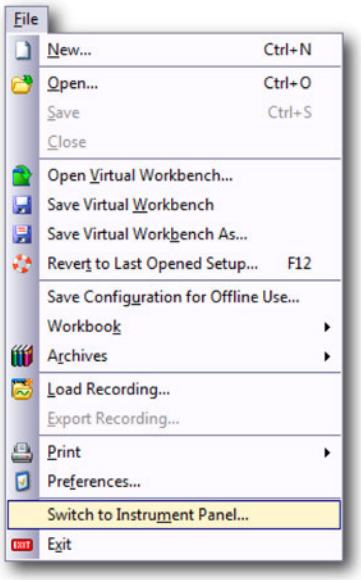


Figure 6.7: Switch to Instrument Panel option

Note *For general information on Perception, please refer to user manual for Perception, which is provided separately.*

Note *For general information on the Instrument Panel, please refer to the user manual for the Instrument Panel Software for GEN3i, which is provided separately.*

Note *The settings from the advances features can be changed when switching to the Instrument Panel mode.*

6.8.1 Windows® logon password and remote desktop access

IMPORTANT

By default the integrated systems do NOT have a password for the default account “GENUser”.

The message that pops up when using remote desktop (RDP) access is a “standard” login message, because RDP connection requires a password. As the integrated system doesn’t have a password, a RDP connection can not be made.

IMPORTANT

The customer need to ADD a password to his integrated system, and then RDP can work (if RDP is enabled on the system).

6.9 Perception language settings

Various program settings are stored in the Perception preferences. These settings include, but are not limited to, **Perception language**, start-up options, options for updates, video information, display settings, etc.

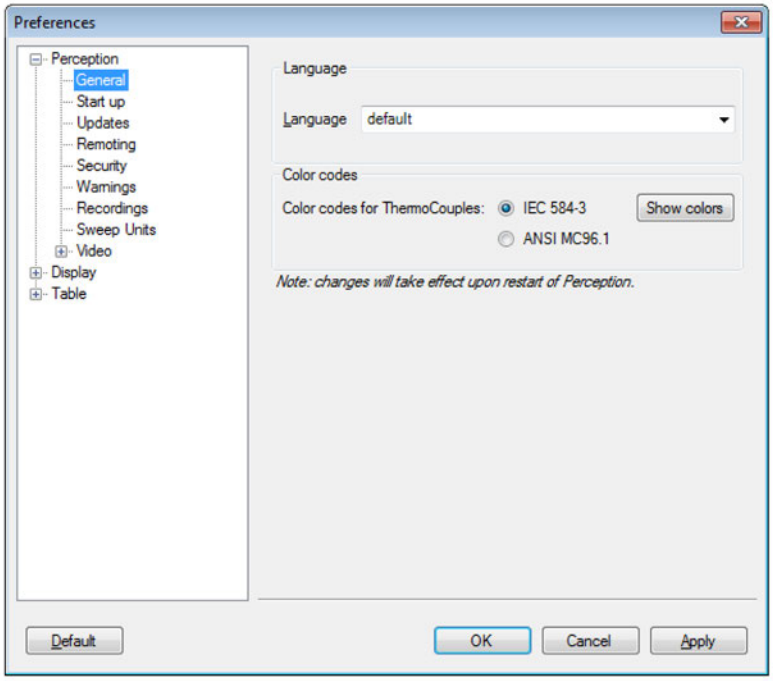


Figure 6.8: Preferences dialog

To open the Preferences dialog:

- Click **Preferences...** in the File menu.

User Interface Language options

To startup Perception in a specific User Interface Language:

1 Click **Preferences...** in the File menu.
2 Select **General** in the tree view of the **Preferences** dialog.
3 In the **Language** drop-down list, you can select from the following choices:

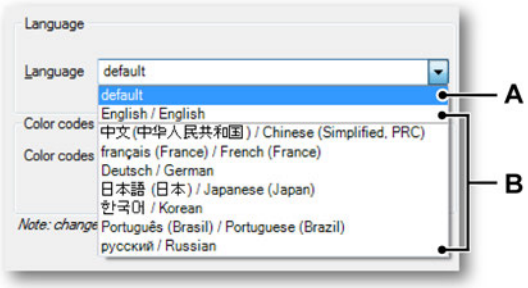


Figure 6.9: User Interface Language area (detail)

A **default:** The software detects the operating system language and uses that language (if available).

B The software is run in the selected language.

User Interface Mode startup options

To start up Perception in a specific User Interface Mode:

1 Click **Preferences...** in the File menu.
2 Select **Start up** in the tree view of the **Preferences** dialog.
3 In the **User Interface Mode** drop-down list, you can select from the following choices:

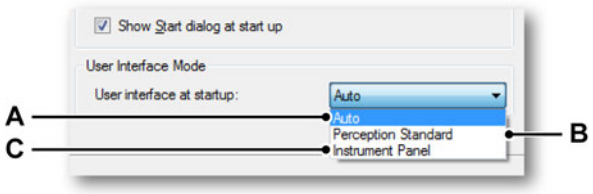


Figure 6.10: User Interface Mode area (detail)

A **Auto** The software detects which system Perception is being run on and starts in the corresponding mode.

B **Perception Standard** The standard Perception GUI. This is the default option on PCs and GEN7i/GEN7iA.

C **Instrument Panel** The Instrument Panel GUI, which is the default option for GEN3i and GEN3iA. For more information, please refer to Figure 6.7 "Switch to Instrument Panel option" on page 91.

Perception will start in the defined User Interface mode.

7 Setting up the GEN3i

7.1 PC connections

GEN3i has a PC motherboard inside. This PC motherboard has a lot of connections that can be used to connect other devices to the GEN3i system.

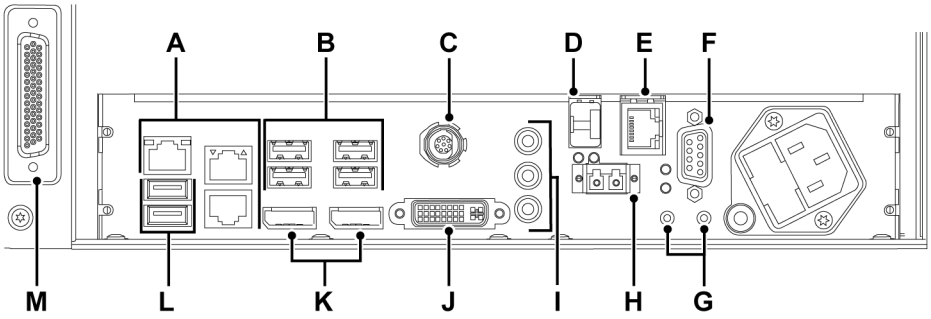


Figure 7.1: PC connections

A **3 * RJ45 - 1 Gbit network ports**
See "Communication and control" on page 156 for more details.

B **4 * USB 3.0 ports**
See "USB 3.0 and USB 2.0 ports" on page 97 for more details.

C **DC power output**
See "DC power output" on page 109 for more details.

D **PTP enabled network optical SFP slot (SFP module is optional)**
See "Communication and control" on page 156 for more details.

E **PTP enabled network RJ45**
See "Communication and control" on page 156 for more details.

F **I/O connector** (trigger in/out, clock in, event out, start/stop)
See "I/O connector" on page 170 for more details.

G **Probe calibration**
See "Probe calibration" on page 107 for more details.

H **Master/Slave synchronization** (optical)
See "Master/Slave Synchronization" on page 159 for more details.

I **Sound, Microphone, Speakers**
See "Sound, microphone, speakers" on page 98 for more details.

J **DVI-I Graphics port**
See "PC connections" on page 96

K **2 * Display ports**
See "DVI-I Graphics and display ports" on page 97 for more details.

L **2 * USB 3.0 ports**
See "USB 3.0 and USB 2.0 ports" on page 97 for more details.

M **Digital Event/Timer/Counter**
See "Digital Event/Timer/Counter" on page 111 for more details.

7.1.1 USB 3.0 and USB 2.0 ports

The GEN series integrated system supports both USB2.0 and USB 3.0 ports.

USB 3.0 is the third major version of the Universal Serial Bus (USB) standard for computer connectivity. Among other improvements, USB 3.0 adds a new transfer mode called "SuperSpeed" (SS) that can transfer data at up to 5 Gbit/s (625 MB/s). This is more than ten times faster than the 480 Mbit/s (60 MB/s) top speed of USB 2.0. USB 3.0 ports and cables are distinguishable from their 2.0 counterparts either by the blue color of the ports or the SS initials on the plugs.

Figure 7.2: USB 3.0 cable and connections

Whenever possible, use the USB 3.0 ports to transfer data faster. It requires USB 3.0 capable devices to allow for operation at USB 3.0 speeds. When a USB 2.0 device is plugged into a USB 3.0 port, the device still operates at USB 2.0 speeds.

When a USB 3.0 device is plugged into a USB 2.0 port, the device still operates at USB 2.0 speeds.

7.1.2 DVI-I Graphics and display ports

- **DVI-Graphics port**
  An external digital monitor can be connected to the DVI_D connector. This connector has also DVI analogue support.
- **Display ports**
  One external digital monitor can be connected to each of these display port connectors.

A total of three external monitors can be connected simultaneously. However, the DVI monitor is a cloned version of the built-in screen in this setup.

7.1.3 Sound, microphone, speakers

The GEN3i unit is delivered with only one internal (mono) speaker. For other audio options, the GEN3i unit has connectors (3.5 mm jack) for line-in, speaker-out and microphone-in.

As soon as the speaker-out connector is used by plugging a 3.5 mm jack into it, the internal speaker is disabled.

Use the Windows® audio setup to control how these connectors are used.

7.2 Removing and installing input cards

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN3i system, its connections or a plug-in card.

CAUTION

The GEN3i Portable data recorder is factory-calibrated as delivered to the customer. Swapping, replacing or removing of cards may result in minor deviations to the original calibration. The GEN3i system should be tested and, if necessary calibrated, at one-year intervals or after any major event that may affect calibration. When in doubt, consult the local supplier.

7.2.1 Removing cards

CAUTION

Heatsink and other parts of the card may be hot when removed just after switch-off.

To remove a card:

1 Power off the GEN3i system and remove the power input cable.
2 Disconnect all cables from the acquisition cards.

3 Loosen the small set screw on both ejectors on the card.

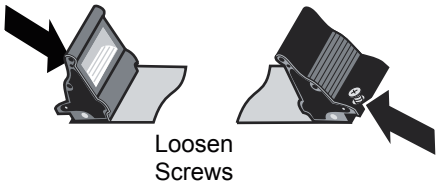


Figure 7.3: Removing card (Part 1)

4 Press the inner grey button on each ejector to release the catch.

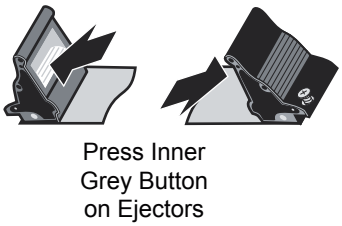


Figure 7.4: Removing card (Part 2)

5 Press both ejectors outward to release the card. They act as levers to gently pull the card from its backplane sockets.
6 Slide the card out of the GEN3i unit.

7.2.2 Installing cards

To install a card:

1 Power off the GEN3i system and remove the power input cable.
2 Ensure that the ejector levers are in the farthest outermost position, tilting away from the card.
3 Slide the card into its guide rails until the ejectors contact the perforated metal strips on the left and right.
4 Press both ejectors inward to seat the card. They act as levers to gently pull the card into its backplane sockets. The grey button should snap to its default position and lock the ejectors.
5 Tighten the small set screw on both ejectors on the card:

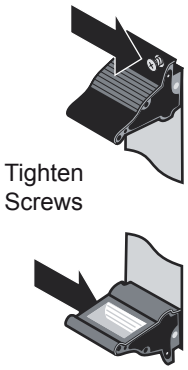


Figure 7.5: Card ejectors with screws

WARNING

Screws must be locked to meet CE emissions.

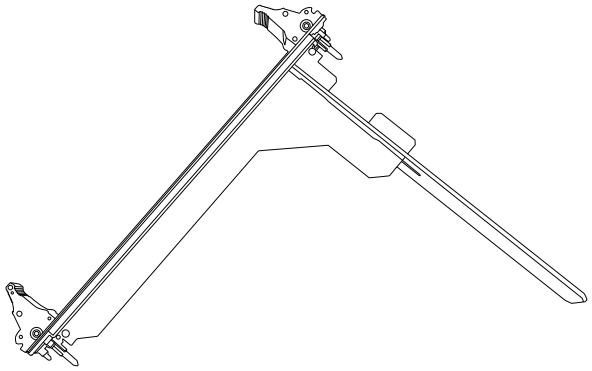


Figure 7.6: Blind panel (1-G009)

WARNING

Any empty slots must be covered with a blind panel on the back to meet the cooling requirements of the mainframe.

7.3 Handle

The handle handles are used to carry the GEN3i system. Only carry the instrument when the handle is in the upright position.

Figure 7.7: GEN3i with handle in the upright position

7.3.1 Turning the handle

You can turn the handle to act as built-in stand:

1 Put instrument on a flat surface.

2 Push in the button on both sides of the handle.

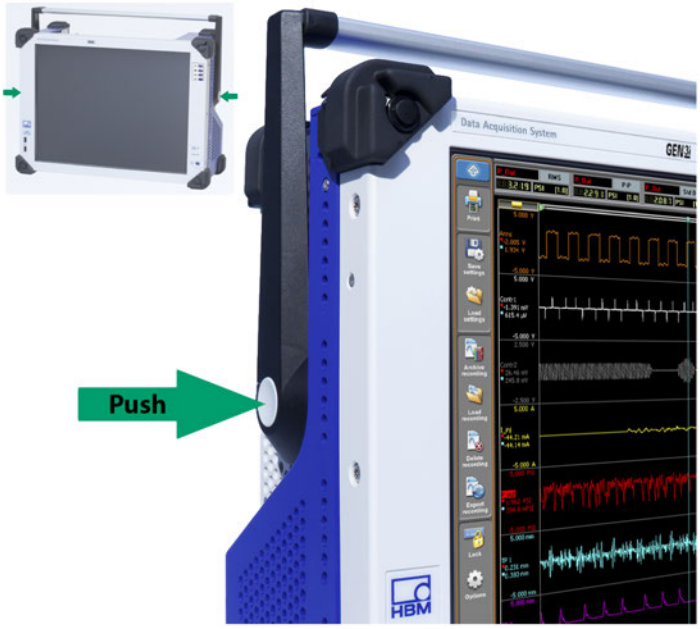


Figure 7.8: Button on the handle

2a Rotate the handle towards the back of the unit and release the buttons on the handles. The handle will snap into one of its fixed positions (30° indexing).

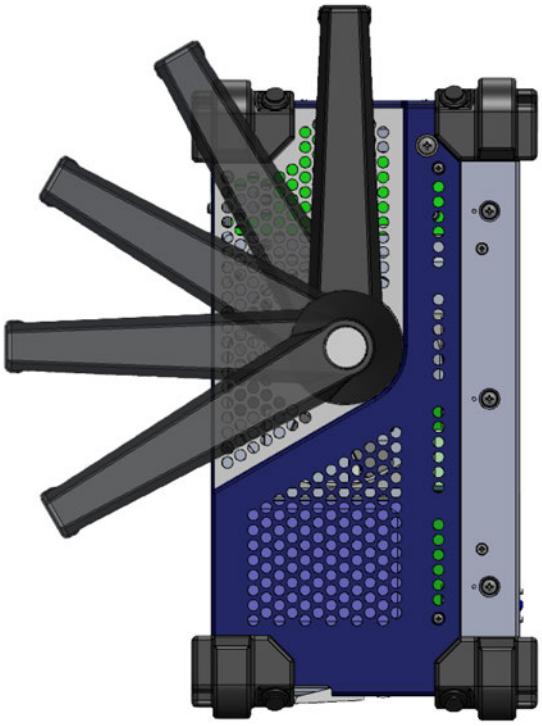


Figure 7.9: GEN3i multiple handle positions

3 Gently turn over the GEN3i unit so that it rests on the handle's flat surface.

4 The GEN3i unit is now supported by its handle.

Figure 7.10: GEN3i supported by its handle

When the handle is turned to back of the unit, it can be used to lift the front of the instrument so that the display is angled towards the user. In Figure 7.10, the angle between the display and horizontal axis is about +40 °. The angle can be changed by using other handle positions accordingly.

7.4 Feet

GEN3i stands on four rubber feet in normal operation position. Two feet are positioned at the rear and two are at the front of the instrument. Two extra, foldable front feet can be used to lift the instrument front so the display angle is towards the user. The angle between display and vertical axis is about +8 ° in this position.

7.4.1 To turn the feet out:

1. Put the instrument on a flat surface.
2. Lift the instrument front.
3. Pull out the front feet by turning the back of the feet towards the front of the instrument.
4. Gently put down the GEN3i front and it will stand on its feet.

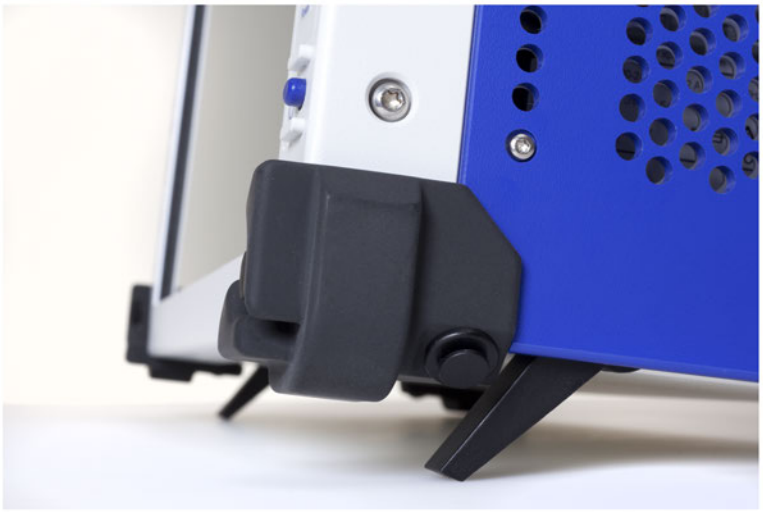


Figure 7.11: GEN3i stand on feet out

7.4.2 To turn the feet in:

1. Put the instrument on flat surface.
2. Slightly lift the instrument front.
3. Push in the front feet by turning the feet towards the back.
4. Gently put down the GEN3i front.

7.5 Probe calibration

The GEN3i mainframe is provided with a probe calibration output. This output can be used to calibrate probes used in combination with the Genesis High-speed measurement system.

The probe calibration output drives a calibration signal with the following characteristics:

- ~1 kHz square wave
- 0 V to 2 V amplitude when using a 1 MΩ load
- 0 V to 1 V amplitude when using a 50 Ω load

In order to calibrate a probe, connect the probe output to an acquisition card and set up the acquisition channel in accordance with the probe calibration signals as described above.

Connect the probe ground wire to the probe calibration ground output pin and the probe input to the probe calibration signal output pin. See Figure 7.12.

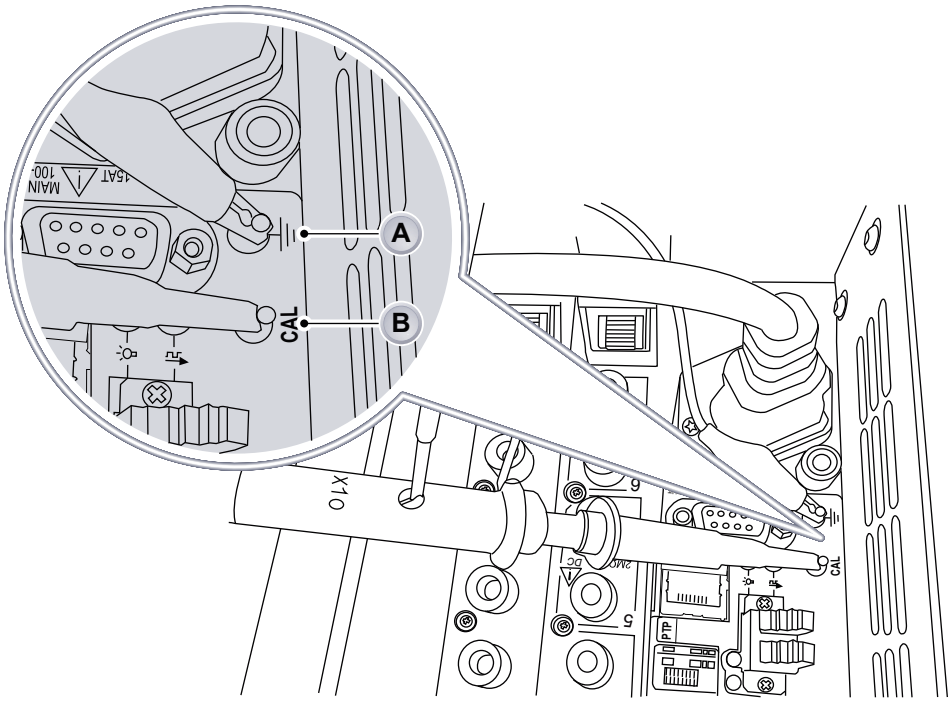


Figure 7.12: Probe calibration

A Probe GND

B Probe input

Set the trimmer of the probe so that the signal in Perception resembles the input signal.
Figure 7.13 below shows how the signal should look. When the trimmer is positioned incorrectly, undershoot or overshoot is seen in the signal.

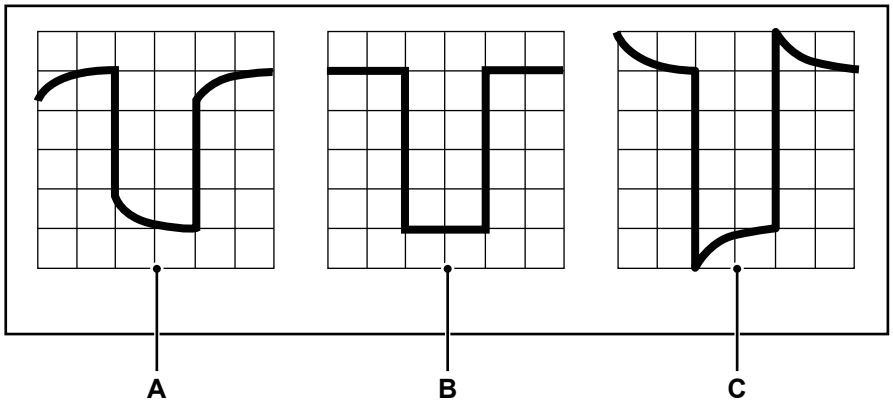


Figure 7.13: Trimming of response - Incorrect and correct waveform responses

A Incorrect - Undershoot

B Correct

C Incorrect - Overshoot

7.6 DC power output

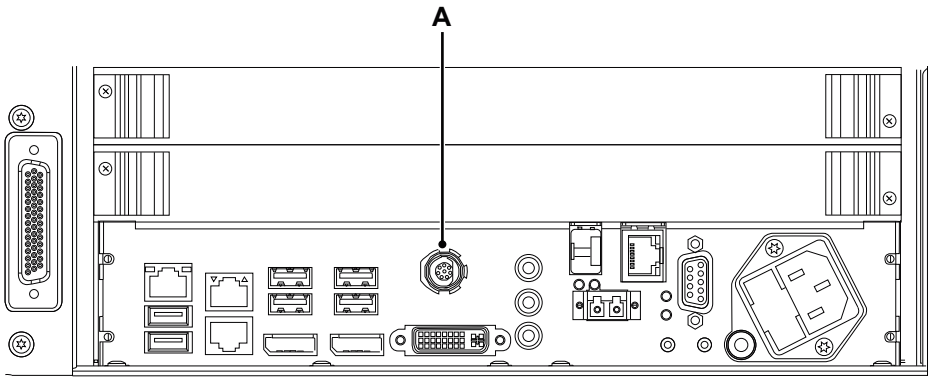


Figure 7.14: DC power output

A DC power output

The system has a DC power output connector to power additional systems requiring a DC input power.

The connection is set up to connect a QuantumX system to the GEN series mainframe directly. It uses a QuantumX compatible connector.

WARNING

QuantumX can connect multiple systems together and attach them all to one power supply. As the power of the GEN series mainframe is limited, make sure not to exceed the maximum power output of this connector.

For more information on using the QuantumX together with GEN series mainframes, please refer to chapter "Synchronizing GEN series and QuantumX using PTP" on page 827.

DC Power Output	
Connector type	ODU, G81L0C-P08LFG0-0000
Mating connector type	ODU, SX1LOC−P08MFG0−0000
Connector pinning	QuantumX compatible; only GND and PWR signals connected
Output Power	15 Watt
Output Voltage	> 11 V; Typically 11.5 V to 12 V
Maximum Output Current	1.4 A; Limited current and short circuit protected

DC Power Output

PIN	Signal
PIN 1	Reserved/not connected
PIN 2	Reserved/not connected
PIN 3	GND
PIN 4	Reserved/not connected
PIN 5	Reserved/not connected
PIN 6	Reserved/not connected
PIN 7	PWR
PIN 8	Reserved/not connected

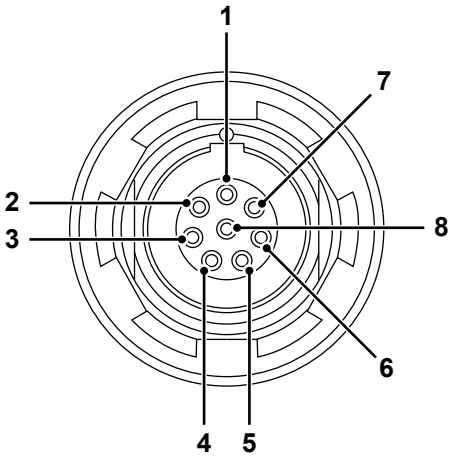


Figure 7.15: Connector power output

7.7 Digital Event/Timer/Counter

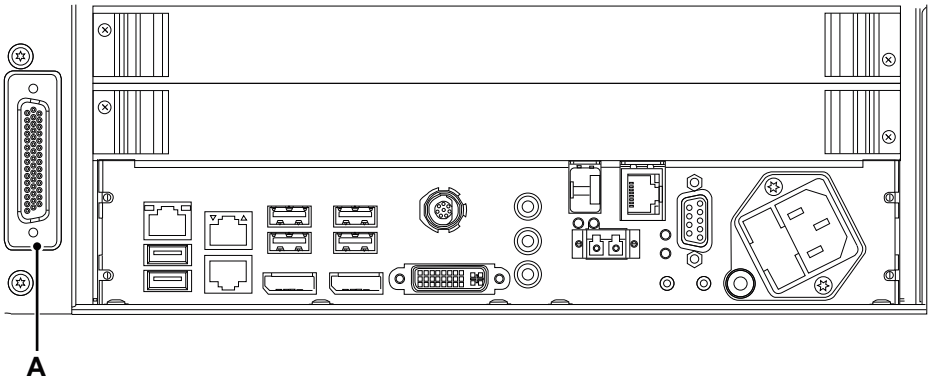


Figure 7.16: Digital Event/Timer/Counter

A Digital Event/Timer/Counter

The current generation GEN series mainframes come with a Digital Event/ Timer/Counter connector. The connector is internally connected to Slots A and B of the mainframe. The acquisition card installed in Slot A and B can use the inputs of the Digital Event/Timer/Counter connector.

WARNING

Not all GEN series acquisition cards have support for the Digital Event/ Timer/Counter connector. Only the acquisition cards that have support listed in their specification sheet will be able to use this connector. (See appendix "B3762-6.0 en (GEN3i Portable Data Recorder)" on page 378 for more details).

Digital Event/Timer/Counter	

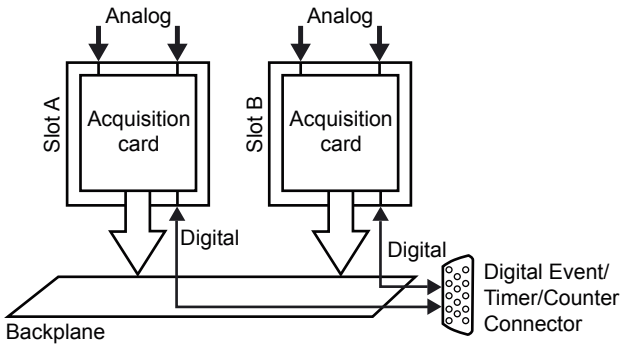
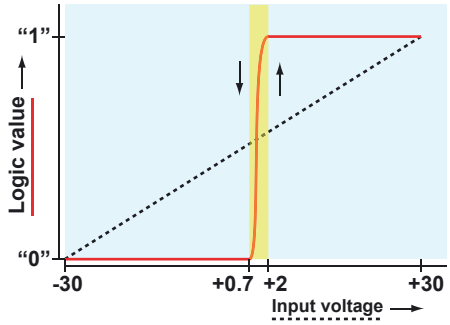
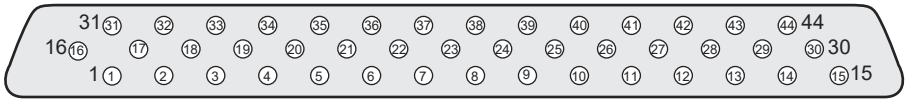


Figure 7.17: Digital Event/Timer/Counter block diagram

Supported cards	See specifications of acquisition cards
Number of connectors	1
Connector type	44 pin, female D-type connector, AMP HD-22 series (Tyco/TE connectivity: 5748482-5)
Mating cable connector type	44 pin, male D-type connector, HDP-22 series (Tyco/TE connectivity: 1658680-1)
Output power	
Voltage	5 ± 0.5 V DC
Maximum current	0.5 A

Digital Event/Timer/Counter	
Event Inputs	
Number of event inputs	16 per card, 2 cards per connector
Levels	TTL Compatible, Low -30 V to 0.7 V, High 2 V to 30 V
	 **Figure 7.18:** Logic threshold voltage levels
Overvoltage protection	± 30 V DC
Timer/Counter	
Number of channels	Two per card, two cards per connector
Functions	See specifications of the acquisition cards that support these inputs
Outputs	
Number of outputs	Two per card, two cards per connector
Functions	See specifications of acquisition cards that support these outputs
Output levels	TTL compatible; 0 V < Low < 0.6V; 2 V < High < 5 V
Output resistance	49.9 Ω ± 1%
Maximum output current	50 mA, short circuit protected

Digital Event/Timer/Counter Connector Pin Assignment



PIN 1 - Event Input 1A & Reset Timer/Counter 2A
PIN 2 - Event Input 2A & Direction Timer/Counter 2A
PIN 3 - Event Input 3A & Clock Timer/Counter 2A
PIN 4 - Event Input 4A
PIN 5 - Event Input 5A
PIN 6 - Event Input 6A
PIN 7 - Event Input 7A
PIN 8 - Event Input 8A
PIN 9 - Event Input 9A
PIN 10 - Event Input 10A & Reset Timer/Counter 1A
PIN 11 - Event Input 11A & Direction Timer/Counter 1A
PIN 12 - Event Input 12A & Clock Timer/Counter 1A
PIN 13 - Event Input 1B & Reset Timer/Counter 2B
PIN 14 - Event Input 2B & Direction Timer/Counter 2B
PIN 15 - Event Input 3B & Clock Timer/Counter 2B
PIN 16 - Event Input 4B
PIN 17 - Event Input 5B
PIN 18 - Event Input 6B
PIN 19 - Event Input 7B
PIN 20 - Event Input 8B
PIN 21 - Event Input 9B
PIN 22 - Event Input 10B & Reset Timer/Counter 1B
PIN 23 - Event Input 11B & Direction Timer/Counter 1B
PIN 24 - Event Input 12B & Clock Timer/Counter 1B
PIN 25 - Event Input 13B
PIN 26 - Event Input 14B
PIN 27 - Ground
PIN 28 - Ground
PIN 29 - Ground
PIN 30 - Ground
PIN 31 - Event Input 15B
PIN 32 - Event Input 16B
PIN 33 - Event Input 13A
PIN 34 - Event Input 14A
PIN 35 - Event Input 15A
PIN 36 - Event Input 16A
PIN 37 - Event Output 2B
PIN 38 - Event Output 1B
PIN 39 - Event Output 2A
PIN 40 - Event Output 1A
PIN 41 - Ground
PIN 42 - Ground
PIN 43 - +5 V Power
PIN 44 - +5 V Power

Figure 7.19: Pin diagram for Digital Event/Timer/Counter connector

7.7.1 Isolated event adapter

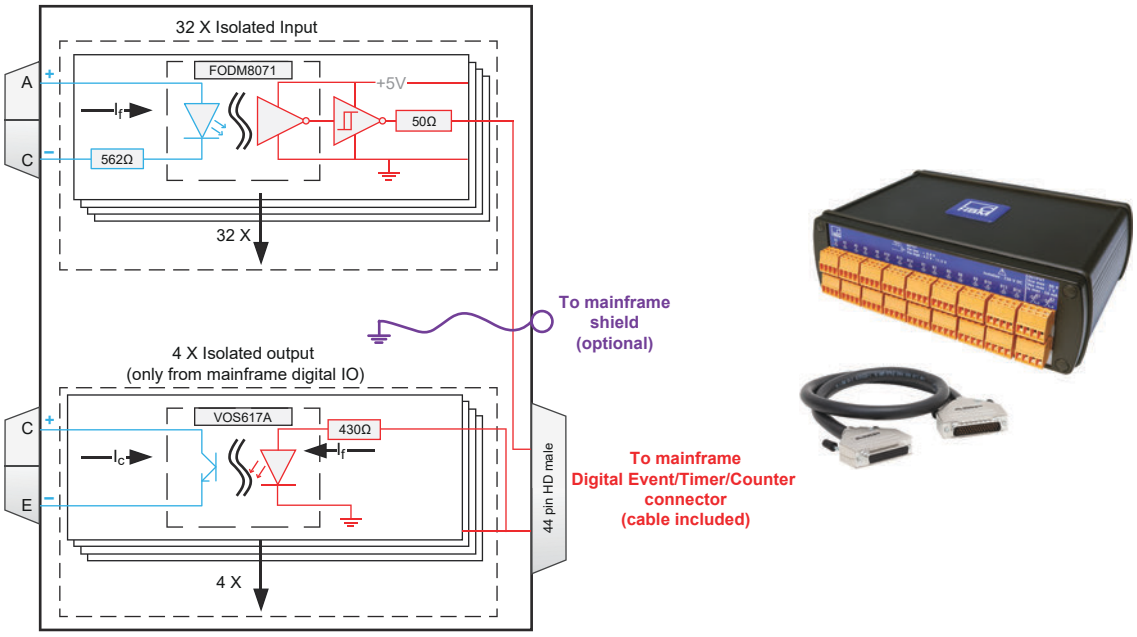


Figure 7.20: Block diagram and image

To isolate the Digital Event/Timer/Counter inputs a special adapter is available. It has a maximum 230 V RMS isolation spec and comes with a connection cable to directly connect the adapter to the mainframe.

The adapter isolates all input and output events and Timer/Counter pins.

See appendix "Mainframe adapters" on page 667 for detailed usages and specification of this adapter.

7.7.2 Torque/RPM adapter

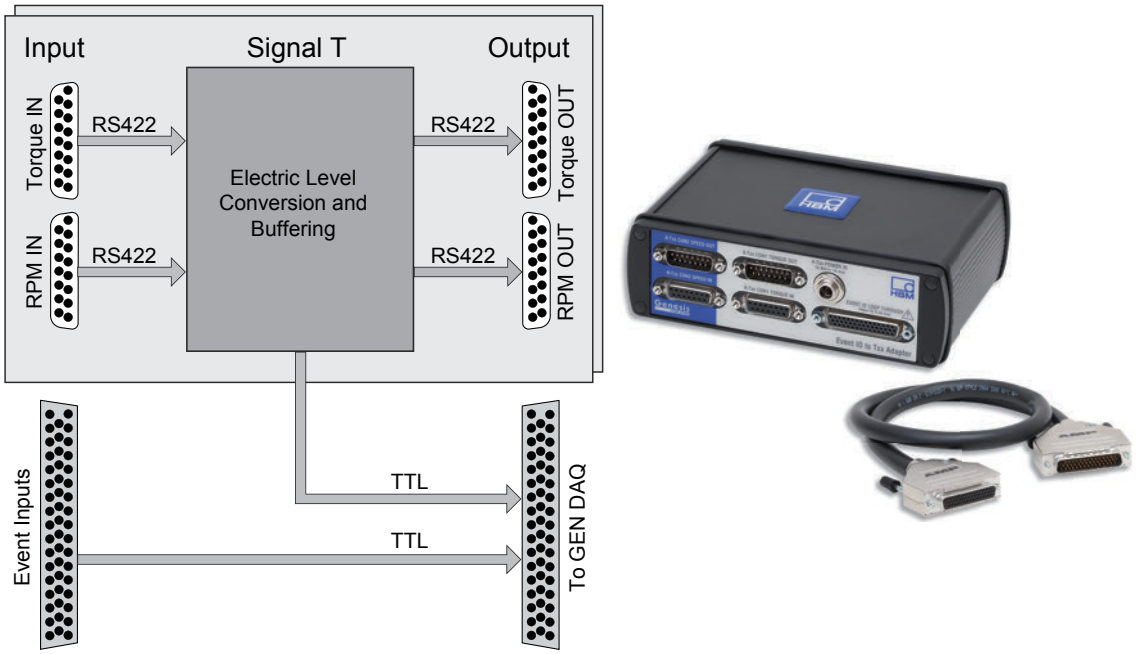


Figure 7.21: Block diagram and image

HBM's Torque and RPM sensors come standard with RS422 digital output signals. As the GEN series Digital Event/Timer/Counter inputs are TTL inputs, signal need to be converted to make both side able to work together.

The Torque/RPM adapter is designed to both perform the signal conversion as well as make sure the connectors used support standard Torque and RPM cables.

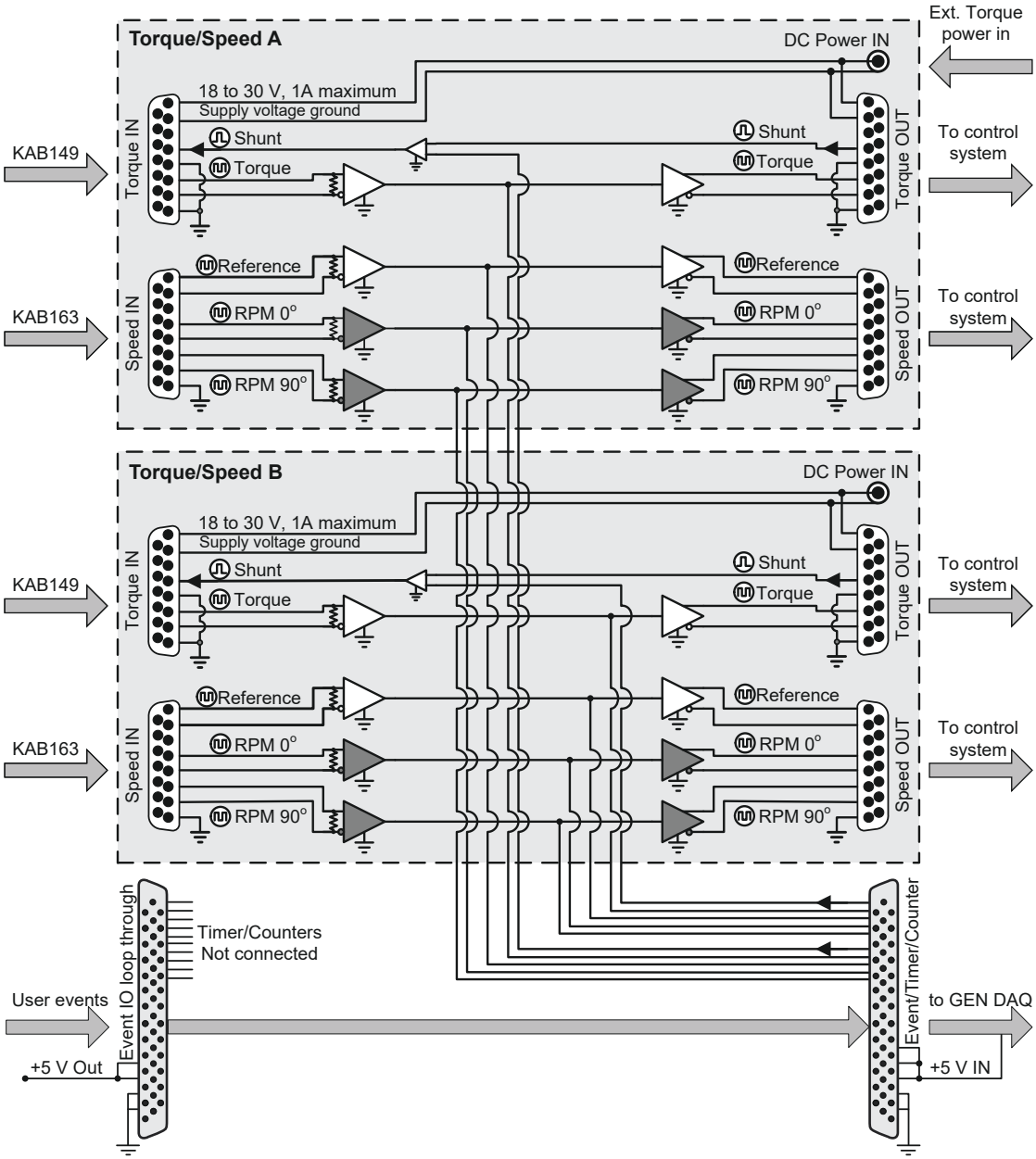


Figure 7.22: Block Diagram Torque/RPM Adapter

Using this adapter T12, T40 and alike torque transducer can be directly connected to the GEN series mainframe without additional need to build your own cables.

The adapter also supports a so called T-function. If the need exists to connect the output of the Torque/RPM sensor both to a GEN series mainframe and any other receiving system, the T-function output renews the original signal with an RS422 transmit buffer. This setup garantees a point to point connection required for proper RS422 usage.

8 Getting Started

8.1 Front panel control

Standby
On GEN3i, the standby button is located on the front panel. When this button is pressed, the instrument state toggles between operating and standby mode. In standby mode, some power is consumed and the instrument is NOT disconnected from the AC supply. To switch off the instrument completely from the mains power disconnect the mains power cable from the instrument.

Figure 8.1: Power button

A Disk active LED - is illuminated when disk is busy.

B Power LED - is illuminated when power is on.

C Standby button - Press to power on or off, or hold for more than four seconds for a forced power off.

When you use this standby button to power off GEN3i, the software displays a confirmation dialog. Follow the on-screen instructions to power off the system correctly. If the system does not respond, press the standby button for at least four seconds until the unit is forced to power off.

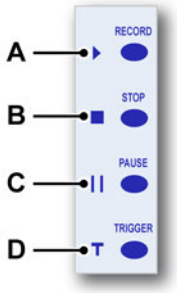


Figure 8.2: Acquistion control - Detail

A Record

B Stop

C Pause

D Trigger

USB ports

Two USB 2.0 ports are located on the front and in the bottom left-hand corner of the unit for easy access. The remaining USB ports are located on the back of the unit.

Figure 8.3: USB 2.0 ports (located on the front of the unit)

A USB 2.0 ports

B Wireless adapter

Wireless adapter

For information on the Wireless adapter, please refer to "Wireless network" on page 123.

8.2 Getting started

When GEN3i is started up for the first time, the software starts and connects to the integrated GEN3i data acquisition unit automatically. The Instrument Panel starts in continuous mode and the acquisition unit starts in preview mode, meaning that incoming signals are monitored, but no data is stored.

If you do not change anything, this is the default behavior each time you start the system.

Each time you power off the system, the changes made to the preferences and settings are saved automatically. These settings are then loaded the next time you power on GEN3i.

8.3 Wireless network

Your GEN3i includes an internal wireless network adapter. With this Wi-Fi network adapter, you have the freedom to connect to your local Wi-Fi network.

HINT/TIP

In some areas or application uses, the presence of a wireless network option in the instrument is not allowed. Disabling the wireless network within Windows® is not a satisfactory solution. Therefore, HBM supports removing or electronically disabling the wireless network. This disables the use of wireless network permanently.
To remove or electronically disable the Wi-Fi, contact HBM before ordering and contact HBM service after delivery.

The adapter features full compliance with the IEEE 802.11 b/g/n wireless standard, offering the best compatibility and future-proof reliability. With data rates up to 300 Mbit/s, the adapter supports a comfortable wireless bandwidth.

Below is a quick start procedure to connect GEN3i to your local network and a quick start procedure to disconnect GEN3i from a network.

For wireless details on network operation, please refer to the Windows® Help system. If you are uncomfortable or not yet familiar with these procedures, please contact your IT department or a network knowledgeable person to assist you.

IMPORTANT

Please note that there are differences of the wireless network connection between Windows® 7 and Windows® 10. For information of installation with Windows® 10, please refer to chapter "Windows 10: To connect GEN3i/GEN3iA to the local wireless network:" on page 126.

8.3.1 Windows® 7: To connect GEN3i/GEN3iA to the local wireless network:

1. Start GEN3i/GEN3iA.
2. When GEN3i/GEN3iA is fully booted, quit Perception.
3. In Windows® 7, access the **Connect to a network** dialog using one of the following options:
   - By clicking **Start** and then clicking **Connect to** from the Windows 7 desktop.
   - From the **Manage wireless connections** dialog.
   - From the **Connect/Disconnect** context menu, select the wireless network adapter option in the Network Connections folder.
4. In the **Connect to a network** dialog, use Show to select:
   - **All** wireless, dial-up and VPN connections.
   - Wireless Only wireless connections.
5. The most common situations that you can encounter when connecting to a wireless network are listed below:
   - **The network is listed:** To connect to a network that is listed in the **Connect to a network** dialog, double-click the network name or click the network name and then click **Connect**. If the connection attempt is not successful, use Windows® Network Diagnostics to diagnose the problem and suggest a solution.
   - **The network is not listed:** If the wireless network you want to connect to is not listed, click **Set up a connection or network.** Windows 7 displays the **Choose a connection option** page where you typically select the **Manually connect to a wireless network** option. At this point, you will need to have sufficient knowledge of your network settings. If you do not have sufficient knowledge, contact your IT department or a network knowledgeable person to assist you.

8.3.2 Windows® 7: To disconnect GEN3i/GEN3iA from the local wireless network:

At start-up, Windows® 7 automatically connects to the wireless network that you have selected.

To prevent this, you have two options:

- Remove the network connection
- Make the network connection a manual procedure (recommended when you do not want to connect GEN3i/GEN3iA to the network automatically).

For both options:

1 Click **Start**, click **Control Panel**, click **Network and Internet**, click **Network and Sharing Center** and select the task **Manage Wireless Networks.**

2 To change a setting, right-click the network's icon. On the context menu that comes up:
   - Select **Remove Network** to remove the network connection, or
   - Select **Properties.** In the properties dialog that appears, make sure that **Connect automatically when this network is in range** is cleared.

When the manual connection has been selected, you can still connect to the network, but you will need to do so manually. To connect to the network, right-click the Windows® 7 networking icon in the task bar and select **Connect to a Network.**

8.3.3 Windows® 10: To connect GEN3i/GEN3iA to the local wireless network:

1 Start GEN3i/GEN3iA.

2 When GEN3i/GEN3iA is fully booted, quit Perception.

3 In Windows® 10, access the **Network & Internet** dialog using one of the following options:

- By clicking **Start ► Settings ► Network & Internet** (see Figure 8.4 on page 126).

  Or

- By clicking the **Network** icon in the task bar (see Figure 8.6 on page 128).

3A Select the **Network & Internet** icon in the Settings panel.

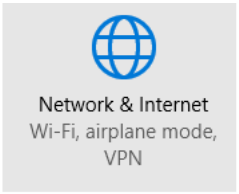


Figure 8.4: Network & Internet icon in Windows® 10 Settings panel

3B Select the **Wi-Fi** option from the **NETWORK & INTERNET** window.

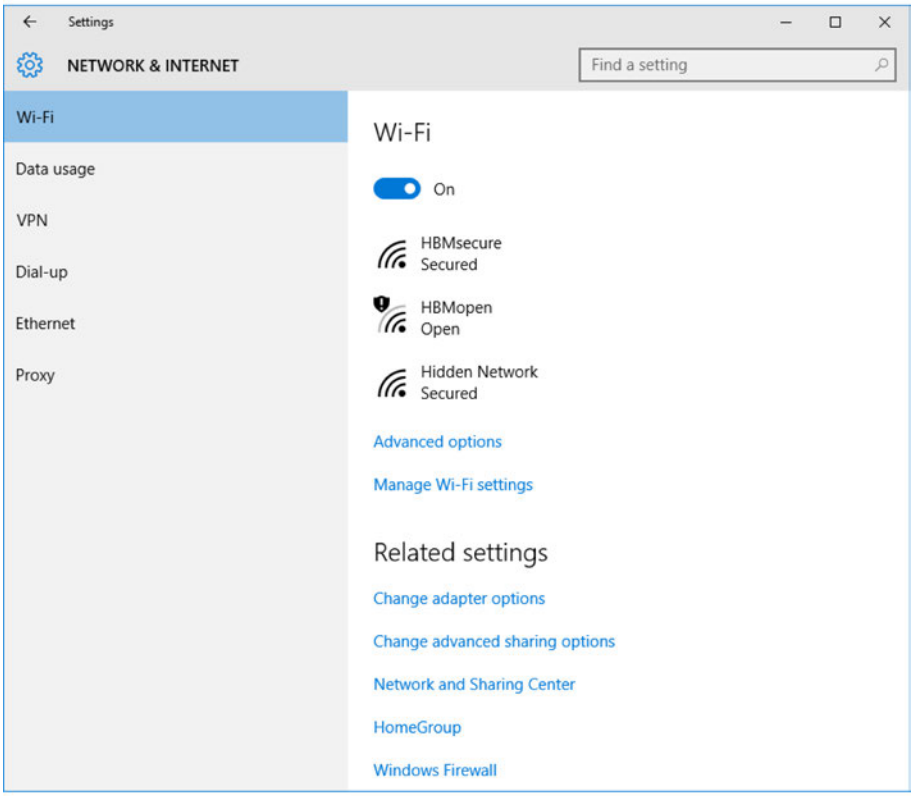


Figure 8.5: Network and Internet options

3A Click the **Network** icon in the task bar and select **Network settings** to open the advanced settings (see Figure 8.7)

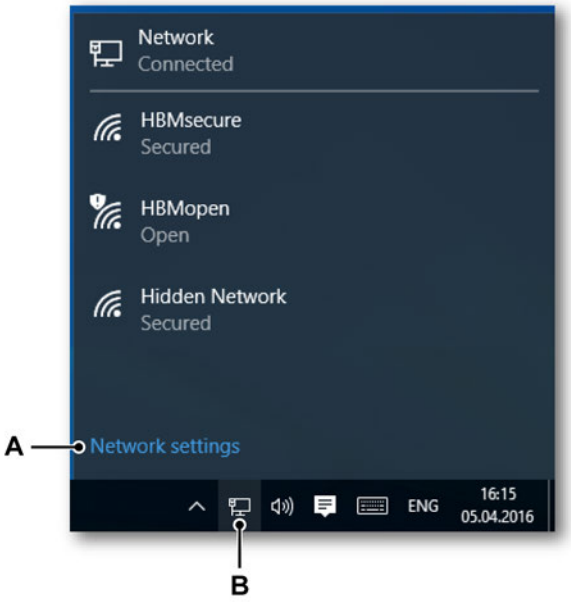


Figure 8.6: Network icon with context menu

A Network settings

B Network icon

3B Select **Wi-Fi** option from **NETWORK & INTERNET** window.
A password is required when connecting to a secured Wi-Fi network. At this point, you need to have sufficient knowledge of your network settings. If you do not have sufficient knowledge, contact your IT department or a network knowledgeable person to assist you.
If the name **(SSID)** of the network is not broadcasted, a **Hidden Network** is listed. When connecting to the hidden network, the name has to be entered.

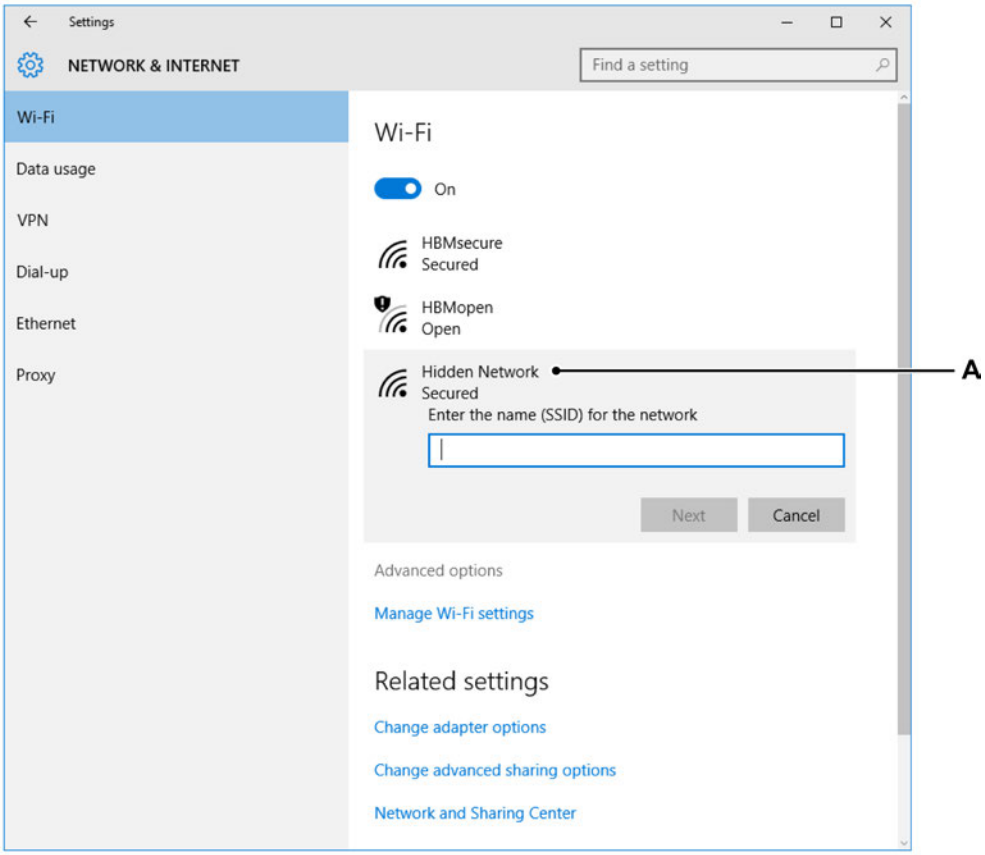


Figure 8.7: Network and internet window (advanced settings)

A Hidden Network area

8.3.4 Windows® 10: To disconnect GEN3i/GEN3iA from the local wireless network:

At start-up, Windows® 10 automatically connects to the wireless network that you have selected.

To prevent this, you have two options:

- Remove the network connection
- Make the network connection a manual procedure (recommended when you do not want to connect GEN3i/GEN3iA to the network automatically).

To remove a network:

1 Click **Start**, click **Settings**, click **Network & Internet**, click **Wi-Fi** and select the option **Manage Wi-Fi Settings**.

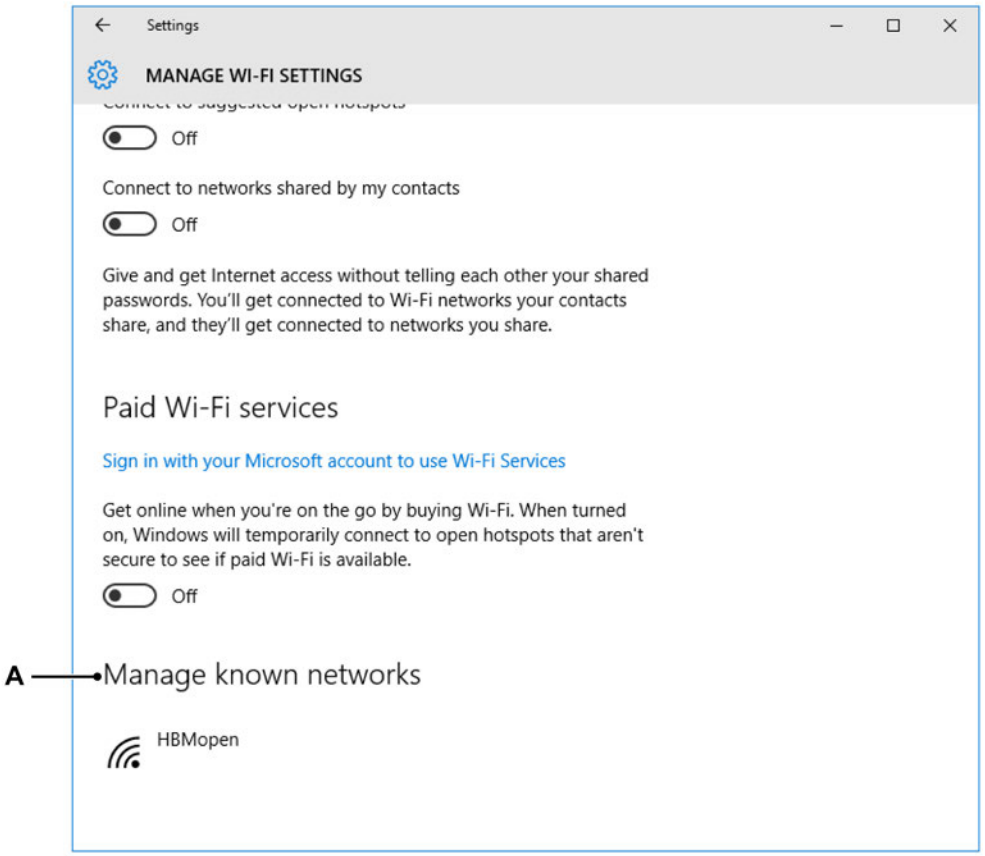


Figure 8.8: Manage WI-FI Settings window

A Manage known networks option

2 In **Manage known networks** option select the network which should be removed. Click **Forget** to remove the network.

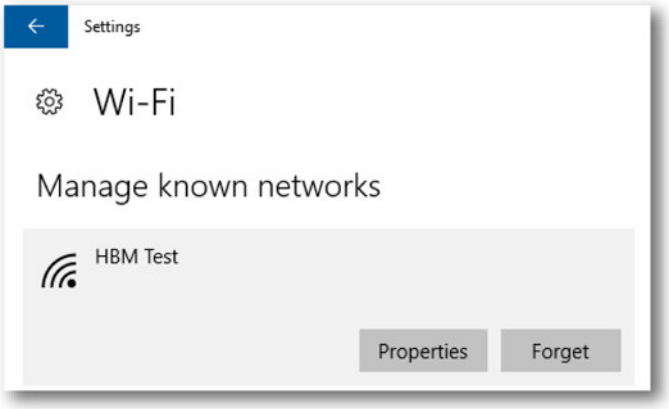


Figure 8.9: Remove network

Make the network connection a manual procedure

1 To change a setting:

- Click **Start**, click **Settings**, click **Network & Internet**, click **Wi-Fi** and select the **Change adapter options** or
- In the **Network Connections**, right-click the **Wi-Fi network** icon. On the context menu that comes up: Select **Status**, select **Wireless Properties**. In the dialog that appears, make sure that **Connect automatically when this network is in range** is cleared.

When the manual connection has been selected, you can still connect to the network, but you will need to do so manually. To connect to the network, click the Windows® 10 networking icon in the task bar, select the **Wi-Fi network** and click **Connect**.

9 Acquisition and Storage

9.1 Introduction

Data acquisition hardware within the GEN3i is based on the concept of a **recorder**. A recorder consists of a number of acquisition **channels** that share the same basic recording parameters: sample rate, sweep length and pre- and post-trigger length. Usually, a single recorder is physically identical to a single acquisition card. Multiple recorders can be placed in a single **mainframe**. The mainframe is the housing for the recorders. The mainframe provides the power and includes the interface for the local area network. A mainframe has its own network address (IP address).

For the sake of simplicity, we will consider a single channel in this section.

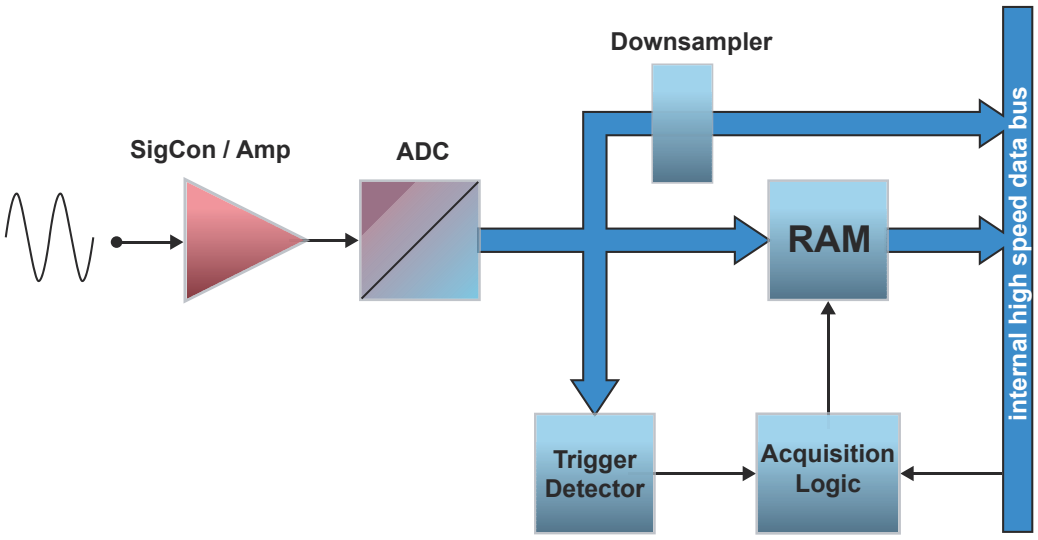


Figure 9.1: Simplified generic single channel data acquisition system

In the GEN3i data acquisition system and the Perception software that goes with it, a separation is made between acquisition and storage. **Acquisition** is the act of digitizing analog data and making it available for monitoring or storage. **Storage** is the actual archiving of digitized data. **Recording** (verb) is acquisition + storage.

9.2 Recording

Since many of the features that are described here are controlled from within the Perception software, it is advised to read this section in combination with the corresponding sections in the Perception manual.

The GEN3i/Perception combination provides the following acquisition controls:

- **RUN** The run command starts recording of data. Now the recorder(s) record(s) data until a stop command is issued. This stop command can be manually or triggered (when in sweep storage mode).
- **STOP** To stop or abort a recording.
- **PAUSE** This mode has two options:
  1. When no recording is active, it places the recorder in the pause or stand-by mode. Although the recorder is digitizing, no data is stored in memory or disk. This is useful for monitoring purposes.
  2. When a recording is active, it places the recorder in a hold mode. Although the recorder is digitizing, no data is stored in memory or disk. At the point when RUN is selected, the current recording continues. When STOP is selected, the recording is finished.

These recording controls are combined with the various storage modes.

9.3 Storage

The GEN3i provides two storage paths, as shown in Figure 9.1 on page 132:

- Store data in on-board RAM at high speed
- Transfer data directly at reduced speed to the controlling PC or (when installed) to a local disk.

In addition to these storage paths, the GEN3i provides two fundamental storage modes:

- **Sweeps:** data storage of predefined length. Sweeps typically use a trigger to define the start and end of the sweep.
- **Continuous:** data storage of an undefined length. The end of this storage mode can be defined by various events, as described later.

When data is stored, this data is organized in recordings. A recording is defined as all the data that has been stored between the start of acquisition (Record command) and the end of acquisition. The end can be defined in various ways. A recording can have one or multiple sweeps, a continuous data stream or a combination of both.

In Perception, a recording is organized as a PNRF file (Perception Native Recording File).

CAUTION

The GEN3i RAM is volatile. Wait until all data is transferred to the recording file before closing Perception or switching off the instrument.

The storage mode defines how data is digitized and saved. The continuous storage mode stores all data. The sweep storage mode stores only the sweeps. However, the resulting file - or recording - will be different for the various storage modes.

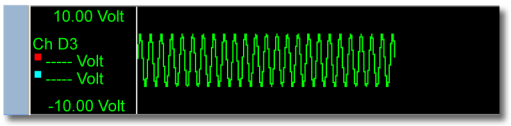


Figure 9.2: Run - Storage: Continuous

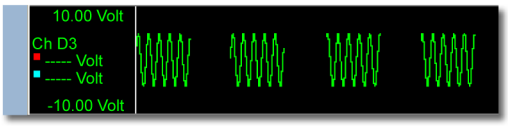


Figure 9.3: Run - Storage: Sweeps only

The basic storage modes can be combined to create more advanced storage modes:

Dual In this mode, sweeps and continuous data are stored. Therefore, the end result is a recording that comprises the higher speed sweeps as well as the lower speed continuous data between the sweeps.

Slow-Fast Sweep In this mode, sweep data with different sample rates are stored. The difference from the dual mode is the fact that the slower data stream is now actually a slower speed sweep, i.e. it has a predefined length and requires a trigger. The trigger position is the same as the trigger of the first high-speed sweep.

9.3.1 More on sweeps

Figure 9.1 "Simplified generic single channel data acquisition system" on page 132 is a very simplified block diagram of the general concept of a single channel digitizer. Once the analog values have been converted by the ADC into binary codes, they are stored in successive order in a buffer memory, the on-board RAM. This memory can be divided into multiple segments to allow for the storage of multiple sweeps.

If the last storage location of a segment is filled and acquisition is still taking place, the first storage location is overwritten with a new sample, followed by the second storage location, etc.

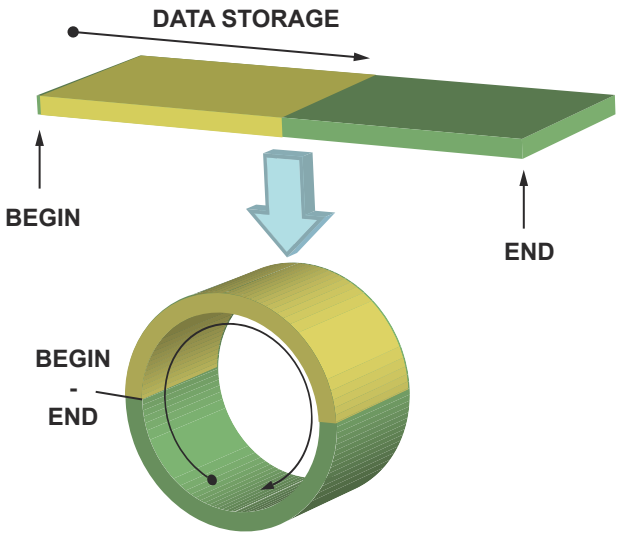


Figure 9.4: Ring buffer operation of memory

The physical memory therefore forms a ring buffer, into which information can be continuously added (see Figure 9.4). This process of filling the ring buffer memory terminates only when the recording logic indicates that the sweep must be ended. Once the sweep recording has stopped, the content of the buffer memory becomes available to the control PC for processing. This is also called **circular recording**. Sweep data is automatically moved from on-board RAM memory to the recording file.

9.3.2 Pre-trigger sweeps

As we have seen, data emerging from the ADC is stored in the buffer memory. When recording, the memory is continuously refreshed with new sample values, until storage is halted. The information available in the memory is a **history** of the recorded signal up to the moment of “end-of-sweep”. The extent of this history depends on the sample rate and the data storage capacity (length) of the memory. If we assume a memory length of 40 000 samples and a sample rate of 10 000 samples per second, then the time window of the history will be:

(EQ 1)

$$t_{window} = \frac{40000}{10000} = 4 \text{ seconds}$$

Storage into the ring buffer can be stopped only by a “stop” signal from the recorder. This signal is called the "trigger". For more information on triggering, please refer to chapter “Digital Trigger Modes” on page 144.

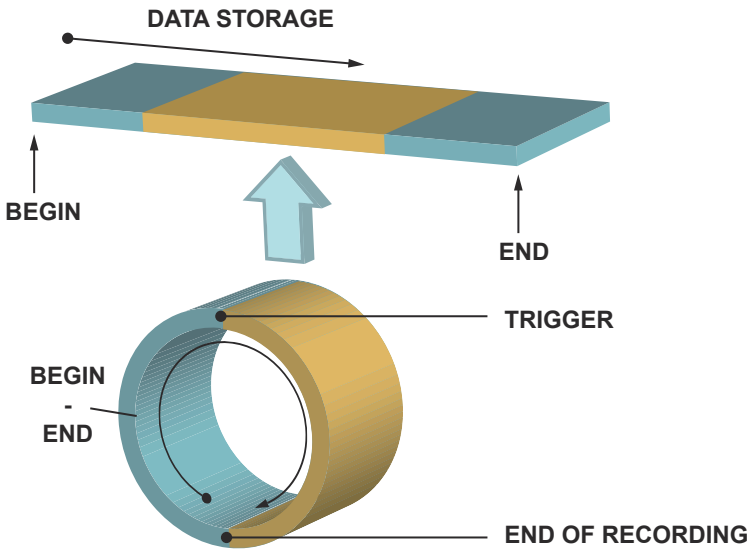


Figure 9.5: Ring buffer with trigger and end-of-recording

Since the trigger stops the storage, all stored information is termed pre-trigger information. When storage stops because the acquired signal has met a trigger condition, only pre-trigger information is available - information recorded before the signal met the trigger condition.

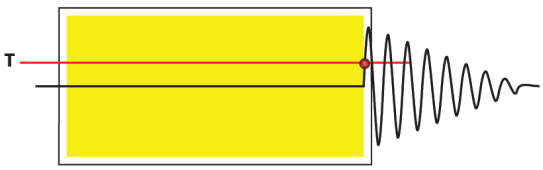


Figure 9.6: Full pre-trigger storage: pre-trigger = 100%

More often, one is interested in what happened just before and after the condition was met. To achieve this aim, a delay is introduced. Once the trigger condition is met, storage is stopped - not immediately, but only after a programmable delay counter has counted out. The memory now contains pre-trigger information and post-trigger information.

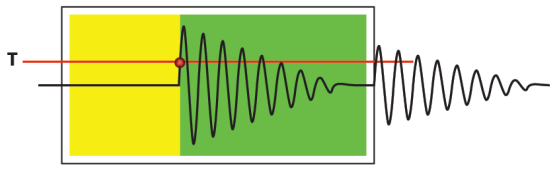


Figure 9.7: Pre-trigger / post-trigger storage: 0% < pre-trigger < 100%

The usage of a variable delay counter allows for a user-definable pre-trigger length. The length of the pre-trigger segment equals the length of the memory segment minus the delay. When the length of the delay is equal to, or exceeds, the length of the memory segment, only post-trigger information is available.

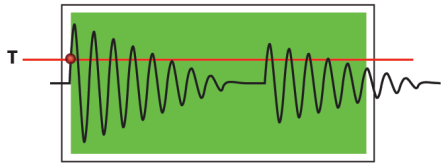


Figure 9.8: Full post-trigger storage: pre-trigger = 0%

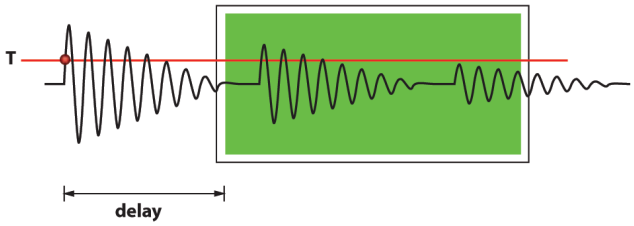


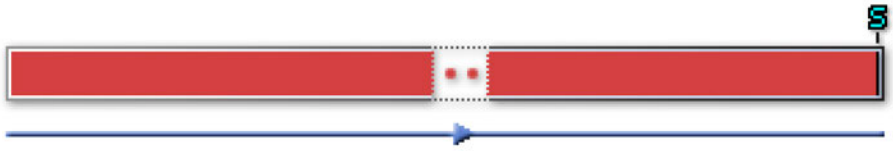
Figure 9.9: Delayed trigger storage: pre-trigger < 0%

9.3.3 More on continuous data storage

The most important difference between continuous data storage and sweeps in a GEN3i is the fact that sweeps are stored in on-board volatile RAM, while continuous storage takes place on the controlling PC's hard disk (or local hard disk when installed).

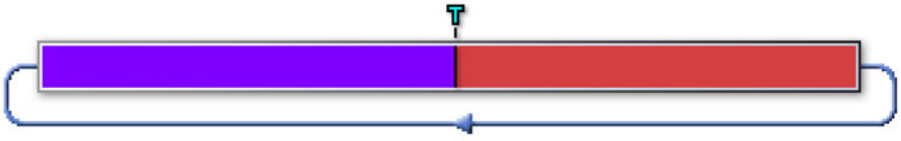
The continuous data storage provides three modes:

- **Standard** The continuous mode is standard when storage is started and is stopped manually as depicted below:



- **Circular** The continuous mode is circular when storage is started and stopped manually AND the length of the buffer is defined. Operation is similar to standard sweep storage, but storage is on the PC hard disk and not in volatile memory. In this mode, the **lead-out** is specified which is basically the same as the post-trigger segment in a sweep recording.

- **Stop on trigger** The continuous mode operates like a pre-trigger sweep, but with storage on the PC hard disk, not in volatile memory.



9.4 Time base

The power of modern data acquisition techniques is achieved by *digitizing* analog information. Digitizing is the conversion of the instantaneous value of an analog signal (static or dynamic) into a numeric value. When the signal varies, *sampling* the instantaneous amplitude at sufficiently rapid intervals converts this signal into a series of numbers that can represent the original analog signal.

9.4.1 Real-time sampling and time base

Real-time sampling is a straightforward sampling method and is the only method to record non-periodical phenomena. In this method, the intervals between the samples taken of the original signal are as short as possible and equidistant. If the sample rate used is high enough, the original signal can be reconstructed without any additional processing.

The sample rate is determined by the time base: the time base is a clock that generates pulses used to drive the A-to-D Convertor. Within the GEN series, the following time base options are available:

- **Internal time base** The clock used to drive the ADC's is the built-in clock.
- **External time base** The clock used to drive the ADC's is the clock signal presented at the external clock input on the GEN series system. The interval between two consecutive samples may not be equidistant. This all depends on the accuracy of the supplied clock signal.

When internal time base is selected, there are two related options:

- **Internal Clock Base Decimal** This setting is used to create time base values that are base 10, e.g. 1 MHz, 100 kHz, 50 kHz, 2.5 Hz, etc. These values are derived from a main oscillator that operates at a base 10 frequency, e.g. 1 MHz.
- **Internal Clock Base Binary** This setting is used to create time base values that are base 2, e.g. 1.024 MHz, 512 kHz, 64 Hz, etc. These values are derived from a main oscillator that operates at a base 2 frequency, e.g. 1.024 MHz.

The selections above can be found in the Perception software in the Settings Sheet ▸ Memory&Timebase ▸ Mainframe ▸ Clock Base and are therefore mainframe-wide, i.e. the same for all recorders.

A binary clock base is a useful time base settings when doing FFTs (frequency domain analysis).

9.4.2 Time base settings for FFTs

When doing FFTs, there are two topics that affect the acquisition:

1. It makes life easier when the final FFT yields spectral lines with a distance ∆ **f** that is a "nice" value. Otherwise stated: the FFT bin size should preferably be a nice value. Sometimes, this is also called the "frequency resolution". The bin size is determined by the actual frame size or frame length: **bin size = 1 / T** in which T is the total frame size time. E.g. a one-second frame size will result in a 1 Hz bin size, a 0.5 second frame size results in a 2 Hz bin size.
2. The frame size in samples should be equal to a power of two. Fundamentally, most FFT algorithms work on data sets with a length of 2^N.

The binary clock base of the internal time base in combination with the division factors allow for a broad range of values that meet both requirements. In the table below (see "Examples of FFT bin sizes" on page 142), various sample rates are given, as well as the corresponding division factor (divisor). The table shows the bin sizes that result from these sample rates in combination with various sweep lengths.

Example: from the table (see "Examples of FFT bin sizes" on page 142) you can read that a sample rate of 40.960 kHz and a frame length of 8192 samples result in a 5 Hz bin size, i.e. the spectral lines are 5 Hz from each other.

"Nice" values are considered to be "minor" values that easily fit in "major" values for (grid) display purposes.

In the table below, the values are in the colored cells and basically comprise the range 1.25, 2.5, 5, 10, 20.

Table 9.1: Examples of FFT bin sizes

TIME BASE MAIN = 1.024 MHZ		FFT SIZE (FRAME LENGTHS)					
		256	512	1024	2048	4096	8192
SMP/S	DIVI-SOR	FFT BIN SIZE IN HZ					
1024000	1	4000	2000	1000	500	250	125
512000	2	2000	1000	500	250	125	62.5
256000	4	1000	500	250	125	62.5	31.25
204800	5	800	400	200	100	50	25
128000	8	500	250	125	62.5	31.25	15.625
102400	10	400	200	100	50	25	12.5
51200	20	200	100	50	25	12.5	6.25
40960	25	160	80	40	20	10	5
25600	40	100	50	25	12.5	6.25	3.125
20480	50	80	40	20	10	5	2.5
12800	80	50	25	12.5	6.25	3.125	1.5625
1024	100	40	20	10	5	2.5	1.25
5120	200	20	10	5	2.5	1.25	0.625
4096	250	16	8	4	2	1	0.5
2560	400	10	5	2.5	1.25	0.625	0.3125
2048	500	8	4	2	1	0.5	0.25
1280	800	5	2.5	1.25	0.625	0.3125	0.0156
1024	1000	4	2	1	0.5	0.25	0.125

Additional information

The Nyquist frequency (f/2) is the maximum frequency that can be accurately measured by a digitizer sampling at a rate of (f). Otherwise stated: a digitizer sampling at a rate of (f) cannot measure an input signal with frequency components exceeding f/2 without experiencing "aliasing" inaccuracies.

Nyquist's theorem determines the range of frequencies that can be measured. They range from DC to one half the sampling rate at which the data was captured. An FFT of a sweep of N points produces N/2 frequency domain data points within the range of frequencies between DC and the Nyquist frequency. So the frequency resolution is:

(EQ 2)

$$\Delta \mathrm{f} = \frac{samplerate \ / \ 2}{N \ / \ 2}$$

For example, assuming that a frame has 8192 points (N=8192) and a sample rate has 40.96 kHz. This will yield the following:

- Frequency resolution Δf = (½ * 40960) / (½ * 8192) = 5 Hz
- Number of frequency domain points: N/2 = 4096
- The minimum frequency component that can be measured is equal to the frequency resolution Δf = 5 Hz
- The maximum frequency component that can be measured is 40.96 kHz / 2 = 20.48 kHz

The FFT X-scale (frequency) will start at 5 Hz, end at 20480 Hz, and has 4096 points.

10 Digital Trigger Modes

10.1 Introduction

Within the GEN3i data acquisition system, every channel is equipped with a **trigger detector**, which makes it possible to record just the phenomenon of interest, instead of having to search the full memory to find it. The trigger detector gives the system the power to capture elusive, short and unpredictable events. It determines how easily the event of interest can be extracted.

The word **trigger** has a dual meaning in recording techniques. In the active sense, the instrument has triggered, indicating that the instrument has responded to a certain stimulus. In the passive sense, as in trigger point, it indicates the point (in time) when the instrument has triggered. In both cases, trigger refers to a known, pre-defined situation.

The trigger can be generated in several ways:

- by the user, i.e. **manually**
- using an externally applied signal, i.e. **external** trigger
- when the acquired **signal** complies with a certain condition: the trigger condition. Each channel within a recorder can trigger this recorder.

For transient recording, this last option is of great importance. To a large extent, the trigger facilities determine the application capabilities of the data acquisition system, i.e. how effectively the data can be captured.

In this chapter, the trigger capabilities of the GEN3i data acquisition system will be explained in full detail.

Each channel within a recorder can trigger this recorder. This functionality is realized by combining all channel triggers into a logical OR combination. When one of the channels (or multiple channels) generates a trigger, the complete recorder triggers. Each channel's trigger detector can be switched off or set to one of the modes described in this chapter.

Note *This chapter describes all GEN series trigger options. However, not every acquisition card will support each described option. Check the specifications of each acquisition card to find out what options are supported for this specific card.*

10.2 Understanding digital triggering

Technically speaking, there are two approaches to determine the known, pre-defined situation of the signal: analog or digital.

Each channel in the GEN series system is equipped with a digital trigger detector. Digital triggering has the benefit of stable vertical reference levels, no horizontal jitter, and not depending on signal frequency.

A disadvantage of a digital trigger detector is its inability to detect events that occur between two consecutive samples. This does not usually interfere with normal operation because the event is not recorded anyway.

10.2.1 Digital trigger detector

Figure 10.1 shows a simplified diagram of a **single-level** digital trigger detector. Digitized values coming from the ADC are fed into an Arithmetic (and) Logic Unit – ALU. The value that comes out of the ALU is then referenced against a preset value (trigger level). The result can be either positive, i.e. the value is larger, or negative, i.e. the value is smaller. Based on this information, the level crossing detector verifies if a level crossing in the correct direction has occurred and, if so, sends out a trigger.

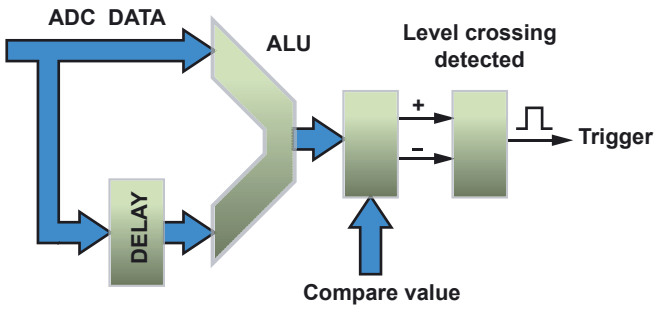


Figure 10.1: Single-level trigger detector

The delay register in front of the ALU is used to compare the ADC value with “older” values. This means that triggering does not react to specific levels, but to the differential signal or **slope**.

As explained later in this chapter, a signal must actually cross the preset level. This is to avoid erroneous triggering due to a small amount of noise on the signal. To make the trigger detector even more stable when noisy signals are used, the single-level trigger detector has been expanded with a **hysteresis**. After the level detector signals a level crossing, a new level crossing will only be signaled if the input signal first goes outside the hysteresis band and then returns to the trigger level.
For the advanced trigger modes, the single-level trigger detector with programmable hysteresis has been implemented twice to provide a **dual-level** trigger detector. Levels are usually referenced as *primary* trigger level and *secondary* trigger level.

10.2.2 Valid trigger conditions

Trigger detection is based on level crossing. A signal has to cross a specified level to be considered a trigger condition. As a consequence, reaching the required level is not a valid trigger condition. Since trigger detection is digital, inter-sample analog values are omitted.

In the following graphs, these conditions are shown.

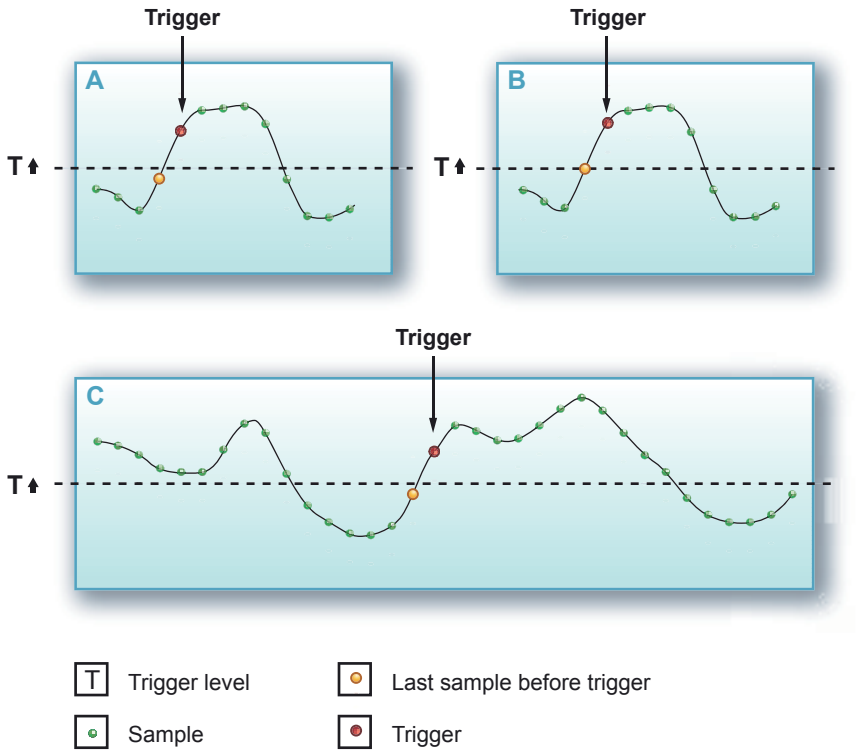


Figure 10.2: Level crossing detector

Figure 10.2 shows the basic trigger mode with a specified level (**T**) and a level crossing in a positive direction. In Figure 10.2 **(A)**, the trigger occurs on the first sample after the level crossing. Figure 10.2 **(B)** shows the situation in which a sample equals the set level. Trigger does not occur until a sample is actually above the required level.

Since the trigger detector requires a level crossing, no trigger occurs when a signal is above the set level when recording starts. This is depicted in Figure 10.2 **(C)**.

Figure 10.3 shows the influence of the additional hysteresis. Fundamentally, everything is the same as described earlier. The only difference now is that a second level (H) is used to “arm” the level trigger detector. Otherwise stated, the trigger level has been expanded to be a trigger zone that spans multiple levels.

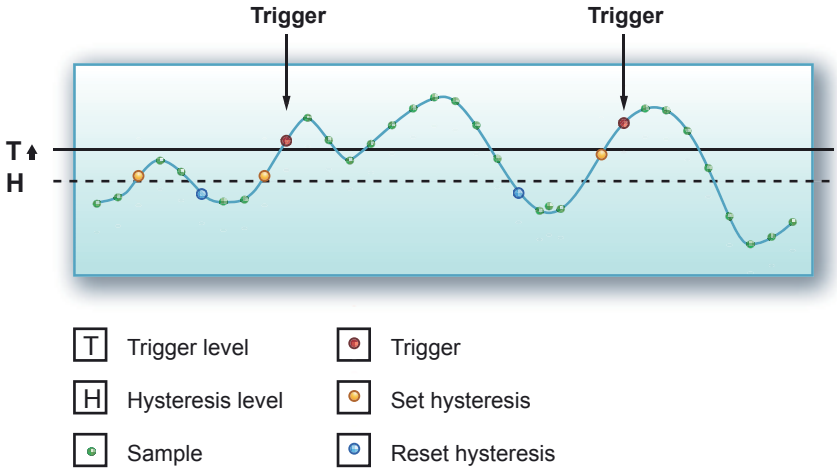


Figure 10.3: Trigger level hysteresis

10.3 Trigger modes

Using the various trigger modes, GEN3i data acquisition system is expanded to an extremely versatile transient recorder. The trigger circuits may be configured to trigger on many types of phenomena. In this section, the different trigger modes and their extensions are discussed in detail.

10.3.1 Basic trigger mode

The basic trigger mode can be compared to the trigger mode available when using an analog trigger detector, for example as found on a classic scope.

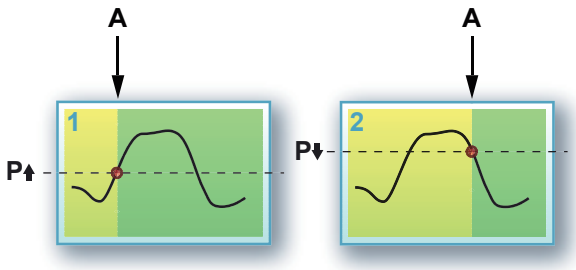


Figure 10.4: Basic trigger mode

A Trigger

In this mode, a single-level trigger detector is active, the primary level. As mentioned previously, the signal needs to actually cross the preset level. Both the level and direction of crossing can be selected.

Relevant settings for this mode:

- Mode: basic
- Primary level: any value within the input range
- Direction: positive or negative
- Hysteresis: any relevant value

10.3.2 Dual trigger mode

In dual trigger mode two detectors are active and working simultaneously: the primary level **P** and the secondary level **S**. With two levels, it is possible to define a range that the input signal must be within. As soon as the signal becomes larger than the upper level or smaller than the lower level, the detector generates a trigger. By inverting the slopes of both detectors, the trigger is generated when the signal returns into the specified range.

Figure 10.5 shows the various possibilities.

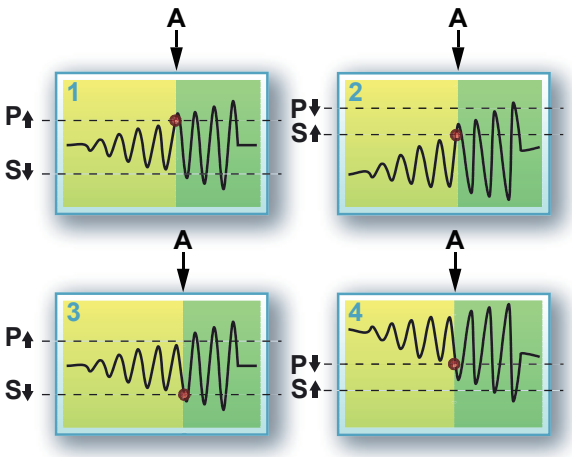


Figure 10.5: Dual trigger mode

A Trigger

Any value for each level and the slope of the primary level can be selected. The slope of the secondary level is automatically set to the opposite direction.

Diagrams **1** and **3** show a signal that exits the range. Diagrams **2** and **4** show signals that enter the range.

Relevant settings for this mode:

- Mode: dual
- Primary level: any value within the input range
- Secondary level: any value within the input range
- Direction: positive or negative for primary level; secondary level is automatically set to the opposite direction
- Hysteresis: any relevant value is used for both levels.

10.3.3 Trigger qualifier

The trigger detectors of a channel can also be used as qualifiers. A trigger qualifier is a situation that enables (arms) the recorder trigger features. The recorder trigger features are a combination of various channel, external, between-recorders and other trigger options.

There are two qualifier modes:

- Basic single-level qualifier. The level detector operates identical to "Basic trigger mode" on page 149.
- Dual-level qualifier. The level detector operates identical to "Dual trigger mode" on page 150.

When in qualifier mode, the output of the trigger detector is sent to a qualifier line of the recorder trigger logic. For more information on the recorder trigger features, please refer to "Recorder and system trigger" on page 152.

10.4 Recorder and system trigger

The trigger modes and features described so far are channel-based. Each analog channel within a GEN series system has a digital trigger detector. The trigger signals of all channels of a single recorder are combined through a logical OR to generate a combined trigger. This trigger can be combined with an external trigger and qualifiers. The final result is a recorder trigger. The triggers that are generated by individual recorders can be distributed to other recorders and mainframes.

The following simplified diagram is from the Perception software and shows the building blocks that make the complete recorder trigger logic. Please note that not all features may be available depending on the exact hardware used.

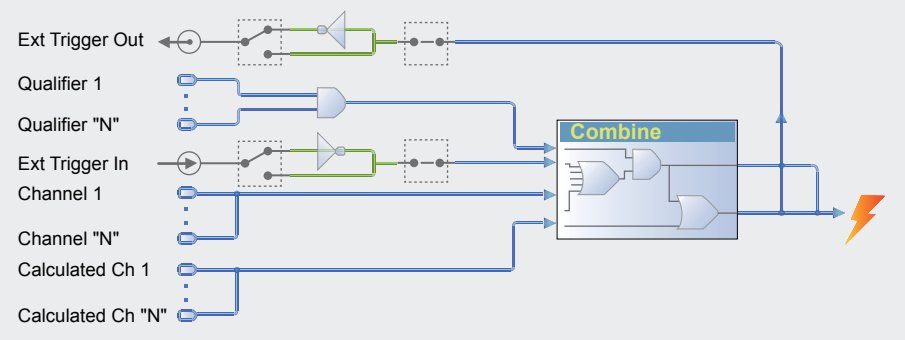


Figure 10.6: Recorder trigger logic

The heart of the recorder trigger logic is the “Combine” block. All trigger sources come together here. The trigger sources can generate a recorder trigger, depending on their settings, However, this can be blocked by qualifiers. If one of the qualifiers is not armed, no recorder trigger can be generated.

- **Channel 1 through N:**These are the channel triggers as described above. Please refer to chapter “Introduction of Digital Trigger Modes” on page 144.
- **External Trigger In:** This is an external trigger signal that is mainframe-related: The input connector is placed on the mainframe controller. Used to select rising or falling edge, all input cards in the mainframe use the same edge. Each input card can select to use the external trigger as a trigger source.
- **Qualifier 1 through N:** hese are the qualifiers as described above: Please refer to chapter "Trigger qualifier" on page 151.

- **External Trigger Out:** The recorder trigger can be used to send a trigger signal to the outside world. The output connector is placed on the mainframe controller. Used to select active High or Low level output, all input cards in the mainframe use the same output level. Each input card can select whether to send the trigger to the external trigger output.

10.5 Channel alarm

Each channel has the capability to generate an alarm. An alarm situation is detected with a basic dual level detector.

There are two alarm modes:

- Basic single-level alarm. The alarm line is active for as long as the signal exceeds the level in the specified direction. For more information on the level comparator, please refer to "Basic trigger mode" on page 149.
- Dual-level alarm. The alarm line is active for as long as the signal exceeds one of the two levels in the specified direction. For more information on the level comparators, please refer to "Dual trigger mode" on page 150.

The output of the alarm detector is sent to an alarm line and combined (OR-ed) with alarm conditions of the other channels and recorders. The result is available as an external output located on the mainframe controller.

11 Interface/Controller

11.1 Introduction

The Interface/Controller uses a high-end CPU with an embedded operating system. It is used to communicate with controlling computers and supports extra storage options.
Each complete mainframe houses an Interface/Controller, which enables data input and output so that the mainframes can be connected.

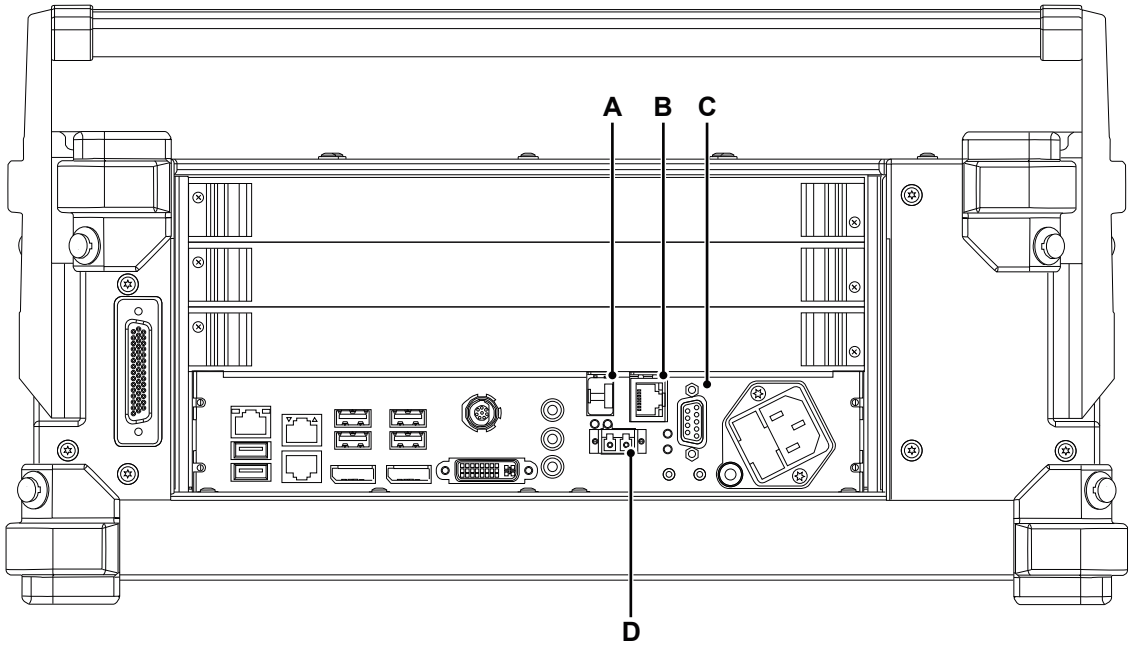


Figure 11.1: Interface/Controller

A PTP enabled network optical SFP slot (SFP module is optional)
B PTP enabled network RJ45
C I/O connector (trigger in/out, clock in, event out, start/stop)
D Master/Slave synchronization (optical)

The Interface/Controller has a unique communication section with one standard Ethernet interface, one optical Ethernet interface with two activity LEDs and a Master/Slave interface with two activity LEDs and the I/O connector.

11.2 Communication and control

The GEN series uses standard TCP/IP protocol over Ethernet to communicate with the PC. The Interface/Controller provides access to the Ethernet network.

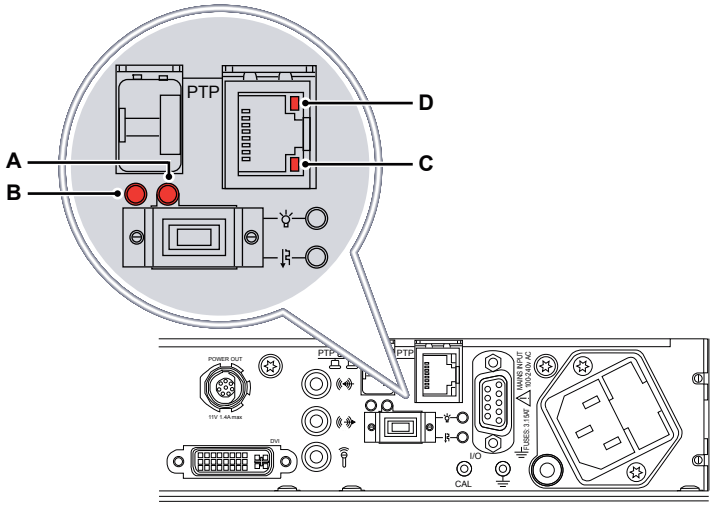


Figure 11.2: Ethernet LED indicators

A Link speed LED optical network
B Activity LED optical network
C Activity LED RJ45 network
D Link speed RJ45 network

Table 11.1: Ethernet LED indicators

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	No cable attached or no signal on cable
100 or 10 Mbit/s network connection	ON	OFF	Network connection with no data exchange
100 or 10 Mbit/s network connection	Blinking	OFF	Network connection with active data exchange
1 Gbit/s network connection	ON	ON	Network connection with no data exchange
1 Gbit/s network connection	Blinking	ON	Network connection with active data exchange

11.2.1 Network protocols and ports

All tethered GEN DAQ series mainframes use Ethernet protocols to communicate with the controlling PC. The following table gives an overview of the used protocols, ports, packet sizes and frequency of use on the network.

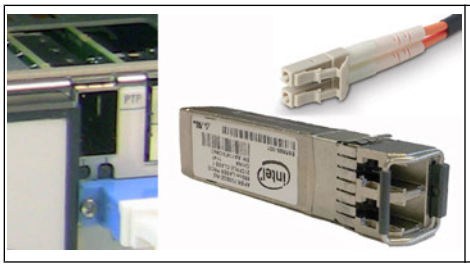
General TCP/IP IPv4 with standard Ethernet V2 fames (MTU = 1500 bytes) is used.

Specific protocols are used for:

Network protocols and ports	
Mainframe Identify	
Protocol	UDP (broadcast and directed)
Used ports	8004 (PC to mainframe) and 8005 (mainframe to PC)
Data size	Variable (<=1016 Bytes)
Frequency	When powering on / powering off / rebooting a mainframe When starting Perception Up to about 10 UDP frames each time, in both directions
More info	Packets have “PLAZADGRAM” at the start of the data area
Network Discovery Protocol	
Protocol	Multicast
Used IP addresses	239.255.77.76 and 239.255.77.77
Used IP ports	31419 (PC to mainframe) and 31418 (mainframe to PC)
Data size	Variable (< 2000 Bytes)
Frequency	When starting Perception When selecting Scan for Mainframes in Perception
Mainframe communication	
Protocol	TCP
Used ports	Connecting to Port 8003
Data size	Variable within MTU size
Data rate	Depending on storage speed, Ethernet Link speed and limited by network bandwidth. Currently maximum 120 MB/s on 1 Gbit Ethernet and 250 MB/s on 10 Gbit Ethernet ports.

Network protocols and ports	
Other protocols	
ARP, DNS	When supported on the network setup
DHCP, AutoIP	When enabled on this mainframe
iSCSI	Default port: 3260
PTP	V2, End-to-End, 1 sync per second

11.2.2 Using the 1 Gbit option connections



LC Connection Using the SFP + Option
LC optical connections that need an SFP device to enable their use with a LC connected optical cable.

The GEN series mainframes come with an optional 1 Gbit optical network support in the form of an SFP module.

The SFP receiver housing is part of the mainframe. Inserting a SFP module enables the use of optical Ethernet. The SFP module is offered in two different wavelengths: 850 nm or 1320 nm.

See appendix "Fiber optic cables and SFPs" on page 660 for detailed usage and specifications.

11.3 Master/Slave Synchronization

The GEN3i Master/Slave synchronization connector supports both standard and extended synchronization.

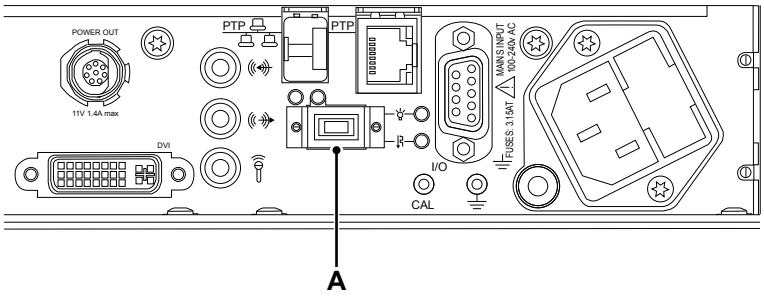


Figure 11.3: Interface/Controller

A Master/Slave synchronization (optical)

Standard Synchronization: Synchronizes the first sample in the recording for each mainframe, prevents frequency drift of the sample rates within each mainframe, synchronously exchanges every channel trigger connected to the Master/Slave trigger bus to/from each connected mainframe and automatically compensates for the cable length delay.

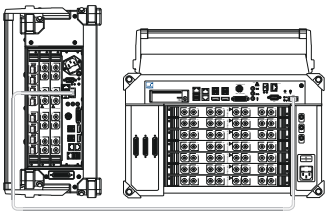
Extended Synchronization: Standard synchronization, Start/Stop and Pause of a recording across multiple mainframes, each controlled by a separate Perception. (Stop recording is a non-synchronous action). Synchronous manual trigger exchange (user software action to trigger all mainframes synchronously). Calculated channel trigger exchange (requires Perception V6.50 or higher).

For detailed specification, please refer to appendix "B3762-6.0 en (GEN3i Portable Data Recorder)" on page 378.

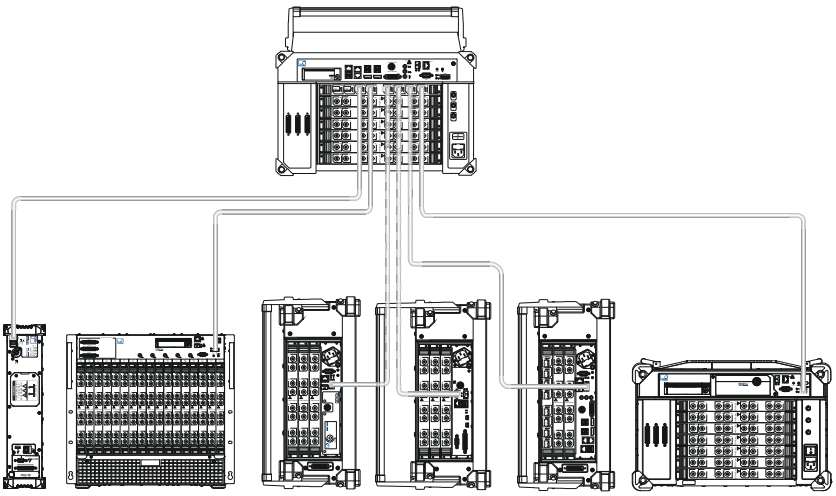
The GEN series can be operated as a fully synchronized Multi-Mainframe system with multiple mainframes using the Master/Slave synchronization connector.

The Master/Slave synchronization connector supports (please refer to chapter "Connecting the Master/Slave Synchronization connector" on page 163 and "Connecting multiple mainframes using the Master/Slave card" on page 163 for wiring details):

- Directly connect to one mainframe using the Master/Slave synchronization connector. Each mainframe can then be Master or Slave. The synchronization works in extended synchronization mode.



- Connect to a group of nine mainframes as Slave. At least one mainframe in this group must use the Master/Slave card option. This mainframe must be Master, as Master/Slave is always a STAR topology. The synchronization works in basic synchronization mode.



Master/Slave Synchronization connector operating modes

The Master/Slave Synchronization connector has three operating modes:

- Master
- Slave
- Stand-alone

In stand-alone mode, the Master/Slave synchronization connector is not used. Cables can be left attached, as no information is exchanged.

Fiber optic cable

The Master/Slave Synchronization has an optical I/O (IN/OUT) using duplex LC connectors that connects to other Master/Slave connectors. The maximum cable length supported is 500 m (For more information, please refer to "Calculating maximum fiber cable length" on page 853). As the connection is optical, no ground loops exist and the communication is not disturbed by external signal sources.

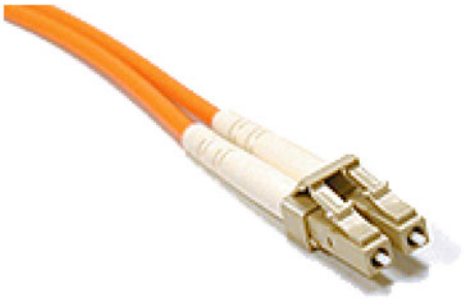


Figure 11.4: Example of a duplex LC® connector

LED indicators

On the front panel of the Master/Slave Synchronization connector, two LEDs indicate the status of the link.
The icon is used to identify the signal detect function.
The icon is for data/synchronization identification.

A icon

B icon

The following table shows the function and possible combinations of the two LEDs.

Table 11.2: Master/Slave card front panel LED indicators

FRONT PANEL LED INDICATORS			
Status			**Description**
No Link	off	off	No valid characters detected/ no optical signal detected
Optical signal detection/ initialization	on	off	Alignment characters detected
Receiving data	on	on	Receiving valid data

11.3.1 Connecting the Master/Slave Synchronization connector

With the fiber optic cable, connect the Master/Slave Synchronization connector of two mainframes.

In this setup, one mainframe must be set to Master while the other mainframe must then be set to Slave. In this setup, extended synchronization is used automatically.

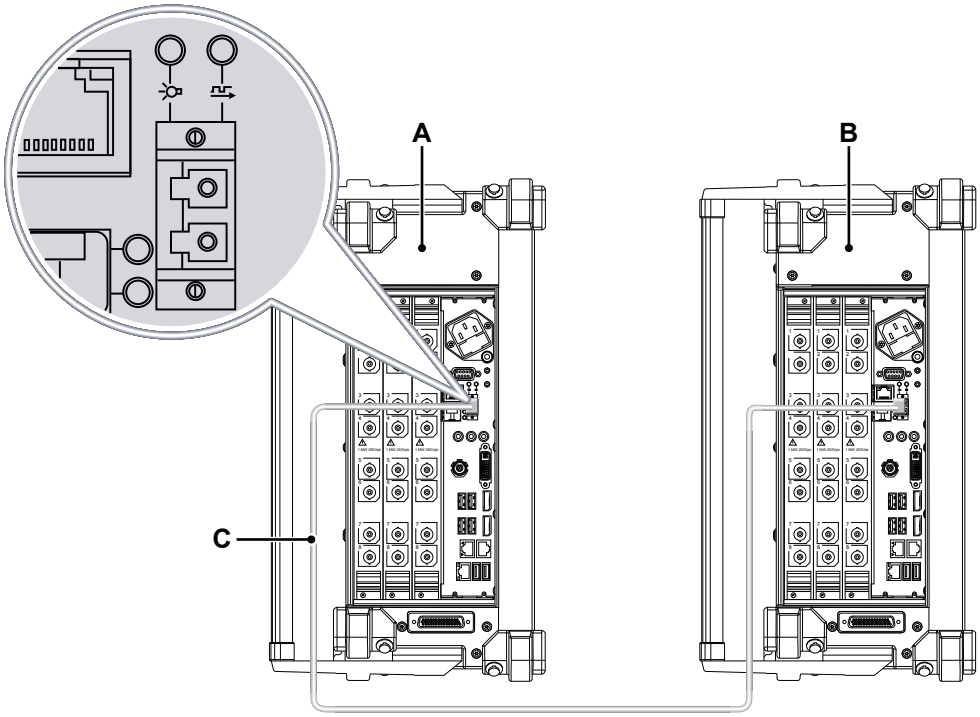


Figure 11.5: Connecting the Master/Slave

A Master mainframe

B Slave mainframe

C Fiber optic cable

11.3.2 Connecting multiple mainframes using the Master/Slave card

The multiple mainframe Master/Slave setup only works in a star configuration. All Master/Slave fiber optic cables are on one side connected to the Master mainframe while the other side connects to one of the Slave mainframes.

The master mainframe needs to be extended with one or more optional option carrier cards (G081). Each option carrier card can be extended with one or two Master output cards (G083).

Maximum Master/Slave overview			
	Option Carrier Card	Master Output Card	Slave Mainframes
GEN2tB	1	2	8
GEN3i	2	4	16
GEN3t	2	4	16
GEN7i	6	12	48
GEN7tA	6	12	48
GEN17tA	16	32	128

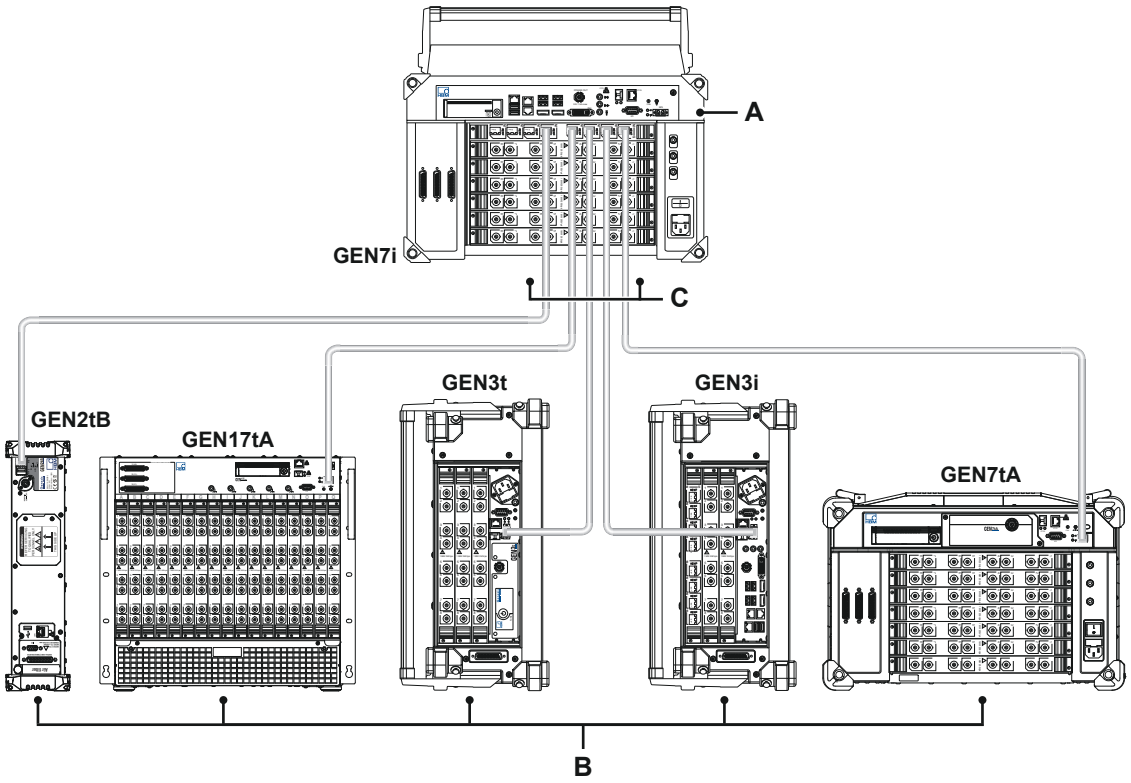


Figure 11.6: Master/Slave configuration with four slave mainframes

A Master mainframe

B Slave mainframes

C Fiber optic cable

1 Connect one of the connectors of the Master Output Card(s) (G083) to the Master/Slave synchronization connector of the Slave mainframe.

2 Connect one of the connectors of the Master Output Card(s) (G083) to the Master/Slave synchronization connector of the **second** Slave mainframe.

3 If **multiple** Slave mainframes are used repeat this setup until all Slave mainframes are connected.

11.3.3 Setting the Master/Slave operating modes

Each mainframe can be used as a Master or Slave by using the Master/Slave synchronization connector. The operating modes are set up using the Perception software.

In the *Perception work* area:

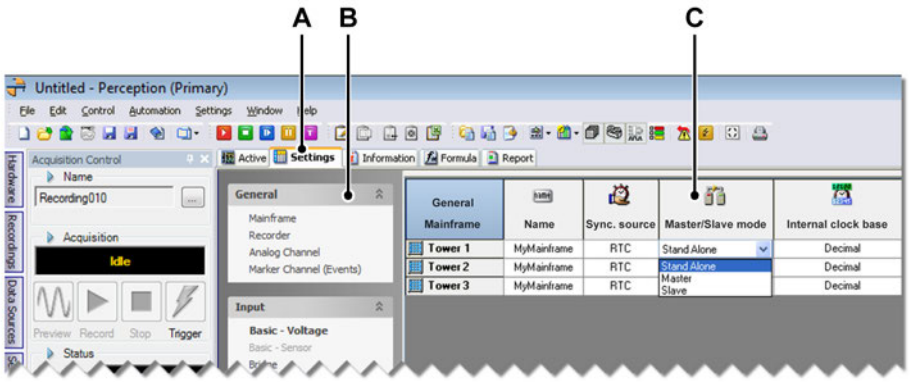


Figure 11.7: Perception work area with Master/Slave

A Settings tab

B General group

C Master/Slave mode column

To set the Master/Slave operation in the Perception software, proceed as follows:

1. Select the **Settings** sheet.
2. In the **Settings** sheet, go to the **General** group in the task pane and select **Mainframe**.
   A list of available mainframes is displayed in the settings area.
3. Set the master:
   - **a** Select the mainframe that should be used as Master.
   - **b** Double-click on the **Master/Slave mode** cell to open it for modification.
   - **c** In the drop-down list that appears, select **Master**.
4. Set one or more slaves:
   - **a** Select the mainframe(s) that should be used as Slave.
   - **b** Double-click on the **Master/Slave mode** cell to open it for modification.
   - **c** In the drop-down list that appears, select **Slave**.

To disable the Master/Slave operation and set the mainframe to Stand-alone mode:

1 Select the mainframe(s) that should be used as Stand-alone.
2 Double-click on the **Master/Slave mode** cell to open it for modification.
3 In the drop-down list that appears, select **Stand-alone**.

HINT/TIP

Cables do not have to be removed, as the mainframe does not use the connected cable during stand-alone mode.

11.3.4 Setting the Master/Slave trigger

When the Master/Slave card is in use, a recorder can either put the recorder trigger on the Master/Slave trigger line and/or pick up the trigger from the Master/Slave trigger line.

There are four settings that can be selected in the Perception software:

- Disabled
  No trigger is transmitted to or received from other mainframes.
- Transmit
  Transmit trigger(s) from this recorder to other mainframes, received triggers are ignored.
- Receive
  Receive trigger(s) from other mainframes, no triggers are transmitted.
- Transceive
  Transmit and receive trigger(s) from other mainframes.

The settings are controlled in the block diagram or through the *Master/Slave trigger* setting in the sheet.

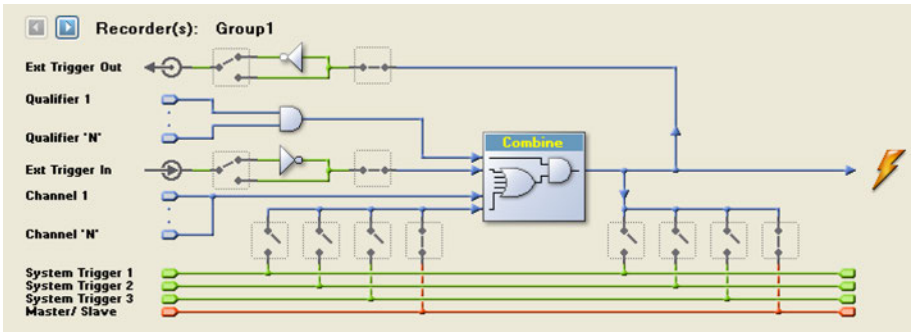


Figure 11.8: Block diagram

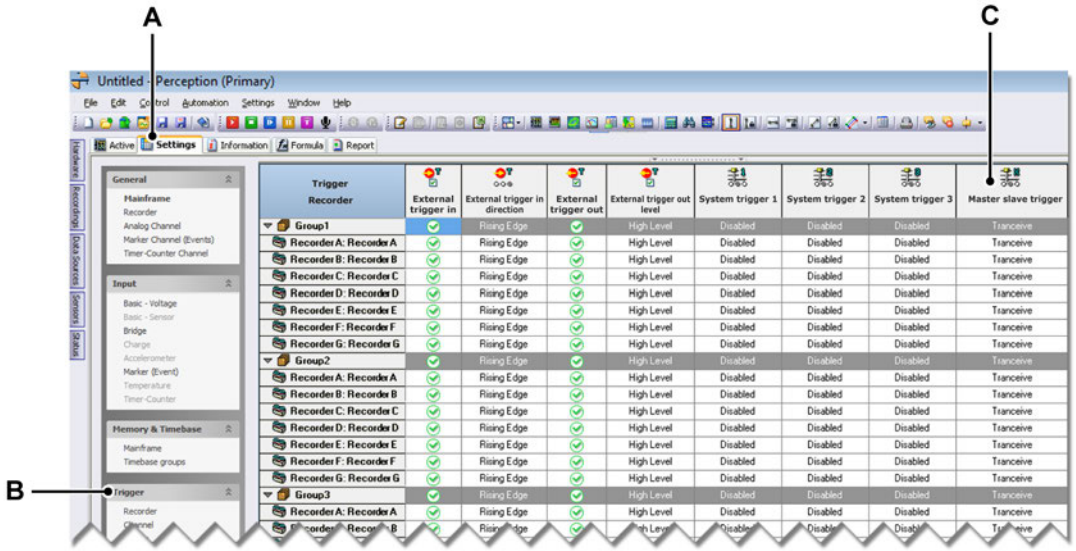


Figure 11.9: Perception work area with Master/Slave trigger

A Settings tab

B Trigger group

C Master/Slave trigger column

To set the Master/Slave trigger in the Perception software, proceed as follows:

1. Select the **Settings** sheet.
2. If it is not already done, switch the **Settings** sheet layout modes to **Advanced** mode.
3. In the **Settings** sheet, go to the **Trigger** group in the task pane and select **Recorder**.
   A list of available recorders is displayed in the settings area.
4. Select the recorder that you want to set.
5. Double-click on the **Master/Slave trigger** cell to open it for modification.
6. In the drop-down list that appears, select the setting that should be used.

Figure 11.10: Master/Slave trigger list

11.3.5 Synchronizing a Master/Slave setup to external time sources

In a Master/Slave setup, all time information is recorded by the Master mainframe only. Synchronization source selection on Slaves is disabled as Slave mainframes are dedicated to follow the Master mainframe.

For the Master mainframe, the date and time are controlled by either the PC (RTC) , PTP master, IRIG or GPS, depending on the synchronization source selected. The source is selected in the Perception software.

In the *Perception work* area:

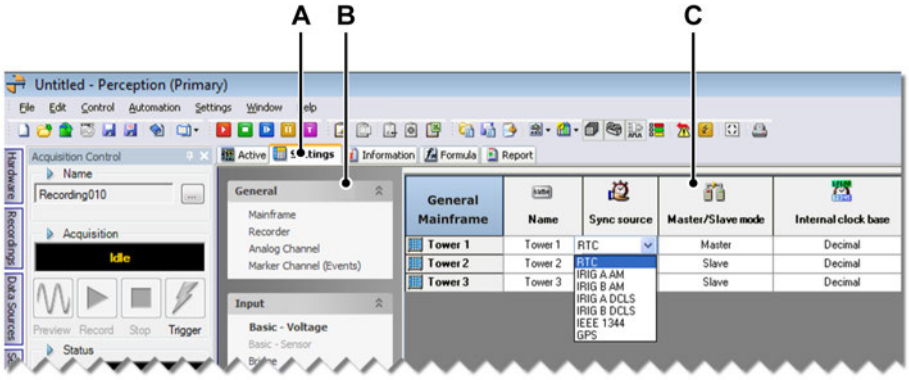


Figure 11.11: Perception work area synchronization source

A Settings tab

B General group

C Sync source column

To set the synchronization source in the Perception software, proceed as follows:

1. Select the **Settings** sheet.
2. In the **Settings** sheet, go to the **General** group in the task pane and select **Mainframe**.
   A list of available mainframes is displayed in the settings area.
3. Select the Master mainframe.
4. Double-click on the **Sync source** cell to open it for modification.
5. In the drop-down list that appears, select the synchronization source that should be used.

For information on how to check synchronization, please refer to appendix "Master/Slave synchronization verification procedure" on page 814.

11.4 I/O connector

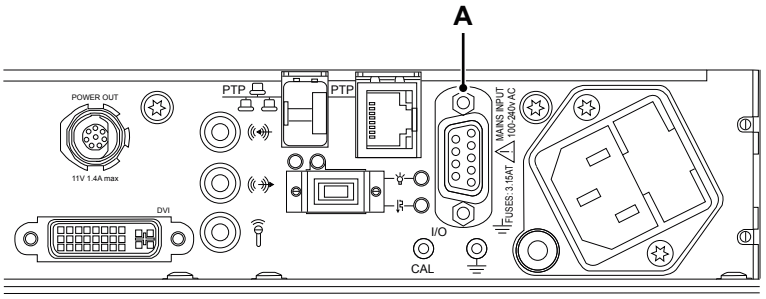


Figure 11.12: Interface/Controller

A I/O connector (trigger in/out, clock in, event out, start/stop)

The I/O connector comes with a BNC breakout cable for direct BNC cable connection to each function (see Figure 11.13).

PIN	Signal
PIN 1	External Time base In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	Ground

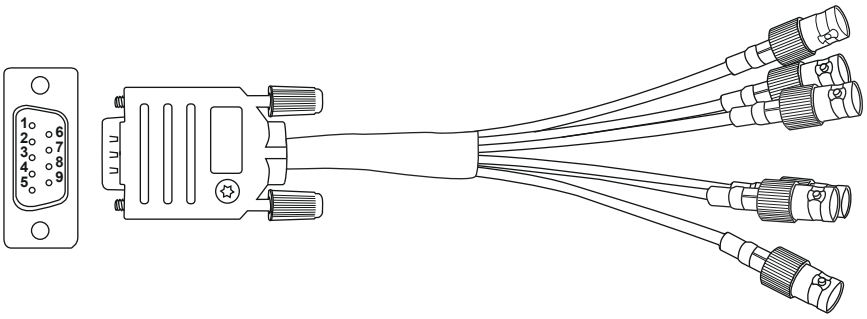


Figure 11.13: BNC breakout cable

11.4.1 I/O connector input overvoltage protection

All inputs of the I/O connector are over voltage protected. All inputs use the following schematic approach.

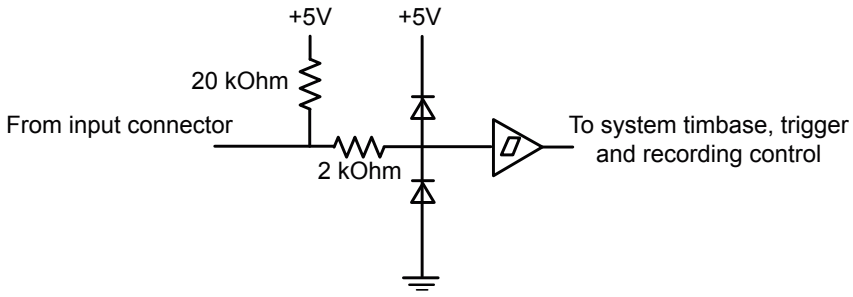


Figure 11.14: I/O connector schematic inputs

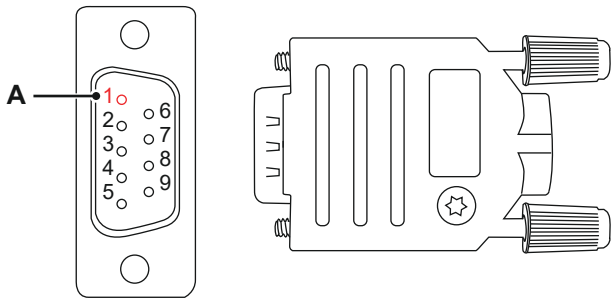
Due to the 20 kΩ pull-up resistor all inputs will be “TTL High” and only need an external short to signal ground to be operated. The 2 kΩ series resistor together with the diode clamps to ground and +5 V protect the digital circuitry up to the specified voltages.

The clamping diodes and other parasitic capacitors do create a capacitive load on your signal source and limit the signal bandwidth. To reach the required bandwidths detailed compensations are made not addressed in this block diagram.

11.4.2 I/O connector functions and connector pinning

A External Time base In

PIN	Signal
PIN 1	External Time base In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V

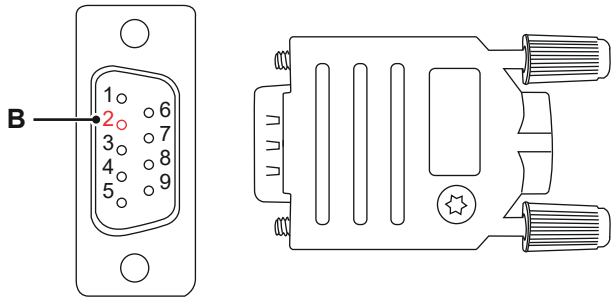


This input can be used to provide another time base for the ADC rather than the internal one. This input is typically used in combination with rotating machinery in which the ADC clock is synchronized with the revolutions. Using Perception software select external time base in the Mainframe section of the Settings.

For an example on how to use ”External Time base In”, please refer to appendix "Rotational External Clock" on page 840.

B External Event Out

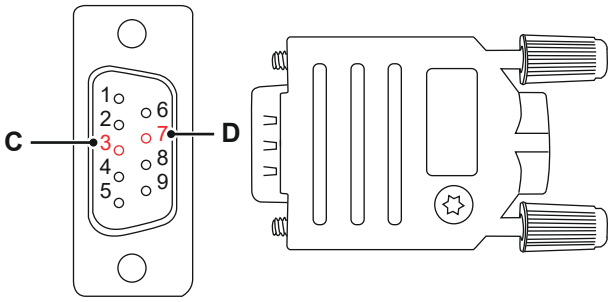
PIN	Signal
PIN 1	External Time base In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V



This output is software selectable between **Alarm Out** and **Recording Active Out.** When *alarm* is selected, the output is driven by channel alarm detectors. When *recording active* is selected, the output is “high” while a recording is in progress.

C/D External Trigger In/Out

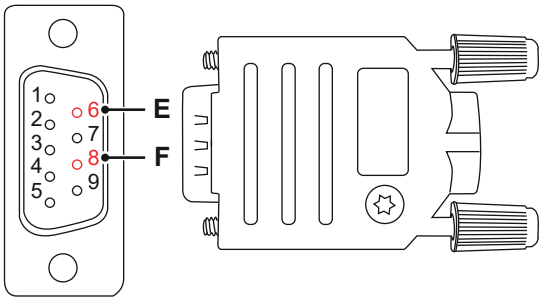
PIN	Signal
PIN 1	External Time base In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V



This input and output are related to the recorder trigger logic. For more information, please refer to “Recorder and system trigger” on page 152.

E/F External Start In/External Stop In

PIN	Signal
PIN 1	External Time base In
PIN 2	External Event Out
PIN 3	External Trigger In
PIN 4	Ground
PIN 5	Ground
PIN 6	External Start In
PIN 7	External Trigger Out
PIN 8	External Stop In
PIN 9	+5V



The **External start/stop** (see Figure 11.15) settings are located in the **General/ Mainframe** setting page of the settings spreadsheet. The settings are only visible when **Advanced (All settings)** is enabled (see Figure 11.16).

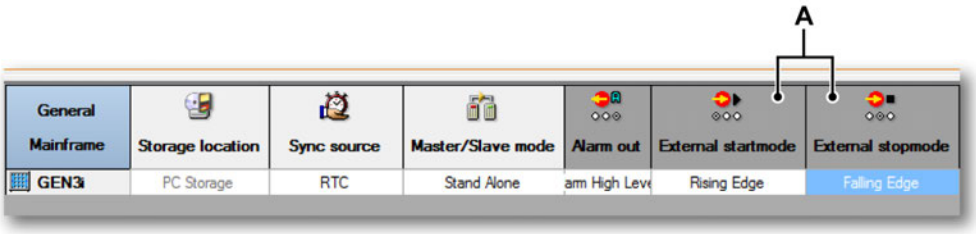


Figure 11.15: General/Mainframe settings

A External start/stop mode columns

To enable the advanced settings, right click on the table header (see Figure 11.16).

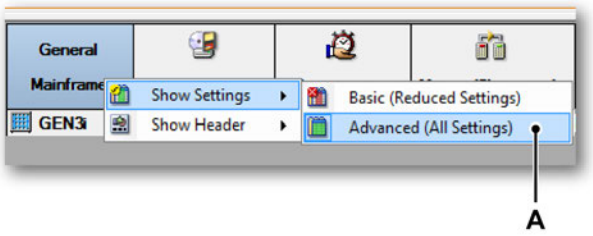
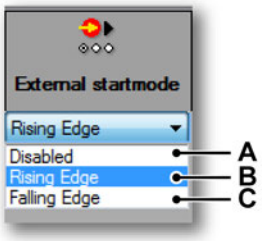


Figure 11.16: Show Settings - Advanced

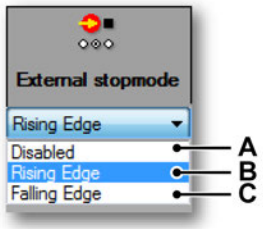
A Advanced (All Settings)

The **External startmode** setting can be used to configure the external start input.



A When selecting **Disabled**, the signal on the input is ignored.
B When selecting **Rising Edge**, a start is initiated when a rising edge is detected.
C When selecting **Falling Edge**, a start is initiated when a falling edge is detected.

The **External stopmode** setting can be used to configure the external stop input.



A When selecting **Disabled**, the signal on the input is ignored.
B When selecting **Rising Edge**, a stop is initiated when a rising edge is detected.
C When selecting **Falling Edge**, a stop is initiated when a falling edge is detected.

The minimum pulse width for both External Start In and External Stop In is 200 ns. Pulses shorter than 200 ns will be ignored.

As the Start/Stop events are software processed events, a one second response time typically passes before the Start/Stop is executed. After an event is received, a “disable” time period of 100 ms starts. The same event will not be detected during the disable time period. For example, if a Start event is received, a new Start event will not be detected for 100 ms. If, however, a Stop event occurred immediately after a Start event had been detected, the Stop event would be detected and processed immediately after the acquisition is started due to the Start event.

11.5 Option - Optical 1 Gbit Ethernet interface

The Interface/Controller supports an optical 1 Gbit Ethernet interface by means of an SFP module. An SFP module is a small, form-factor and pluggable transceiver that supports direct optical network connections.

WARNING

Laser Safety
The system is classified as a Class 1 laser product. The SFP uses an optical light source for data and command communication. It does not emit hazardous light, but direct exposure to the beam should be avoided.

This simple and powerful plug-in-and-use option enables the use of an optical network connection on the Interface/Controller. There are two models available to choose from:

- 1 Gbit (850 nm) - Multi Mode
- 1 Gbit (1310 nm) - Single Mode

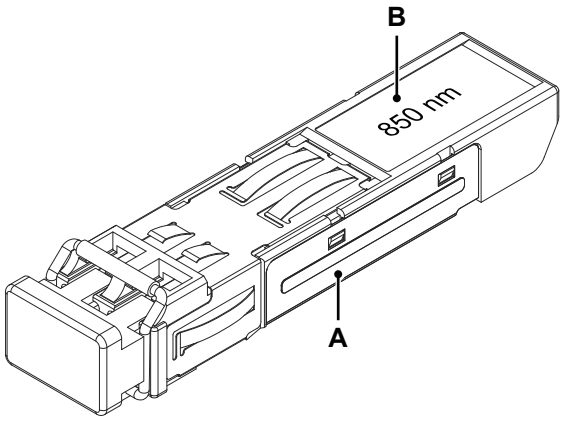


Figure 11.17: SFP optical network device

A SFP shown with dust cap and removal bar

B SFP label - 850 or 1310 nm

Note *1310 nm Single Mode (SM) and 850 nm Multi Mode (MM) optical fiber transceivers use specific cables and connectors. Therefore, make sure that the correct mode/specification of fiber optic cable is used.*

Selecting cables and cable lengths:
Cables need to have different properties when they exceed certain lengths. These cable properties are based on the properties of light in an optical fiber.

Single Mode The cable is a type of cable that has a relatively small light-carrying core. Light in a small core makes fewer internal reflections so that the path of light is close to a straight line. Therefore, the light can travel further distances.

Multi Mode The cable is a type of cable that has a relatively large light-carrying core. Light in a larger core makes more reflections and can only travel shorter distances.

For specifications and ordering information, please refer to "B3762-6.0 en (GEN3i Portable Data Recorder)" on page 378.

For information on how to install and remove the SFP module, please refer to section "Installing a 1 Gbit SFP/10 Gbit SFP+ Module" on page 185.

11.6 Option - 10 Gbit Ethernet interface (SFP+ Module)

The 10 Gbit Ethernet option is a Factory installed, ready to use Ethernet option with two available Ethernet interfaces.

The 10 Gbit Ethernet card can be installed in addition to the standard on-board 1 Gbit Ethernet connection. The 10 Gbit Ethernet card allows you to double the throughput speed of communication when compared to the standard 1 Gbit Ethernet. If installed, the 10 Gbit Ethernet option can replace the use of the standard 1 Gbit Ethernet connection.

WARNING

Laser Safety
The system is classified as a Class 1 laser product. The SFP uses an optical light source for data and command communication. It does not emit hazardous light, but it is recommended to avoid direct exposure to the beam.

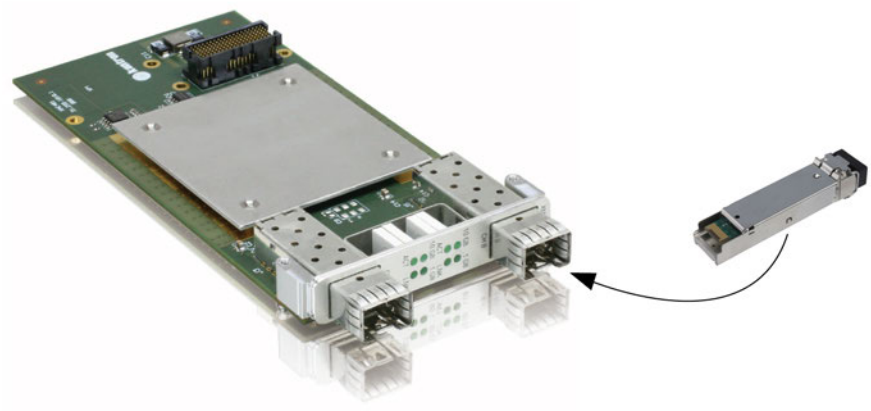
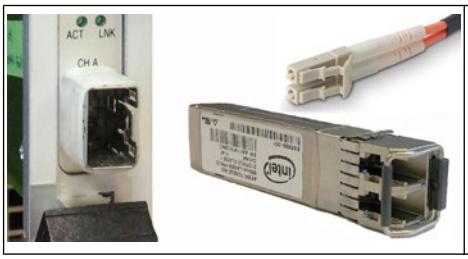


Figure 11.18: 10 Gbit Ethernet card - with SFP+ module

Note *The maximum 10 Gbit throughput speed is per-card. Throughput speed is therefore a shared specification for both interfaces combined. It is possible that two interfaces can be used at the same time but only when one interface is used for communication and the other is used for storage. Two interfaces cannot be used at the same time for storage purposes nor can they be used at the same time for communication purposes.*

Connections and using the 10 Gbit Option



A 10Gbit LC Connection Using the SFP+ Option
10Gbit LC optical connections need an SFP+ module to enable their use with LC connected optical cable.

Note *([1]) The 10 Gbit speed rating can be achieved with **optimized settings** using compatible equipment and devices of similar speed ratings. Please see appendix "Optimal Windows® settings for 10 Gbit Ethernet card" in GEN series Data Acquistion manual for further details on the specific **optimized settings**.*

Front panel layout

The front panel of the 10 Gbit Ethernet option has the following layout:

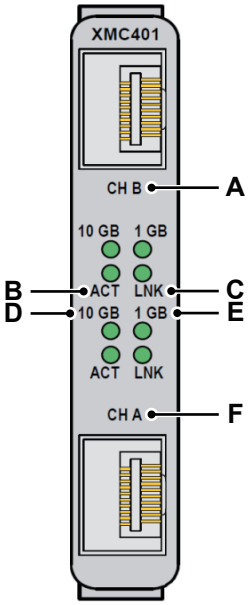


Figure 11.19: Front panel of XMC401 10 Gbit Ethernet card

A **CH B = NIC2** (Requires SFP+ module, not shown)

B ACT (green): Ethernet Activity (on when active)

C LNK (green): Ethernet Link (on when active)

D 10 Gbit (green): Ethernet Speed 10 Gigabit (always on)

E 1 Gbit (green): Ethernet Speed 1 Gigabit (always on)

F **CH A = NIC1** (Requires SFP+ module, not shown)

Figure 11.19 shows the two interfaces of this option without installed SFP+ option, for further details on the SFP+ options please see the next section.

Once the SFP+ option is installed in the 10 Gbit Ethernet interface, an LC optical cable can be connected.

10 Gbit Ethernet Option accessories
The 10 Gbit Ethernet card supports two (10 Gbit) SFP+ modules which are separately available, see options in the specifications sheet of this section for ordering.

The two types of 10 Gbit SFP+ module that are used with this Ethernet card are:

- 10 Gbit (850 nm) - Multi Mode
- 10 Gbit (1310 nm) - Single Mode

Note *__SFP__ modules rated at 1 Gbit and are not suitable for this card. Please select the __SFP+__ modules which are rated at 10 Gbit.*

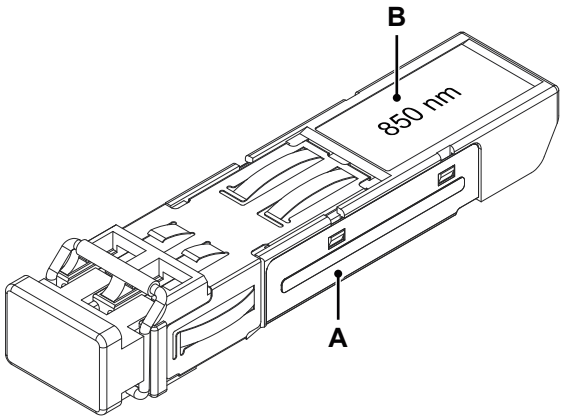


Figure 11.20: SFP Optical Network devices

A SFP shown with dust-cap and removal bar

B SFP label - 850 or 1310 nm

Note *1310 nm Single Mode (SM) and 850 nm Multi Mode (MM) optical fiber transceivers use specific cables and connectors therefore please check the correct mode/specification of fiber optic cable is used.*

Cable selection and lengths:
Cables require different properties when they exceed certain lengths based on the properties of light in an optical fiber.

Single Mode Cable is a type of cable that has a relatively small light carrying core and therefore makes fewer internal reflections so that the path of light is closer to a straight line and thus can travel further distances.

Multi Mode Cable is a type of cable that has a relatively thicker light carrying core. Light in a thicker core makes more reflections and is therefore only suited to shorter distances. The following table shows what mode of fiber is required for each distance covered.

For Installation and removal of the SFP+ module see section "Installing a 1 Gbit SFP/10 Gbit SFP+ Module" on page 185.

10 Gbit Ethernet card in GENDAQ series networks
There are several different ways to connect individual components together when using the 10 Gbit Ethernet card therefore this card allows the user more freedom to set up their system with different configurations.

The 10 Gbit Ethernet card can essentially be used to communicate at double the throughput speed of the standard 1 Gbit Ethernet or with more advanced setups can act as a manually switchable storage selector or even a dual communication and storage interface.

The following Figure 11.21 shows a simple setup using the 10 Gbit Ethernet card. A PC with an optical Ethernet interface which has SFP+ support is connected via optical cable to the interface of the 10 Gbit Ethernet card option of the GENDAQ unit. This setup utilizes the higher speed communication of the 10 Gbit Ethernet card for communication with Perception.

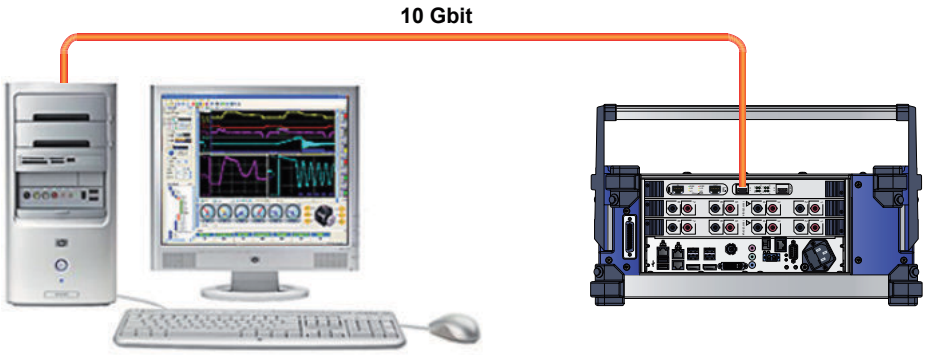


Figure 11.21: Basic setup - 10 Gbit Ethernet to PC

Connecting the 10 Gbit Ethernet Option to a PC

To be able to use this option you also need the correct connection or interface attached to your PC. The correct connection is not always an SFP+ module but there must be a network card or adaptor installed that supports the same specifications as the SFP+ modules used on the GENDAQ side.

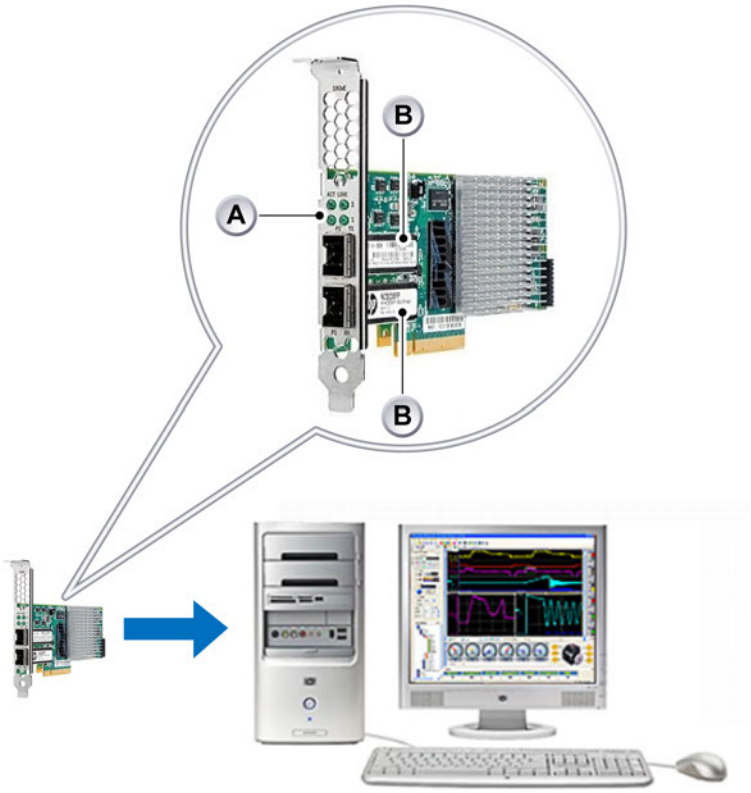


Figure 11.22: Connect the 10 Gbit Ethernet Option to a PC

A 10 Gbit Ethernet card

B SFP+ modules

A 10 Gbit PC network card without SFP+ modules inserted and Ethernet switch with an SC optical connection can be used to communicate with the 10 Gbit Ethernet card.

Network Interface selection in Perception
With the 10 Gbit Ethernet option installed and ready to go you will be provided with the two following interfaces for selection:

- Optical 10 Gbit NIC1
- Optical 10 Gbit NIC2

In Perception these interfaces are available in the **Settings** menu > **Mainframe Network Setup** see Figure 11.23 below.

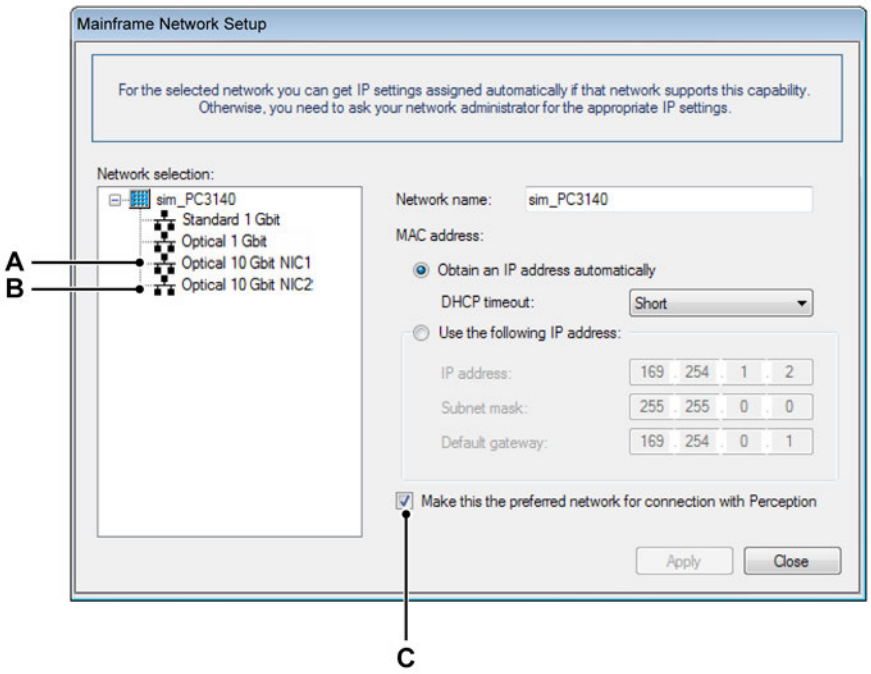


Figure 11.23: Mainframe Network Setup

A Optical 10 Gbit NIC1

B Optical 10 Gbit NIC2

C Make this the preferred network for connection with Perception

In **Mainframe Network Setup** you can define the IP address of each individual interface if needed.

If Perception finds more than one interface for **Network Selection** as shown in Figure 11.23, then the interface that has a Check in the box **Make this the preferred network connection with Perception** will be the interface used for communication with Perception. For the 10 Gbit Ethernet card check the box for the **Optical 10 Gbit NIC1 or 2**.

Click **Apply** then **Close** when done.

Windows® 7 - optimum settings

IMPORTANT

To best achieve data transfer rates greater than 200 MB/s please make sure the following settings are introduced to your network adaptor via the settings in Windows.

Windows® 7 10G network adapter settings:

- Interrupt moderation rate: **high**
- Receive side scaling ques: **8**
- Receive buffers: **2048**

For more information on how to do this please see appendix "10 GB Ethernet Windows settings" on page 873.

Note *The above Windows® settings were tested and chosen using a specific setup of equipment (Intel® Ethernet Server adaptor x520). These setting may not be the optimal settings for your specific system.*

11.6.1 Installing a 1 Gbit SFP/10 Gbit SFP+ Module

Introduction

This section explains how to install and remove the Small Form Factor Pluggable (SFP or SFP+) transceiver device from any interface that supports SFP or SFP+ modules.

This device enables an optical network connection to be plugged directly into the front panel, in the optical network interface of the Interface/Controller. This option is also required in order to use the 10 Gbit Ethernet card.

Warnings

Before installing this device, please read and make sure that you have understood the following warnings, which are specific for this device.

Description of Electrostatic Discharge (ESD)

CAUTION

Electrostatic discharge (ESD) can cause damage to electronic devices if discharged into the device. Take steps to avoid such an occurrence.

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). ESD damage is quite easy to induce, often hard to detect, and always costly. Therefore, we must emphasize the importance of ESD preventions when handling a GEN series system, its connections or a plug-in card.

WARNING

Laser Safety
The system is classified as a Class 1 laser product. The SFP uses an optical light source for data and command communication. It does not emit hazardous light, but it is recommended to avoid direct exposure to the beam.

Installation steps

1 First, make sure that the mainframe unit is switched off. Then locate the available SFP slot and remove the plastic plug (if inserted).

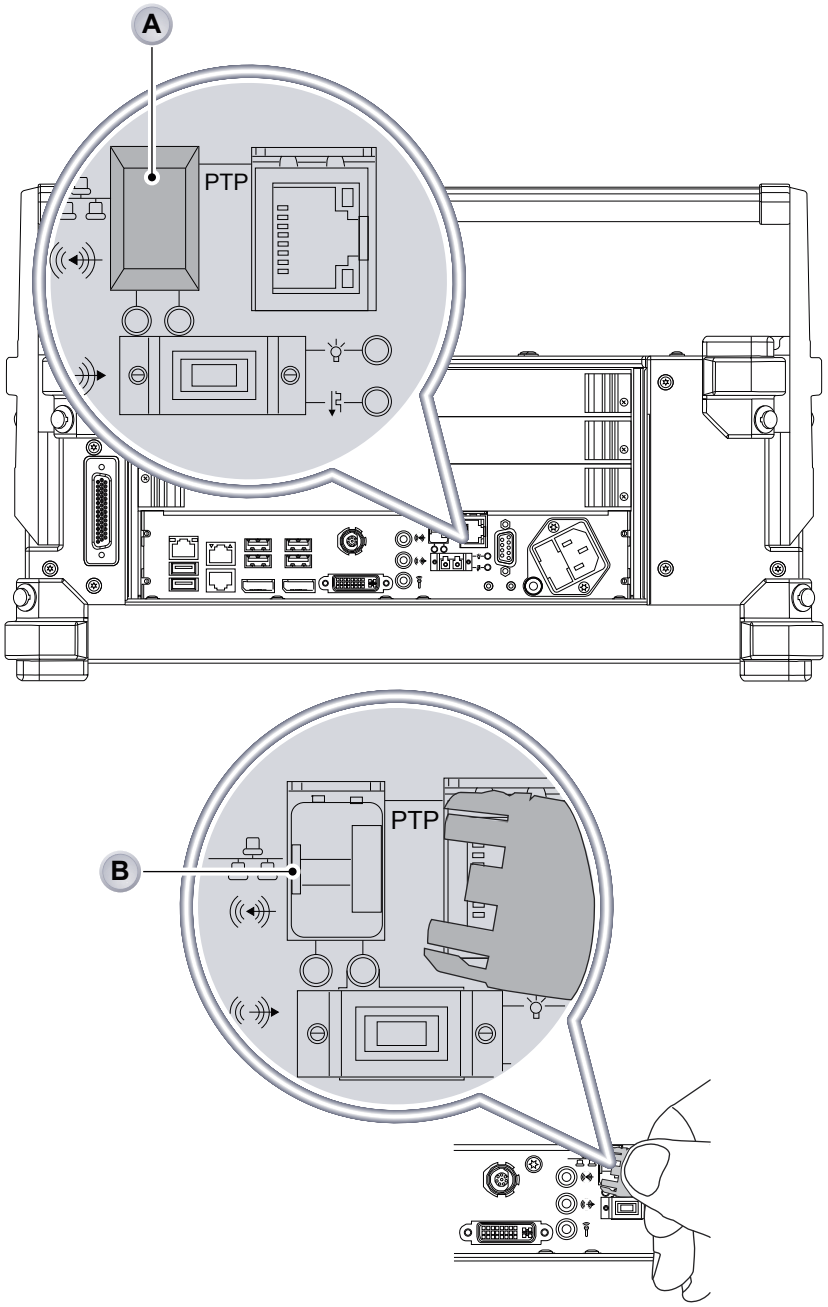


Figure 11.24: Interface/Controller SFP location

A Interface/Controller SFP location

B Remove cap

2 Grasp the module between fingers and thumb at the end with the small black removal bar. Push the back end into the available SFP slot, until you hear a click.

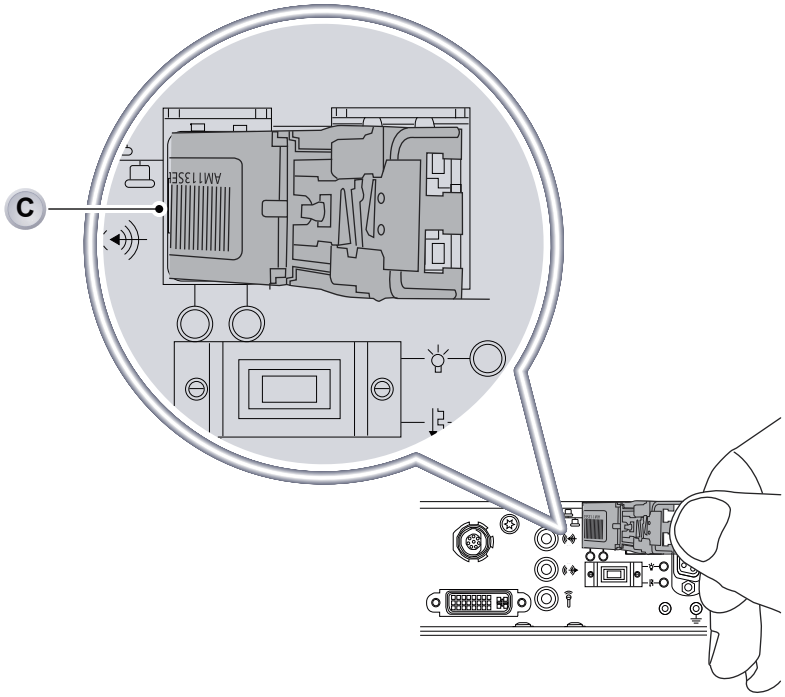


Figure 11.25: Insert device in SFP slot

C Insert device

3 Embedded software detects the device and automatically connects to it when the mainframe is powered on.

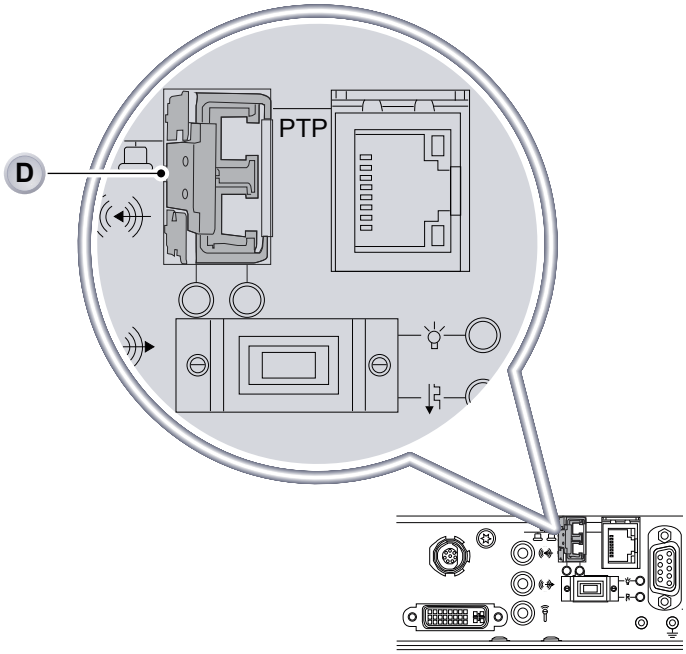


Figure 11.26: SFP slot with device

D Device being inserted

11.6.2 Removing a 1 Gbit SFP/10 Gbit SFP+ Module

To remove the module from the mainframe, first make sure that the mainframe is powered off. Then grasp the small black removal bar and pull it away and out from the mainframe. The spring-loaded removal bar releases the SFP from the front panel.

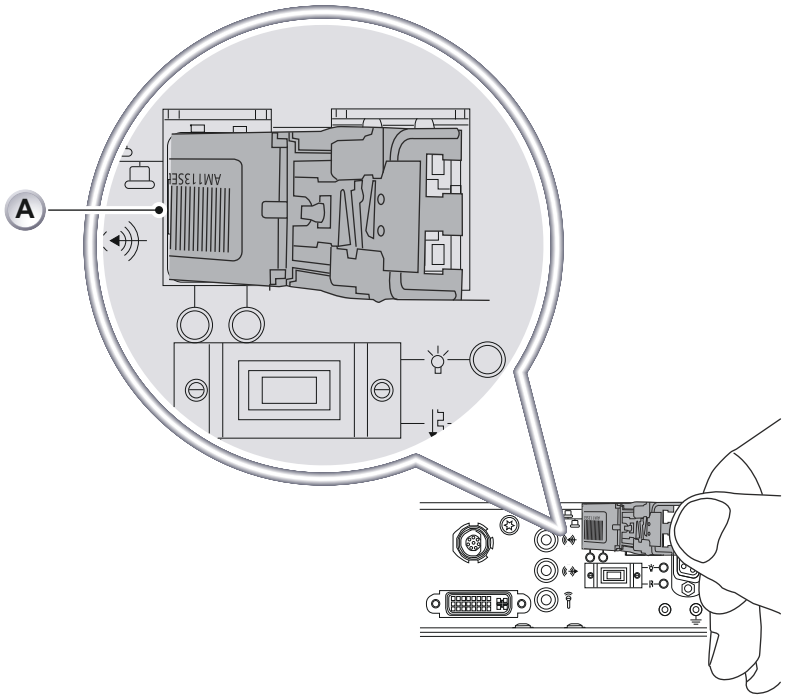


Figure 11.27: SFP slot - Remove device

A Remove device

Then, if available, replace the small plastic plug to protect the optical inlet.

12 Input Cards

12.1 Available input cards

Table 12.1: Model overview (Part 1)

Model Overview											
Model	**Basic**	**Basic sensor**	**Bridge**	**IEPE**	**Piezoelectric**	**RTD**	**Thermocouples**	**Current loop**	**Galvanic isolation**	**Analog resolution [Bits]**	**Maximum sample rate [S/s] (not multiplexed)**
GN610B	✓								✓	18	2 M
GN611B	✓								✓	18	200 k
GN815	✓			✓					✓	18	2 M
GN816	✓			✓					✓	18	200 k
GN840B	✓	✓	✓	✓	✓	✓	✓	✓	✓	24	500 k
GN1640B	✓	✓	✓	✓	✓	✓	✓	✓	✓	24	500 k
GN1202B	✓									14	100 M
GN8101B	✓									14	250 M
GN8102B	✓									14	100 M
GN8103B	✓									14	25 M
GN3210	✓			✓	✓					24	250 k
GN3211	✓									24	20 k

Table 12.2: Model overview (Part 2)

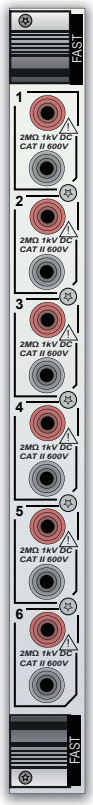
Model Overview									
Model	**Analog channels / card**	**Analog resolution [Bits]**	**Maximum sample rate [S/s] (not multiplexed)**	**Digital events / card**	**Digital Timer/Counters / card**	**Memory / card (Shared by channels)**	**Standard streaming**	**Fast Streaming (GEN3i/7i, GEN3t,7tA,17tA)**	**Slot width**
GN610B	6	18	2 M	16	2	2 GB		✓	1
GN611B	6	18	200 k	16	2	2 GB		✓	1
GN815	8	18	2 M	16	2	2 GB	✓	✓	1
GN816	8	18	200 k	16	2	200 MB	✓	✓	1
GN840B	8	24	500 k	16	2	2 GB		✓	1
GN1640B	16	24	500 k	16	2	2 GB		✓	2
GN1202B	(1)	(1)	100 M	16	2	2 GB		✓	1
GN8101B	8	14	250 M	16	2	2 GB		✓	1
GN8102B	8	14	100 M	16	2	2 GB		✓	1
GN8103B	8	14	25 M	16	2	2 GB		✓	1
GN3210	32	24	250 k	16	2	2 GB	✓		1
GN3211	32	24	20 k	16	2	200 MB	✓		1

(1) 12 Optical fiber transmitter channels supported. For details see table “Optical Fiber Transmitter Channels” on page 193.

Optical Fiber Transmitter Channels					
Transmitter Every transmitter is a single channel unit. Every unit has an unbalanced differential input, amplifier, analog anti-alias filter and ADC with an optical data and control link to the receiver card. The receiver card has the recording logic, sample rate selection and memory.					
Model	**Receiver card**	**Power**	**Sample rate**	**Resolution**	**Isolation**
GN110	GN1202B	Battery	100 MS/s	14 bit	User application defined
GN111	GN1202B	Battery	25 MS/s	15 bit	User application defined
GN112	GN1202B	120/ 240 V AC	100 MS/s	14 bit	1800 V RMS
GN113	GN1202B	120/ 240 V AC	25 MS/s	15 bit	1800 V RMS

12.2 Isolated 1kV input cards

12.2.1 GN610B, Isolated 1kV 2MS/s input card with real-time formula database



- 6 analog channels
- Isolated, balanced differential inputs
- ± 10 mV to ± 1000 V input range
- Basic accuracy 0.02%
- Basic power accuracy 0.02%
- 600 V RMS CAT II reinforced isolation, tested up to 6.4 kV
- Analog/digital anti-alias filters
- 18 bit at 2 MS/s sample rate
- Real-time formula database calculators (option)
- Triggering on real-time results
- Digital Event/Timer/Counter support
- 1 kV RMS CAT IV probe
- 5 kV RMS certified probe

The isolated balanced differential input offers voltage ranges from ± 10 mV to ± 1000 V.
Tested up to 6.4 kV, the reinforced isolation allows for safe measurements up to 600 V RMS CAT II (without probes).
Optimum anti-alias protection is achieved by the 7-pole analog anti-alias filter combined with a fixed 2 MS/s sampling Analog-to-Digital converter. The digital filters operating at the full ADC sample rate offer a large range of high order anti-alias filter characteristics with precise phase match and noise-free digital output.
The two Timer/Counters and the G070A torque/RPM adapter allow for direct interfacing to HBM torque transducers or other torque and speed sensors.
The real-time formula database calculators offer math routines to solve almost any real-time mathematical challenge. Dynamic digital cycle detection enables real-time storage as well as 1 µs latency digital output of calculation results like True-RMS on all analog, torque, angle, speed and Timer/Counter channels.
Channel to channel math creates computed channels with 1 µs latency obtaining mechanical power and/or multiphase (not limited to three) electric power (P, Q, S) or even efficiency calculations. Real-time calculated results can be used to trigger the recording or signal alarms to the external world.

For specification and ordering information, please refer to "B04374_02_E00_00 (GEN series GN610B)" on page 398.

12.2.2 GN611B, Isolated 1kV 200kS/s input card with real-time formula database

- 6 analog channels
- Isolated, balanced differential inputs
- ± 10 mV to ± 1000 V input range
- Basic accuracy 0.02%
- Basic power accuracy 0.02%
- 600 V RMS CAT II reinforced isolation, tested up to 6.4 kV
- Analog/digital anti-alias filters
- 18 bit at 200 kS/s sample rate
- Real-time formula database calculators (option)
- Triggering on real-time results
- Digital Event/Timer/Counter support
- 1 kV RMS CAT IV probe
- 5 kV RMS certified probe

The isolated balanced differential input offers voltage ranges from ± 10 mV to ± 1000 V.
Tested up to 6.4 kV, the reinforced isolation allows for safe measurements up to 600 V RMS CAT II (without probes).
Optimum anti-alias protection is achieved by the 7-pole analog anti-alias filter combined with a fixed 2 MS/s sampling Analog-to-Digital converter. The digital filters operating at the full ADC sample rate offer a large range of high order anti-alias filter characteristics with precise phase match and noise-free digital output.
The two Timer/Counters and the G070A torque/RPM adapter allow for direct interfacing to HBM torque transducers or other torque and speed sensors.
The real-time formula database calculators offer math routines to solve almost any real-time mathematical challenge. Dynamic digital cycle detection enables real-time storage as well as 1 µslatency digital output of calculation results like True-RMS on all analog, torque, angle, speed and Timer/Counter channels.
Channel to channel math creates computed channels with 1 µs latency obtaining mechanical power and/or multiphase (not limited to three) electric power (P, Q, S) or even efficiency calculations. Real-time calculated results can be used to trigger the recording or signal alarms to the external world.

For specification and ordering information, please refer to "B04375_02_E00_00 (GEN series GN611B)" on page 425.

12.2.3 Using the GN610B/GN611B

WARNING

High bandwidth and measurement cabling

Due to the high bandwidth measurement capabilities of the acquisition card, combined with the high measurement sensitivity of the card, it is important to pay close attention to the measurement cabling.

Some advice to prevent measuring unwanted disturbances:

- Keep measurement cables as short as possible in order to reduce the reception of environmental disturbances.
- Use shielded cables. The cable should have the measurement cables paired inside a shield. Preferably, the shield should be connected to the chassis of the measurement Genesis High Speed equipment. Alternatively, the shield could also be connected to the chassis of the object under test.

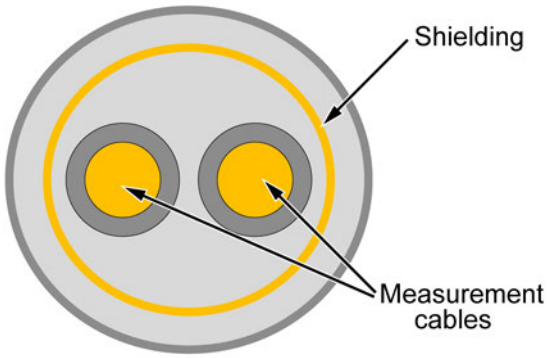


Figure 12.1: Shielded cable principles

HBM KAB290 cables are designed to meet this setup:

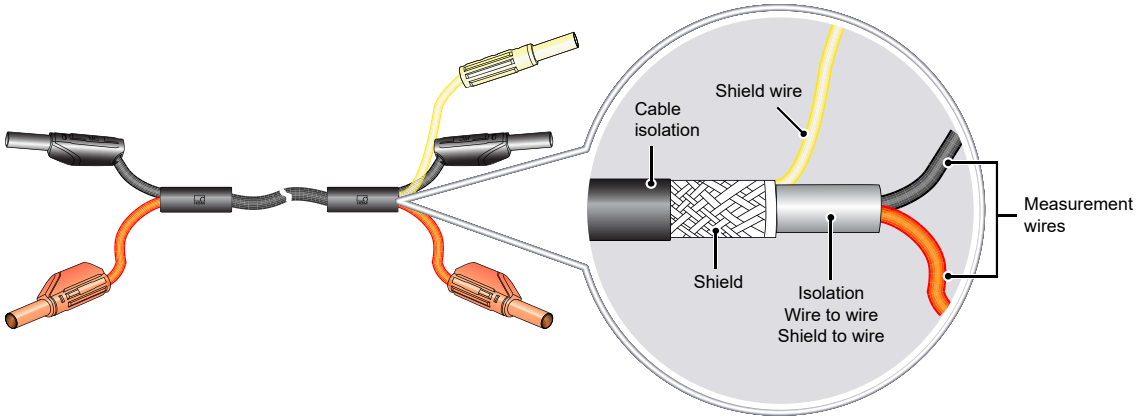


Figure 12.2: Shielded cable setup

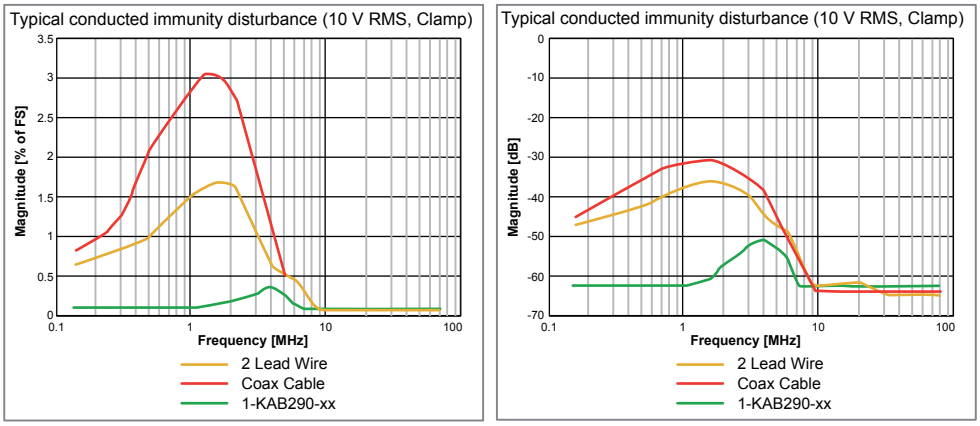


Figure 12.3: Typical conducted immunity

More KAB290 details can be found in the appendix "Measurement cables" on page 691.

- For high frequency disturbances where high bandwidth measurement is not required, the measurement bandwidth can be reduced by using the lowpass filter of the acquisition card.
- If unshielded cables are used, keep them as close together as possible, i.e. position them next to each other (to keep the loop small).
- Make sure that measurement cables that are used for measuring high dynamic or distorting signals are not closely positioned to measurement cables used for measuring small sensitive signals.
- Keep all measurement cables well separated from cables connected to high switching loads or motor cables.

- Separate measurement equipment and cables from potentially interfering equipment like frequency inverters or wireless equipment.

General cabling remark: Only use properly rated cables to measure the signal. Both the voltage and current rating should be matched to the signal for measurements.

WARNING

This instrument must be properly grounded.

When using this card, we advise using the standard GEN series protective ground connections to ensure that the entire unit is grounded.
Please see section "Connecting power" on page 72 for further details.

If connection to a protective ground is not possible for any reason, then please refer to the international safety standard EN 50191:2000

WARNING

Overvoltage and current protection

All signal inputs are protected against voltage overload. This is specified at ± 1000 V for all ranges except for the ± 1000 V range that is limited to ± 1250 V. Exceeding these limits, particularly when connected to potentially high-current sources, can cause severe damage that is not covered by the manufacturer's warranty.

WARNING

Disconnect voltages before removing the card from the system.

The measuring circuit can carry hazardous voltages and should be disconnected before the card is removed from the card slot of the measurement system.

WARNING

High voltage and qualified personnel

For measurements falling within the scope of the EN 50110-1 and EN 50110-2, please note that all cards with working voltages above 50 V AC RMS or 120 V DC may only be connected by a qualified technician or a person trained in electrical engineering and supervised by a qualified technician. (Qualified technicians are persons who, due to their specialist training, knowledge and experience, as well as their knowledge of the relevant provisions, are able to assess the work with which they are entrusted and detect possible risks and who have been nominated as qualified technicians by their employer).

WARNING

Connectors and cables

Do not use non-protected or non-shrouded connectors.
The following connectors are not safe to use with this card and must not be used (see Figure 12.4).

Figure 12.4: Unsafe connectors

The inputs on the 1kV card are compatible with the following connectors and cables (see Figure 12.5). All cables used with the 1kV card must support 1000 V DC (or 1000 V AC peak) and 600 V CAT II. All required cables and connectors can be found in the appendix “Options, to be ordered separately” on page 635 .

Figure 12.5: Safe connectors

12.2.4 Understanding the GN610B/GN611B category rating

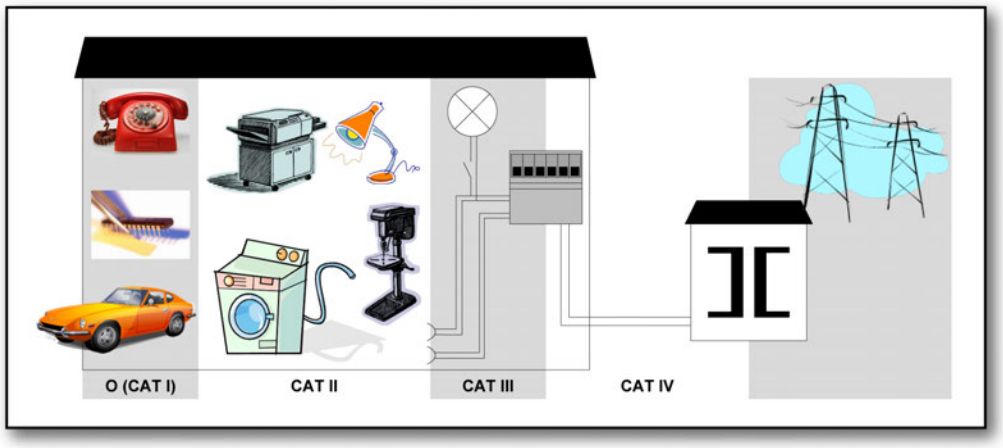


Figure 12.6: Category indication in accordance with IEC 61010-2-030:2010

Example: A measurement device is specified as 600 V CAT II, maximum input voltage 1000 V DC.

Table 12.3: Insulation test voltages in accordance with IEC 61010-2-030:2010

Nominal voltage (V RMS or V DC)	IEC 61010-2-030:2010					
	5 sec. AC test (V RMS)			Impulse test (V)		
	CAT II	CAT III	CAT IV	CAT II	CAT III	CAT IV
≤ 150	840	1.390	2.210	1.550	2.500	4.000
> 150 ≤ 300	1.390	2.210	3.310	2.500	4.000	6.000
> 300 ≤ 600	2.210	3.310	4.260	4.000	6.000	8.000
> 600 ≤ 1 000	3.310	4.260	6.600	6.000	8.000	12.000

Using the table above, it can be concluded that this specification informs the user that the device has passed the insulation tests; 5 sec at 2.210 V RMS and an impulse of 4.000 V. The maximum operating input voltage is 1000 V DC. This device is to be used to measure CAT II circuitry up to 600 V.

12.2.5 Understanding the GN610B/GN611B input

The signal input channels of the GN610B/GN611B are of the balanced type. This means that both inputs within one channel pair are exactly the same. The only difference is an opposite polarity or sign. A (simplified) schematic representation of the input channel can be found below.
The input channels are of the isolated type. This means that the input channel and amplifier are fully isolated from (earth) ground. Fully isolated in this context means a very high resistance and very small capacitive coupling to ground.

Characteristics per channel:

- The Resistance/Capacitance from each terminal to ground is identical.
- Both terminals have isolated connectors (i.e. isolated from system ground).
- The isolated ground is not externally accessible, as shown in Figure 12.7.

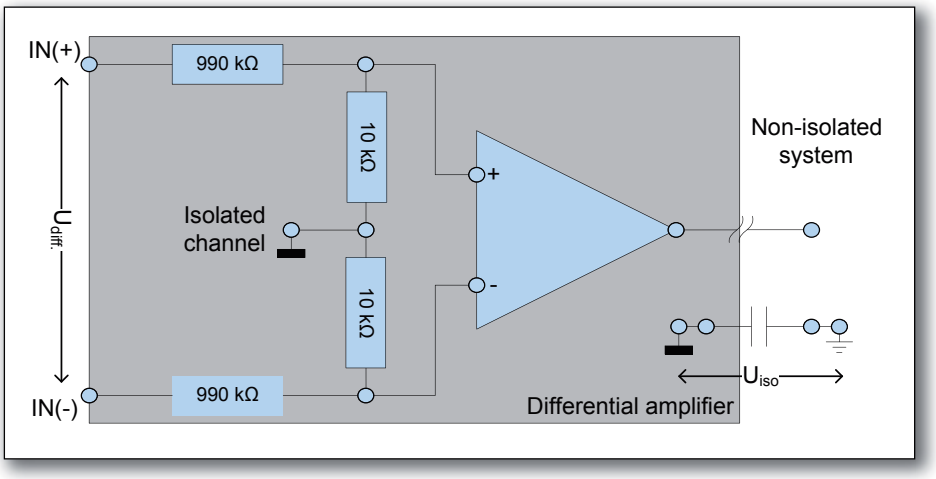


Figure 12.7: Isolated balanced input channel

(Not) using probes:
Using passive voltage probes together with balanced isolated inputs is very difficult and not recommended. The main reason for this is that there is no ground reference for the probe to divide the input voltage.

Looking at Figure 12.7, the GN610B/GN611B specifies U IN(+), U IN(-) and |Uiso| ≤ 1 kV. Using a standard passive 10:1 probe, combined with the GN610B/GN611B results in the situation shown in Figure 12.8.

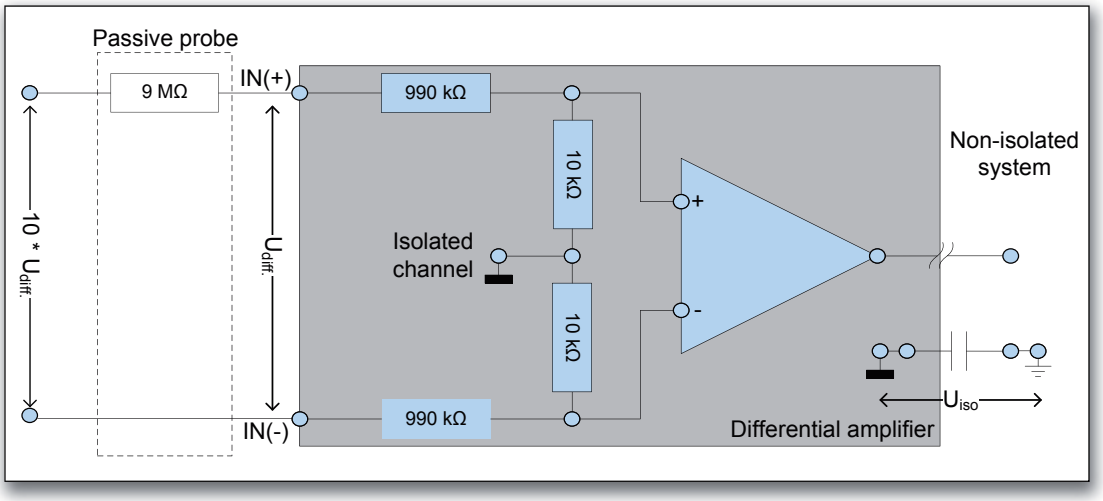


Figure 12.8: Isolated balanced input channel with passive probe

Example1:

In this setup, U IN(-) is not divided, so it is required that |U IN(-)| ≤ 1 kV. Assuming that U IN(-) is connected to 0 V, the voltages at U_{iso} and U IN(+) can be calculated:

Assuming:	U IN(-) = 0V 10:1 probe used, probe input voltage applied is 10* U_{diff}
Results in:	U IN(+) = 10 * U_{diff} / 11M * 2M = 1.82 * U_{diff} U_{iso} = 10 * U_{diff}/ 11M * 1M = 0.91 * U_{diff}

Due to the 2 MΩ impedance between U IN(+) and U IN(-), the probe does not divide by 10, but by 5.5 (10 / 1.82). So if the maximum specified U_{diff} of 1 kV is considered, this smaller division factor results in the U IN(+) level being way above the channels specification.

Example2:

Since U IN(-) is not divided, there are very strict consideration on how signals can be attached. Assume the U IN(+) and U IN(-) are reversed by accident. We can calculate U_{iso} and U IN(-).

Assuming:	U IN(-) = 10 * U_{diff} U IN(+) = 0 V
Results in:	U_{iso} = 10 * U_{diff} / 11M * 10M = 9.1 * U_{diff}

If the maximum specified U_{diff} of 1 kV is considered, both U IN(-) and U_{iso} are way above the channels specification.

12.2.6 Using the High Precision Differential Probe

Figure 12.9: High Precision Differential Probe (HDP)

The High Precision Differential Probe is designed to reduce the resistive/current load on the device under test by increasing the input impedance to 10 MΩ with 0.2% inaccuracy. The use of the 10:1 divider reduces the lowest user range to ± 0.1 V. The highest input range is ± 1000 V due to the maximum voltage rating of the probe.

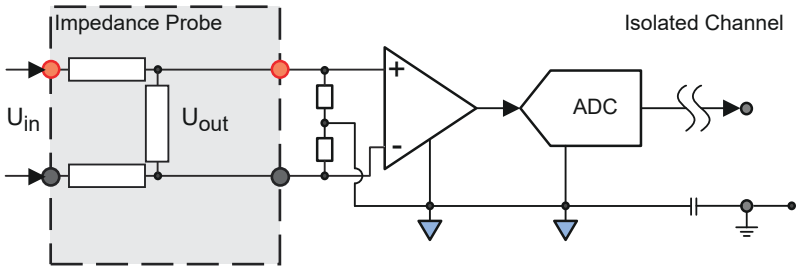


Figure 12.10: High Precision Differential Probe concept

Different to standard probes the HDP uses a balanced input divider, that matches both the resistive and capacitive characteristics of the GN610B/ GN611B acquisition cards. Therefore users do not need to perform probe compensations before using this probe.

Standard this probe uses a divide by 10 input stage. Either use the Perception Sensor Database to apply the correct probe or use a technical unit multiplier 10 to scale the channels input sensitivity to match the attached probe.

IMPORTANT

Although the HDP probe uses a divide by 10 factor, the highest available input range is not scaled by a factor of 10. The HDP is not specified to be used above 1000 V RMS. So both highest input range and maximum isolation voltages are unchanged when using the HDP probe together with the GN610B/GN611B acquisition cards.

To increase the maximum input range of the GN610B/GN611B input card a similar HDP probe concept can be used. However as the channels are NOT connected to earth the isolation specification of 1000 V RMS will not be increased by such a probe design. Extra care must be taken to prevent over voltages on the input pins of the GN610B/GN611B acquisition cards.

It is recommended to use the following approach:

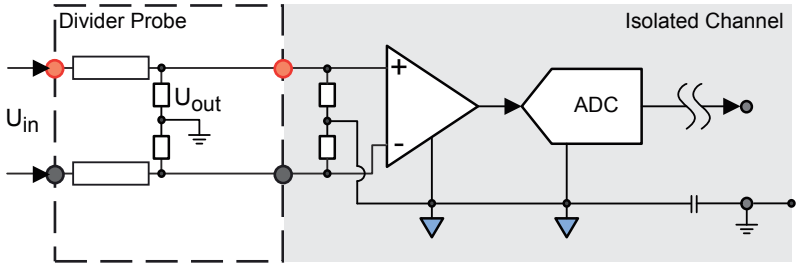


Figure 12.11: Differential Probe concept with common mode divider

In this setup the output of the probe is dividing the input U_{in} to earth on both inputs.

WARNING

Make sure when using such a probe the U+ and U- of the GN610B/GN611B channel never exceeds the specification of 1000 V DC.

IMPORTANT

This probe concept increases the input voltage levels while maintaining the protection of the GN610B/GN611B acquisition cards. Care must be taken that the full isolated measurement is lost as the probe is attached to earth. It's recommended to use high impedance series resistors to keep both the current load on the device under test low as well as any potential ground loop currents low.

12.2.7 Measuring currents

The GN610B/GN611B acquisition cards do not support direct current measurements. The use of current shunts, current clamps and/or current transducers is required to measure currents.

A typical setup could look like this:

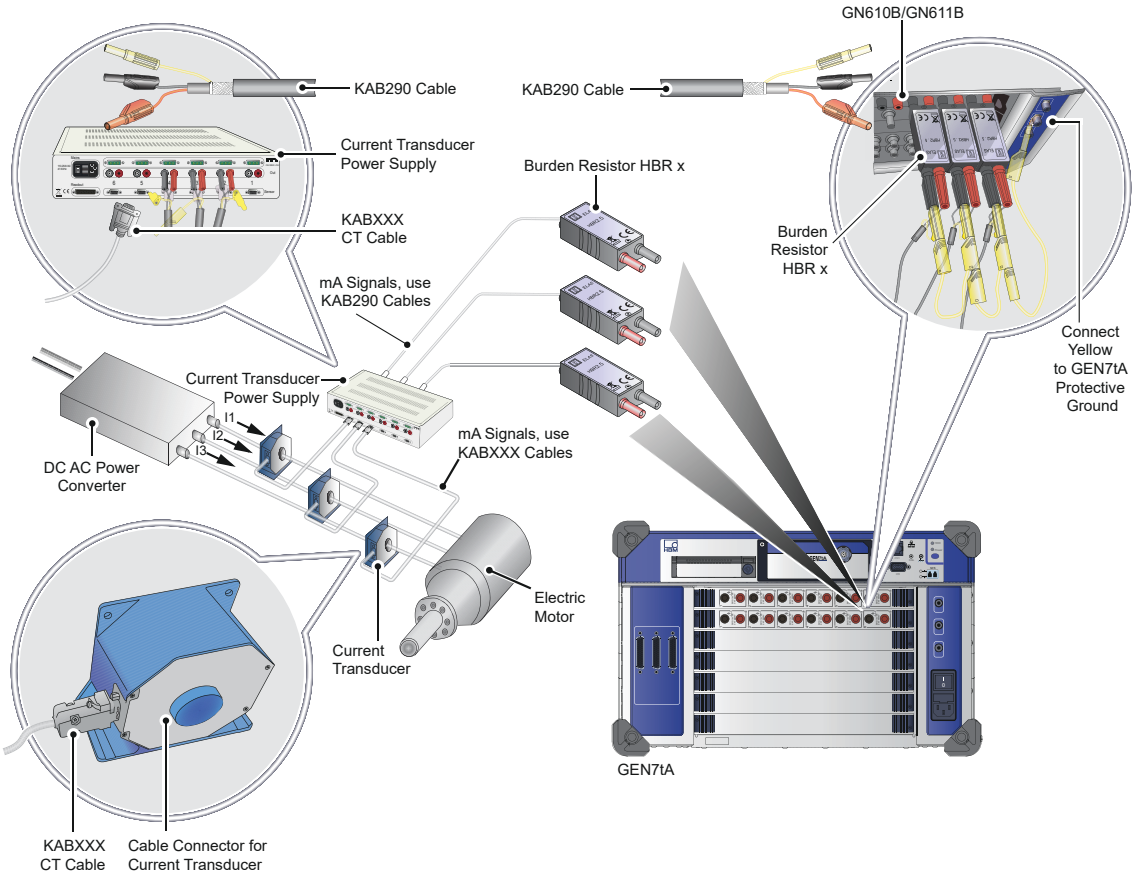


Figure 12.12: Current transducer connection diagram

All required accessories, can be found in the appendix “Card Options, to be ordered separately” on page 644.

12.2.8 GN610B/GN611B Isolation and type testing

An overview of the GN610B/GN611B card isolation and input is shown below (see Figure 12.13). The isolation of the channel to chassis is 1000 V RMS and is also qualified as 600 V CAT II (or 300 V CAT III). The common mode of the differential input channel (isolated GND) can be 1000 V RMS with respect to the chassis. If one channel has its common mode at +1000 V and one at -1000 V (with respect to chassis), the voltage between the two channels is 2000 V. The standards at which the card is certified is IEC61010-1:2010 and IEC61010-2-030:2010.

Isolation	
Input signal to chassis	1000 V RMS, 600 V CAT II (REINFORCED)
Channel to chassis	1000 V RMS, 600 V CAT II (REINFORCED)
Channel to channel	2000 V RMS, (BASIC)

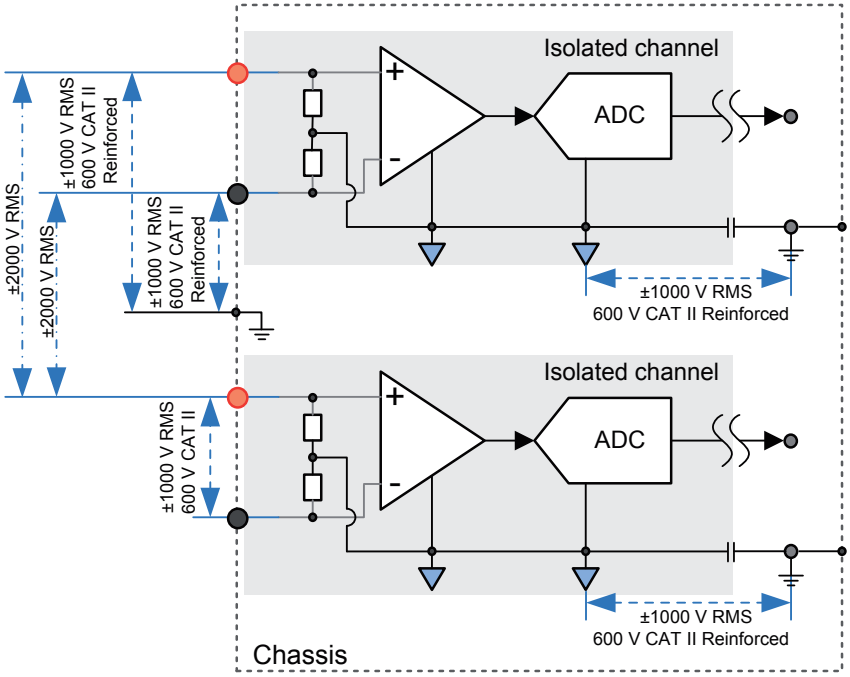


Figure 12.13: Isolation 1kV card overview

- The isolation between the channel and chassis is classified as **REINFORCED**. This can be seen as double isolation, which is necessary because the chassis might be accessible (conductive parts can be touched) to users (personal safety).
- Isolation between channels is **BASIC**, since a channel is not accessible. Therefore, there is no direct risk to users (product safety).
- **REINFORCED** or **DOUBLE** isolation has higher test values than **BASIC** isolation.

Channel to chassis isolation test

To qualify the isolation as 1000 V RMS and 600 V CAT II (REINFORCED), certain tests are performed on some cards during the engineering design qualification phase. These tests are known as type tests. These tests are described in the IEC61010-1:2010 and IEC61010-2-030:2010 standards. The principle of the tests is described below.

For the isolation barrier test, both the DC and AC tests below (see Figure 12.14 and Figure 12.15) are used with DC voltage √2 higher than the AC voltage. The test value meets the requirements for 600 V CAT II REINFORCED. The test value for 1000 V RMS is lower and therefore also covered by this test. Tests are conducted for one minute. For details, please refer to IEC61010.

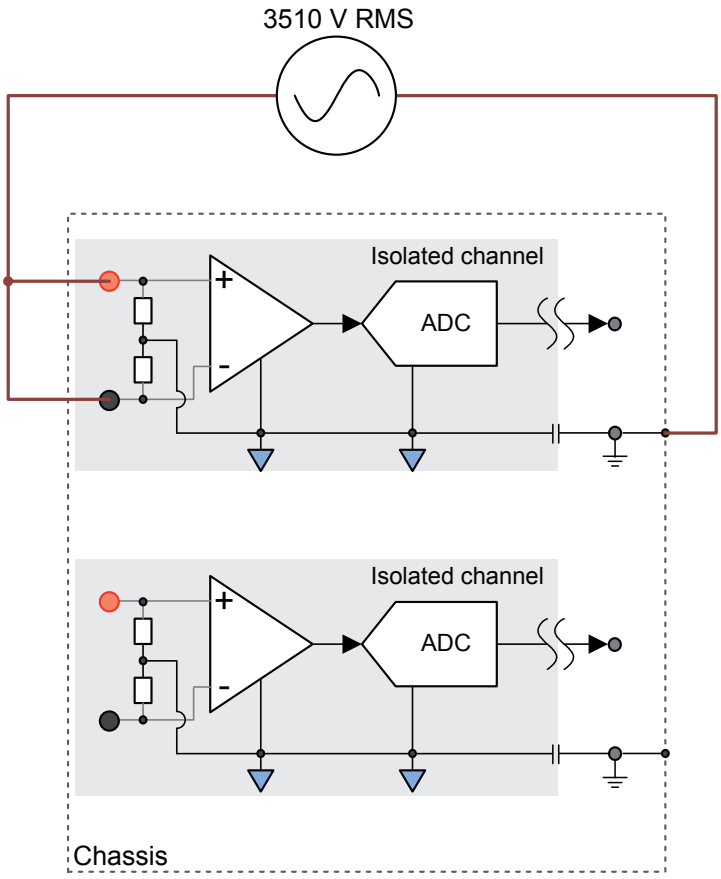


Figure 12.14: AC type test channel to chassis

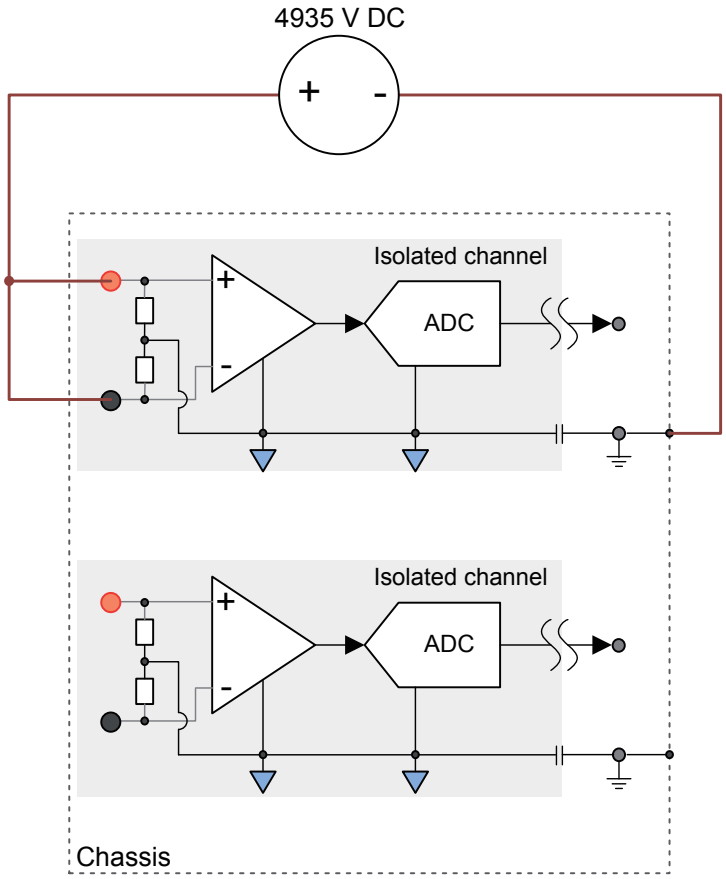


Figure 12.15: DC type test channel to chassis

Channel to channel isolation test

For the channel to channel test, both the DC and AC tests below (see Figure 12.16 and Figure 12.17) are used with DC voltage √2 higher than the AC voltage. The test value meets the requirements for 600 V CAT II REINFORCED. The value for 2000 V RMS BASIC is lower and therefore also covered by this test. Tests are conducted for one minute. For details, please refer to IEC61010-1.

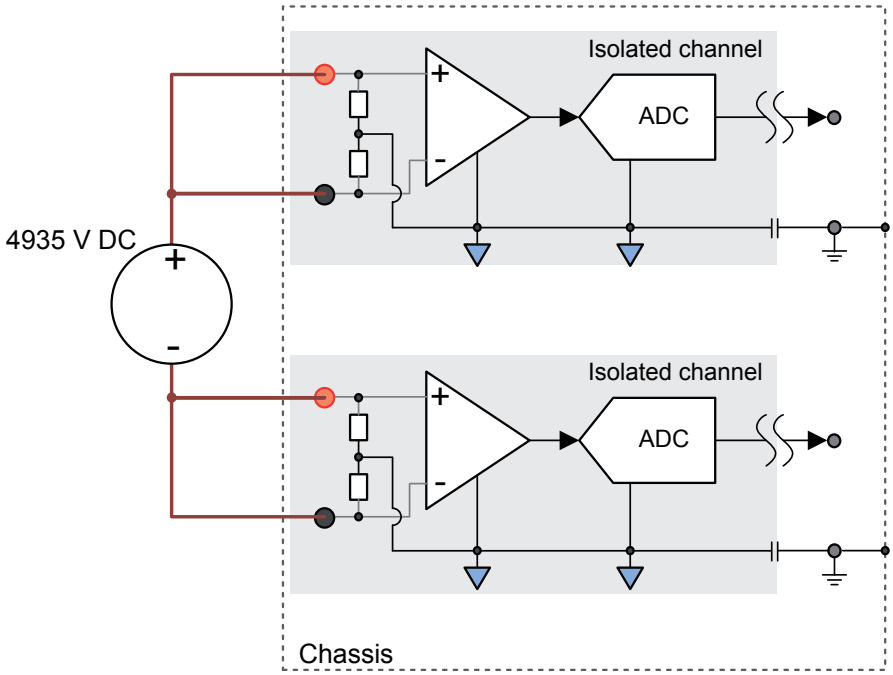


Figure 12.16: DC type test channel to channel

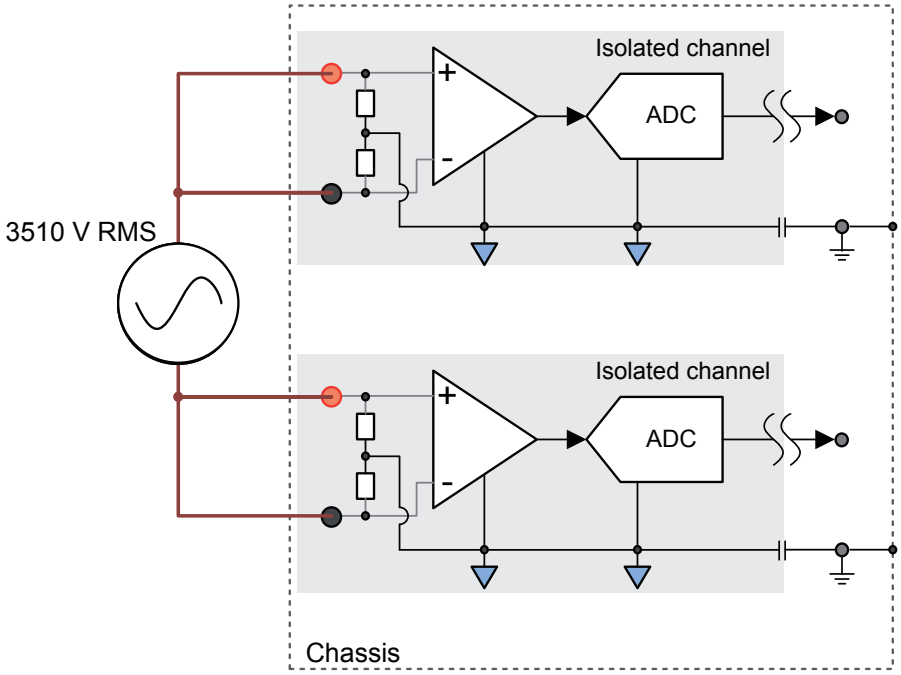


Figure 12.17: AC type test channel to channel

High potential test

The type tests are performed on a selection of cards to test the design. Every card produced undergoes a production test to verify that the card has been designed correctly and that the card is safe. The tests are called “hipot” (high potential) tests (see Figure 12.18 and Figure 12.19).

The test are performed in two steps to make sure that the channels that are side by side on the card can withstand the high potential voltages.

1 The inputs of Channel 1, 3 and 5 are tested using a 1500 V RMS common mode signal with signal negative attached to chassis ground and the inputs of Channel 2, 4 and 6 all connected to chassis ground.
2 The inputs of Channel 2, 4 and 6 are tested using a 1500 V RMS common mode signal with signal negative attached to chassis ground and the inputs of Channels 1, 3 and 5 all connected to chassis ground.

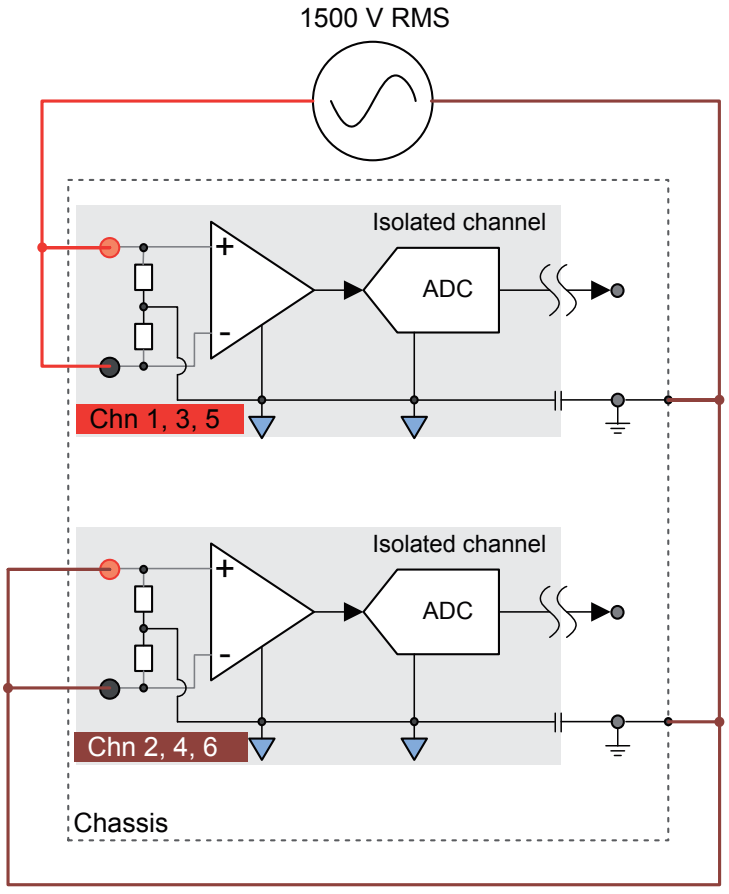


Figure 12.18: Hipot testing Channels 1, 3 and 5

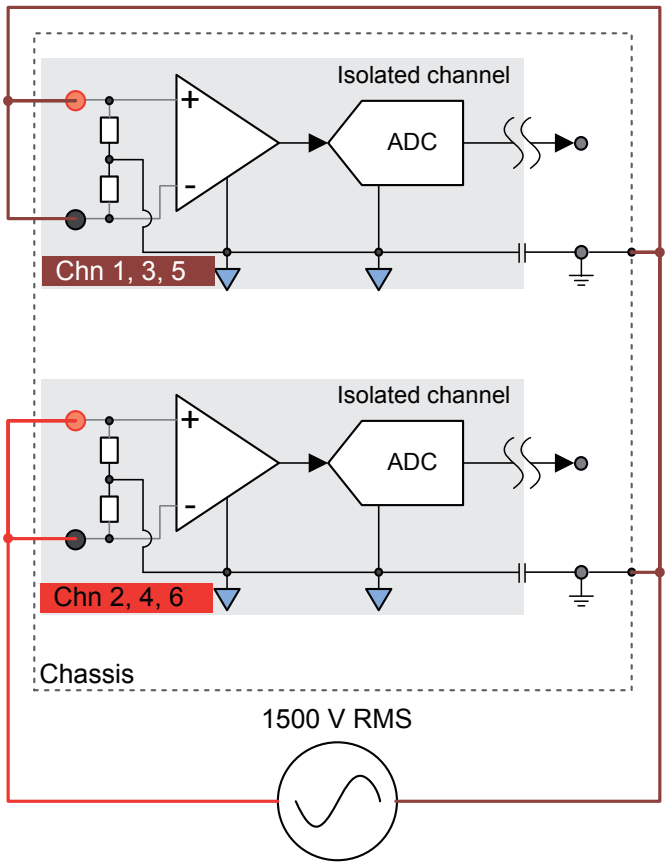


Figure 12.19: Hipot testing Channels 2, 4 and 6

Engineering tests

Besides the type tests and the production tests, HBM has also performed several engineering tests to verify the robustness of the design during the engineering design qualification phase.

Component tests

Every component crossing the isolation barrier is tested and/or examined to make sure it will pass the type test. The test voltage used is the same high voltage DC that is used for the type tests, as well as an additional impulse voltage of up to 6 kV. The test voltage uses a 1.2 µs rise time and an amplitude reduction of 50% of the maximum peak voltage in 50 µs after the peak has been reached.

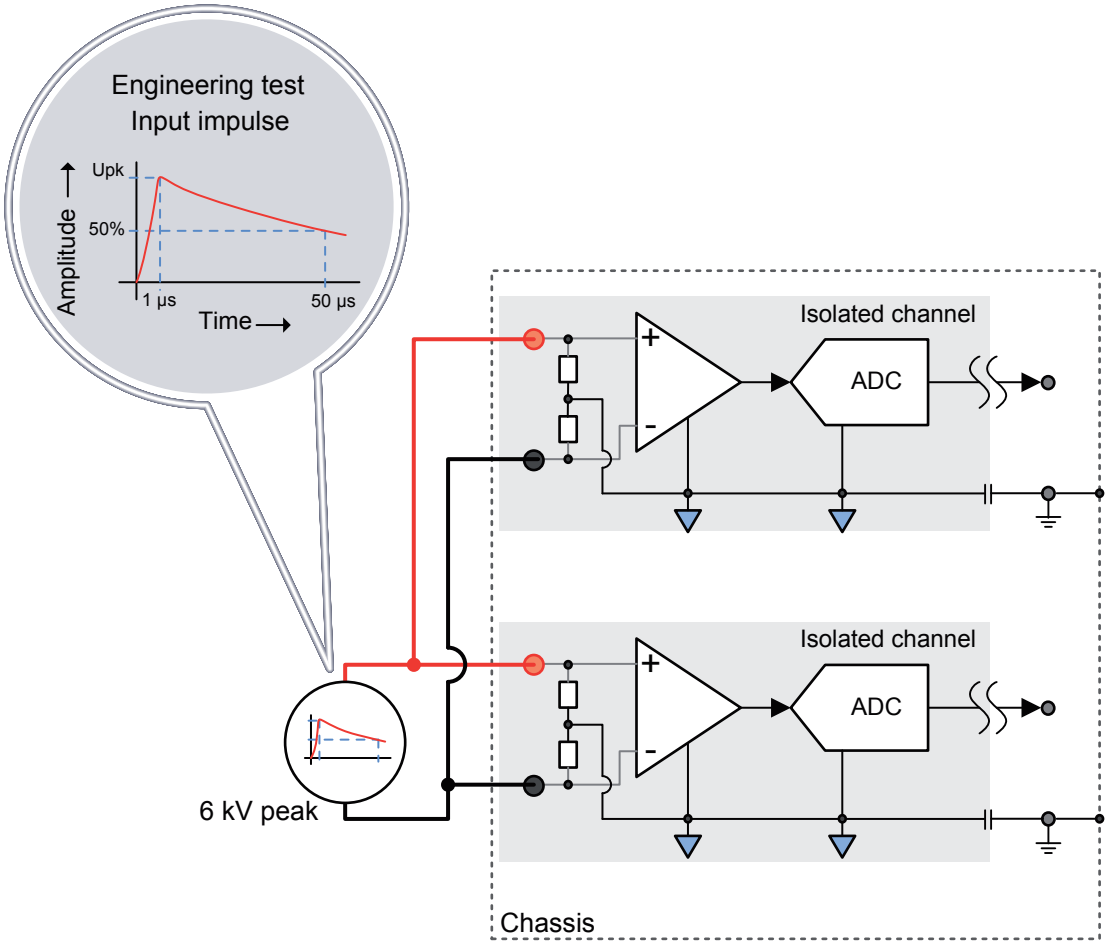


Figure 12.20: Example of 1.2/50 µs impulse

Active input switch test

To guarantee the stability of the channels, the input relays are tested with the maximum input voltage (1000 V) applied. The inputs of the channels have been switched from isolated GND to DC by the input relay, resulting in the 1000 V being applied to the input as a step pulse.

This test is performed with the highest input range (± 1000 V) and repeated with the lowest input range (± 20 mV). Both tests are performed with an input voltage of 1000 V and repeated over 1000 times. These tests have all passed successfully.

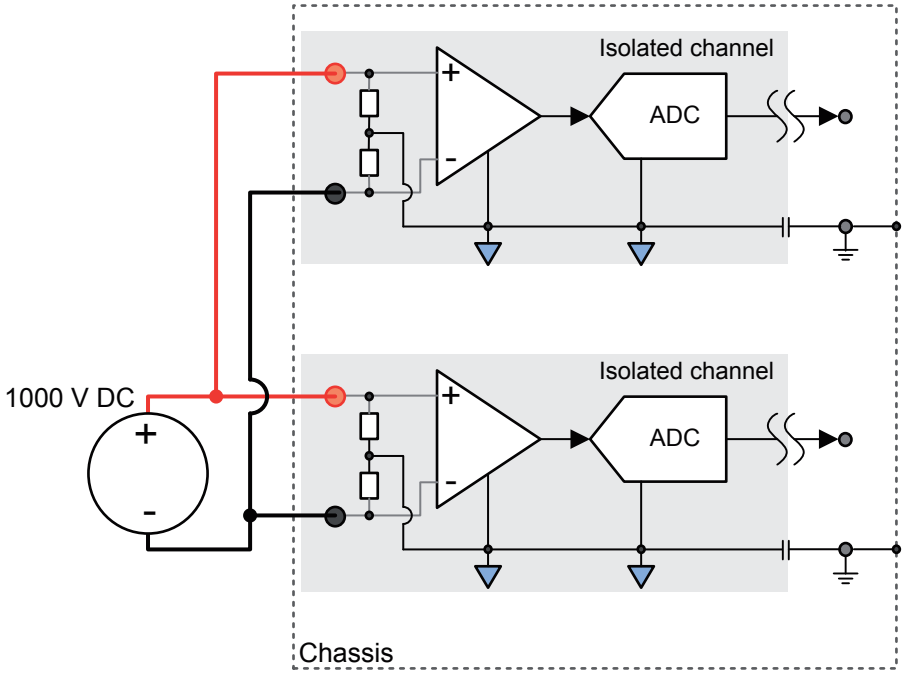


Figure 12.21: Engineering input switching test

12.2.9 GN610B/GN611B protection mechanisms

Overvoltage and current protection

All signal inputs are protected against voltage overload. This is specified at ± 1000 V for all ranges, except for the ± 1000 V range that is limited to ± 1250 V. Exceeding these limits can damage the input card.

GN610B/GN611B input overload protection

The input section has several methods to protect against voltage overload on the input.

Every selected input range allows a 200% overload without any change of input resistance or auto ranging. This 200% overrange is designed to allow for smaller voltage overloads without affecting the measurement. Within this 200% overload, the amplifier is also able to respond with normal rise/fall times and the signal is restored within the standard selected range.

When exceeding the 200% overload, the input impedance might start to increase. The impedance increase lowers the input current. A positive side effect of the lowered current is that the dissipated heat is lowered. It is the excessive heat dissipation that typically damages the input channel.

The first action of the system is to add an additional current load to the input signal to create an extra voltage drop in the input series resistance. The resulting additional current depends on several factors and is therefore unpredictable. A negative side effect of this additional current is that the extra power is dissipated in the input section, which in turn results in additional heat dissipation.

Secondly, the input section starts switching to disconnect itself from the input signal to reduce the power dissipated within the lower ranges of the amplifier (≤ ± 5 V ranges).

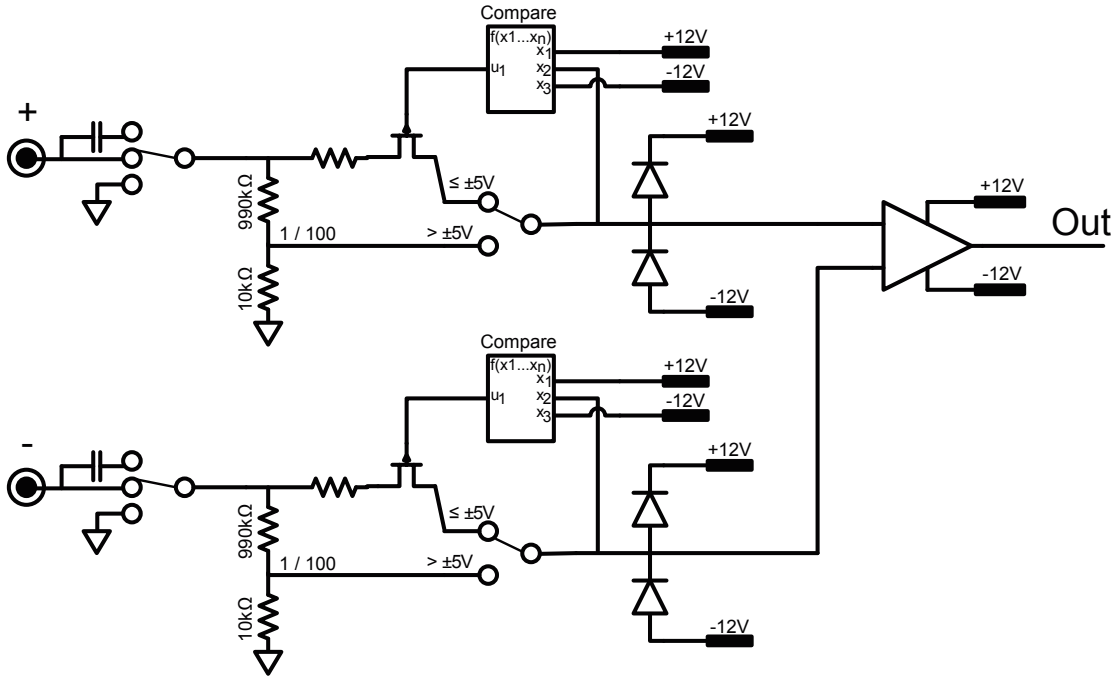


Figure 12.22: Input overload protection - Schematic diagram

Thermal monitor of the input channels
Any overload results in extra heat being generated within the channel. The extra heat is the result of the extra current flowing through the input resistance. The extra heat is also caused by internal amplifier sections driving their local output to maximum levels, which creates excessive heating within the amplifier.

As a third protective mechanism, every input is equipped with a thermal sensor to monitor the local temperature. When the local temperature reaches maximum levels, the system automatically starts changing the input range that has been selected by the user to reduce the dissipated heat. As the heat dissipation does not start the auto ranging immediately, short overloads do not result in auto ranging. A longer overload leads to a higher local temperature, which starts the auto ranging process.

Whenever an overload pushes local temperature to exceed the maximum level, the input range is adapted to a range that is less sensitive by a factor of ten. For example, if the user has selected a range of ± 40 mV and it is necessary, the system changes the range to ± 400 mV. As this might not be enough due to an even higher overvoltage, the system keeps monitoring the local temperature. If the local temperature is not reduced within the expected response time, the system automatically increases the input range by a factor of 10 for a second or third time or however many times it requires to reach safe conditions that do not increase the local temperature anymore.

Every one of the automatic range changes is identified within the measurement data. Not only is the measured input scaled with the adapted input range correctly, but the exact moment when the automatic range change happens is also identified within Perception software.

As the highest range that can be selected, ± 1 kV is the ultimate protection for the system to disconnect the input from the external signal source. This step is only executed if the system is in the ± 1 kV range and the local temperature is still outside maximum operating limits. Disconnecting from the external signal source is done by grounding the input. When inputs are grounded, the only connections to the external signal are the input connectors and the input pin of the ground relay.

Thermal shutdown in critical conditions

This protective scheme allows for any overload that the input could be confronted with during normal operation. For any other failure that could result in excessive heat dissipation, the GEN series probes have a last protective stage built in. When local temperatures reach critical limits, the system automatically turns off the mains power to prevent damage to the system or other systems near the GEN series system. Maximum and critical temperatures are defined as such that it is very unlikely the system would ever reach these critical temperatures when operating within its specified conditions.

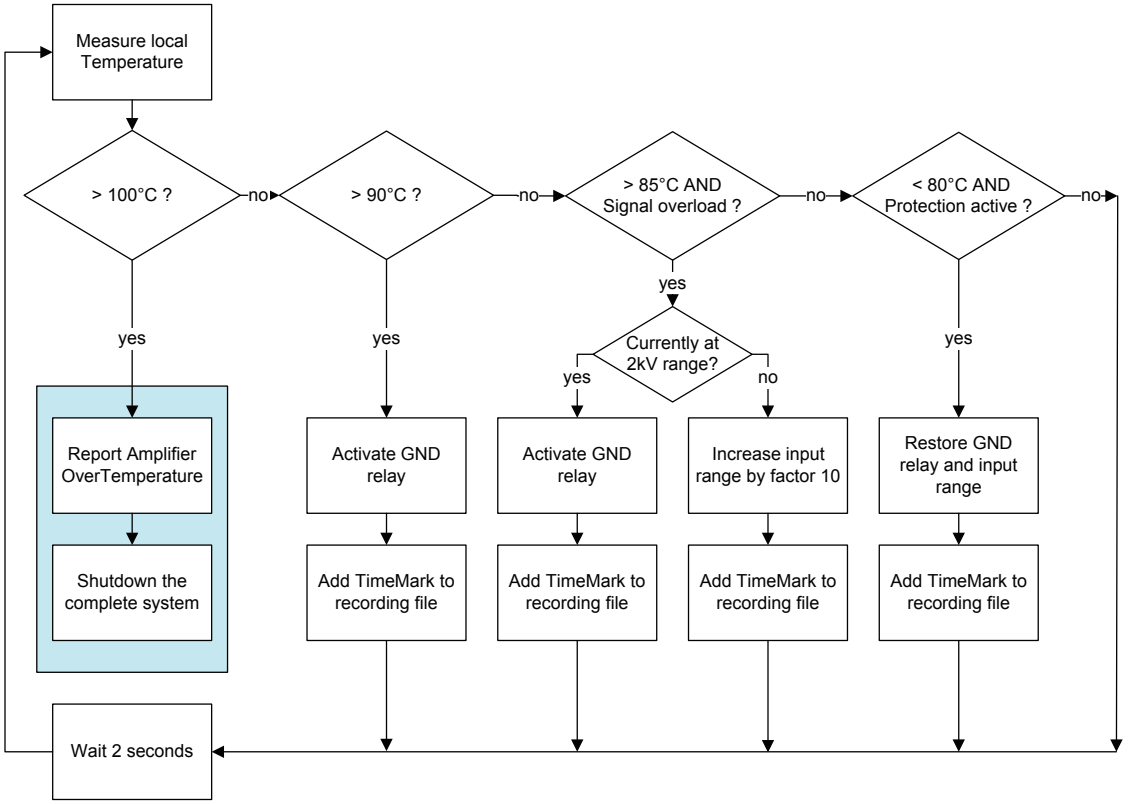


Figure 12.23: Automatic thermal overload response

Restore range selected by user automatically

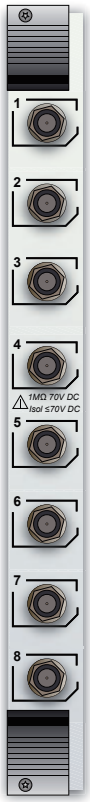
As the GEN series system is designed to measure 24 hours a day, 7 days a week, the automatic range switching has the negative side effect of reducing the sensitivity of the amplifier. During the actual overload, the channel is unable to measure the input signal. Therefore, there are no extra negative side effects. If the overload disappears and the system runs unattended, the input range that is selected automatically will not be the best measurement range. Therefore, the amplifier "remembers" the range that the user originally selected and restores this range as soon as regular thermal conditions are restored. A temporary large overload will then only result in input sensitivity that is adjusted temporarily.

The automatic range adaptation is started due to thermal conditions typically as a result channel input overload. Therefore, the overload might still be present. If this is the case the automatic range restore restarts, the thermal increase and leads to re-trigger the automatic range adaption process and the overload is handled exactly the same way as before.

If the overload is permanent, the system keeps on automatic ranging to reduce the dissipated heat. The system then restores the range selected by the user, causing overheating again and thereby restarting the automatic ranging process again. This cycle will repeat forever until the overload condition disappears.

12.3 Isolated Basic/IEPE cards

12.3.1 GN815, Isolated Basic/IEPE 2MS/s input card

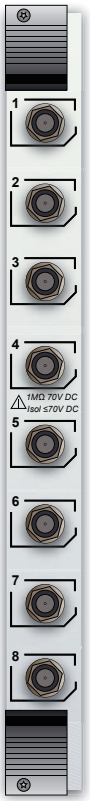


- IEPE transducer support
- TEDS Class 1 support for IEPE
- Isolated, unbalanced differential inputs
- ± 10 mV to ± 50 V input range
- Analog/digital anti-alias filters
- 18 bit at 2 MS/s sample rate
- 8 analog channels
- 2 GB memory
- Isolated metal BNC per channel
- Real-time cyclic calculators
- Triggering on real-time results
- Digital Event/Timer/Counter support
- 1 kV RMS CAT II probe
- 1 kV RMS differential probe
- Current clamps and burdens

The GEN DAQ Basic/IEPE ISO 2 MS/s Input Card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or probes and current clamps.
This card also supports IEPE transducers and TEDS Class 1 for easy setup of the acquisition channels. Built-in diagnostics supports automatic sensor connected, open or shorted detection.
The amplifier provides voltage inputs from ± 10 mV to ± 50 V. Optimum anti-alias protection is achieved by the 7-pole analog anti-alias filter combined with a fixed 2 MS/s sampling Analog-to-Digital converter. The digital filters operating at the full ADC sample rate offer a large range of high order anti-alias filter characteristics with precise phase match and noise-free digital output.
For true real-time analysis, the card offers real-time cycle or timer based calculations. Automatic zero crossing detection allows for asynchronous true RMS, mean and other calculations that can be used to trigger the recording.
The GEN DAQ series input card offers 16 digital input events, two digital output events and two Timer/Counter channels.
Using voltage probes a single-ended 600 V RMS CAT III / 1000 V CAT II or a differential 1000 V RMS CAT III (1000 V RMS common mode) measurement range is created. The use of current clamps and external burdens allow for direct current measurements.

For specification and ordering information, please refer to "B03997_02_E00_00 (GEN series GN815)" on page 450.

12.3.2 GN816, Isolated Basic/IEPE 200kS/s input card



- IEPE transducer support
- TEDS Class 1 support for IEPE
- Isolated, unbalanced differential inputs
- ± 10 mV to ± 50 V input range
- Analog/digital anti-alias filters
- 18 bit at 200 kS/s sample rate
- 8 analog channels
- 200 MB memory
- Isolated metal BNC per channel
- Real-time cyclic calculators
- Triggering on real-time results
- Digital Event/Timer/Counter support
- 1 kV RMS CAT II probe
- 1 kV RMS differential probe
- Current clamps and burdens

The GEN DAQ Basic/IEPE ISO 200 kS/s Input Card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or probes and current clamps.
This card also supports IEPE transducers and TEDS Class 1 for easy setup of the acquisition channels. Built-in diagnostics supports automatic sensor connected, open or shorted detection.
The amplifier provides voltage inputs from ± 10 mV to ± 50 V. Optimum anti-alias protection is achieved by the 7-pole analog anti-alias filter combined with a fixed 2 MS/s sampling Analog-to-Digital converter. The digital filters operating at the full ADC sample rate offer a large range of high order anti-alias filter characteristics with precise phase match and noise-free digital output.
For true real-time analysis, the card offers real-time cycle or timer based calculations. Automatic zero crossing detection allows for asynchronous true RMS, mean and other calculations that can be used to trigger the recording.
The GEN DAQ series input card offers 16 digital input events, two digital output events and two Timer/Counter channels.
Using voltage probes a single-ended 600 V RMS CAT III / 1000 V CAT II or a differential 1000 V RMS CAT III (1000 V RMS common mode) measurement range is created. The use of current clamps and external burdens allow for direct current measurements.

For specification and ordering information, please refer to "B03998_02_E00_00 (GEN series GN816)" on page 472.

12.3.3 Using the GN815 and GN816

WARNING

High bandwidth and measurement cabling

Due to the high bandwidth measurement capabilities of the acquisition card, combined with the high measurement sensitivity of the card, it is important to pay close attention to the measurement cabling.

Some advice to prevent measuring unwanted disturbances:

- Keep measurement cables as short as possible in order to reduce the reception of environmental disturbances.
- Use shielded cables. The cable should have the measurement cables paired inside a shield. Preferably, the shield should be connected to the chassis of the measurement Genesis High Speed equipment. Alternatively, the shield could also be connected to the chassis of the object under test.

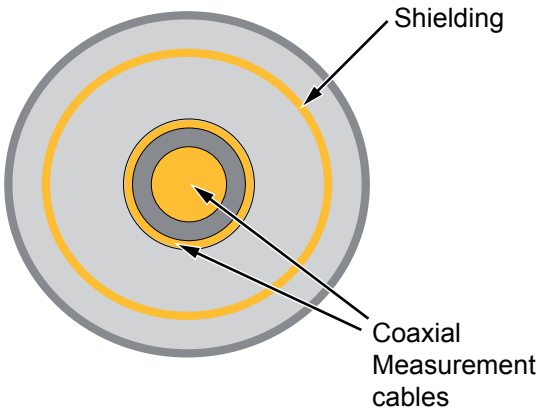


Figure 12.24: Shielded cable

- For high frequency disturbances where high bandwidth measurement is not required, the measurement bandwidth can be reduced by using the lowpass filter of the acquisition card.
- If unshielded cables are used, keep them as close together as possible, i.e. position them next to each other (to keep the loop small).
- Make sure that measurement cables that are used for measuring high dynamic or distorting signals are not closely positioned to measurement cables used for measuring small sensitive signals.

- Keep all measurement cables well separated from cables connected to high switching loads or motor cables.
- Separate measurement equipment and cables from potentially interfering equipment like frequency inverters or wireless equipment.

General cabling remark: Only use properly rated cables to measure the signal. Both the voltage and current rating should be matched to the signal for measurements.

WARNING

This instrument must be properly grounded.

When using this card, we advise using the standard GEN series protective ground connections to ensure that the entire unit is grounded.
Please see section "Connecting power" on page 72 for further details.

If connection to a protective ground is not possible for any reason, then please refer to the international safety standard EN 50191:2000

WARNING

Overvoltage and current protection

The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is inactive as long as the input voltage is less than 200% of the selected input range.

WARNING

Disconnect voltages before removing the card from the system.

The measuring circuit can carry hazardous voltages and should be disconnected before the card is removed from the card slot of the measurement system.

WARNING

Connectors and cables

The specified ± 50 V DC voltage range of the Isolated Basic acquisition card is such that it falls below the low voltage limit as specified in IEC61010.

The limit for safe voltage and currents is set in the IEC61010-1 standard in Section 6.3 – limit values for accessible parts. The limits are:

Table 12.4: Limit for safe voltage and currents is set in the IEC61010-1

	Normal operation	Single fault condition
Voltage	70 V DC	140 V DC
	33 V RMS	55 V RMS
	46.7 V peak	78 V peak
Current	2 mA DC	15m A DC
	0.5 mA RMS	3.5m A RMS
	0.7 mA peak	5 mA peak

It is good practice to use isolated measurement cables. However, since the voltage range of the Isolated Basic card falls below the low voltage limit for accessible parts, non-protected or non-shrouded connectors can also be used with this card.

Figure 12.25: Safe connectors for use with Isolated Basic acquisition cards

12.3.4 Understanding the GN815 and GN816 isolation

The specified ± 50 V DC voltage range of the Isolated Basic acquisition card is such that it falls below the low voltage limit as specified in IEC61010.

The isolation of the Isolated Basic card (GN815 and GN816) is in line with the limit for safe voltage and currents as mentioned above.

Table 12.5: Limit for safe voltage and currents (GN815 and GN816)

Input signal to input signal	± 140 V DC, 55 V RMS (low voltage limit)
Input signal-to-chassis	± 70 V DC, 33 V RMS (low voltage limit)
Channel to chassis	± 70 V DC, 33 V RMS (low voltage limit)
Channel to channel	± 70 V DC, 33 V RMS (low voltage limit)
Nondestructive, to chassis (earth)	± 70 V DC, 33 V RMS AC (low voltage limit)

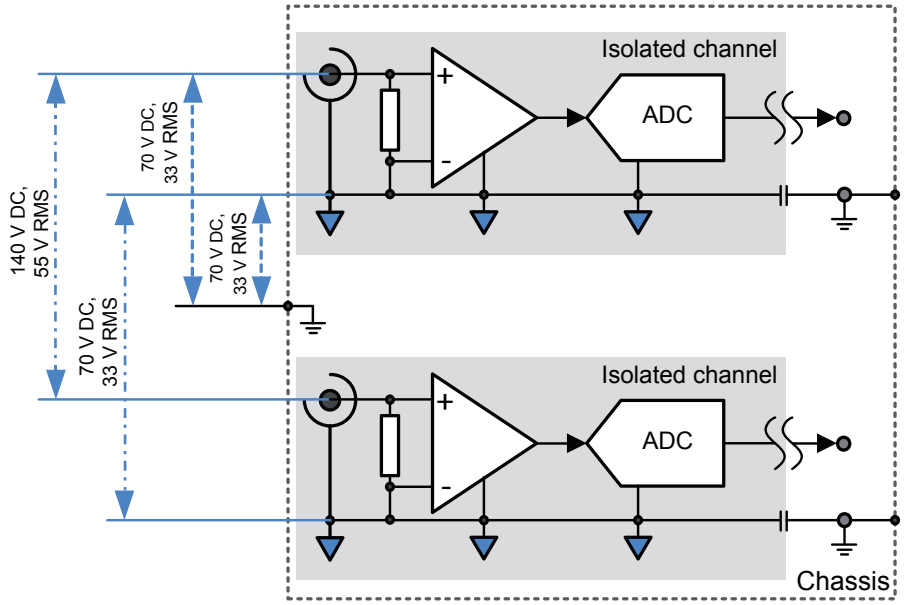


Figure 12.26: Isolation of the Isolated Basic card (GN815/GN816)

12.3.5 Understanding the GN815 and GN816 input

The isolation of the GN815's and GN816's signal input channels are single-ended (also termed unbalanced isolated or unbalanced differential isolated).

This means that one signal of both inputs within one channel pair is directly connected to the isolated channel ground (this is the outer signal of the BNC plug). The other signal is connected to the conditioning amplifier.

A (simplified) schematic representation of the input channel of the GN815 and GN816 can be found below.

The input channels of the GN816 and GN816 are isolated. This means that the input channel and amplifier are fully isolated from (earth) ground. In this context, fully isolated means a very high resistance and a very small capacitive coupling to ground. This is for safety and to avoid ground loops.

Characteristics per channel:

- The input BNC connector is isolated from the system ground.
- The isolated ground is externally accessible, as shown in Figure 12.27.

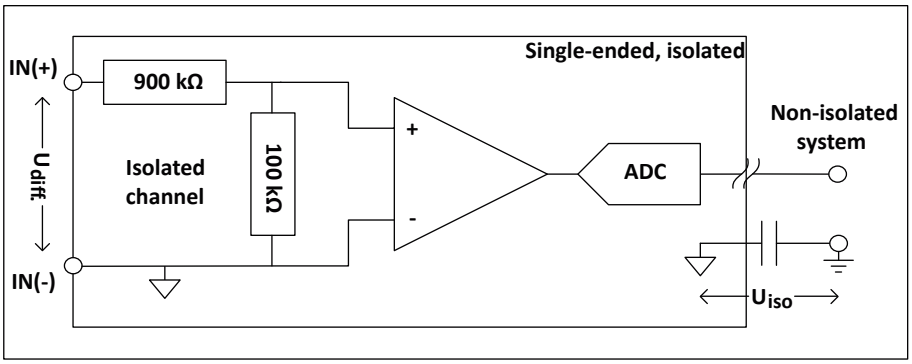


Figure 12.27: Single-ended isolated input channel

Using probes:

It is possible to use passive voltage probes with single-ended isolated inputs.

Using a standard passive 10:1 probe in combination with the GN815 and GN816 results in the situation shown in Figure 12.28.

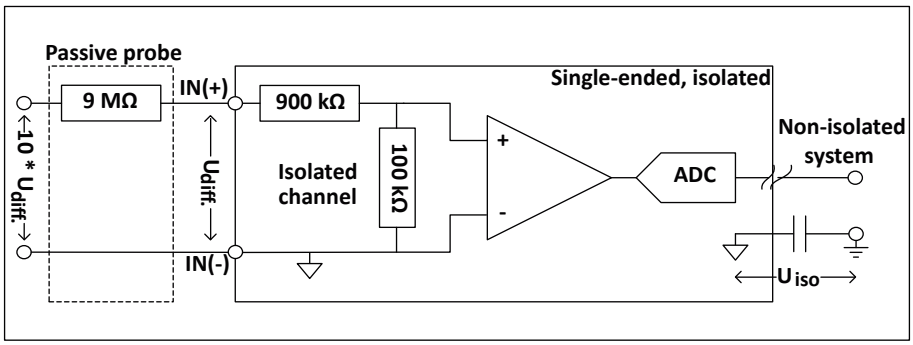


Figure 12.28: Input channel with a standard 10:1 passive probe

Using a high voltage passive 10:1 probe in combination with the GN815 and GN816 results in the situation shown in Figure 12.29. The voltage division is done externally in the probe to maintain accuracy.

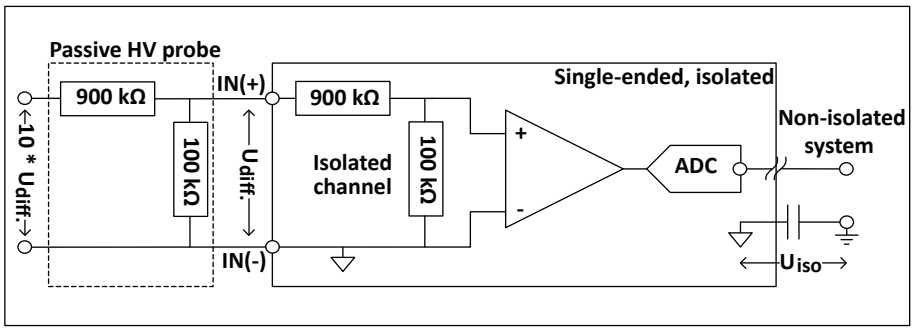


Figure 12.29: Input channel with a high voltage 10:1 passive probe

12.3.6 GN815 and GN816 Input overload protection

The input section has several methods to protect against voltage overload on the input.

Every selected input range allows a 200% overload without any change of input resistance or auto ranging. This 200% overrange is designed to allow for smaller voltage overloads without affecting the measurement. Within this 200% overload, the amplifier is also able to respond with normal rise/fall times and the signal is restored within the standard selected range.

When exceeding the 200% overload, the input channel might start to take protective actions.

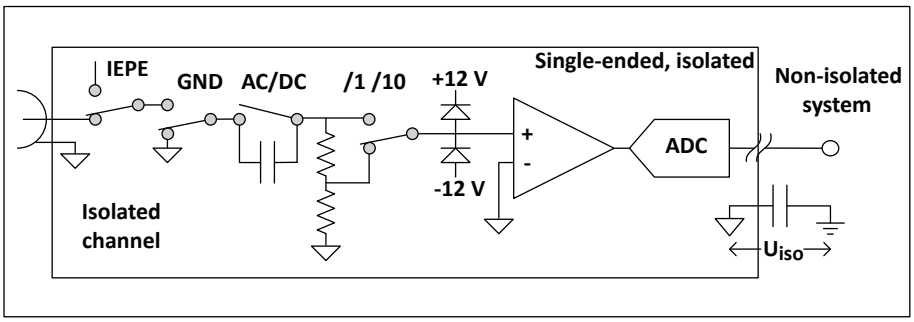


Figure 12.30: Input overload protection - Schematic diagram

The **first** action of the system is to add an additional current load to the input signal to create an extra voltage drop in the input series resistance. The resulting additional current depends on several factors and is therefore unpredictable. A negative side effect of this additional current is that the extra power is dissipated in the input section, which in turn results in additional heat dissipation.

Thermal monitor of the input channels
Any overload results in extra heat being generated within the channel. The extra heat is the result of the extra current flowing through the input resistance. The extra heat is also caused by internal amplifier sections driving their local output to maximum levels, which creates excessive heating within the amplifier.

The **second** action of the system is to react to the increased temperature in the channel as a result of the overvoltage. Every input is equipped with a thermal sensor to monitor the local temperature. When the local temperature reaches maximum levels, the system automatically starts changing input range selected by the user to reduce the dissipated heat. As the heat dissipation does not start the auto ranging immediately, short overloads do not result in auto ranging. A longer overload leads to higher local temperature, which starts the auto ranging process. The system automatically increases the input range for as many times as it requires to reach a safe conditions that do not increase the local temperature anymore.
Every one of the automatic range changes is identified within the measurement data. Not only is the measured input scaled with the adapted input range correctly, but the exact moment when the automatic range change happens is also identified within Perception software.

Restore range selected by user automatically
As the GEN series system is designed to measure 24 hours a day, 7 days a week, the automatic range switching has the negative side effect of reducing the sensitivity of the amplifier. During the actual overload, the channel is unable to measure the input signal. Therefore, there are no extra negative side effects. If the overload disappears and the system runs unattended, the input range that is selected automatically will not be the best measurement range. Therefore, the amplifier "remembers" the range that the user originally selected and restores this range as soon as regular thermal conditions are restored. A temporary large overload will then only result in input sensitivity that is adjusted temporarily.

The automatic range adaptation is started due to thermal conditions typically as a result channel input overload. Therefore, the overload might still be present. If this is the case the automatic range restore restarts, the thermal increase and leads to re-trigger the automatic range adaption process and the overload is handled exactly the same way as before.

The **third** action of the system takes effect if the second action is unsuccessful and the local temperature remains outside of the maximum operating limits. The input signal is disconnected from the channel. Grounding the input disconnects the input signal from the external signal source. When inputs are grounded, the only connections to the external signal are the input connectors and the ground relay's input pin.

Thermal shutdown in critical conditions

This protective scheme allows for any overload that the input could be confronted with during normal operation. For any other failure that could result in excessive heat dissipation, the GEN series probes have a last protective stage built in. When local temperatures reach critical limits, the system automatically turns off the mains power to prevent damage to the system or other systems near the GEN series system. Maximum and critical temperatures are defined as such that it is very unlikely the system would ever reach these critical temperatures when operating within its specified conditions.

12.4 Basic high speed input card

12.4.1 GN8101B/GN8102B/GN8103B, Basic 250, 100, 25 M/s input cards

- 8 analog channels
- Single-ended inputs
- 1 MΩ or 50 Ω termination
- ± 10 mV to ± 100 V input range
- Analog/digital anti-alias filters
- 14/16 bit resolution
- Real-time formula database
- Digital Event/Timer/Counter
- Multi-sweep transient recorder
- Continuous/Dual sample rate
- Differential input using probes

The input card is a general purpose single-ended voltage input card. An external active differential probe supports measuring the differential signal directly at the source and creates the best high frequency common mode suppression possible.
For high frequency measurements, the inputs support a built-in 50 Ω termination option. The use of the 50 Ω termination supports voltage inputs from ± 10 mV to ± 5 V. The alternative 1 MΩ termination provides voltage inputs up to ± 100 V.
In multi-sweep transient recorder mode triggers can be recorded without any re-arm time between sweeps, combined with sweep stretch to create variable post-trigger lengths.
Optimum anti-alias protection is achieved by the 6-pole analog anti-alias filter combined with a fixed high speed sampling Analog-to-Digital converter.
For sample rates 100 MS/s and lower, the digital anti-alias filter allows for a large range of high order filter characteristics with precise phase match and noise-free digital output.
The real-time formula database calculators option offers math routines to solve many real-time mathematical challenge like obtaining mechanical power and/or multi-phase (not limited to three) electric power (P, Q, S) or even efficiency calculations.
Every cycle based result from the real-time formula database can be transferred in real-time to the EtherCAT® output card.
Using voltage probes a single-ended 600 V RMS CAT III / 1000 V CAT II or a differential 1000 V RMS CAT III (1000 V RMS common mode) measurement range is created. The use of current clamps and external burdens allow for direct current measurements.

For specification and ordering information, please refer to "B04596_01_E00_01 (GEN series GN810xB)" on page 607.

12.5 High resolution universal input card

12.5.1 GN840/GN1640 Universal 500 kS/s 8/16 channel input cards

- Ranges ± 0.2 mV/V up to ± 500 mV/V
- Quarter/Half/Full bridge
- 6 wire configuration
- Quick sensor test (shunt)
- Voltage excited sensors
- IEPE sensors
- IEEE 1451.4 TEDS class 1
- Piezoelectric/Charge sensors
- 4 to 20 mA sensors
- Pt10, Pt100, Pt500, Pt1000 and Pt2000 (3 and 4 wire RTD)
- Thermocouples K, J, T, B, E, N, R, S, C
- 33 V RMS Isolation
- Analog/digital anti-alias filters
- 500 kS/s sample rate/channel
- 24 bit ADC resolution

The Universal Sensor Card supports quarter, half and full bridges with built-in 350 Ω and 120 Ω quarter bridge completion resistors. The shunt resistor offers a quick test of the sensor.
In IEPE mode the card supports open and shorted wire detection and TEDS sensor setup. Thermocouples, piezoelectric, RTD and 4 to 20 mA sensors are all directly supported.
All sensor types connect to the input without external adapters.
Measurement ranges starting at ± 0.2 mV/V up to ± 500 mV/V and sensor impedance from 17 Ω up to 10 kΩ support virtually any sensor.
Superior, best in class anti-alias protection is achieved by a unique, multi stage approach.
The first stage the Sigma Delta converter with built in anti-aliasing filter creates an alias free digital data stream at constant rate of 500 kS/s.
The second stage feeds the 500 kS/s data stream into a user selectable digital filter, to reduce the signal to the desired maximum bandwidth. The digital filter supports both 11 or 12 orders as well as bessel/butterworth or elliptic filter characteristics.
The third stage decimates the 500 kS/s filtered signal to the desired sample rate.

The digital filter before decimation guarantees a superior phase match, ultra-low noise and alias free result.
The optional real-time formula database calculators solve almost any mathematical challenge. Real-time digital cycle detection enables periodic results like PeakToPeak. Real-time channel to channel sample math can reverse calculate crosstalk interdependencies within a three axes force sensor. Calculated results can be used to trigger the recording or signal alarms to the external world.
For more information on the High resolution universal input card, please refer to "B04170_02_E00_00 (GEN series GN840B, GN1640B)" on page 492.

Supported sensor modes

- "Basic mode and cabling" on page 233
- "Bridge mode and cabling" on page 234
- "Basic sensor and cabling" on page 239
- "Integrated Electronic Piezoelectric (IEPE) mode and cabling" on page 240
- "Piezoelectric (Charge) mode and cabling" on page 241
- "Resistive Temperature Detectors (RTD) mode and cabling" on page 242
- "Current loop mode and cabling" on page 243
- "Thermocouple mode and cabling" on page 244

12.5.2 Basic mode and cabling

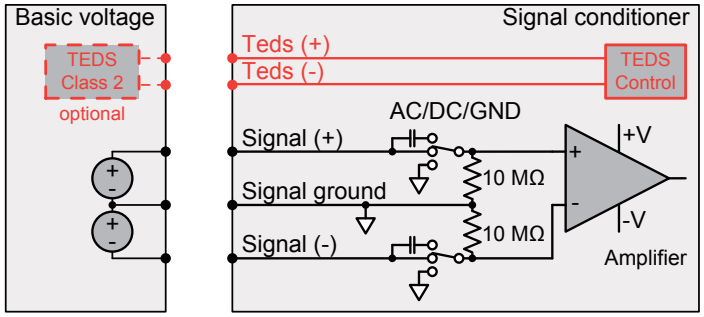


Figure 12.31: Basic mode block diagram

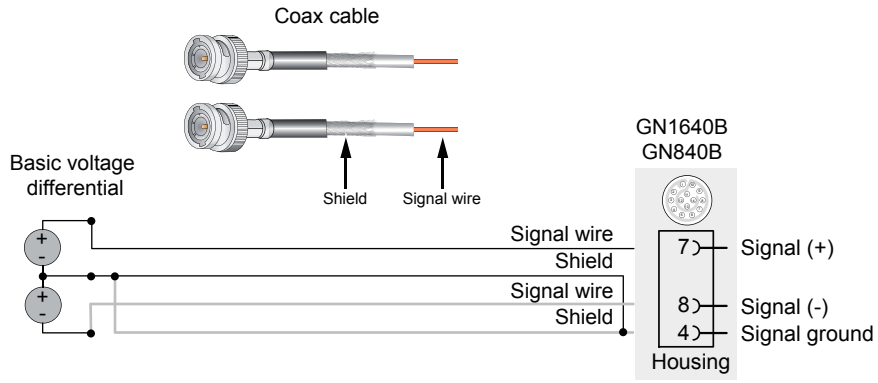


Figure 12.32: Recommended basic voltage differential connection

12.5.3 Bridge mode and cabling

Bridge amplifier configuration

Input diagrams and typical connection diagrams for the GN840B/GN1640B bridge mode are shown on this and the following pages. For the maximum versatility, the amplifiers allow a wide range of configurations. A minimum of three wires are necessary for a quarter- or half-bridge sensor and four wires for a full bridge. Optional remote sensing of excitation voltage is supported for precision transducer applications, which adds two wires. If remote sense is not required, the sense wires must be connected within the channel connector as the sense lines are always active. Remote shunt calibration is possible with the addition of one more wire. An isolated common is provided for preferred double shielding.

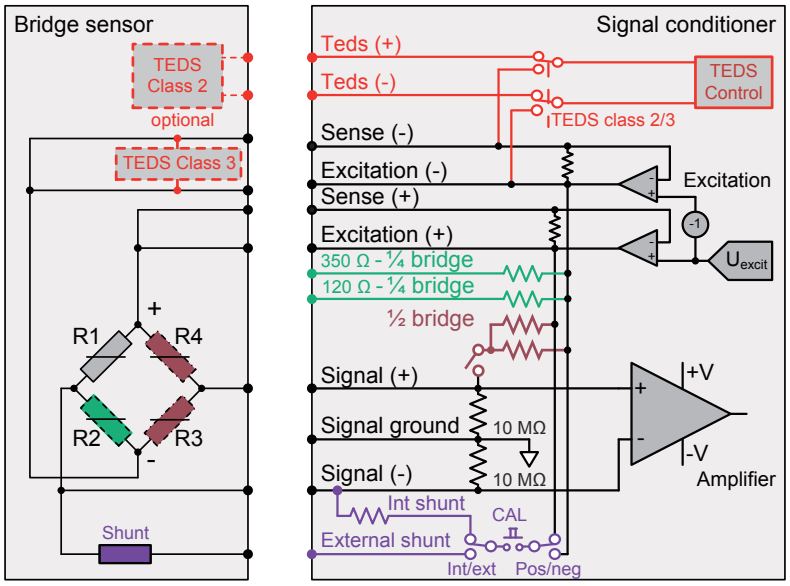


Figure 12.33: Bridge mode block diagram

Bridge completion

Each bridge amplifier channel contains a pair of fixed 10 kΩ resistors for half bridge completion that can be switched in by software control. Additional pins on the input connector provide a precision 120 Ω and 350 Ω resistor for quarter-bridge completion.

Sense lines
Remote sensing of excitation voltage, is commonly recommended for use with precision, commercial transducers to prevent lead-wire resistance changes (due to changes in either temperature or length) from affecting transducer span, or sensitivity. Lead-wire attenuation presents a potentially significant error source in transducers utilizing a Wheatstone bridge circuit. The lead-wires represent a parasitic resistance, and a portion of the excitation voltage intended for the bridge circuit is dropped in the lead-wire system, reducing the voltage actually present at the transducer, and effectively reducing the transducer sensitivity.

Bridge balance
The bridge circuit is only in balance (has no output when the bridge voltage is applied) when R1 / R2 = R4 / R3. Taking the various resistance tolerances on the strain gauge(s), resistors and lead wires into account, an initial unbalance is invariably present. Adjusting the initial balance so that there is zero output at zero strain is achieved by bridge balancing.

Shunt calibration
Each bridge amplifier channel contains 100 KΩ, 0.1% fixed precision resistor that can be switched in by software control. With a gage factor of 2.00, this resistor simulates the following values of deflection for various bridge configurations.

Table 12.6: Deflection for various bridge configurations

	100 KΩ		
BRIDGE	**1000 Ω**	**350 Ω**	**120 Ω**
mV/V	2.4888	0.873	0.299
µstr full bridge	1244	437	150
µstr $^1/_2$ bridge	2488	873	300
µstr $^1/_4$ bridge	4975	1747	600

A second calibration resistor can be connected to the connector pin externally. Either one of the shunt calibration resistors can be switched in by software control to provide multi-point calibration and linearity verification.

Shielding and immunity increase
Using high bandwidth amplifiers like the GN840B/GN1640B, any external disturbance typically is immediately reflected in the measured signal. To minimize external disturbance pick-up the excitation, sense and signal leads are generally separately twisted and shielded within the cable to minimize the cross-coupling that would otherwise occur.

Double shielding is strongly recommended to maximum disturbance reduction. Attach the signal ground to an inner shield of the double shielded cable. The inner shield is as close as possible to a potential that is equal to the common mode voltage of the bridge. The shield now minimizes the potential difference between the internal conductors and the inner shield, thereby reducing the amount and levels of partial discharges between them. In all cases, the shield is terminated only at the conditioner terminal.

When the inner shield is surrounded by an outer shield that is terminated to ground at the mainframe connector. The ground shield is used to keep most of the external disturbances away.

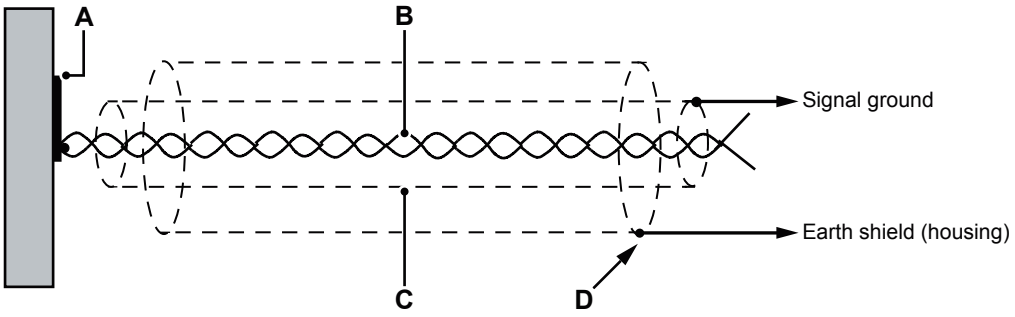


Figure 12.34: Double shielded cable to minimize induced noise

A Strain gauges

B Signal conductors

C Inner shield
Signal ground

D Outer shield
Terminated at connector (measurement channel)

Various bridge configurations

The diagrams below shows possible bridge configurations.

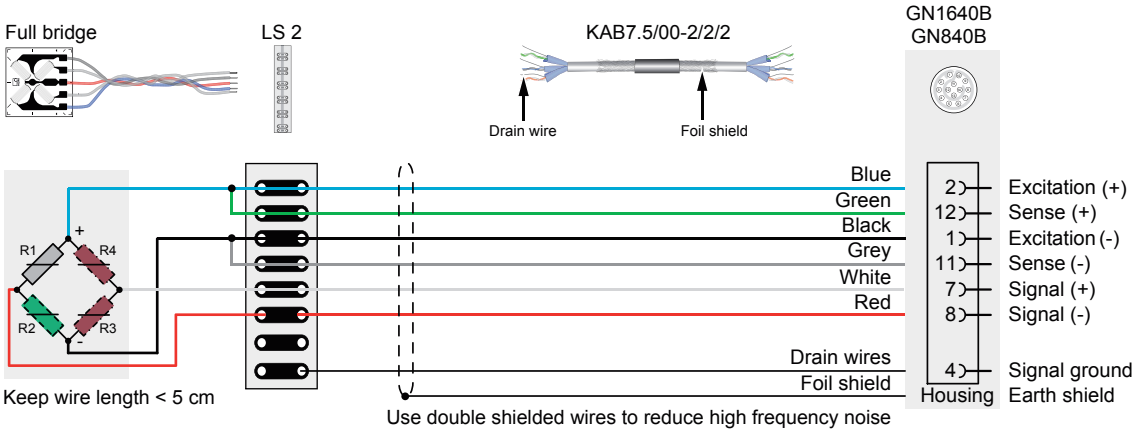


Figure 12.35: Recommended 6 wire full bridge connection (more options are available)

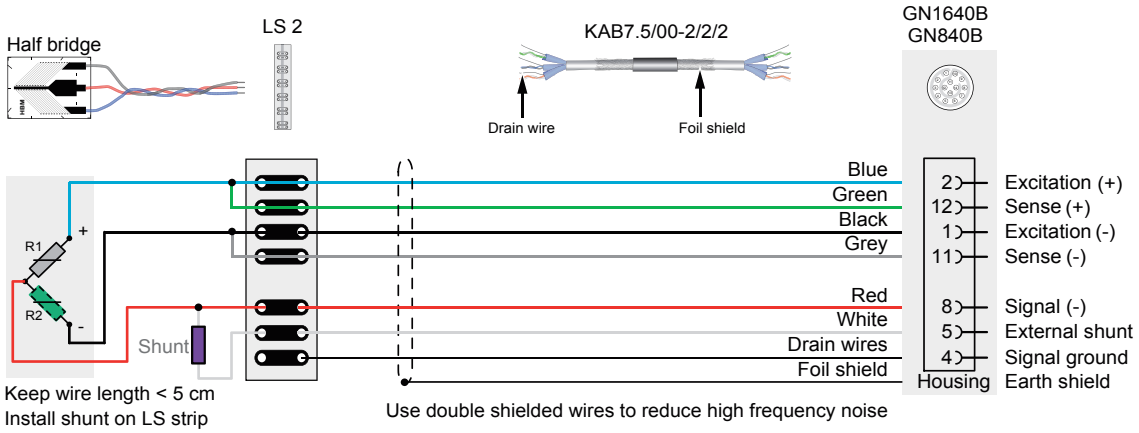


Figure 12.36: Recommended 6 wire half bridge with shunt resistor connection (more options are available)

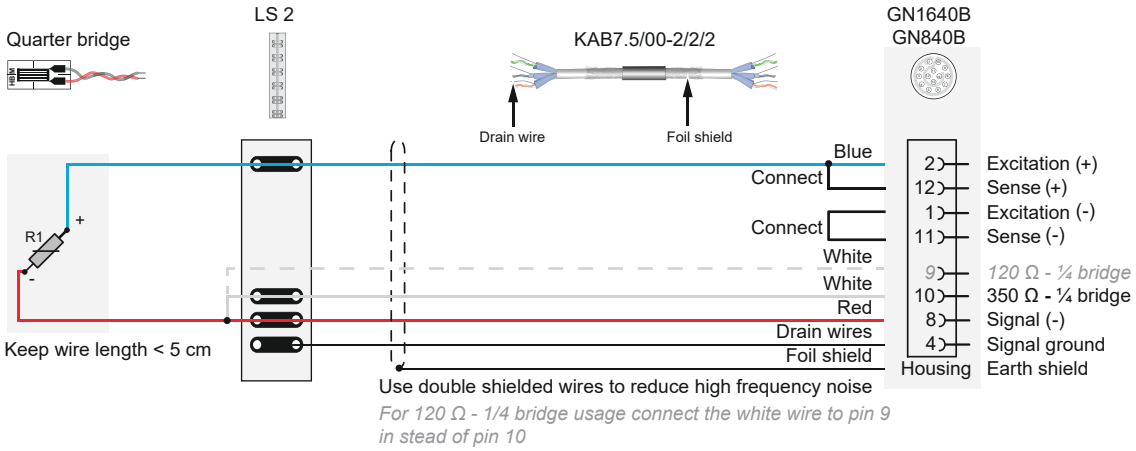


Figure 12.37: Recommended 3 wire 350 Ω quarter bridge connection (more options are available)

12.5.4 Basic sensor and cabling

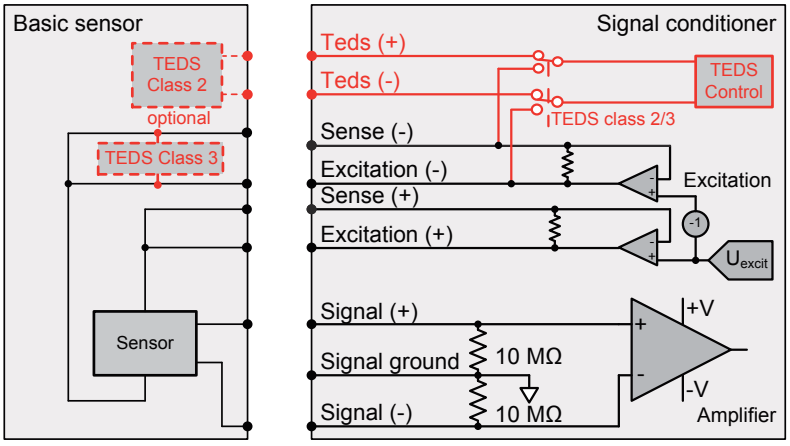


Figure 12.38: Basic sensor mode block diagram

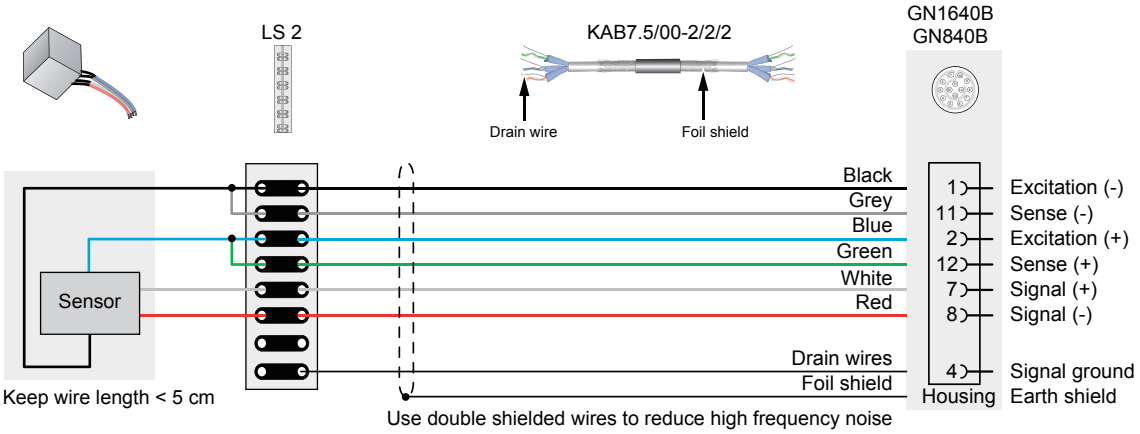


Figure 12.39: Recommended 6 wire basic sensor connection (more options are available)

12.5.5 Integrated Electronic Piezoelectric (IEPE) mode and cabling

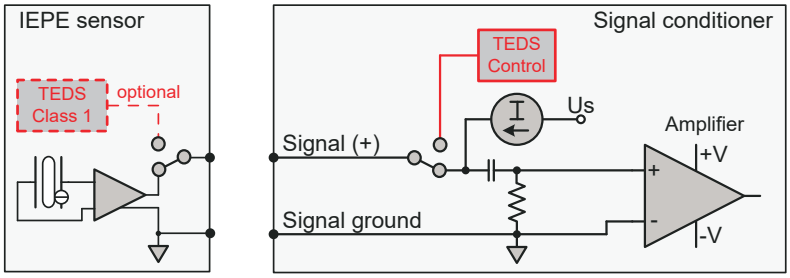


Figure 12.40: IEPE mode block diagram

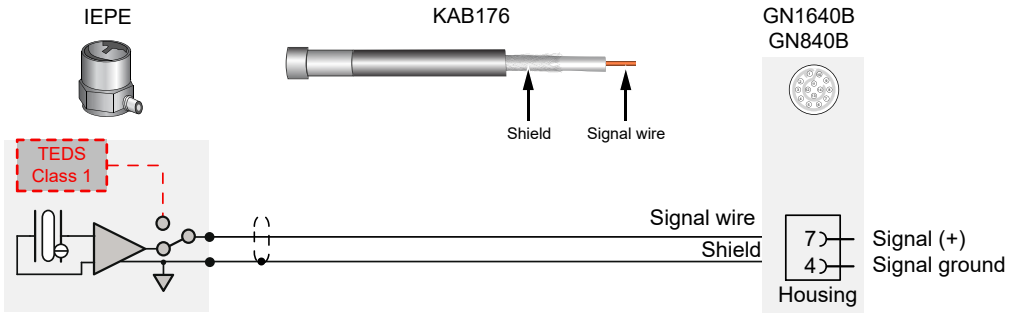


Figure 12.41: Recommended IEPE connection

12.5.6 Piezoelectric (Charge) mode and cabling

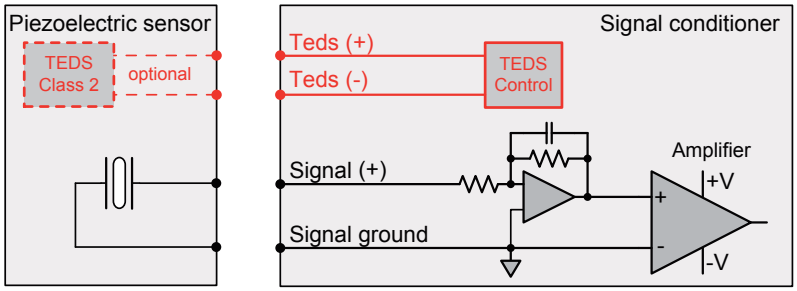


Figure 12.42: Piezoelectric mode block diagram

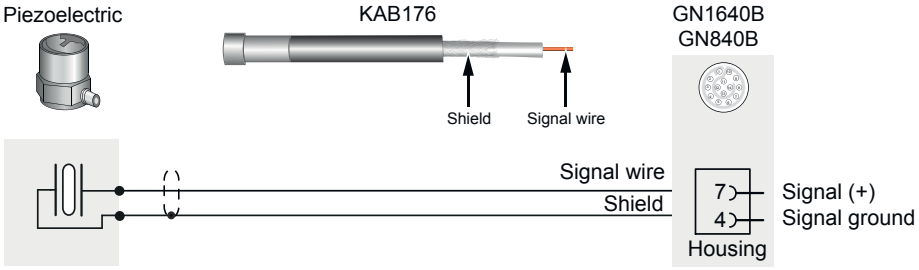


Figure 12.43: Recommended piezoelectric connection

12.5.7 Resistive Temperature Detectors (RTD) mode and cabling

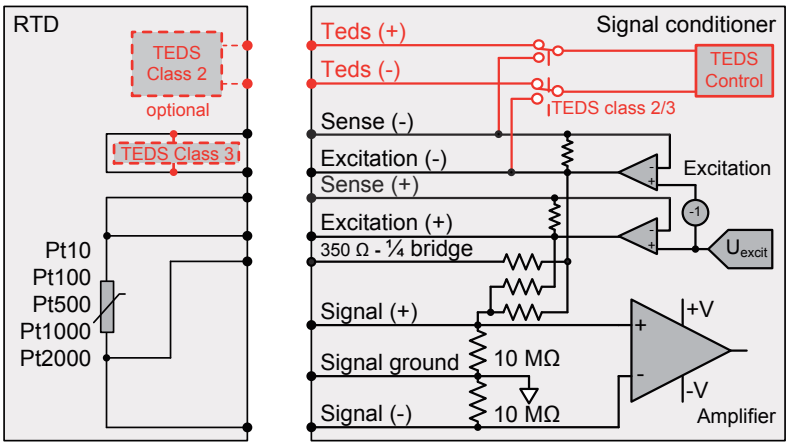


Figure 12.44: RTD mode block diagram

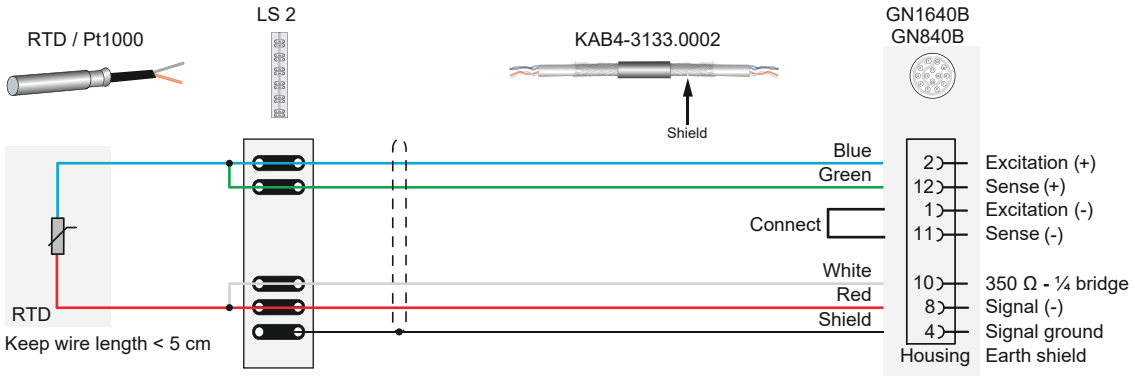


Figure 12.45: RRecommended 4 wire RTD connection (more options are available)

12.5.8 Current loop mode and cabling

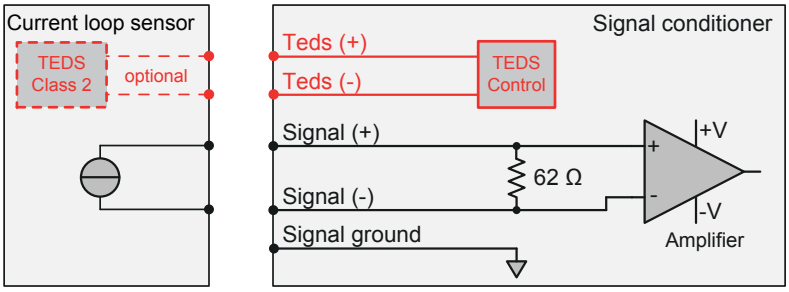


Figure 12.46: Current loop mode block diagram

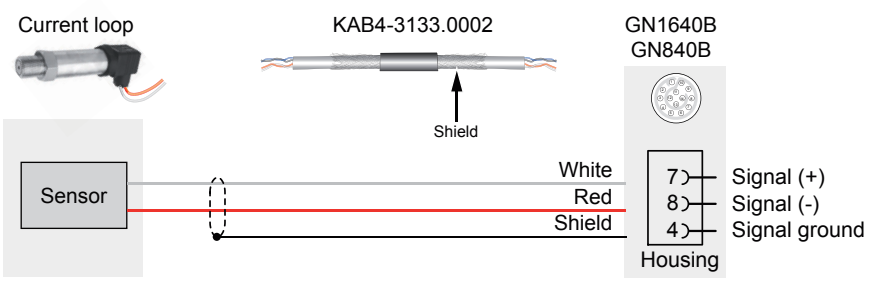


Figure 12.47: Recommended current loop connection

12.5.9 Thermocouple mode and cabling

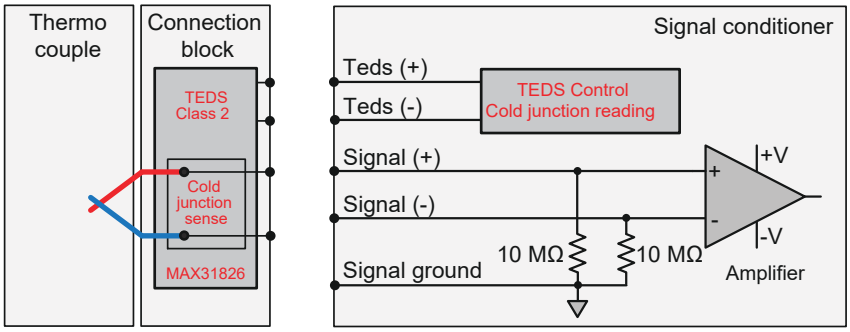


Figure 12.48: Thermocouple mode block diagram

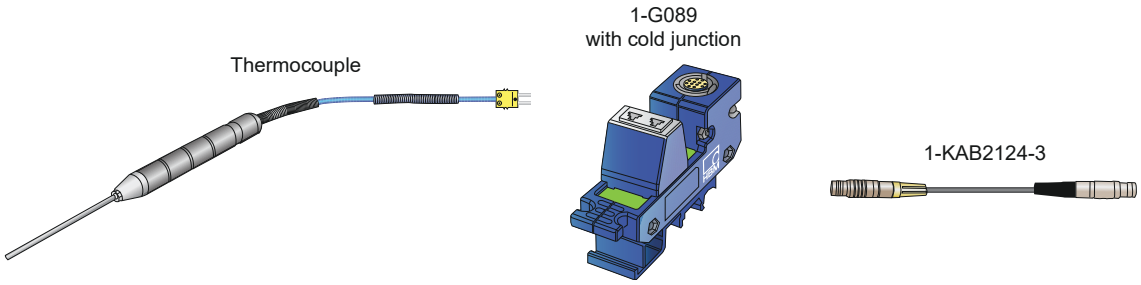


Figure 12.49: Recommended thermocouple tools

12.5.10 DIN rail breakout

HINT/TIP

For quick connect and reconnect din rail breakouts are available.

Three different models exist:

1 Generic breakout G088

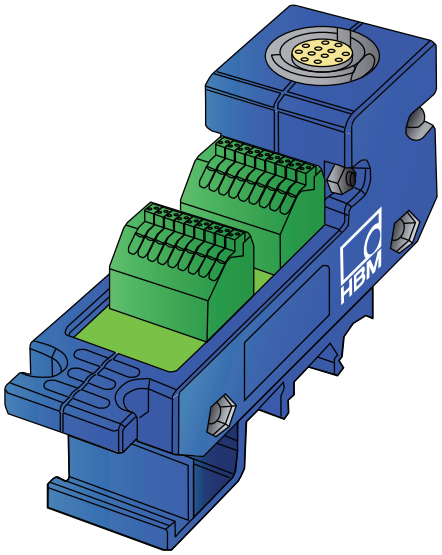


Figure 12.50: DIN rail mountable breakout block (1-G088-02)

The G088 supports spring/push-in connectors for all wire connection to/ from the GN840B/GN1640B card. It is especially suited to support Bridge/ Basic sensor/RTD/Current loop sensors.

The breakout supports wire connections for TEDS class 2 and 3.

2 Thermocouple breakout G089

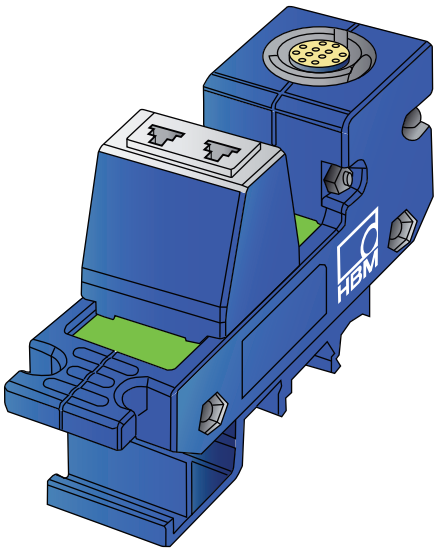


Figure 12.51: DIN rail mountable breakout block (1-G089-02)

The G089 is specifically designed to support thermocouple input connections to/from the GN840B/GN1640B card. The built-in digital cold junction sensor is used by the GN840B/GN1640B card to compensate the thermal errors caused by the sensor to measurement junction.

The breakout supports a flash memory to enable TEDS information to be written into the breakout. Using TEDS, the breakout can be made uniquely recognizable by the controlling software, avoiding hours of system setups.

3 Basic/IEPE/piezoelectric breakout terminal G090

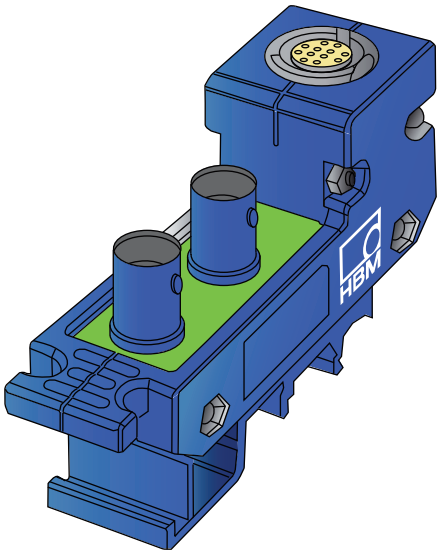


Figure 12.52: DIN rail mountable breakout block (1-G090-02)

The G090 is specifically designed to support BNC input connections to/from the GN840B/GN1640B card. The breakout supports two isolated metal BNCs to allow full differential input wiring.

In basic voltage mode the software allows the selection of differential or single-ended input only.

In IEPE and piezoelectric mode the input is automatically selected as single-ended.

The breakout supports a flash memory to enable TEDS information to be written into the breakout . Using TEDS, the breakout can be made uniquely recognizable by the controlling software, avoiding hours of system setups.

12.5.11 Flexible wiring

HINT/TIP

Using the different terminals, cables and other existing support material a flexible wiring setup can be created to match almost any wish list.

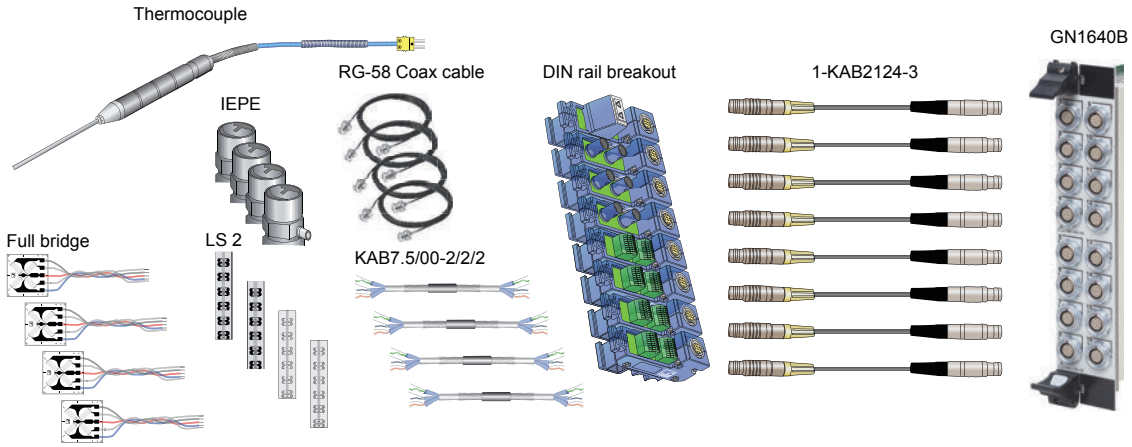


Figure 12.53: Flexible wire diagram

Contact custom systems at: customsystems@hbm.com for more options and or support on your wiring requests.

12.6 Optical fiber isolated input card

12.6.1 GN1202B, Optical fiber isolated 100 MS/s input card

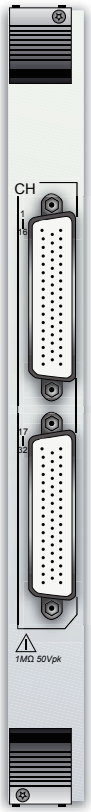
- 12 transmitters per receiver card
- Digital fiber optic connection, noise/error and drift free
- Cable length up to 1000 m
- Automatic cable length phase compensation
- Battery powered transmitter
- Continuous powered transmitter with 1.8 kV RMS isolation
- 1 isolated, unbalanced differential input per transmitter
- ± 20 mV to ± 100 V input ranges
- Analog/digital anti-alias filters
- Calibration values stored in transmitter
- 25 MS/s or 100 MS/s transmitter
- 15 or 14 bit resolution
- Metal BNC input on transmitter

The optical fiber isolated system consists of up to 12 transmitter units (GN110, GN111, GN112 or GN113) connected to the GN1202B receiver card built into a GEN series mainframe using a fiber optic cable.
By converting the analog signal into a digital signal and transmitting the signal to the receiver card via fiber optic cable, the transmission does not add any drift or error to the measured signal. The automatic cable length compensation phase matches all fiber optic isolated channels to any standard analog input channel. The GN112 and GN113 offer continuous powered isolation at 1.8 kV RMS, while the GN110 and GN111 offer higher isolation options using battery power with a continuous operation time of 30 hours. Optimum anti-alias protection is achieved by the 6-pole analog anti-alias filter combined with a fixed sample rate Analog-to-Digital converter. At lower sample rates the digital anti-alias filters allow for a large range of 8^{th} order Bessel IIR filters with precise phase match and ultra low noise output.
Using the full transient and data recorder feature set of the GN1202B with the powerful Perception software eliminates the need to use separate data acquisition hardware or software.

For specification and ordering information, please refer to "B4770-1.1 en (GEN series GN1202B)" on page 534.

12.7 High resolution IEPE and Charge input cards

12.7.1 GN3210 IEPE and charge 250 kS/s input card



The **GN3210 IEPE and charge 250 kS/s** input card is a no-compromise solution for high channel count data acquisition systems.

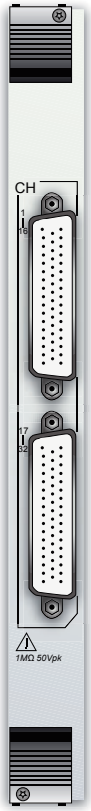
This card brings:

- A cost-effective solution with 16 or 32 channels per card
- High precision with a 24 bit A-to-D convertor for each channel
- Sample rates up to 250 kS/s (both decimal and binary)
- Flexibility; each channel can be individually assigned one of the following signal conditioners:
  - IEPE for accelerometers, microphones, etc.
  - Charge for pressure transducers, piezoelectric accelerometers, etc.
  - Voltage (full differential and single-ended)
- TEDS readout support for IEPE transducers
- Digital event and timer-counter support (on compatible mainframes only)
- 1.8 GB on-board memory

The large number of channels on this single card requires special attention. Therefore, the card is equipped with 50 pin D connectors. To provide easy access to all channels, breakout cables with 19-inch panels for BNC connectors are available as an option.

For specification and ordering information, please refer to "B3240-3.1 en (GEN series GN3210)" on page 561.

12.7.2 GN3211 basic 20 kS/s input card



The **GN3211 basic 20 kS/s** input card is a no-compromise solution for high-channel-count data acquisition systems.

This card offers:

- A cost-effective solution with 16 or 32 channels per card
- High precision with a 16 bit A-to-D convertor for each channel
- Sample rates up to 20 kS/s (both decimal and binary)
- Digital event support (on compatible mainframes only)
- 200 MB on-board memory

The large number of channels on this single card requires special attention. The card is therefore equipped with 50 pin D connectors. To provide easy access to all channels, breakout cables with 19-inch panels for BNC connectors are available as an option.

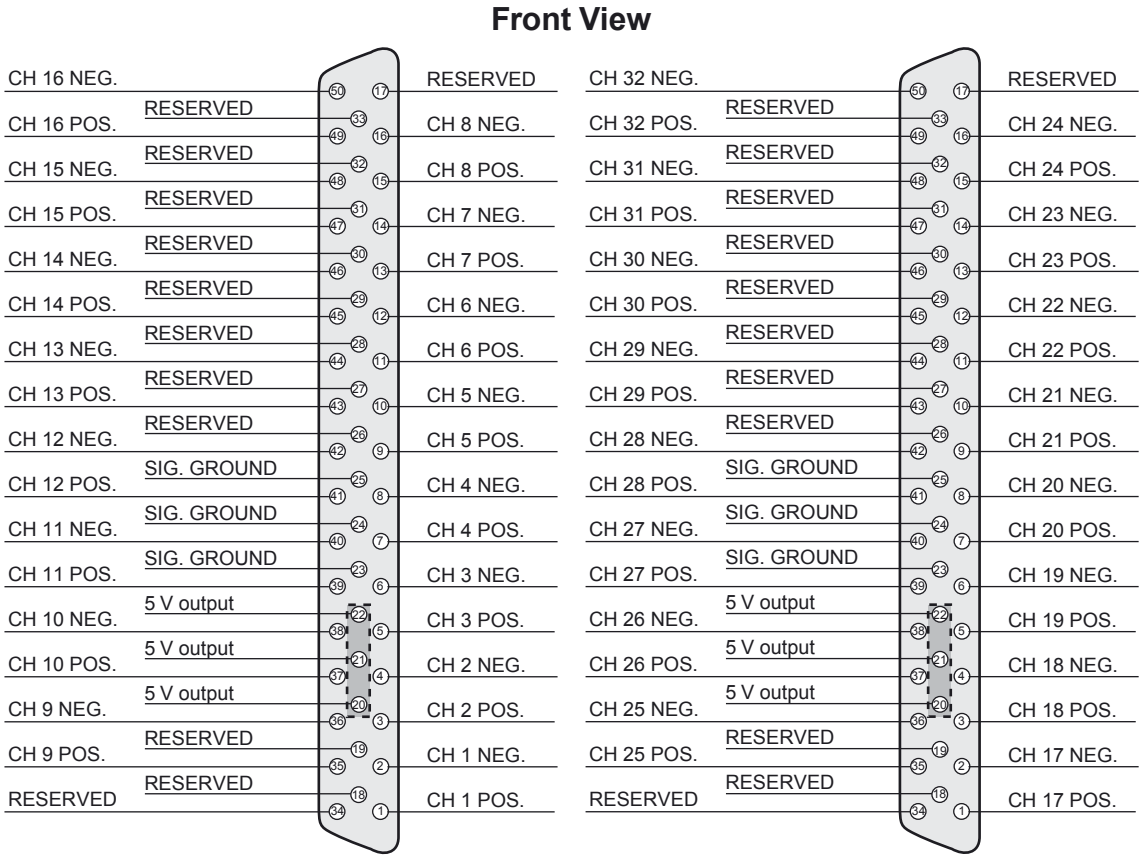


Figure 12.54: Pin diagram for top 16 channel connector (left), Bottom 16 channel connector (right)

Note *Both positive and negative pins must be connected to avoid erroneous measurement results with noise.*

Note *There are three output pins available on each connector. Each pin's output voltage is 5 V. The maximum current for each pins is 0.1 A. When connecting all three pins 0.3 A can be used.*
Over current protection is add for the maximum 0.3 A using an automatic resettable fuse.

For more information on the 16/32 Channel Basic Card 20 kS/s input card, please refer to "B3264-3.1 en (GEN series GN3211)" on page 587.

13 Option Cards

13.1 Option Carrier Card (OCC)

The option carrier card is used to add all kinds of additional digital interfaces to the outside world. The most typical interfaces it is designed for are synchronization to various time sources like IRIG/GPS etc., but also faster Ethernet or real-time EtherCAT® communication busses.

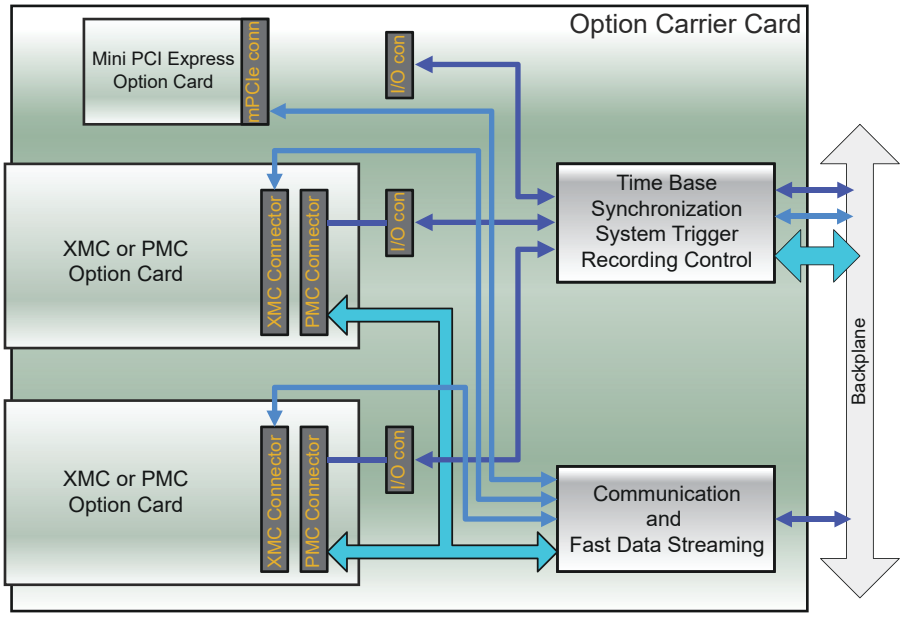


Figure 13.1: Block diagram option carrier card

The OCC supports two XMC/PMC slots and one mini PCI express slot. Each of these form factors are industrial type form factors that are widely used in the industry.

A standard OCC uses one slot of the mainframe. When adding an OCC, it is recommend to start using the last slot of the mainframe first. This preference only exists because of the first slots of each mainframe are attached to the mainframes Digital Event/Timer/Counter connectors. The OCC has no support for these connectors, so it is best to use data acquisition cards in the first slots. The OCC can be used in every slot of the mainframe. To enable the use of a mainframe at least one acquisition card needs to be installed.

13.1.1 Option cards supported

At release of this manual the following option cards are supported:

Part number	Function
G064	10 Gbit Ethernet card, optical
G082	EtherCAT®
G083	Master Output Card (Synchronize multiple slaves)
G084	10 Gbit Ethernet card, electrical

See appendix "Option carrier card extensions" on page 646 for detailed usage and specification of the option carrier card and all of the option cards supported.

14 GEN series Synchronization Methods

14.1 GEN series synchronization methods compared

GEN series systems support four different synchronization methods. Each method has its own advantages and disadvantages. It is mostly the customer's application use that determines the correct choice.

Synchronization overview				
	Master/Slave	**PTP**	**GPS**	**IRIG**
Signal Phase	Very good	Very good	Good	Average/Good
Trigger(s) / Sweep(s)	Very good	Average and extra cabling required	Average and extra cabling required	Average and extra cabling required
Absolute time of day	When combined with PTP or GPS	When using a synchronized Grandmaster	Always	When using a synchronized IRIG source
Start of recording	Very good	Average	Average	Average
Stop of recording	Average	Average	Average	Average

As the GEN series systems support several recording modes, the impact of each of these choices needs to be considered with respect to the recording mode.

14.1.1 Signal phase shift synchronization

Since typical GEN series applications use sample rates ranging from 10 kS/s to 100 MS/s, channel to channel phase match is the vital system characteristic.

Channel to channel phase shift is defined as the phase/time differences measured between two channels recording the exact same signal. Phase shifts should therefore not be measured by comparing the first or last samples of a recording or sweep. Measuring phase shift should compare a single signal recorded by mulitple mainframes and then establish the exact time difference of the different signals when shown within Perception.

A quick and easy verification method uses a square wave and compares the rising edge of the square wave. Make sure to use a square wave signal with a time period that is longer than the expected phase match. This avoids larger phase errors being missed, as the different subsequent rising edges cannot be separated from each other. For example, a square wave of 100 kHz (10 µs period time) and a phase shift of 10 µs would show a 100% synchronized trace. Lowering the square wave frequency to 10 kHz would suddenly show the 10 µs phase error. When in doubt, lower the frequency and measure again.

HINT/TIP

As a square wave has an instantaneous transition by definition, it is not possible to establish phase shifts smaller than a single sample period. A complex but more accurate phase shift measurement uses a sine wave with a period time that is ten times lower than the specified phase shift. Using a computed best fit sine wave on both signals allows for the extraction of the sine waves phase at point X of each trace. The difference between each calculated sine wave's phase is the phase shift between channels.

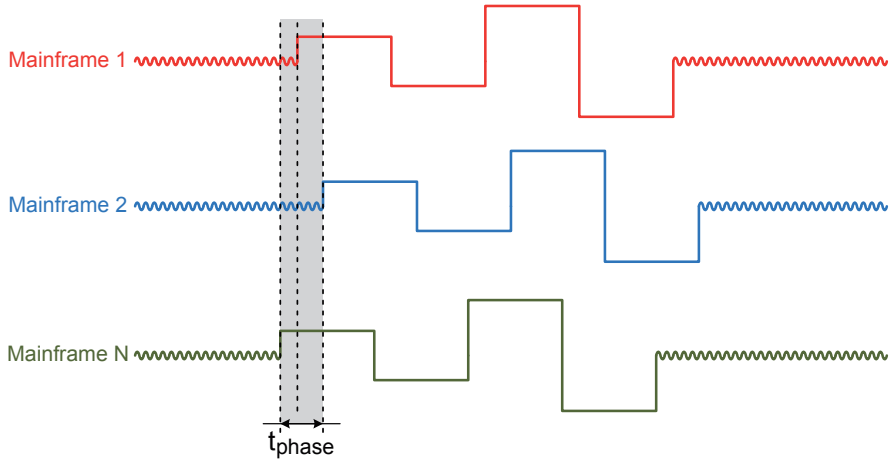


Figure 14.1: Determining phase shift

HINT/TIP

Master/Slave and PTP are typically the best choices for phase synchronizing multiple GEN series systems. PTP does not support trigger exchange and should therefore typically be used when using the continuous recording user mode within Perception.

14.1.2 Trigger synchronization

When in Single sweep, Multiple sweep, Slow-Fast Sweep or dual rate mode, the second most important synchronization, after the channel to channel phase match, is the trigger exchange. As sweeps are always initiated by a trigger, the trigger point within each mainframe defines the start and end of the sweep period.

It is important to know that sweeps are shown with the trigger aligned at t_0. The net effect is that triggers received with a time delay are actually time shifted in the software, as if these triggers had happened 100% synchronous in time. If triggers are not 100% synchronous in all systems, signal phase shifts are introduced by this effect.

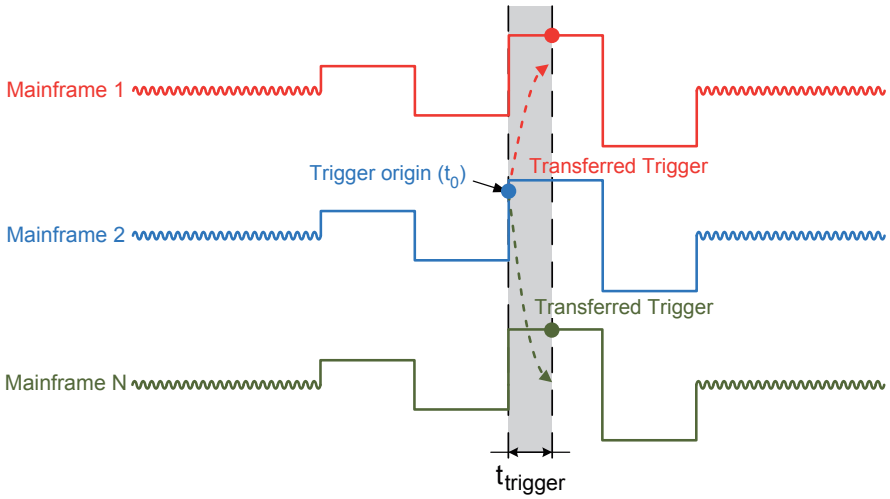


Figure 14.2: Triggering due to trigger transfer delays

The measured signals above appear within Perception as follows:

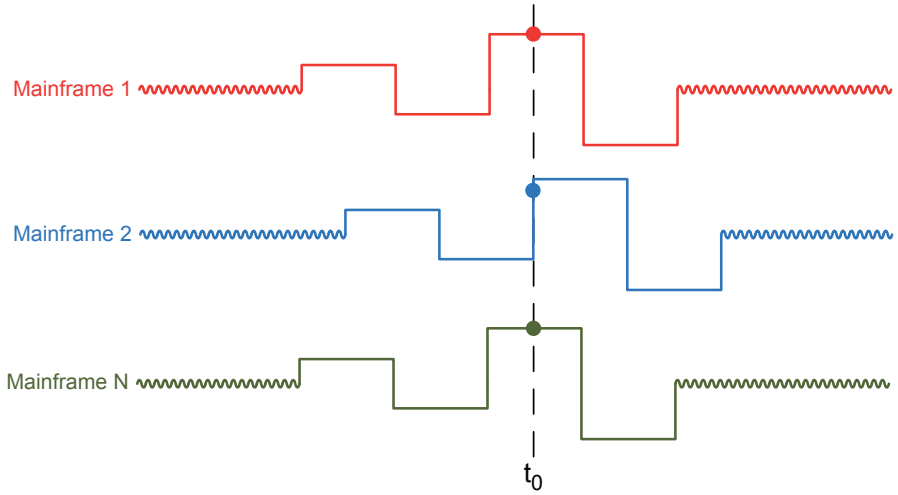


Figure 14.3: Signal phase shift introduced by t_0 alignment caused by trigger transfer delays

14.1.3 Absolute time of day synchronization

The relevancy of this synchronization is a pure user application requirement. GEN series systems are synchronized to the controlling PC when Perception makes the first connection to the mainframe. If the PC is connected to the internet or an intranet, the NTP process running within the operating system allows the GEN series mainframe to synchronize to approximately one second to the absolute time of day.

In most cases, this time indication meets the generic requirements to trace the time of day that the recording was made.

HINT/TIP

GEN series systems store this time inside the PNRF file and set the file date/time to this same time as well. However, copying files from one storage medium to the next, such as during archiving, might change the file date and time listed. Perception software only uses the date/time stored inside the PNRF recording file. This information is never affected by the adjustment that might occur while transferring the datafile.

If GEN series recorded data needs to be correlated to other (GEN series) systems that are not directly synchronized to the same time source, a more accurate absolute time of day is required to enable data correlation at a later point in time.

HINT/TIP

Whenever a GEN series recording is made using any of the available synchronization methods, the need for absolute time of day synchronization is not required to get a correct signal phase match.

A typical use of absolute time of day synchronization would be two GEN series systems, each at different locations that cannot be connected by wires. Using GPS absolute time synchronization would allow recorded data to be compared, even if these two systems were not connected.

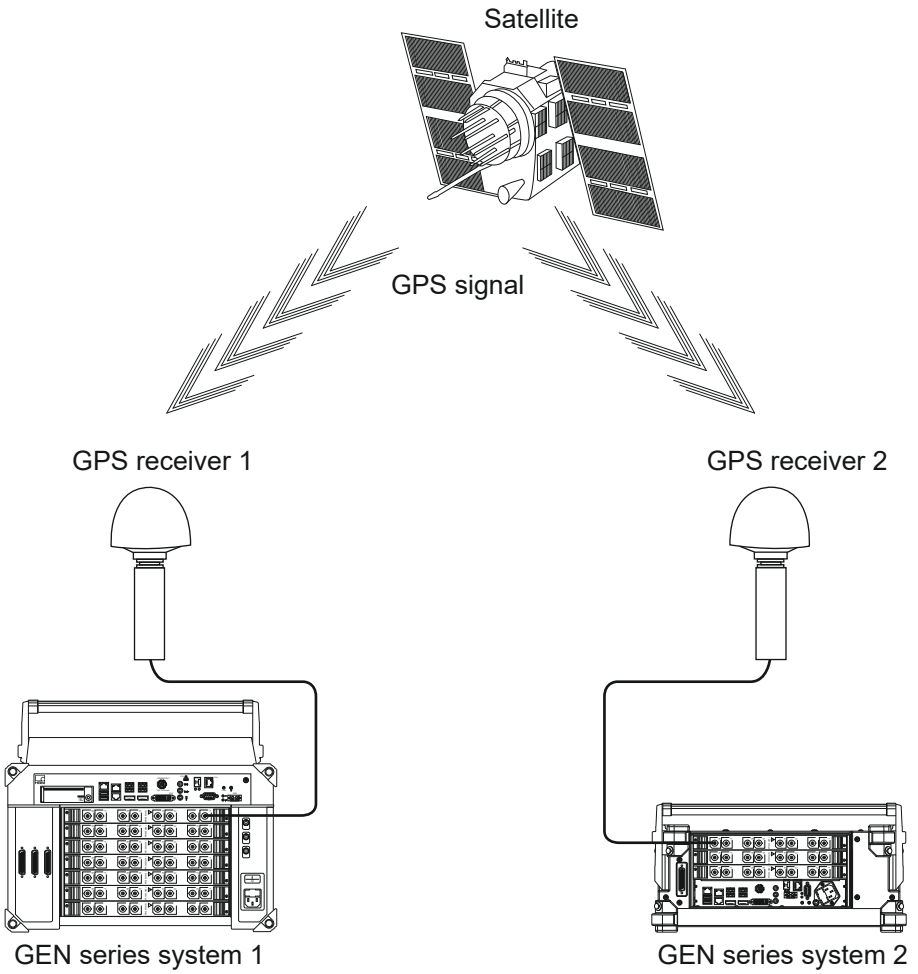


Figure 14.4: Typical GPS absolute time of day setup

14.1.4 Start/Stop synchronization

When using multiple mainframes in continuous mode, expectations are typically that the first sample of each channel aligns. However, depending on how the start and stop actions are synchronized, this might not be the reality. The response time within GEN series systems is not specified, e.g. the time from when the Start button has been pressed to when the mainframe actually captures the first sample. The response time varies and is dependent on a number of parameters, e.g. the number of acquisition cards within the mainframe and the the speed of the Windows® PC. Given this variation in response, a system start should be executed in time to guarantee the recording of all important data.

When in Single sweep, Multiple sweep or Slow-Fast Sweep mode, the start and stop synchronization of the recording is irrelevant. The entire recorded sweep data is determined by the trigger origin with a fixed pre- and post-trigger time frame. In sweep-based recordings, the acquisition system is typically started first. Checks on all system parts are then performed and the first trigger is inserted only when all systems are ready.

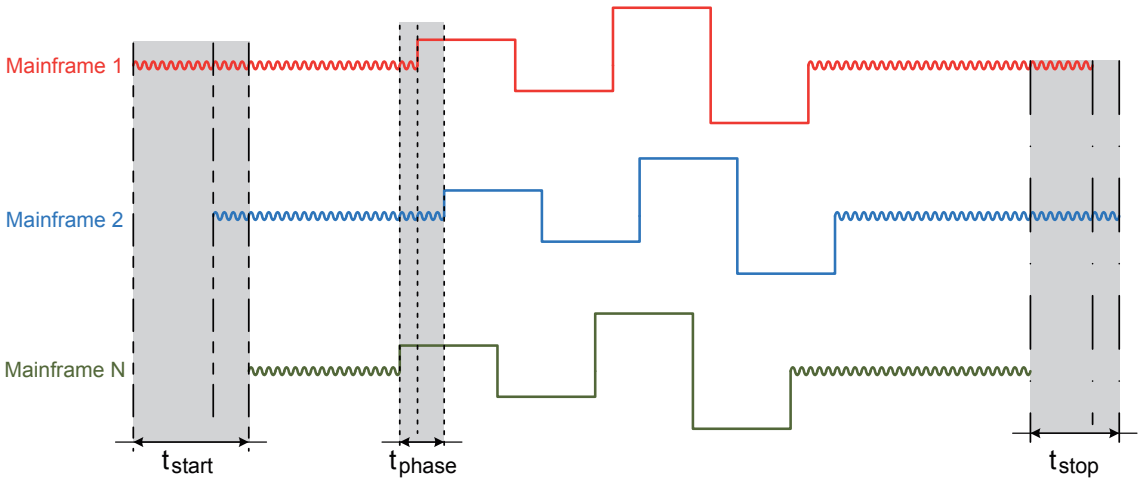


Figure 14.5: Measuring start/stop synchronization accuracy

14.1.5 Synchronization specification overview

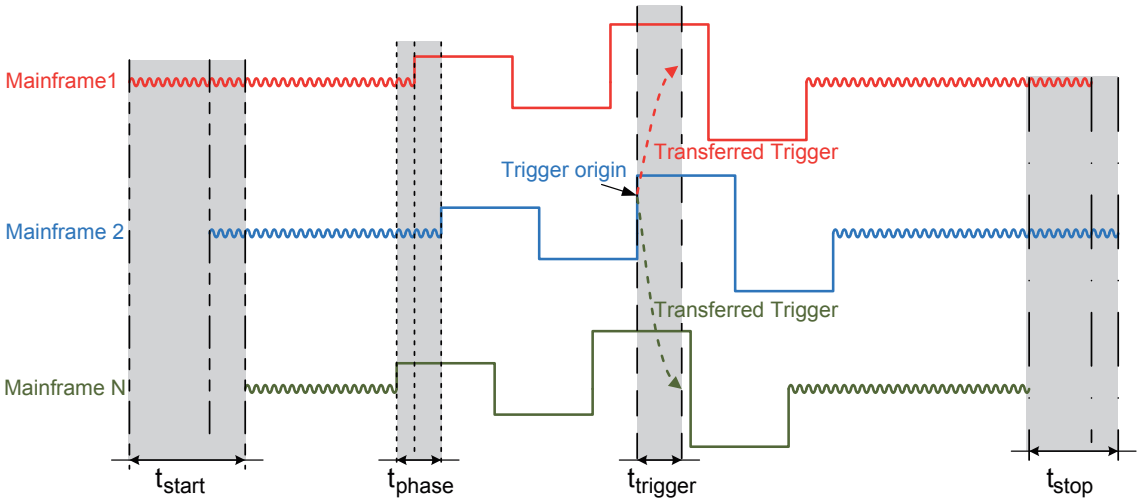


Figure 14.6: Synchronization specification overview

Master to Slave and Slave to Slave timing	**t_{phase} (1)**	**t_{start} (2)**	**t_{stop} (3)**	**$t_{trigger}$ (4) (5)**	**QuantumX Support**
Synchronization source					
Master/Slave	≤ 150 ns	≤ cable delay	≤ 1 s	≤ 150 ns	Combined using PTP
PTP	≤ 150 ns	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)	Yes
GPS	≤ 1 µs	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)	No
IRIG	≤ (10 µs + cable delays)	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)	
No synchronization source					
Mainframes simultaneous connected by Perception	≤ 1 s	≤ 1 s	≤ 1 s	≤ 1 s	--
Additional error after connection	≤ 0.5 s/hour	≤ 0.5 s/hour	≤ 0.5 s/hour	≤ 0.5 s/hour	--

(1) $\mathbf{t_{phase}}$ Maximum phase difference between signals. *(This specification is not affected by any of the other specifications).*

(2) $\mathbf{t_{start}}$ Maximum delay between start of recording of each mainframe.

(3) $\mathbf{t_{stop}}$ Maximum delay between stop of recording of each mainframe.

(4) $\mathbf{t_{trigger}}$ Maximum delay to transfer a trigger from a mainframe to all other mainframes.

(5) **Note** on trigger exchange
Trigger exchange is included in the Master/Slave synchronization cable. All other synchronization modes require that the mainframes are connected from each External Trigger Out to each External Trigger In on all mainframes in order to exchange triggers.

14.2 PTP

14.2.1 PTP technology background(1)

(1) Source: Wikipedia® the free encyclopedia

The **Precision Time Protocol (PTP)** is a protocol used to synchronize clocks throughout a computer network. On a local area network, it achieves clock accuracy in the sub-microsecond range, making it suitable for measurement and control systems.

PTP was originally defined in the **IEEE 1588-2002** standard, officially entitled *"Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems"* and published in 2002. In 2008, a revised standard, **IEEE 1588-2008** was released. This new version, also known as PTP Version 2, improves accuracy, precision and robustness but is not backwards compatible with the original 2002 version.

Architecture

The IEEE 1588 standards describe a hierarchical master-slave architecture for clock distribution. Under this architecture, a time distribution system consists of one or more types of communication media (network segments) and one or more clocks. An ordinary clock is a device with a single network connection and is either the source (master) of or destination (slave) for a synchronization reference. A boundary clock has multiple network connections and can accurately bridge synchronization from one network segment to another. A synchronization master is selected for each of the network segments in the system. The root timing reference is called the grandmaster. The grandmaster transmits synchronization information to the clocks residing on its network segment.

The boundary clocks with a presence on that segment then relay accurate time to the other segments to which they are also connected.

A simplified PTP system frequently consists of ordinary clocks connected to a single network. No boundary clocks are used. A grandmaster is elected and all other clocks synchronize directly to it. IEEE 1588-2008 introduces a clock associated with network equipment used to convey PTP messages. The transparent clock modifies PTP messages as they pass through the device. Timestamps in the messages are corrected for time spent traversing the network equipment. This scheme improves distribution accuracy by compensating for delivery variability across the network.

14.2.2 PTP Protocol details

Synchronization and management of a PTP system is achieved through the exchange of messages across the communications medium. To this end, PTP uses the following message types.

- **Sync, Delay_Req, Follow_Up** and **Delay_Resp** messages are used by ordinary and boundary clocks and communicate time-related information used to synchronize clocks across the network.
- **Pdelay_Req, Pdelay_Resp** and **Pdelay_Resp_Follow_Up** are used by transparent clocks to measure delays across the communications medium so that they can be compensated for by the system. Transparent clocks and these messages associated with them are not available in IEEE 1588-2002.
- **Announce** messages are used by the best master clock algorithm in IEEE 1588-2008 to build a clock hierarchy and to select the grandmaster.
- **Management** messages are used by network management to monitor, configure and maintain a PTP system.
- **Signaling** messages are used for non-time-critical communications between clocks. Signaling messages were introduced in IEEE 1588-2008.

Messages are categorized as **Event** and **General** messages. Event messages are time-critical in that accuracy in transmission and receipt timestamp accuracy directly affects clock distribution accuracy.

Event messages:

- Sync
- Delay_Req
- Pdelay_Req
- Pdelay_resp

General messages :

- Announce
- Follow_Up
- Delay_Resp
- Pdelay_Resp_Follow_Up

General messages are more conventional protocol data units in that the data in these messages is of importance to PTP, but their transmission and receipt timestamps are not.

Management and **Signaling** messages are members of the **General** message class.

14.2.3 Best master clock algorithm (BMC)

The **best master clock** (BMC) algorithm performs a distributed selection of the best candidate clock based on the following clock properties:

- **Identifier**
  A universally unique numeric identifier for the clock. This is typically constructed based on a device's MAC address.
- **Quality**
  Both versions of IEEE 1588 attempt to quantify clock quality based on expected timing deviation, technology used to implement the clock or location in a stratum schema, although only V1 knows a data field stratum. PTP V2 defines the overall quality of a clock by using the data fields clockAccuracy and clockClass.
- **Priority**
  An administratively assigned precedence hint used by the BMC to help select a grandmaster for the PTP domain. IEEE 1588-2002 used a single boolean variable to indicate precedence. IEEE 1588-2008 features two 8 bit priority fields.
- **Variance**
  A clock's estimate of its stability based on observation of its performance against the PTP reference.

IEEE 1588-2008 uses a hierarchical selection algorithm based on the following properties, in the indicated order:

1 Priority 1
2 Class
3 Accuracy
4 Variance
5 Priority 2
6 Unique identifier (tie breaker)

(1) “PTP technology background”, “PTP Protocol details” and “Best master clock algorithm”: Source: Wikipedia® the free encyclopedia

HBM systems use the following details for BMC:

	GEN3i/GEN3iA/GEN7i GEN3t/GEN7tA GEN17tA	**QuantumX (B hardware)**
Priority 1	128	128
Class	248	248
Accuracy	FE	FE
Variance	FFFF	FFFF
Priority 2	122	128

When using any of the HBM systems listed in this table, the systems in the leftmost column are granted Master rights based on the BMC algorithm.

Adjustments to synchronize to an external clock result in small deviations of the sample period. Technically speaking, this could be seen as jitter on the ADC clock. Depending on the jitter value, this results in noise, especially during frequency domain evaluations (FFT).

If sample rates are higher, the small corrections are relatively large compared to the same adjustment to sample rates that are 100 times lower. Therefore, the faster sampling systems are prioritized within the HBM range to become clock master.

HINT/TIP

For each field, the smallest value will wins. For example, if Priority 1 for System A is smaller when compared to System B, all the other fields are no longer monitored/analyzed, as the weight of the first field outweighs all other fields.

14.2.4 PTP switch types

Within the PTP specification, two types of switches are defined:

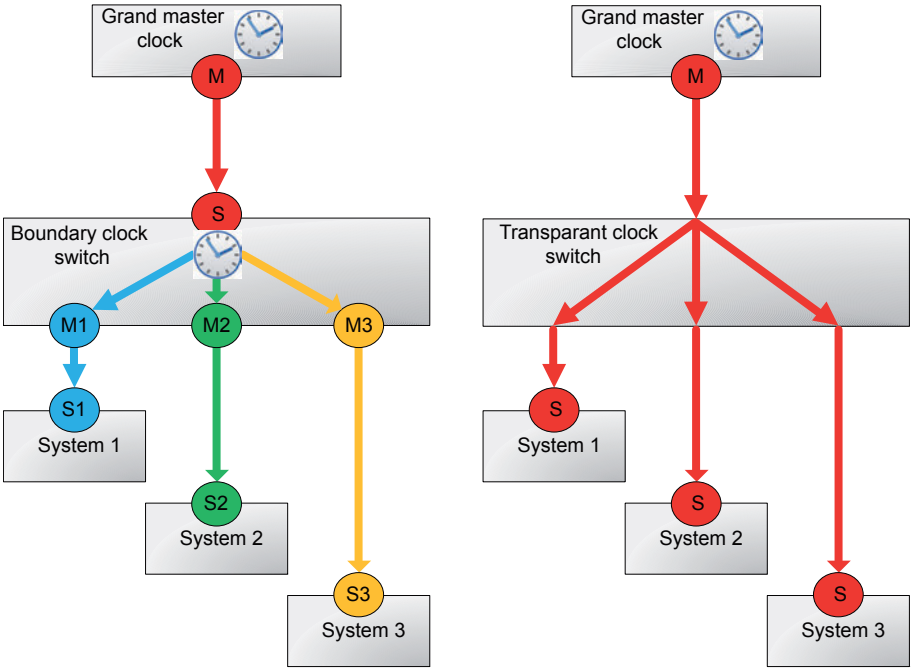
- Boundary clock switches
- Transparent clock switches

Boundary clock

Boundary clocks are defined within a PTP system to be integrated in place where standard network switches or routers are used. Boundary clocks are defined as PTP clocks with more than a single PTP port, with each port providing access to a separate PTP communication path. The boundary clock acts as an interface between separate PTP domains intercepting and processing all PTP messages and passing all other network traffic. The BMC algorithm is used by the boundary clock to select the best clock any port can see. The chosen port (the one that receives the best clock) is set as a slave and all other ports of the boundary clock are asserted as masters to their domain (to forward the clock).

Transparent clock

Transparent clocks have been added to Version 2 of the standard as an improved method of forming cascaded topologies. Rather than acting as a multi-port ordinary clock as boundary clocks do, transparent clocks update a newly introduced time-interval field within PTP event messages. This 64 bit time-interval correction field allows for switch delay compensation to a potential accuracy of less than a picosecond. There are two types of transparent clocks, End-to-End and Peer-to-Peer. End-to-End transparent clocks update the time interval field for the delay associated with individual packet transfers, whereas Peer-to-Peer transparent clocks measure the line delay associated with the ingress transmission path and include this delay in the correction field also. Peer-to-Peer transparent clocks can allow for faster reconfiguration after network topology changes.



Boundary clock operation

Transparent clock operation

Figure 14.7: Boundary clock versus transparent clock switch synchronization mode

Switches using boundary clocks

Switches using boundary clocks have a built-in clock and they create separate synchronization domains by segmenting the synchronization path from the master clock to several slave clocks. As a result, systems downstream of a boundary clock do not communicate PTP messages with the selected (grand) master directly. Standard Ethernet messages are passed through the switch while synchronization messages are used to synchronize the boundary slave clock.

HINT/TIP

As boundary clock switches create their own internal clock, the overall stability and/or accuracy of the grandmaster clock is no longer available for any of the attached systems.

Switches using transparent clocks
Switches using transparent clocks forward the master clock synchronization message to every port of the switch. The time required to transfer the message from the incoming port to the outgoing port must be measured and transferred together with the original synchronization message. There are two methods used to communicate the internal delay information to the original synchronization messages:

- End-to-End
- Peer-to-Peer

Each of these two methods has its advantages and disadvantages.

End-to-End transparent clocks
End-to-End transparent clocks create a higher load on the master clock, as the master “sees” all the slaves. End-to-End transparent clocks support a 1:N topology with one master communicating with a large number of slaves. They are, however, good for linear systems with a number of daisy-chained clocks.

Peer-to-Peer transparent clocks
Peer-to-Peer clocks avoid the higher master load, but introduce the need to be aware of how the synchronization messages are routed through the network topology. They cannot resolve 1:N topologies, as they cannot determine which line delay is being calculated and they must also maintain path delay measurements.

One-Step and Two-Step clock synchronization
PTP allows for two different types of time stamping methods:

- **One-Step** clock synchronization
  One-Step clocks update time information by adjusting the time information within the original synchronization messages (sync and delay request) on-the-fly.
- **Two-Step** clock synchronization
  Two-Step clocks transmit the precise timestamps of packets using additional general messages (follow-up and delay response).

A One-Step End-to-End transparent clock updates for switch delay in sync and delay request messages as they pass through the switch while a Two-Step transparent clock updates a field in the non-time-critical general message.

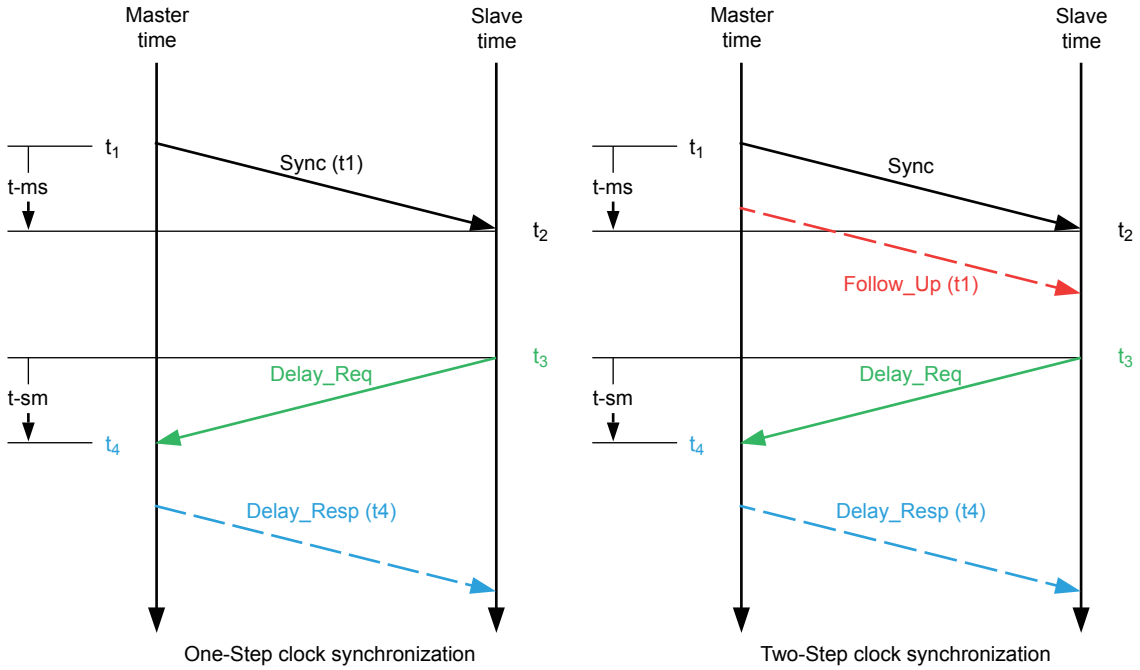


Figure 14.8: One-Step versus Two-Step clock synchronization

HBM systems are designed to work with End-to-End Two-Step PTP protocol only. Switches that do not support the End-to-End Two-Step PTP protocol are not tested or supported by HBM.

14.2.5 Transparent clock switch synchronization

The operation of PTP relies on a measurement of the communication path delay between the time source, referred to as a master, and the receiver, referred to as a slave. This process involves a message transaction between the master and slave where the precise moments of transmit and receive are measured - preferably at the hardware level. Messages containing current time information are adjusted to account for their path delay, therefore providing a more accurate representation of the time information conveyed. The path delay measurement process of PTP involves the precision timing of two messages - a sync message and a delay request. The average path delay of the two messages gives the one-way delay. This, however, assumes that the communication path is completely symmetric. This assumption does not hold in a switched network, however, largely due to the buffering process within Ethernet switches. PTP allows transparent clocks to measure and account for this delay in a time-interval field within timing packets, thus making the switches temporary transparent to master and slave nodes. Transparent clocks must perform this operation very accurately and at the communication speed without introducing more delays. The End-to-End transparent clock forwards all messages just as a normal switch does.

Message-based synchronization

PTP is based upon the transfer of network datagrams to determine system properties and to convey time information. A delay measurement principle is used to determine path delay, which is then accounted for in the adjustment of local clocks. At start-up, a master/slave hierarchy is created using what is called the Best Master Clock (BMC) algorithm to determine which clock has the best source of time. The BMC algorithm is then run continuously to quickly adjust for changes in network configuration. Synchronization is achieved using a series of message transactions between master and slaves. There are five message types - Sync, Delay Request, Follow Up, Delay Response and Management - which are used for all aspects of the protocol. A sequence of message transactions takes place to synchronize a pair of clocks as shown in Figure 14.9.

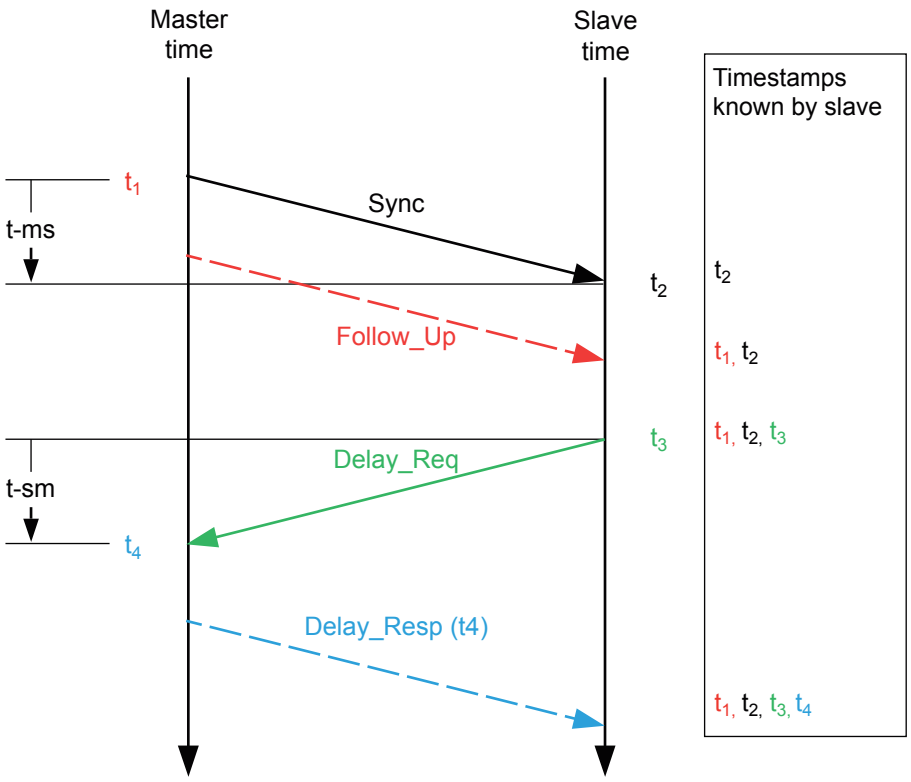


Figure 14.9: Master/Slave offset measurement

The message exchange process is as follows:

1. The master sends a **Sync** message to the slave and notes the time, $\mathbf{t_1}$, at which it was sent.
2. The slave receives the **Sync** message and notes the time of reception, $\mathbf{t_2}$.
3. The master conveys the **timestamp $\mathbf{t_1}$** to the slave the by either
   - **a** Embedding the **timestamp $\mathbf{t_1}$** in the **Sync** message (One-Step). This requires some sort of hardware processing for highest accuracy and precision

     or
   - **b** Embedding the **timestamp $\mathbf{t_1}$** in a **Follow_Up** message (Two-Step).
4. The slave sends a **Delay_Req** message to the master and notes the time, $\mathbf{t_3}$, at which it was sent.
5. The master receives the **Delay_Req** message and notes the time of reception, $\mathbf{t_4}$.
6. The master conveys the **timestamp $\mathbf{t_4}$** to the slave the by embedding it in a **Delay_Resp** message.

After this message exchange, the slave has four timestamps from which both the slave offset (time offset by which the slave clock leads or lags the master) and the network delay (the time taken for packets to traverse the network link between the two nodes) can be determined.

The link delay can be calculated as follows:

$$\mathrm{MasterSlave}_{\mathrm{delay}} = t_{ms} = t_2 - t_1$$

$$\mathrm{SlaveMaster}_{\mathrm{delay}} = t_{sm} = t_4 - t_3$$

In each case, the time differences refer to times taken from different clocks which may be offset from each other. However, if the assumption is made that the delay in one direction is the same as the delay in the opposite direction, then the two equations can be combined as follows:

$$\mathrm{Delay} = \frac{(t_2 - t_1) + (t_4 - t_3)}{2}$$

From Figure 14.9, it can be seen that the slave clock offset (the time interval by which the slave leads the master) is given by:

$$\mathrm{Offset} = t_2 - (t_1 + \mathit{Delay})$$

Substituting from Figure 14.9 above:

$$\mathrm{Offset} = t_2 - (t_1 + \tfrac{1}{2}\,[(t_2 - t_1) + (t_4 - t_3)])$$

rearranging results in:

$$\begin{aligned}\mathrm{Offset} &= t_2 - t_1 - \tfrac{1}{2}t_2 + \tfrac{1}{2}t_1 - \tfrac{1}{2}t_4 + \tfrac{1}{2}t_3 \\ &= \tfrac{1}{2}(2 \times t_2 - 2 \times t_1 - t_2 + t_1 - t_4 + t_3) \\ &= \frac{(t_2 - t_1) - (t_4 - t_3)}{2}\end{aligned}$$

If two sets of Sync and Follow up messages are sent, then the drift between the two clocks (the phase change rate) can be found by comparing the Δtime between the successive sync messages.

$$\text{Drift} = \frac{\Delta time_{slave} - \Delta time_{master}}{\Delta time_{master}}$$

HINT/TIP

Grand masters might have a setting to control the number of synchronization events sent per second time interval. For GEN series system to synchronize to a PTP grandmaster within its published specifications, a minimum of one PTP synchronization per second is required. Two updates per second improves the short-term stability. Higher update rates have not proven to be more stable.

Switch delays

The majority of Ethernet switches on the market use a store-and-forward method to decide where to send individual packets. Incoming packets are stored in local memory. The packet is checked for errors before being sent out from the appropriate port/ports. This process introduces variations in the forward and return latency time of the packet. The variations in these delays mean that the assumption that packet delay is the same in each direction is invalid, thus rendering the path delay calculations of PTP inoperable. This issue has been compensated for with the use of two special switches, **boundary clocks** and **transparent clocks**. For more information, please refer to "PTP switch types" on page 267.

14.2.6 Common terms used in IEEE 1588

(source www.nist.gov/el/isd/ieee/terms1588.cfm)

- **Boundary clock:** A boundary clock is a clock with more than a single PTP port, with each PTP port providing access to a separate PTP communication path. Boundary clocks are used to eliminate fluctuations produced by routers and similar network elements.
- **Clock:** A device providing a measurement of the passage of time since a defined epoch. There are two types of clocks in 1588: boundary clocks and ordinary clocks.
- **Direct communication:** The communication of PTP information between two PTP clocks with no intervening boundary clock is termed a direct communication.
- **External synchronization:** It is often desirable to synchronize a single clock to an external source of time, for example to a GPS system to establish a UTC time base. This synchronization is accomplished by means other than those specified by 1588 and is referred to as external synchronization.
- **Grandmaster clock:** Within a collection of 1588 clocks, one clock, the grandmaster clock, serves as the primary source of time to which all others are ultimately synchronized.
- **Master clock:** A system of 1588 clocks may be segmented into regions separated by boundary clocks. Within each region, there is a single clock, the master clock, serving as the primary source of time. These master clocks turn synchronize to other master clocks and ultimately to the grandmaster clock.
- **Ordinary clock:** An ordinary clock is a 1588 clock with a single PTP port.
- **Preferred master clock set:** 1588 allows for the definition of a set of clocks that are favored over those not so designated in the selection of the grandmaster clock.
- **PTP:** PTP is an acronym for **P**recision **T**ime **P**rotocol, the name used in the standard for the protocol.
- **PTP domain:** A PTP domain is a collection of one or more PTP subdomains. A subdomain is a logical grouping of 1588 clocks that synchronize to each other using the PTP protocol, but that are not necessarily synchronized to PTP clocks in another PTP subdomain. Subdomains provide a way of implementing disjoint sets of clocks, sharing a common network, but maintaining independent synchronization within each set.
- **PTP message:** There are five designated messages types defined by 1588: Sync, Delay_Req, Follow-up, Delay_Resp, and Management. Multicast communication: 1588 requires that PTP messages be communicated via a multicast. In this style of communication, any node may post a message and all nodes in the same segment of a subdomain receive this message. Boundary clocks define the segments within a subdomain.

- **Synchronized clocks:** Two clocks are synchronized to a specified uncertainty if they have the same epoch and measurements of any time interval by both clocks differ by no more than the specified uncertainty. The timestamps generated by two synchronized clocks for the same event differ by no more than the specified uncertainty.

14.2.7 PTP and Master/Slave

When using PTP in combination with Master/Slave synchronization, these two synchronization protocols interact. The MS master synchronizes to the PTP master clock and the MS slaves follow their MS Master.

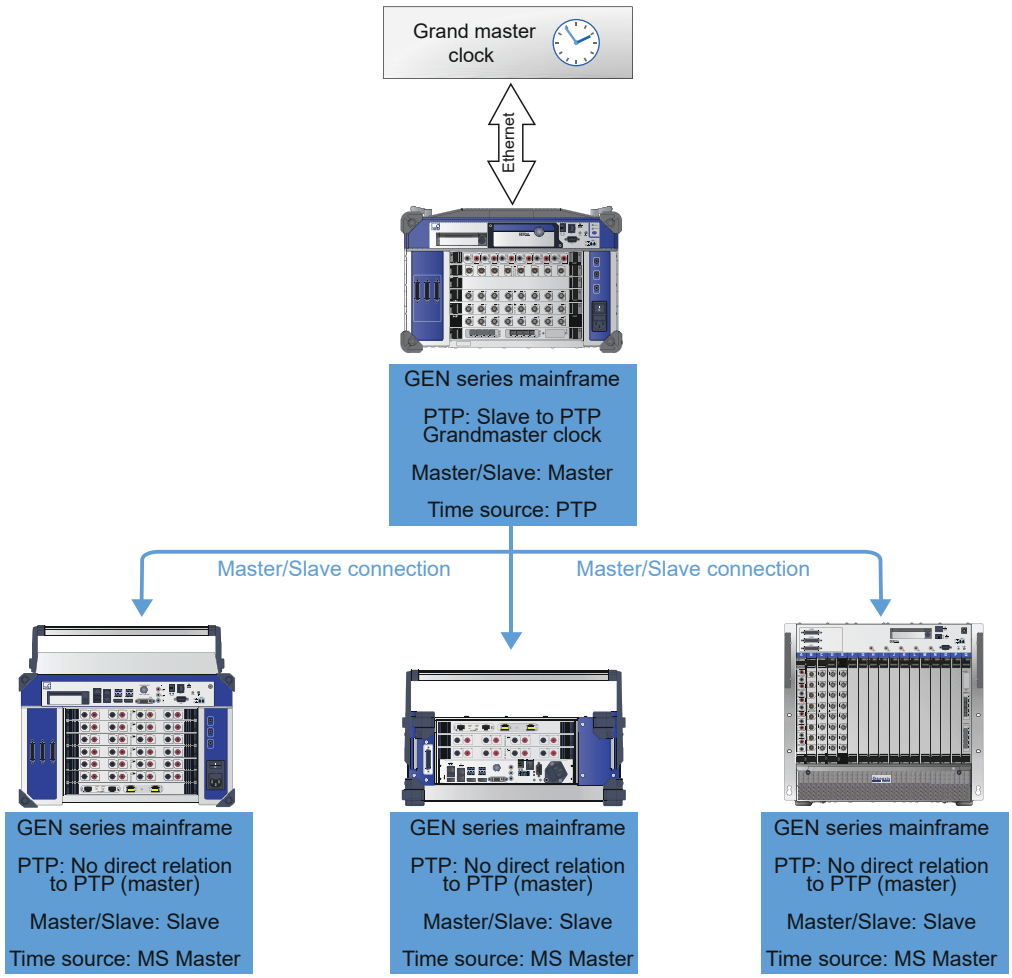


Figure 14.10: Grandmaster clock with Master/Slave connected Slaves

The PTP synchronization process “oscillates” due to a certain control strategy. To align PTP synchronization and Master/Slave synchronization the amount of oscillation in this PTP synchronization process needs to be sufficiently large. In fact, this required oscillation range exceeds the tightest PTP tolerance of 150 ns. Therefore, once a mainframe is set to be a MS Master, the PTP tolerance will be fixed to 1000 ns*.

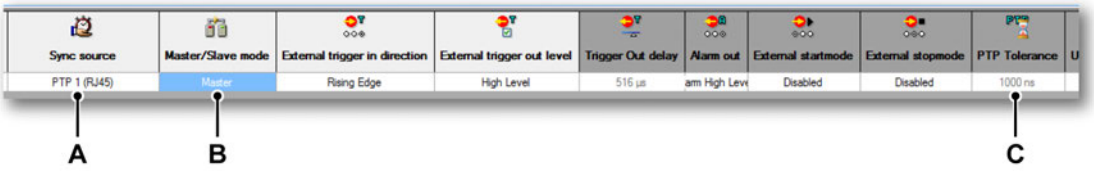


Figure 14.11: Fixed PTP tolerance

A Sync source: PTP (or GPS OTMC 100)

B Master/Slave mode: Master

C PTP Tolerance: fixed 1000 ns

Note ** When selecting IRIG GMR1000 as **Sync source**, this will always fix the **PTP tolerance** to 2000 ns, independent of stand-alone or being MS Master, due to the nature of the IRIG synchronization signal jitter.*

14.3 GPS

14.3.1 Installation

When connecting the GPS antenna to the mainframe, please follow the steps described below.

IMPORTANT

As the GPS antenna is typically placed on a roof or otherwise hard to access position, it is highly recommended to connect the GPS antenna to the PoE injector and plug the injector into mains. Please refer to the LED overview to verify that the GPS antenna is properly powered and optionally connect to the web client to verify the GPS antenna is fully operational.

1 Place the GPS antenna in a position with clear view to the sky. For more information, please refer to chapter "GPS antenna placement" on page 296.

1A **Test:** Power the antenna temporarily and verify if satellites can be found using the antenna's web interface.

Note *For this test, the antenna should be connected directly to a PC, not the GEN series mainframe.*

2 Create outdoor/indoor pass through, ensure enough space is available to position the Surge Protector.

Note *Make sure the wall pass through is clean and does not contain sharp edges or objects that may damage the cable.*

3 Place the Optical Ethernet power over Ethernet Injector (PoE) and connect to mains power.
Verify that the power LED is lit.

4 Make sure the section of cable between the Surge Protector and PoE injector that is outside of the wall is as short as possible.

Note *Make sure the fiber optic cables do not break or get damaged when connecting.*

WARNING

It is highly recommended that the Surge Protector grounding is lightning proof.

5 Connect the cable from the PoE injector to the GEN series mainframe PTP enabled fiber optical Ethernet port.

6 After finishing these steps the G002B option is fully installed and operational. Please refer to for an overview of the installed option.

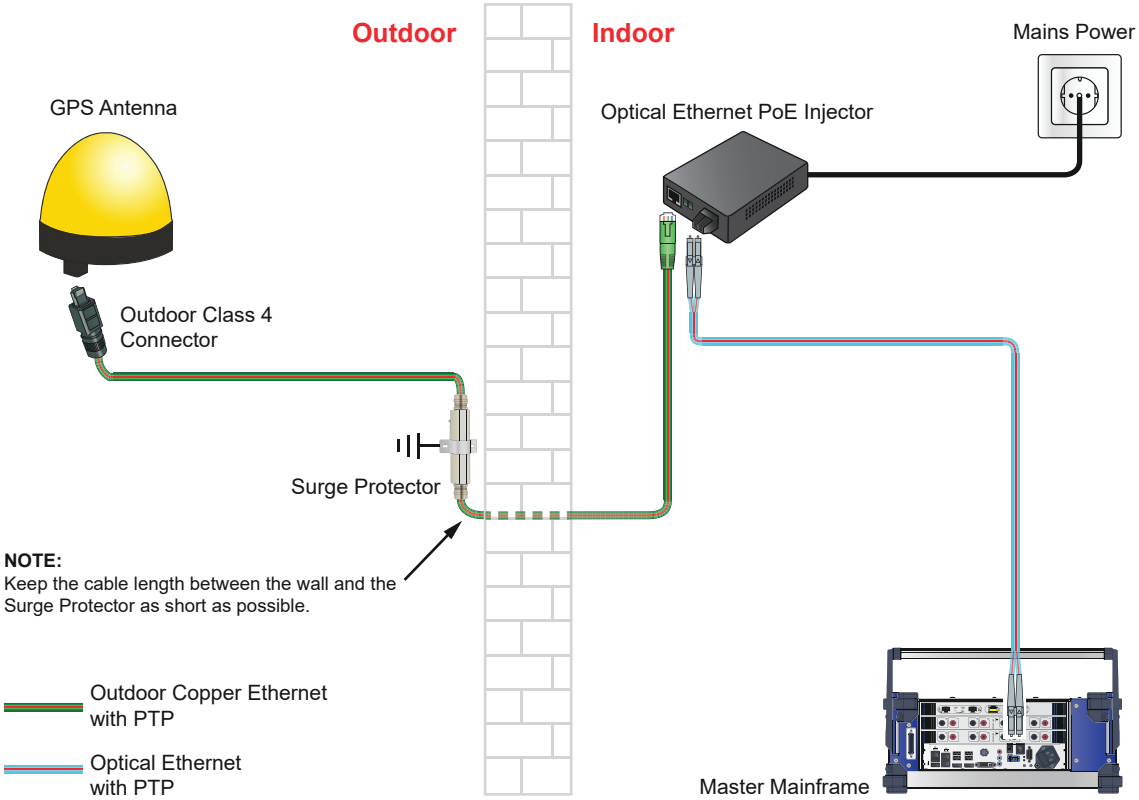


Figure 14.12: Block diagram GPS time synchronization

14.3.2 Using the GPS antenna

The antenna used in G002B uses GPS as a time source and acts as a PTP master clock for the rest of the system (see Figure 14.13).

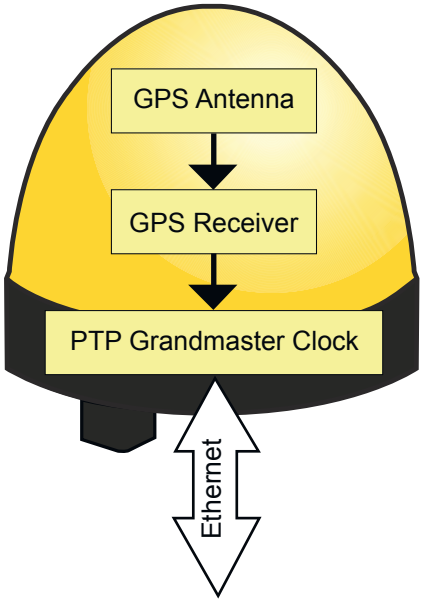


Figure 14.13: GPS antenna architecture

Note *This means that most references in the system setup are **PTP** related, and not **GPS** related.*

Perception setup

To perform time synchronized data acquisition using GEN series mainframes and the G002B option it is necessary to further setup the system. This section explains how to accomplish that using the **HBM Perception Data Acquisition** software.

Note *This section assumes you are familiar with basic operations in Perception such as connecting to data acquisition hardware and changing settings.*

Note *G002B requires usage of Perception version 7.00 or higher.*

1 Start Perception

2 Connect to the mainframe.

3 Open the settings sheet and select advanced settings:

3a In the main menu select **Settings**.

3b In the Settings menu select **Show Settings ►**.

3c In the submenu select:

- **Basic:** this will show only the relevant settings
- **Advanced:** this will show all settings

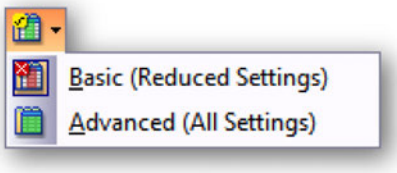


Figure 14.14: Perception settings sheet options

4 In the **Sync source** column select the required PTP option.

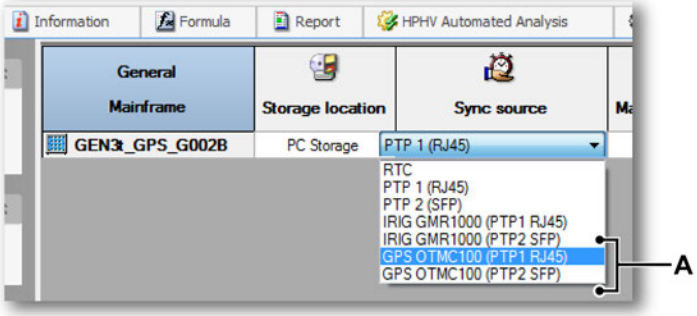


Figure 14.15: Sync source selection

A **GPS OTMC 100 (PTP1 RJ45)** and **GPS OTMC 100 (PTP2 SFP** options

Change the synchronization source to **GPS OTM C100 (PTP2 SFP)**.

Note *G002B setup: Using the fiber optic Ethernet connection provides maximum system safety against lightning impact,in this case select GPS OTMC 100 (PTP2 SFP).*
If a standard RJ45 Ethernet cable is used, select GPS OTMC 100 (PTP1 RJ45).

5 The acquisition system tries to find and synchronize to the PTP signal. The system status goes through the following states:

- No signal
- Out of synchronization
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

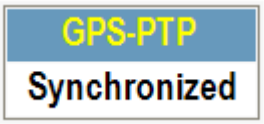


Figure 14.16: GPS-PTP status - Synchronized

6 The GPS antenna acts as a highly accurate PTP master in the network, therefore enable **Use Accurate Master** to ensure that a warning appears if another another PTP node becomes the master in the network (see Figure 14.17).

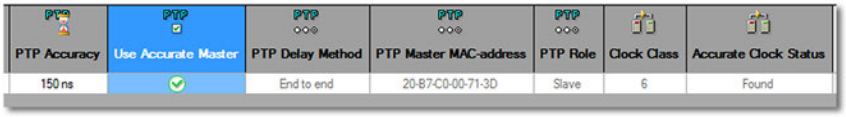


Figure 14.17: PTP - Use Accurate Master

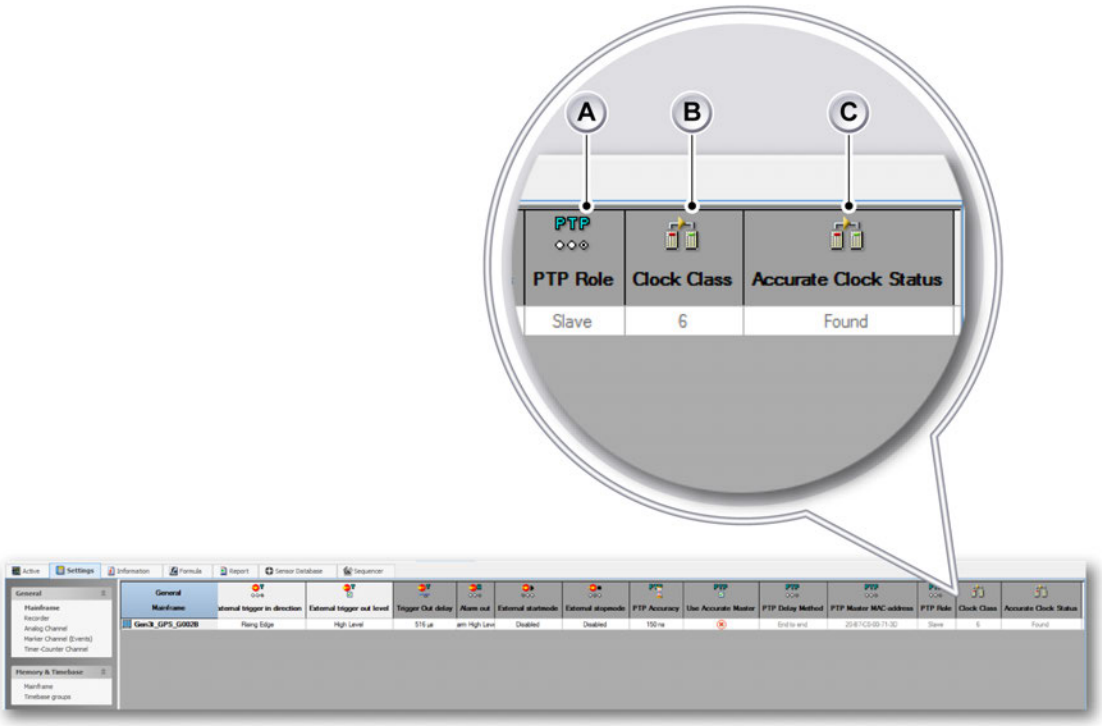


Figure 14.18: PTP synchronization status

Please verify the following settings:

A **PTP Role:** Slave

B **Clock Class:** 6

C **Accurate Clock Status:** Found

Verify setup and installation

Once the setup is complete there are several steps that can be taken to verify if the setup was successful.

Status information

The overall system time base information is displayed in the status window. This will give a system wide overview showing the most imprecise time source from all connected mainframes.

Note *As all mainframes are expected to be on PTP, the status should show PTP, and should have the default colors blue and white (see Figure 14.19).*

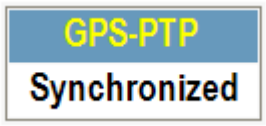


Figure 14.19: GPS-PTP status - Synchronized

Note *In case the status shown is orange / red a problem has occurred, please refer to the “Troubleshooting” chapter (on page 299) for detailed information.*

System topology

An overview can be found in the system topology overview. The system topology will show the information per connected mainframe.

1 In the menu bar choose **Help ► System Topology** (see Figure 14.20).

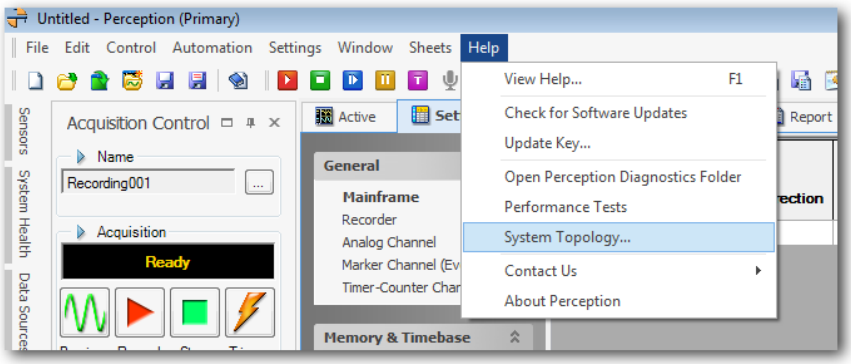


Figure 14.20: System Topology Help

2 The **System Topology** overview opens (see Figure 14.21):

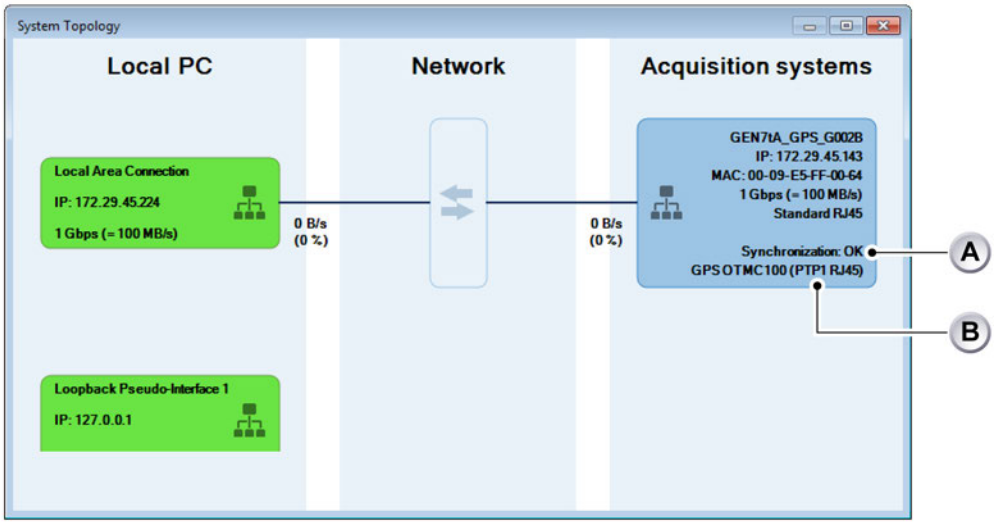


Figure 14.21: System Topology

In **System Topology** overview, please verify the following information:

A States that **Synchronization** is OK

B States that **GPS OTMC 100** is connected as selected (**PTP1 RJ45** for RJ45 connection as shown in Figure 14.21, **PTP2 SFP** if you are using the optical Ethernet connection).

Note *Network peripherals such as switches and routers are not visualized within the network topology overview.*

Recording information

When a recording is created using PTP time synchronization, the PTP master clock information is available in the recorded information in the Yt display in Perception (see Figure 14.22).

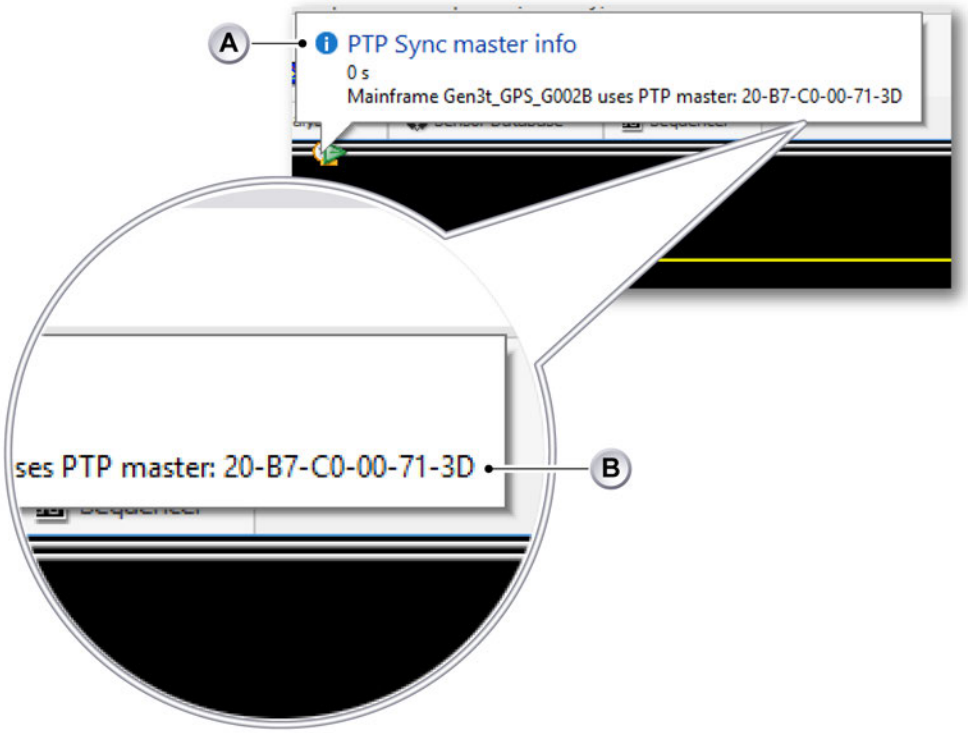


Figure 14.22: PTP synchronization master information

A PTP master clock information

B PTP master MAC adress

Note *Please refer to the “Trouble-shooting” chapter "Trouble-shooting guide for G002B" on page 299 in case this information is not shown or is not correct.*

Complex setups

- G002B: GPS Receiver with Master/Slave connected Slaves (see Figure 14.23)
- G002B: GPS receiver with tethered mainframes plus QuantumX (see Figure 14.29)

Complex setup: G002B: GPS Receiver with Master/Slave connected Slaves

It is possible to create synchronized recordings between multiple GEN series mainframes using a single GPS antenna. This section explains how to setup this configuration and what the benefits and limitations are.

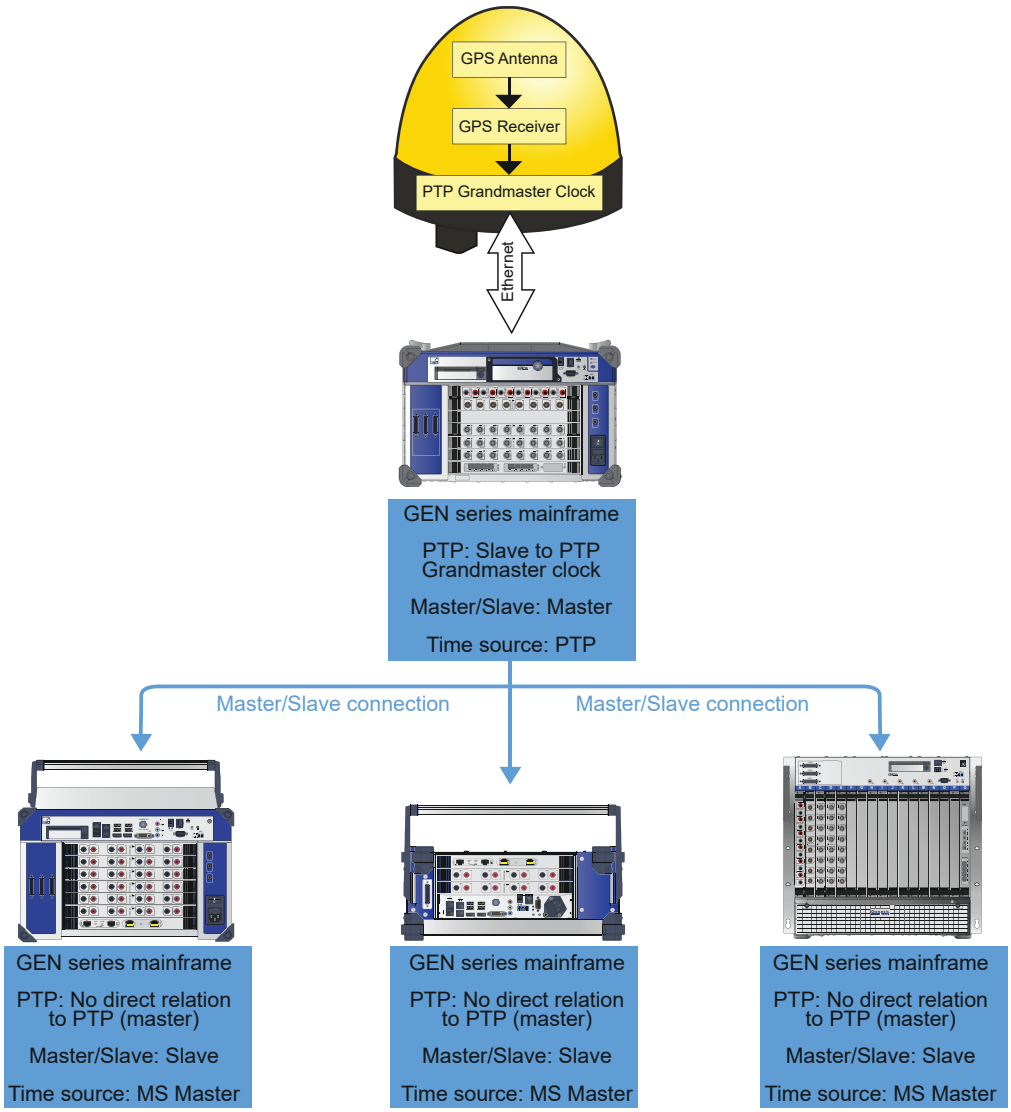


Figure 14.23: GPS Receiver with Master/Slave connected Slaves

Installation

1 Connect the Master mainframe to the G002B GPS antenna and verify if it is operating correctly as explained in the earlier chapters.

2 Connect the Master/Slave optical cables between the Master mainframe and the Slaves (For more information, please refer to "Connecting the Master/Slave Synchronization connector" on page 163).

3 Set the Master/Slave mode to Master for the mainframe connected to the GPS (see Figure 14.24).

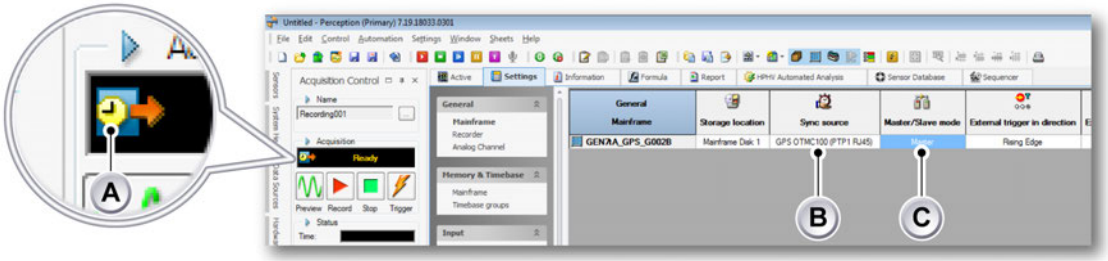


Figure 14.24: Settings for Master/Slave mode to Master in Perception

A This icon indicates that the mainframe is the Master in the Master/ Slave setup.

B The sync source is set to GPS OTMC 100 during the G002B setup.

C This indicates the role in the Master/Slave setup, should be Master.

4 Set the Master/Slave mode to Slave for the mainframes connected to the Master mainframe. It will go through these stages:

- **No master** (see Figure 14.25)
- **Searching for master** (see Figure 14.26)
- **Master detected** (see Figure 14.27)

No master

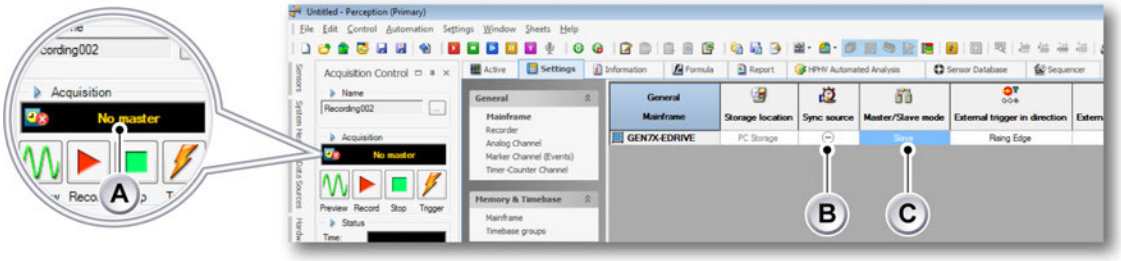


Figure 14.25: Status - No master detected

A This icon indicates that there is currently no Master found on the Master/Slave bus.

B The Sync source is not relevant for the Slave; the time source is the Master in the Master/Slave mode.

C This indicates the role in the Master/Slave setup, should be Slave

Searching for Master

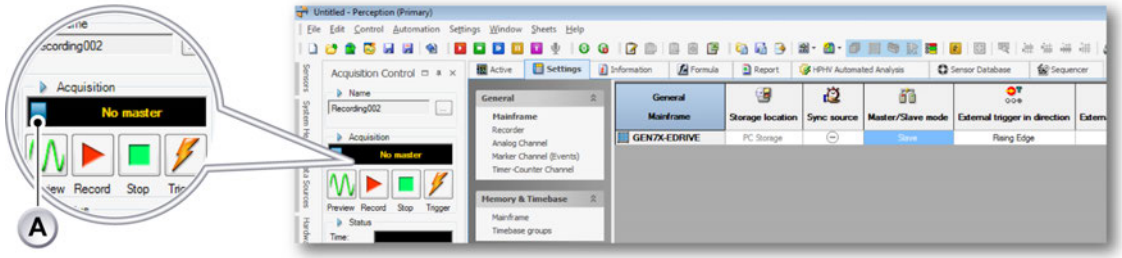


Figure 14.26: Status - Searching for Master

A After a short period, the icon **(A)** starts blinking. This indicates that the Slave system is searching for a Master mainframe on the Master/Slave bus.

Master detected

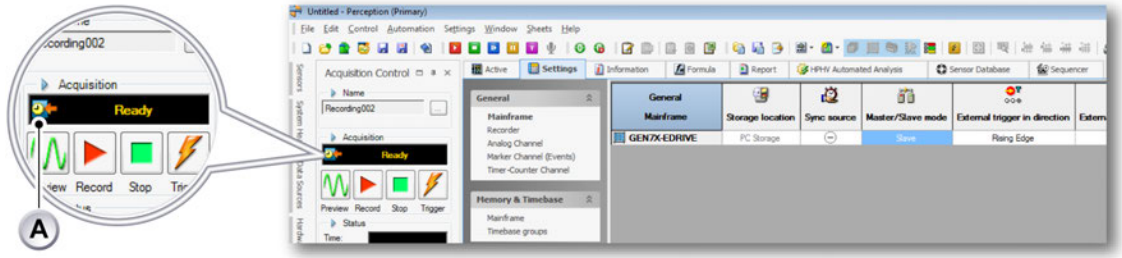


Figure 14.27: Status - Master detected

A Once the Master is found, the icon **(A)** will change indicating the Master is now the time source. In case no Master is detected it will go back to the **No Master** mode.

(For more details of Master/Slave operation in the Perception software, please see "Setting the Master/Slave operating modes" on page 165).

Note *In case of multiple Slaves, the worst-case status will be shown. So, if one of the Slaves is not properly connected,* ***No Master*** *will be reported.*

Conditions and constraints

Additional GEN series hardware is required to synchronize more than two mainframes. For more information, please refer to "Master/Slave Synchronization" on page 159.

Note *It is only possible to synchronize GEN series mainframes through the Master/Slave bus. No support for QuantumX modules or other data acquisition hardware.*

Connection overview

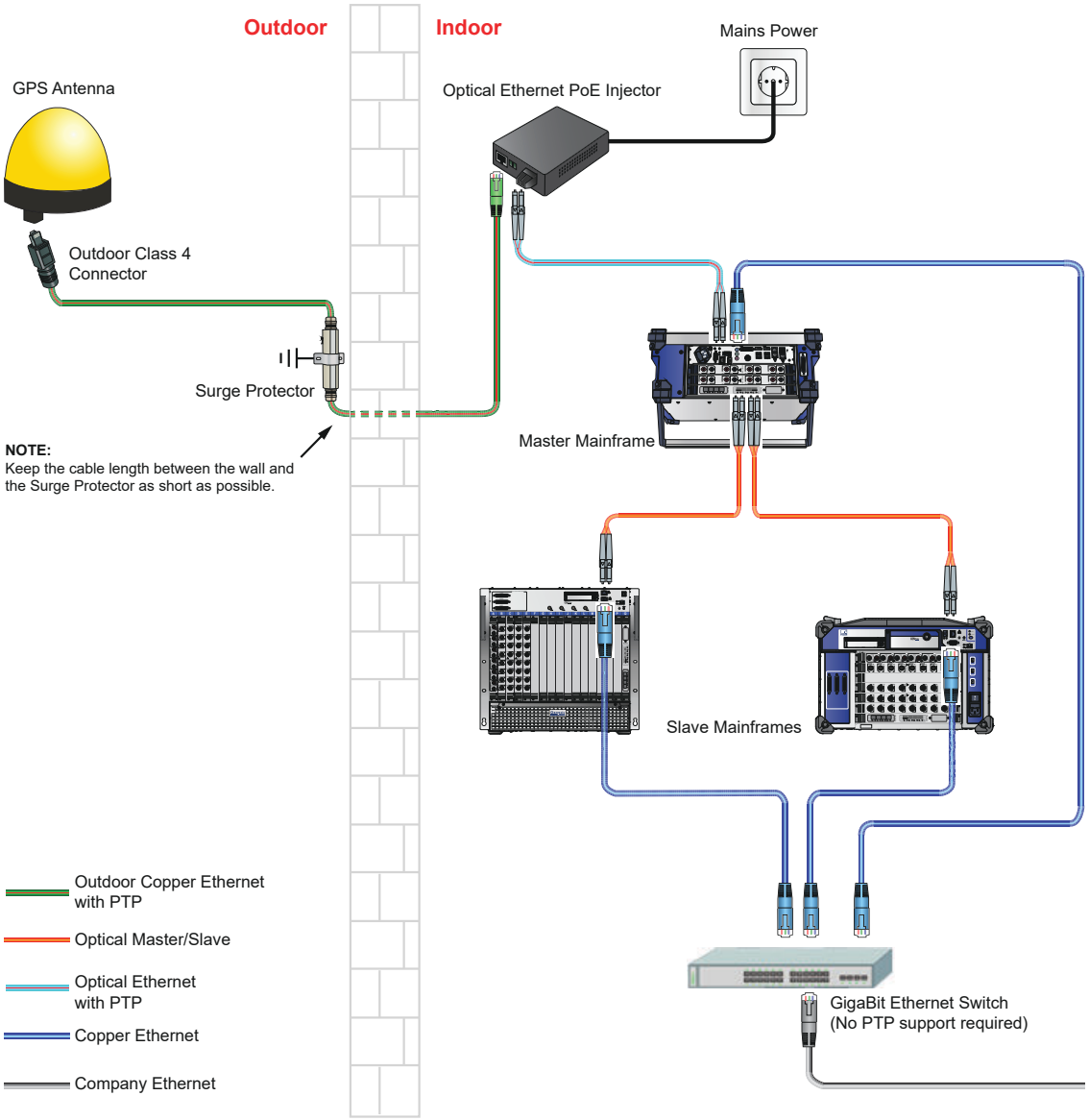


Figure 14.28: GPS setup for tethered mainframe with Master/Slave connected Slaves

Complex setup: G002B: GPS receiver with tethered mainframes plus QuantumX

When using other data acquisition hardware besides GEN series mainframes, it is not possible to connect everything through the Master/Slave mechanism. In this case, using PTP allows multiple mainframes to synchronize against a single GPS antenna.

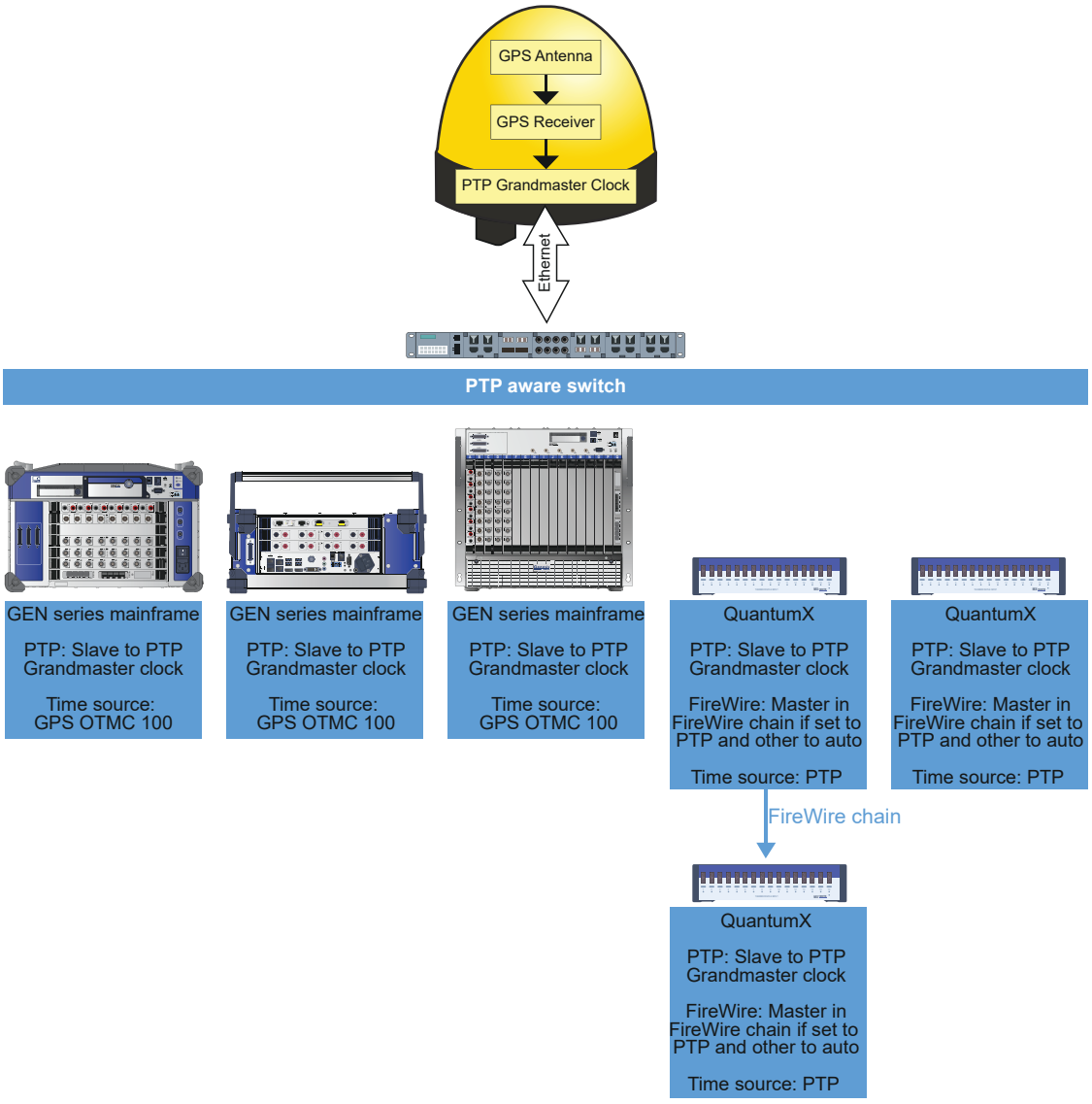


Figure 14.29: GPS receiver with tethered mainframes plus QuantumX

Installation

When connecting the GPS antenna to the mainframe, please follow the steps described below.

IMPORTANT

As the GPS antenna is typically placed on a roof or otherwise hard to access position, it is highly recommended to connect the GPS antenna to the PoE injector and plug the injector into mains. Please refer to the LED overview to verify that the GPS antenna is properly powered and optionally connect to the web client to verify the GPS antenna is fully operational.

1 Place the GPS antenna in a position with clear view to the sky. For more information, please refer to chapter "GPS antenna placement" on page 296.

1A **Test:** Power the antenna temporarily and verify if satellites can be found using the antenna's web interface.

Note *For this test, the antenna should be connected directly to a PC, not the GEN series mainframe.*

2 Create outdoor/indoor pass through, ensure enough space is available to position the Surge Protector.

Note *For this test, the antenna should be connected directly to a PC, not the GEN series mainframe.*

Note *Make sure the wall pass through is clean and does not contain sharp edges or objects that may damage the cable.*

3 Place the Optical Ethernet power over Ethernet Injector (PoE) and connect to mains power.
Verify that the power LED is lit.

4 Make sure the section of cable between the Surge Protector and PoE injector that is outside of the wall is as short as possible.

Note *Make sure the fiber optic cables do not break or get damaged when connecting.*

WARNING

It is highly recommended that the Surge Protector grounding is lightning proof.

5 Connect the cable from the PoE injector to the PTP switch.

6 Connect the cable between the mainframe RJ45 PTP aware connector and the PTP switch. Repeat this step for all mainframes that need to synchronize to the GPS antenna.

7 After finishing these steps the G002B option is fully installed and operational (see also Figure 14.30).

Connection overview

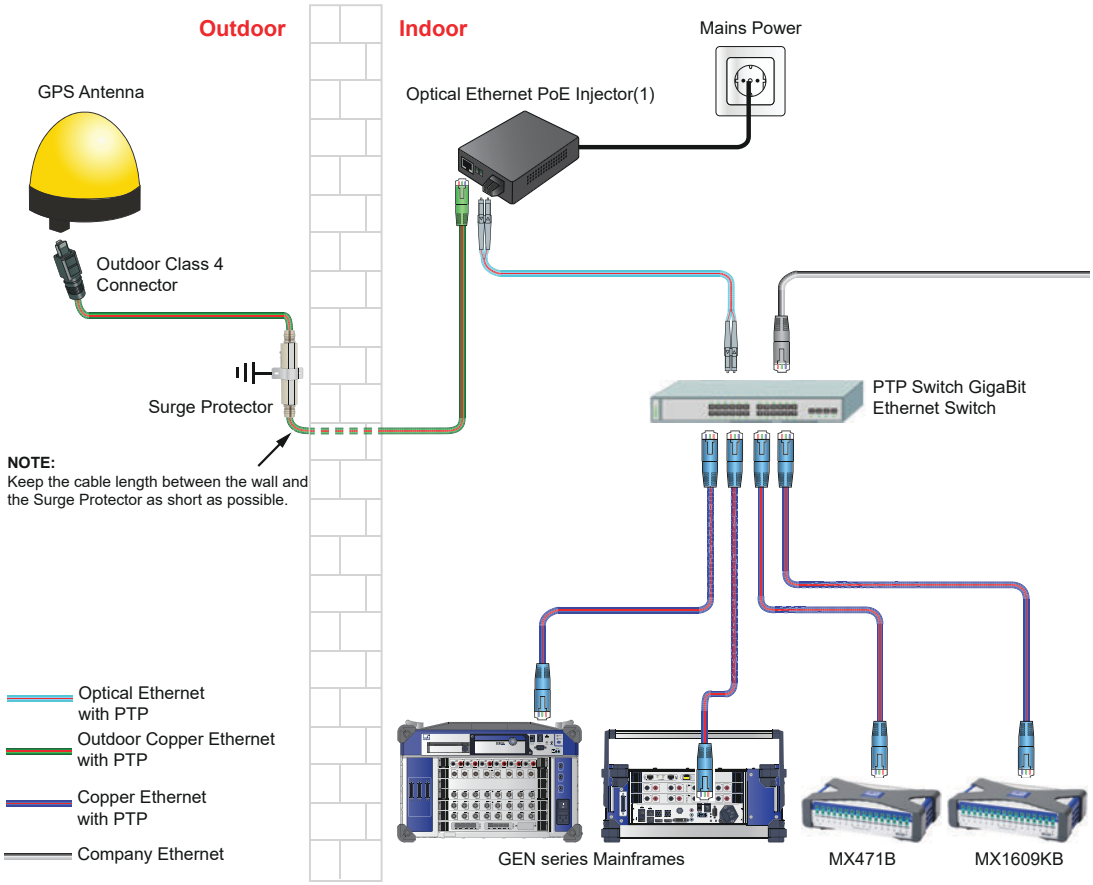


Figure 14.30: GPS setup for tethered mainframes and QuantumX

(1) Ethernet PoE injectors using dual RJ45 electrical connections can be ordered through customs systems. Contact custom systems at: customsystems@hbm.com

For more information about QuantumX and GEN series mainframes, please refer to chapter "Synchronizing GEN series and QuantumX using PTP" on page 827.

14.3.3 Setup comparison

Synchronization characteristic	G002B directly to mainframe	G002B with Master/Slave connected mainframes	G002B with Tethered mainframes
Accuracy	150 ns to UTC	150 ns to UTC	150 ns to UTC
Geographical distribution	Worldwide	Limited to the Master/Slave range	Limited to the PTP network range
Scalability	Unlimited	Up to 128 mainframes No QuantumX	Depends on the PTP network setup. Supports QuantumX **Note** *Can be combined with Master/Slave to extend scalability*
Complexity	Low	Medium Requires Master/ Slave setup	High Requires correct setup of PTP network
Electrical safety	Highest Built-in Surge Protector(1) and use of fiber optical connection. No link between mainframes	High Built-in Surge Protector(1) and use of fiber optical connection.	Depends on PTP network
Cost	High Each mainframe requires a PTP master	Low One Master Output card needed for every four slave mainframes	Medium PTP network setup
Reliability	High No SPOF (Single Point of Failure)	Medium 2 x SPOF G002B antenna Master mainframe	Unknown 1x known SPOF G002B antenna + PTP aware network

(1) **Note** *Surge Protector grounding must be lightning safe.*

14.3.4 GPS antenna placement

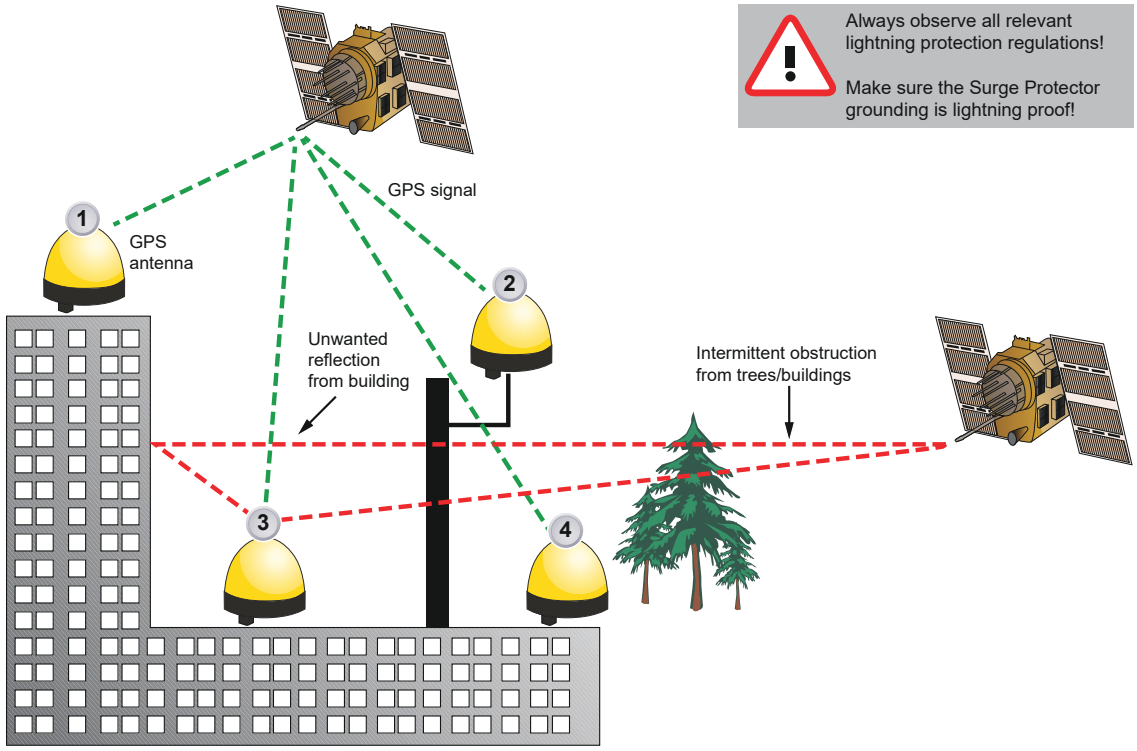


Figure 14.31: Recommended GPS antenna positions

BEST mounting position with best possible reception of GPS signals.
This mounting position provides direct view to the sky. The view is not hindered by any objects and the GPS signals are not influenced by any reflections.

POSSIBLE mounting position on pole providing sufficient reception of GPS signals under most conditions. This mounting position provides direct view to the sky in a range nearly 180°. The view is only partly hindered and there is negligible danger of reflections that could influence the GPS signals.

BAD mounting position. Do not use!
This mounting position provides direct view to the sky for a range only 90° Half the sky is blocked by the taller part of the building and the reception of GPS signals will be considerably influenced by reflections. The *OTMC 100* will not work properly!

NOT RECOMMENDED mounting position. Only use if no other mounting position is available.
This mounting position provides direct view to the sky for a range more than 90° but much less than 180°. The view to the left is hindered by the taller part of the building and there is an increased danger of reflections that could influence the GPS signals.

Note *Mount the OTMC 100 in an upright position with the protective cap to the top only (see Figure 14.32)!*

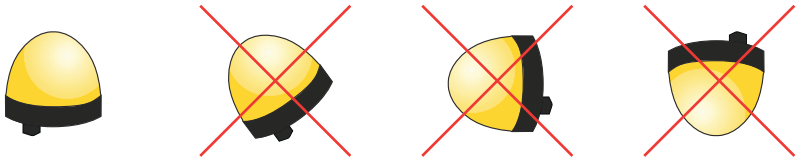


Figure 14.32: GPS antenna mounting positions

2 **Optional:** Install lightning impact protection rod near antenna.

Note *Repeat the test described in chapter "Installation" on page 278 (Step **1A**) to ensure the lightning impact rod does not obstruct satellite detection.*

14.3.5 GPS antenna lightning protection

WARNING

It is highly recommended to apply lightning protection such as a lightning rod to the placement of the GPS antenna (see Figure 14.33).

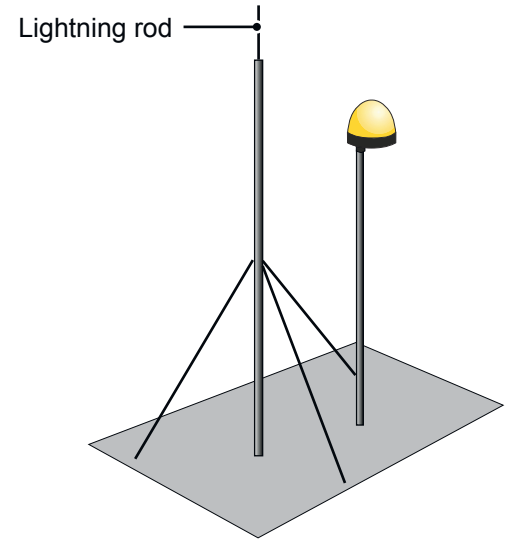


Figure 14.33: GPS antenna with applied lightning protection

14.3.6 Trouble-shooting guide for G002B

This document gives some hints on what to check if the OTMC 100 does not work as expected. It will first explain how to use Perception to determine if there is a problem and then offer help on diagnosing and solving the issue.

In case this information does not solve the problem, call your local HBM Support group.

Note *The PTP settings used in this document are displayed only in the **Advanced** settings mode of Perception.*

To open the **Advanced** settings do the following:

1. Open the settings sheet
2. In the main menu select **Settings**.
3. In the Settings menu select **Show Settings ►**.
4. In the submenu select:
   - **Basic:** this will show only the relevant settings
   - **Advanced:** this will show all settings

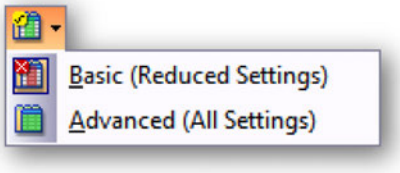


Figure 14.34: Perception settings sheet options

How to check synchronization

The synchronization status is displayed in the status window of Perception: When PTP is selected, the system status goes through the following states:

- No signal
- Out of sync
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

Note *The system status returns an overall status for all connected mainframes. To determine which mainframe(s) is causing problems, please see “Finding the system that is causing the problems” on page 303.*

Note *Please be aware that GPS synchronization may take a long time. Do not use this troubleshooting guide in case you have not waited for at least the specified synchronization time.*

The state remains at “No signal”	
Category	**Description**
Cause	The mainframe cannot find the GPS antenna.
Solution	Check these components: **1** Perception setup (see "Checking the Perception setup" on page 303) **2** GEN series network port (see "Verify the GEN series network port" on page 305) **3** PoE injector (see "Checking the SFP PoE injector" on page 308) **4** Verify that the GPS antenna is operational and functioning (see "Checking the GPS antenna" on page 314).
Recording	When starting a recording the mainframes that are in the state “no signal” run on their internal clock (RTC) and the recording is not synchronized.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “Out of sync”	
Category	**Description**
Cause	This problem can be caused by a faulty GPS antenna or malfunctioning network peripherals.

The state remains at “Out of sync”	
Category	**Description**
Solution	Check the GPS antenna and network peripherals.
Recording	When starting a recording the mainframes that are in the state “out of sync” try to follow the signal from the GPS antenna, the recording is most likely **not** synchronized. The time used in the recording is undetermined.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “NO OTMC 100”	
Category	**Description**
Cause	This problem is caused because the mainframe is synchronizing to a PTP master other than the OTMC 100.
Solution	Check the GPS antenna and network peripherals.
Recording	When starting a recording the mainframes that are in the state “NO OTMC 100” try to follow the signal from the PTP grandmaster they did find. The time used in the recording is undetermined. The PTP settings can be used to determine the synchronization source. If the PTP Role is Master, the mainframe has become the master in the PTP network. If the PTP Role is Slave, the PTP Master MAC-address can be used to determine which node in the network is the PTP master. In-depth knowledge of networking is required to obtain this information.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “Coarse”	
Category	**Description**
Cause	A network switch is causing jitter on the PTP timestamps in the network.
Solution	**1** See "PTP capable switch" on page 837 **2** Increase the PTP Accuracy, see chapter "Checking the Perception setup" on page 303.

The state remains at “Coarse”	
Category	**Description**
Recording	When starting a recording the mainframes are typically **not** synchronized within the specified accuracy. The samples at the start of the recording are expected to be synchronous within 10 times the specified accuracy, but may drift apart as the recording proceeds depending on the cause of the problem.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

Use accurate master is set, status is orange	
Category	**Description**
Cause	The mainframe is synchronized to a PTP master that has a clock class worse than 7.
Solution 1	GPS antenna is not found, the mainframe has become PTP master. Treat this the same as “No signal”.
Solution 2	Wait for approximately five minutes, the GPS antenna may still be evaluating its clock class.
Recording (different non- accurate masters)	Each mainframe operates synchronized to its master, data in the recording maybe shifted.
Recording (single non-accurate master)	The data of all mainframes are typically synchronized to the PTP master; however, some systems may apply additional sanity checks and adjust sample times when these checks fail. **Note** *This setup requires any additional network peripherals to be PTP aware.*

Finding the system that is causing the problems

The status described in the previous section is an overall system status showing the most important status in the system. To verify the synchronization details per mainframe, please refer to the chapter "System topology" on page 284.

Checking the Perception setup

The following settings can all be found in the Perception Settings (see Figure 14.35).

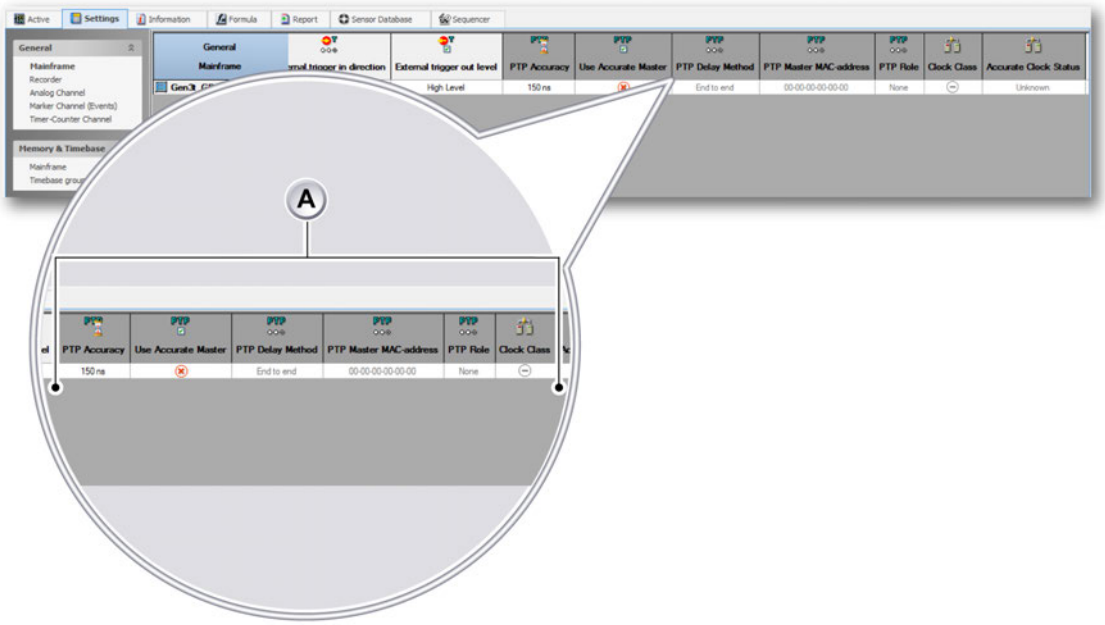


Figure 14.35: Perception General Mainframes settings

A PTP related settings in Perception General Mainframes settings

Sync source	
Network port used	**Sync source setting**
RJ45	GPS OTMC 100 (PTP1 RJ45)
Optical 1 Gbit	GPS OTMC 100 (PTP2 SFP)

PTP Accuracy
This should typically be set to 150 ns for best accuracy. **Note** *This setting only needs to be changed if a network switch without PTP support is being used and more jitter is acceptable.* **Note** *Interaction between different time synchronization types in complex set-ups may induce a fixed accuracy.*

Use Accurate Master
Ensure that “accurate master”’ setting is enabled.

PTP Role (read-only)
Verify that the PTP Role is slave. If Master is listed in this column, the GEN series mainframe itself is the master rather than the GPS antenna.

Clock Class
The clock class should be 6 (GPS clock class if the GPS antenna is synchronized).

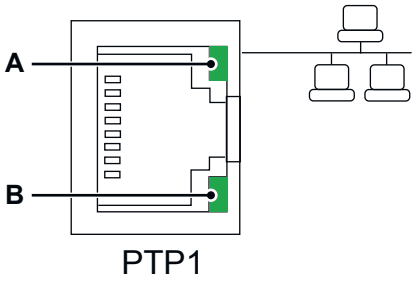
Note *If the clock class is 7, the GPS antenna is currently not locked and runs on its internal clock.*
If the clock class is 52, the GPS antenna was never synchronized.

PTP Master MAC-address
This is the GPS antenna MAC-address, or the boundary clock MAC-address when boundary clocks are used.

Verify the GEN series network port

The following section explains how the LEDs on the ports can be used to diagnose system synchronization problems. The images herein are schematic, for actual port images and positioning of the ports in the system, refer to appendix “PTP Synchronization” on page 819.

PTP1 RJ45 network connection



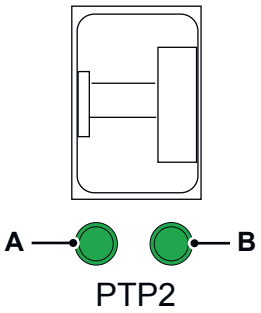
A Activity LED RJ 45 network (blinking)

B Link speed RJ45 network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	**1** Make sure the PoE injector is powered by checking the power LED. **2** Make sure PoE injector IN and OUT are correctly connected. **3** Replace the cables used to verify the cables are not causing the problem.(1)
100 or 10 Mbit/s network connection	ON	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
100 or 10 Mbit/s network connection	Blinking	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
1 Gbit/s network connection	ON	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.
1 Gbit/s network connection	Blinking	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.

(1) **Note** *In case the problem remains unsolved, contact HBM service.*

PTP2 Optical 1 Gbit network connection



A Activity LED optical network

B Link speed LED optical network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	Refer to the “Verify SFP PoE injector” section (see details on page 308). If no problem is found, swap the SFP with the SFP in the PoE injector and retry. If a problem occurs now it is related to the SFP, contact HBM Service for information on how to replace it. **Note** *In case the problem remains unsolved, contact HBM service.*
100 or 10 Mbit/s network connection	ON	OFF	See section "Optical Network (SFP)" on page 813 for additional checks.
100 or 10 Mbit/s network connection	Blinking	OFF	See section "Optical Network (SFP)" on page 813 for additional checks.
1 Gbit/s network connection	ON	ON	This is expected.
1 Gbit/s network connection	Blinking	ON	This is expected.

Checking the SFP PoE injector

The “PoE injector LEDs trouble-shooting diagram” helps to determine the connection problems (see Figure 14.37).
The LED names that are referenced in the diagram can be found on the front of the device (see Figure 14.36).

PoE injector LEDs

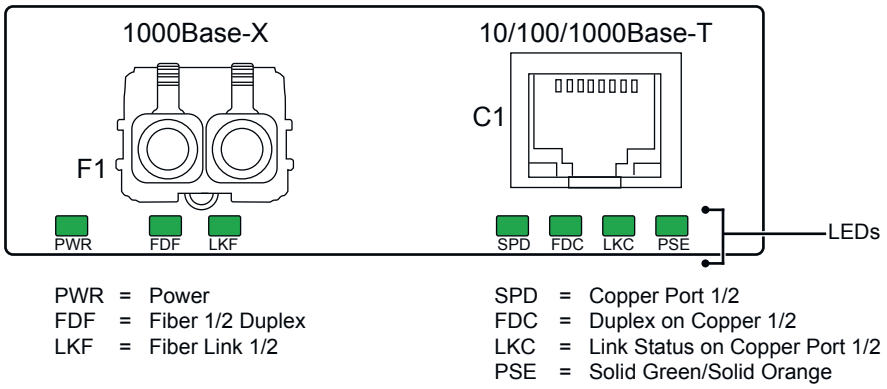


Figure 14.36: Power over Ethernet injector LEDs details

Checking the PoE injector LEDs

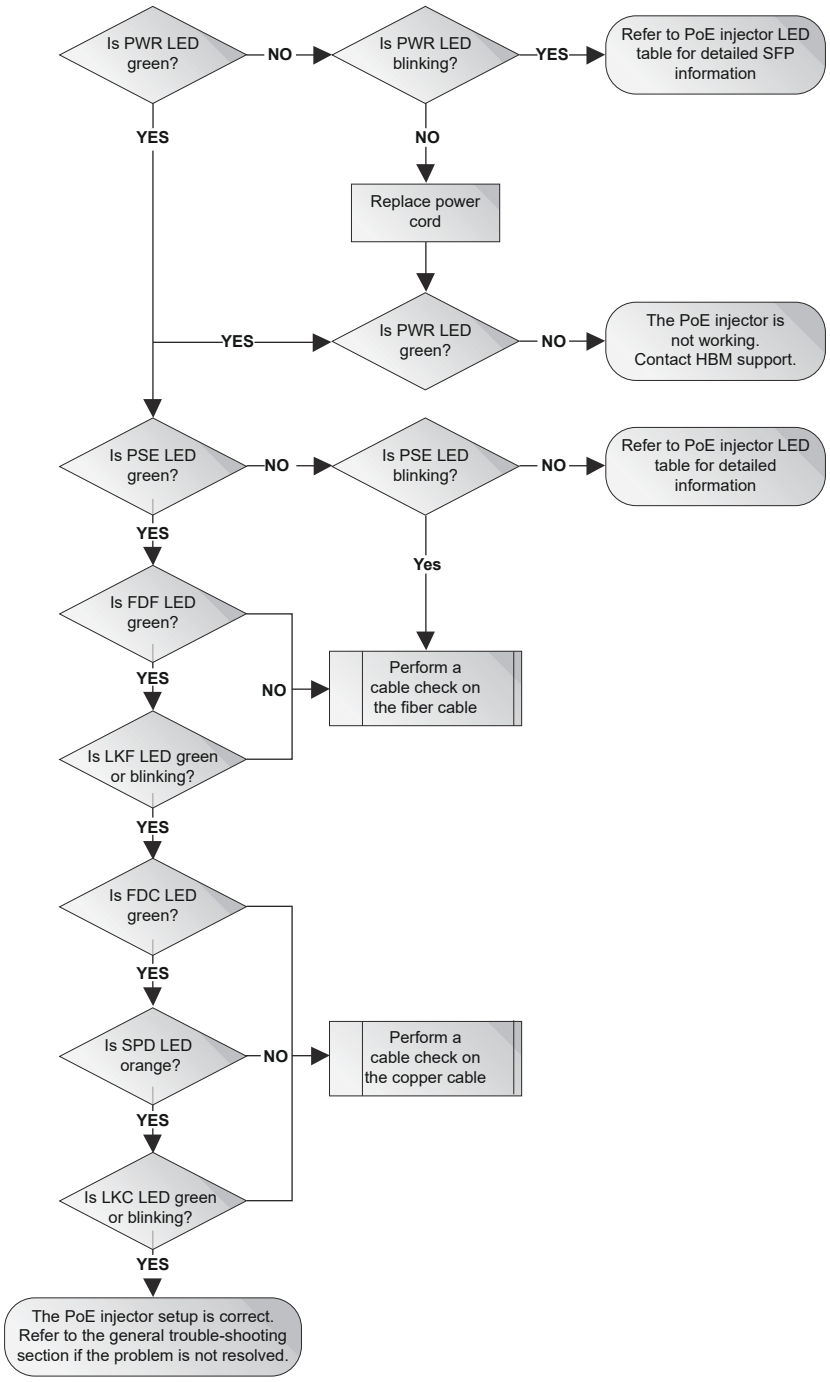


Figure 14.37: PoE injector LEDs trouble-shooting diagram

Checking PoE injector cables

When asked to check cables connected to the PoE injector, please use the following workflow to systematically rule out problems related to the network cables (see Figure 14.38).

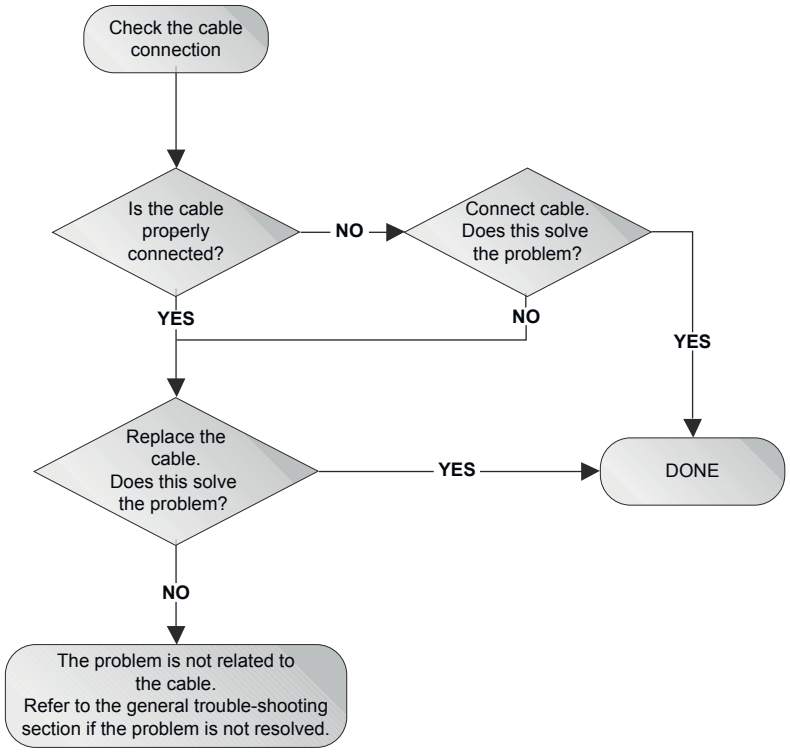


Figure 14.38: PoE injector cables trouble-shooting diagram

PoE injector settings

DIP switches can be used to configure settings on the PoE injector. All DIP switches should be in the factory default position. This means that all switches should be in the “up” position (see Figure 14.39).

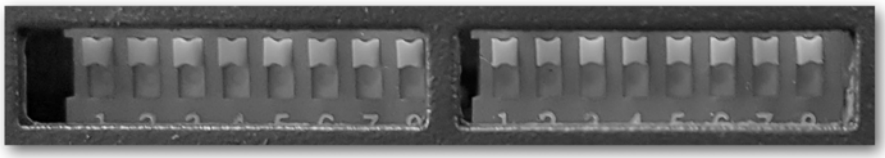


Figure 14.39: DIP switches on media converter

PoE injector LED status overview

The following tables give an overview of the LEDs' status for the PoE injector and can be used as reference. This information is an extract from the GPS antenna's manual, please refer to that manual directly for more detailed information.

Status LED

The Perle PoE/PoE +10/100/1000 rate Media convertors have status LEDs located on the front panel of the unit.

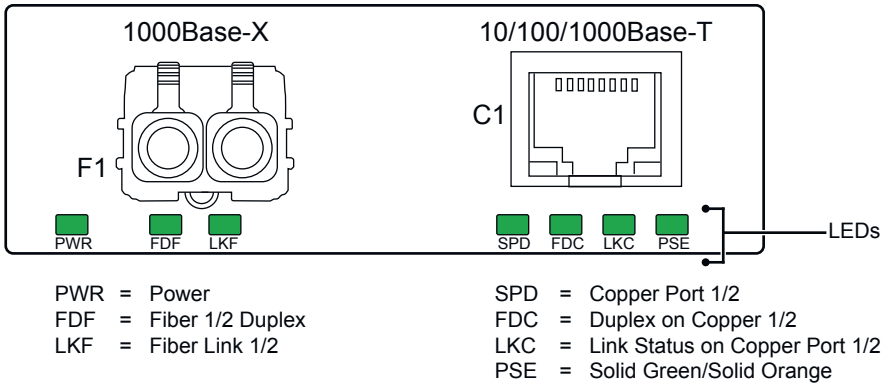


Figure 14.40: Power over Ethernet injector LEDs details

Status LED	Activity	Description
PWR	ON	Power is applied to the unit.
	Blinking (slow)	Loopback mode (one or both fiber interfaces are in loopback mode)
	Blinking (fast)	*Power ON* failure. See LED pattern table to determine pattern combination and failure cause*

***LED pattern**				
FDF	LKF	FDC	PSE	
OFF	OFF	ON	ON	SFP incompatible
All other LED patterns				Internal hardware failure

Status LED	Activity	Description
FDF-1/2 (Fiber 1/2 Duplex)	ON	Full Duplex
	OFF	Half Duplex

Status LED	Activity	Description
LKF-1/2 (Status on Fiber Link 1/2)	ON	Fiber Link is present
	OFF	No Fiber Link is present
	Blinking (slow)	Fiber Link appears functional - Fiber Link has been brought down by Smart Link pass-through
	Blinking (fast)	Fiber Link up and receiving data

Status LED	Activity	Description
SPD-(Copper port 1/2)	Green	1000 Mbps
	Orange	100 Mbps
	OFF	10 Mbps (if link is currently established)

Status LED	Activity	Description
FDC-1/2 (Duplex on Copper 1/2)	ON	Full Duplex mode
	OFF	Half Duplex mode

Status LED	Activity	Description
LKC-1/2 (Link status on Copper port 1/2)	ON	Copper link is present
	OFF	No Copper link is present
	Blinking (slow)	Copper link appears functional - Copper link has been brought down by Smart Link pass-through
	Blinking (fast)	Copper link up and receiving data

Status LED	Activity	Description
PSE-1/2	Solid green (Active)	The PSE has successfully detected a compliant PD and is applying power over the UTP
	Solid orange (Inactive)	The PSE is not active. The PSE has been configured to provide power, however ● Compliant is not detected - no power applied ● PSE has turned off power for Reset function
	OFF - (Disabled)	The PSE function is disabled in the configuration
	Error conditions A **blinking red light** is an error condition. The LED light will cycle with a three second stop interval between the error condition code.	
	Red (1 blink)	PD Capacitance too high
	Red (2 blinks)	PD Resistance too low or short circuit
	Red (3 blinks)	PD Resistance too high

Checking the GPS antenna

The status of the antenna can be checked by the LED under the antenna.

LED status	Description
Green	OK
Red	Antenna is booting
OFF	Antenna has no power
Blinking	Antenna internal problem, please refer to the GPS antenna manual for detailed information.

Using a direct connection to the PC, the status and configuration of the antenna can be viewed in more detail.

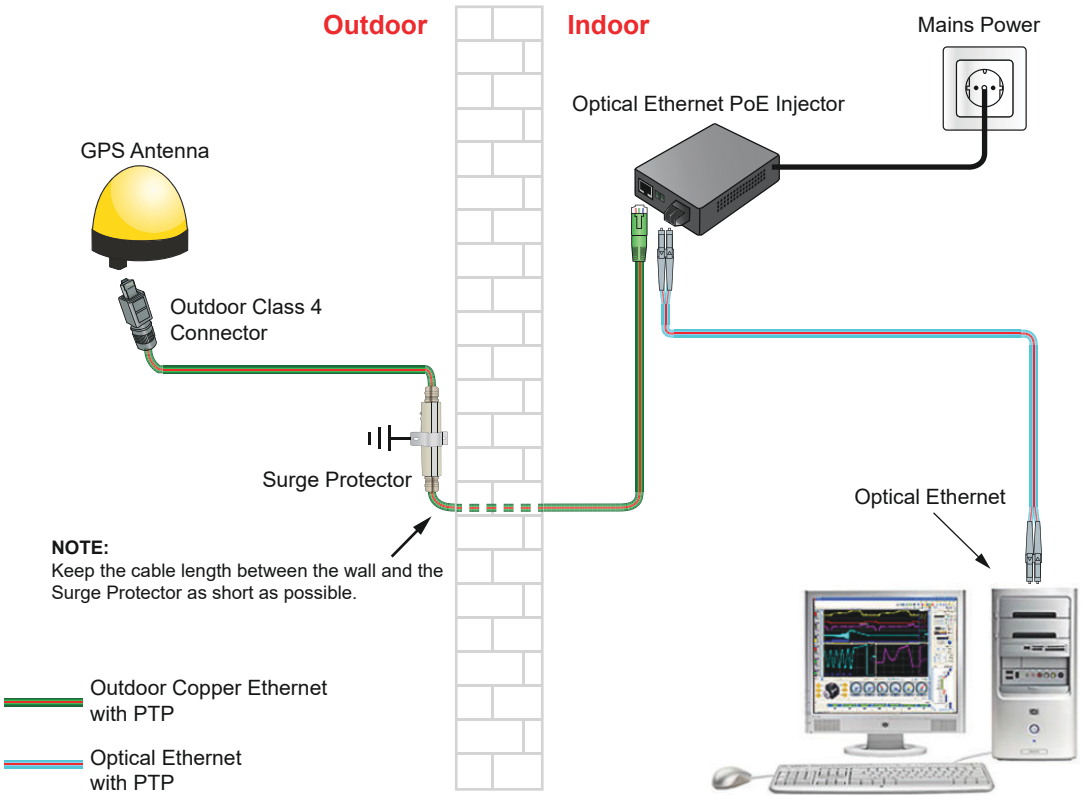


Figure 14.41: GPS antenna - PC connection (example)

Note *Use an RJ45 to RJ45 PoE injector to make a direct connection to a PC if the PC does not contain an optical network port.*

The Omnicron® device browser (for the OTMC GPS antenna) has to be installed on the PC, refer to the GPS antenna manual for detailed instructions on how to install and use the software.

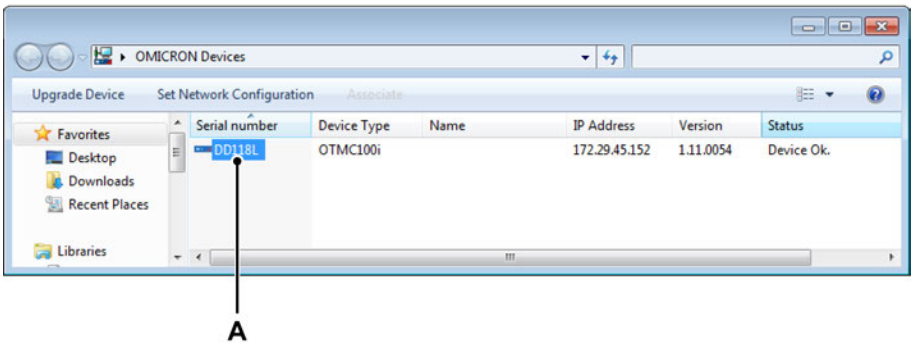


Figure 14.42: Omnicron® device browser

A Omnicron® GPS antenna OTMC 100*i*

Right-click on the device to open the web browser (see Figure 14.43).

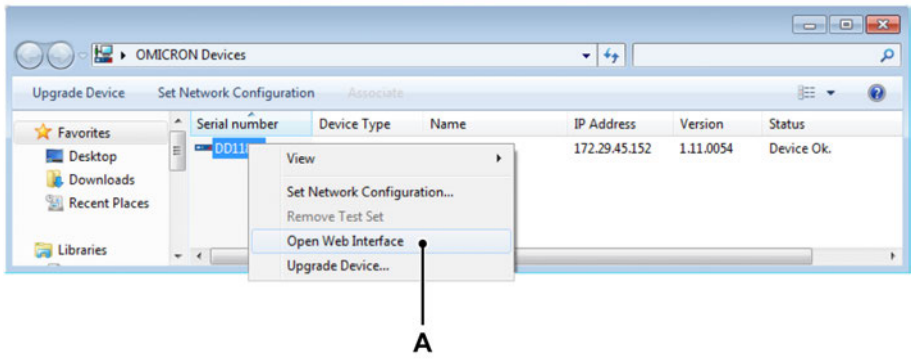


Figure 14.43: Opening Omnicon® web interface

A Web inferface configuration for GPS antenna

The details of the **Web Interface** are explained in the next section.

Verify the PTP Master MAC-address

In **Overview** ► **Network** option, the MAC address is shown (see Figure 14.44).

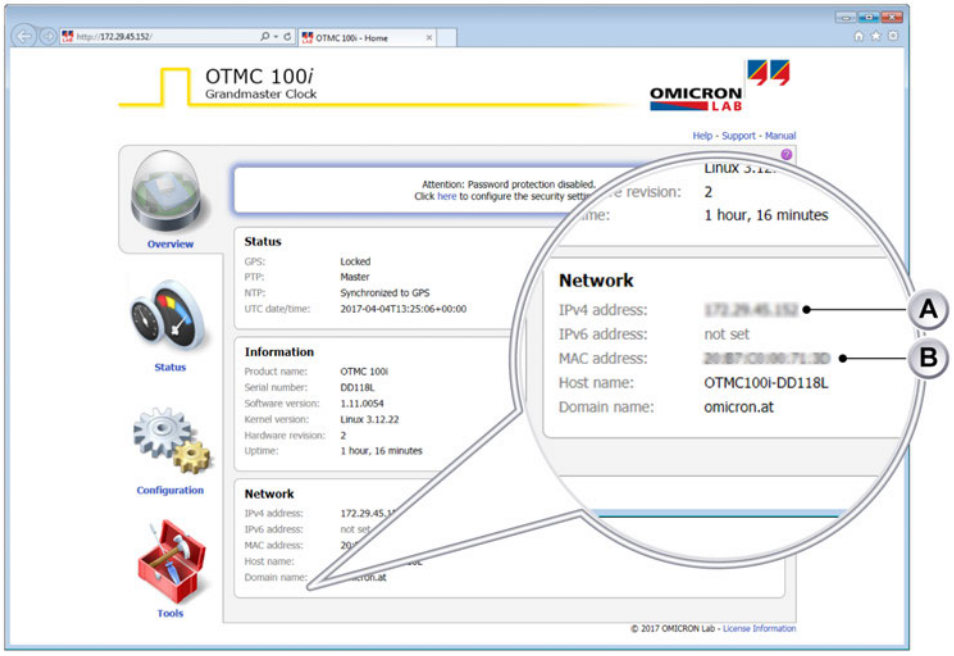


Figure 14.44: OTMC 100 MAC/IP address

A IP address

B MAC address

Verify the usable GPS antenna satellite reception

In **Status ► GPS** option, a minimum of six satellites is recommended for proper PTP operation (see Figure 14.45).

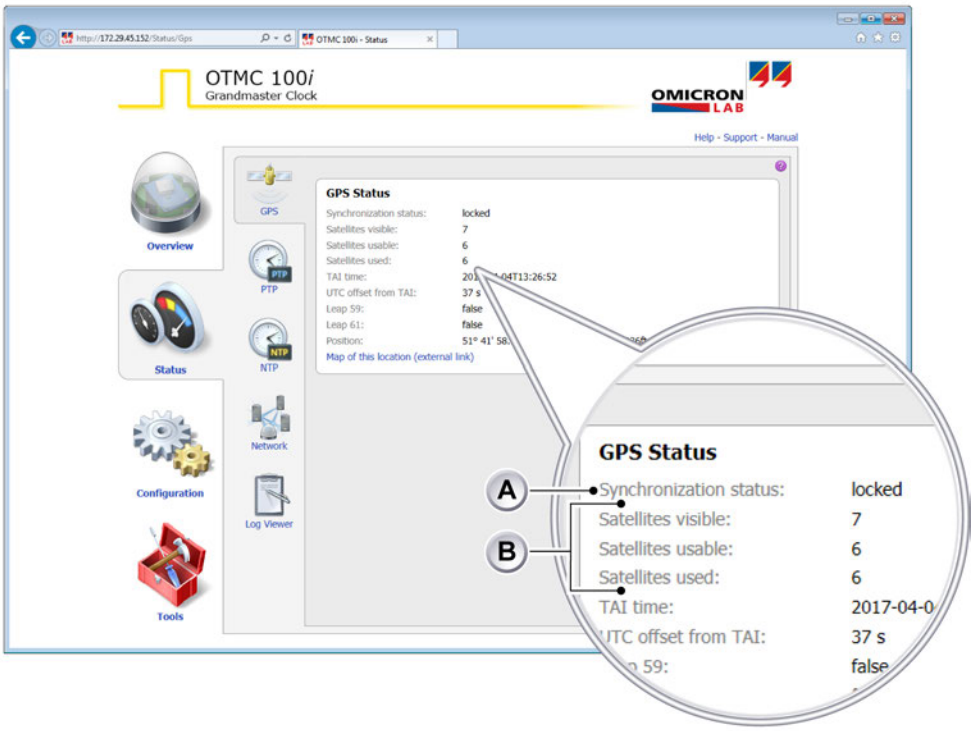


Figure 14.45: OTMC 100 GPS status information

A GPS/Synchronization status

B GPS status of satellites

PTP Settings

The antenna should work with Perception using the factory default settings, however it is possible to change the PTP settings. An overview of the actual PTP settings can be found in the PTP options (see Figure 14.46).

In **Status ► PTP** option, the settings should match the values shown in the image below (see Figure 14.46) for the **Port** and **Default** sections. The only exceptions are **Profile ID** and **Clock identify** as these may vary per antenna and their value does not affect the PTP protocol operation.

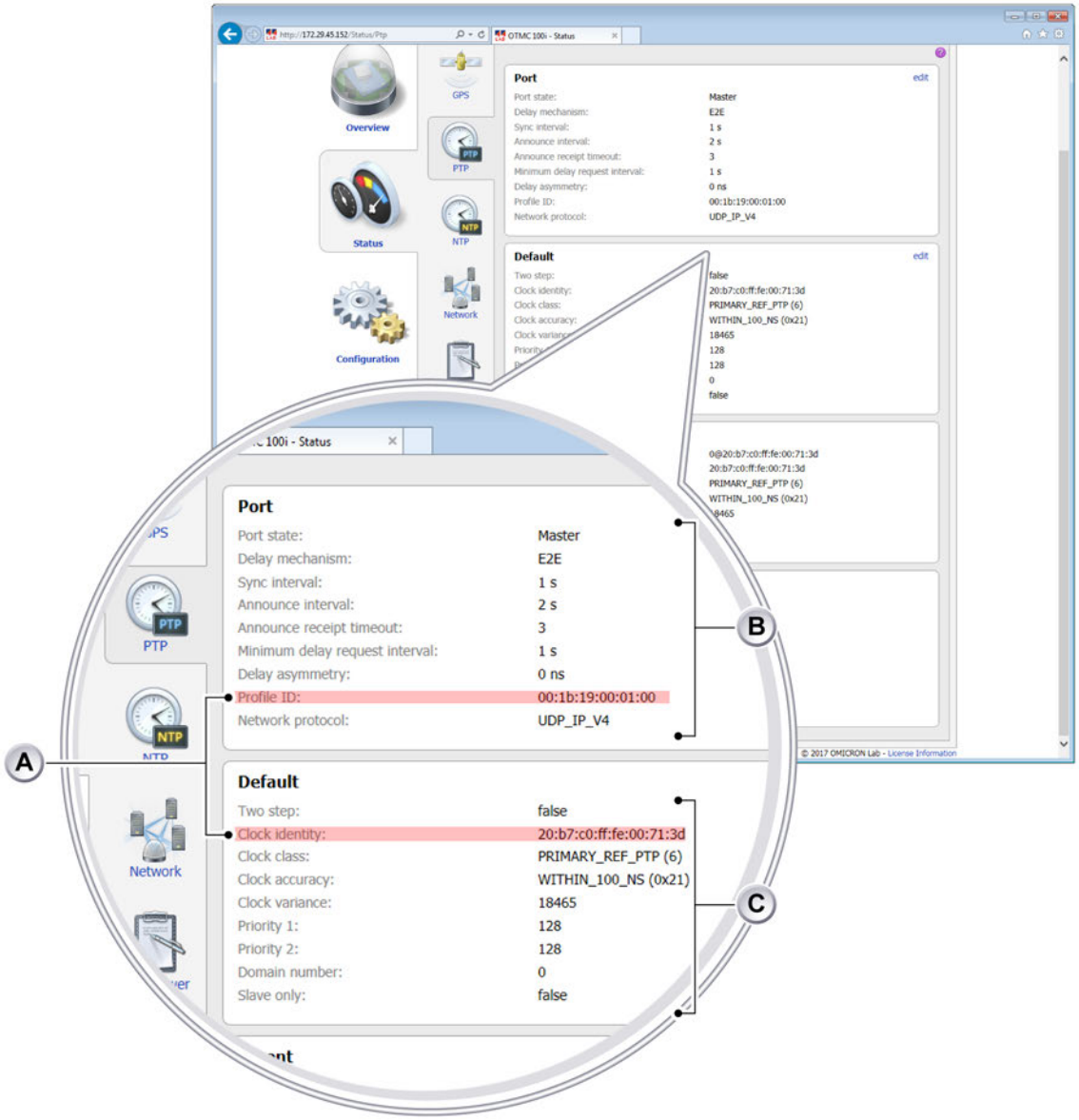


Figure 14.46: OTMC 100 PTP status information

A **Port**: **Profile ID** may vary per antenna.
Default: **Clock identify** may vary per antenna.

B **Port**: Standard settings for PTP.

C **Default**: Standard settings for PTP.

Network settings

In **Configuration ► Network** option, make sure that **Precision Time Protocol (PTP)** is enabled (see Figure 14.47).

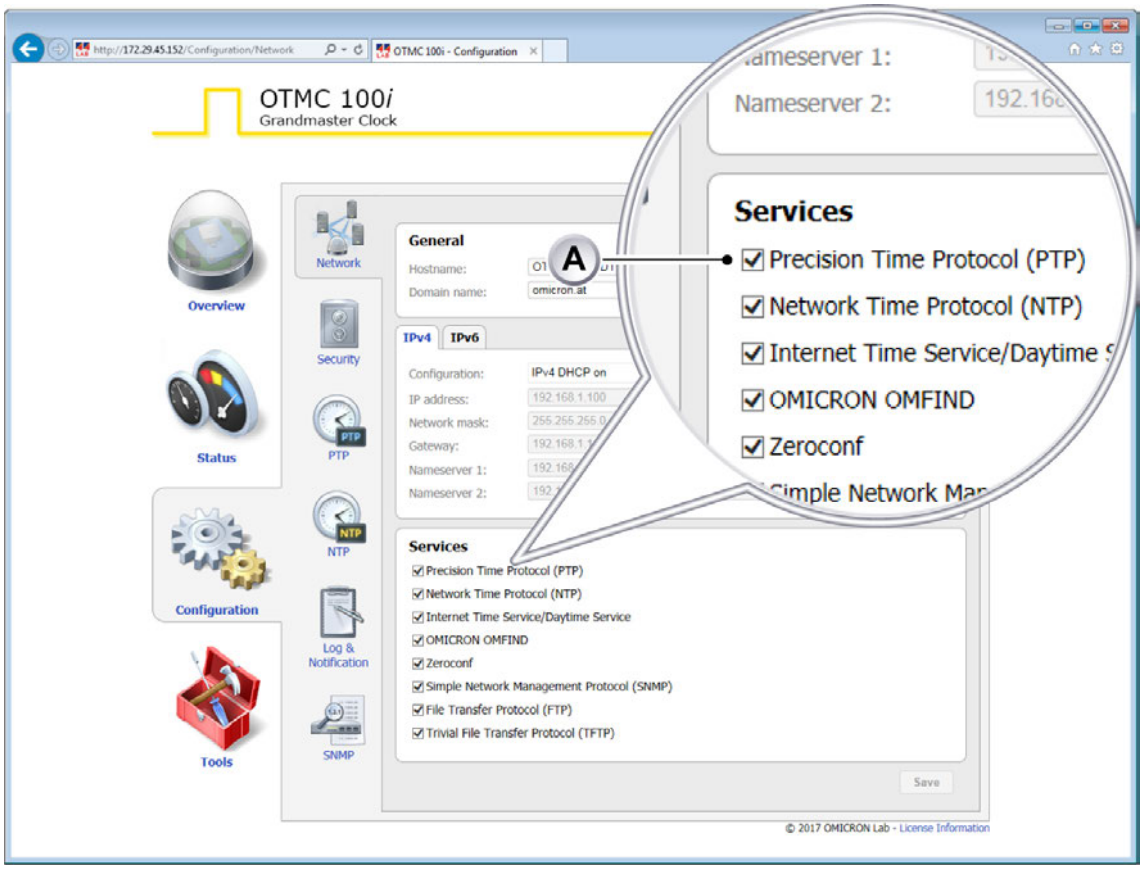


Figure 14.47: OTMC 100 Network status information

A Precision Time Protocol (PTP)

Other

For more detailed GPS antenna related troubleshooting, use of the web interface and resetting the antenna to its factory defaults, please refer to the manual delivered with the GPS antenna.

14.4 IRIG

14.4.1 System overview

G001B: Direct connection setup

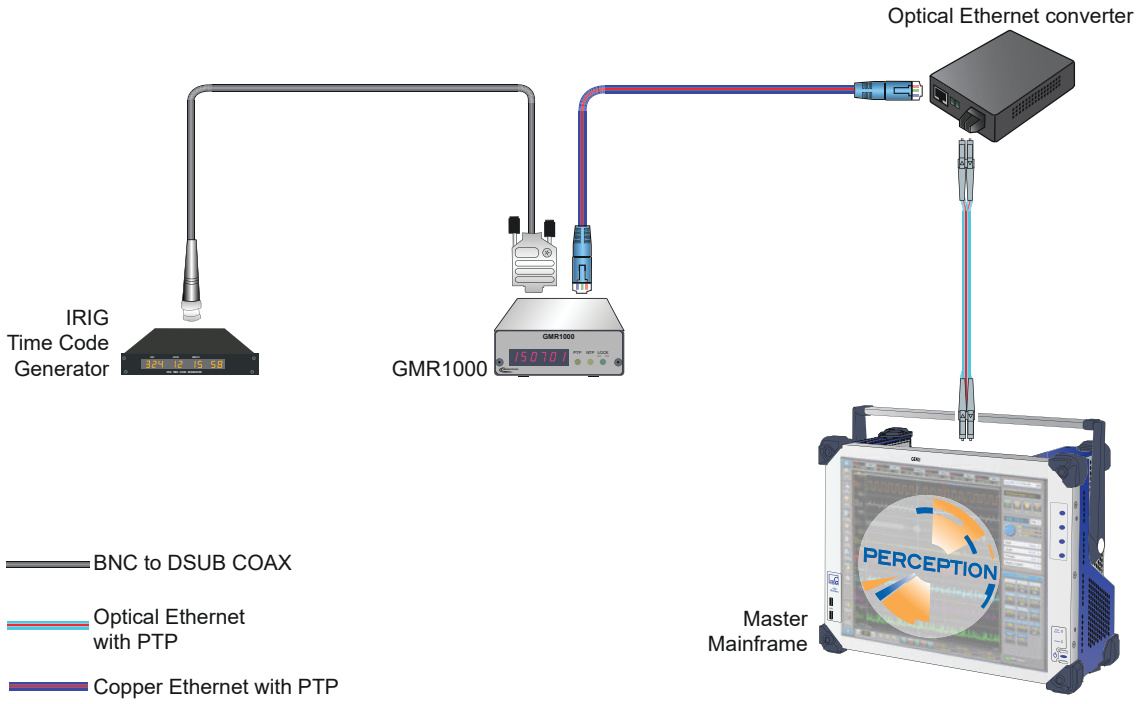


Figure 14.48: Block diagram IRIG synchronization

G001B: Direct connection setup with optical Ethernet

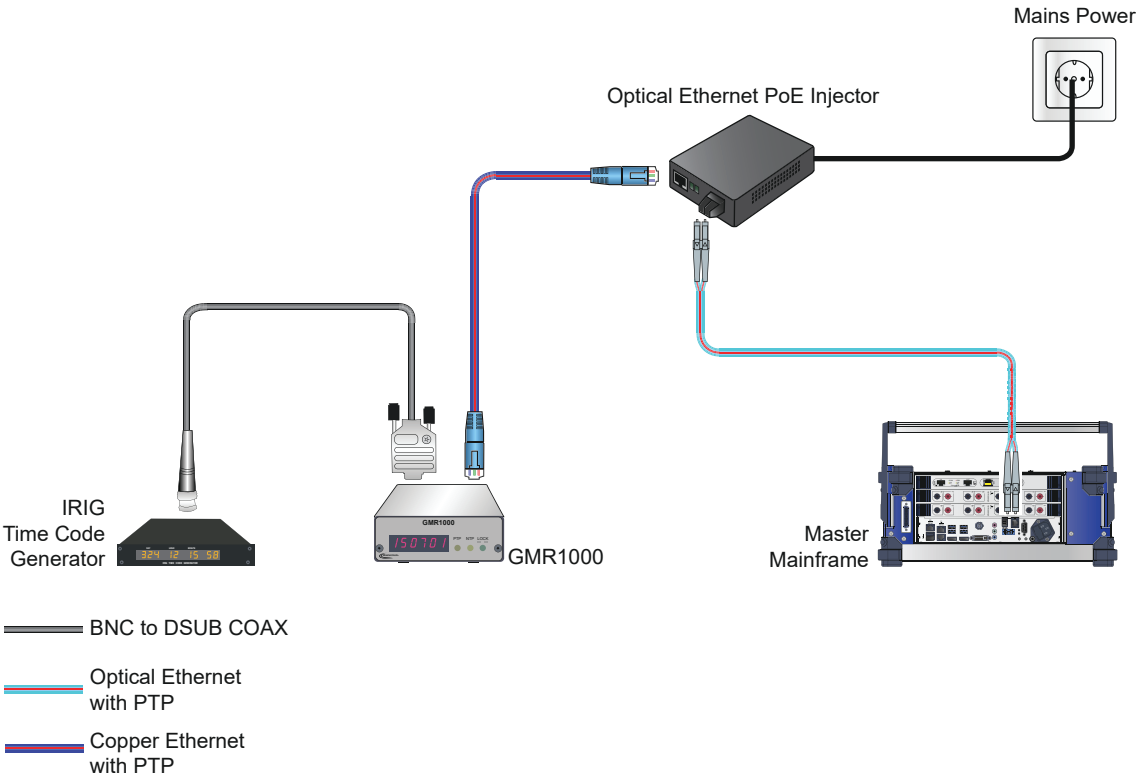


Figure 14.49: Block diagram IRIG synchronization

Note *Use optical Ethernet when there is a large distance between the GMR1000 and the mainframe.*

G001B: IRIG to PTP with tethered mainframes plus QuantumX

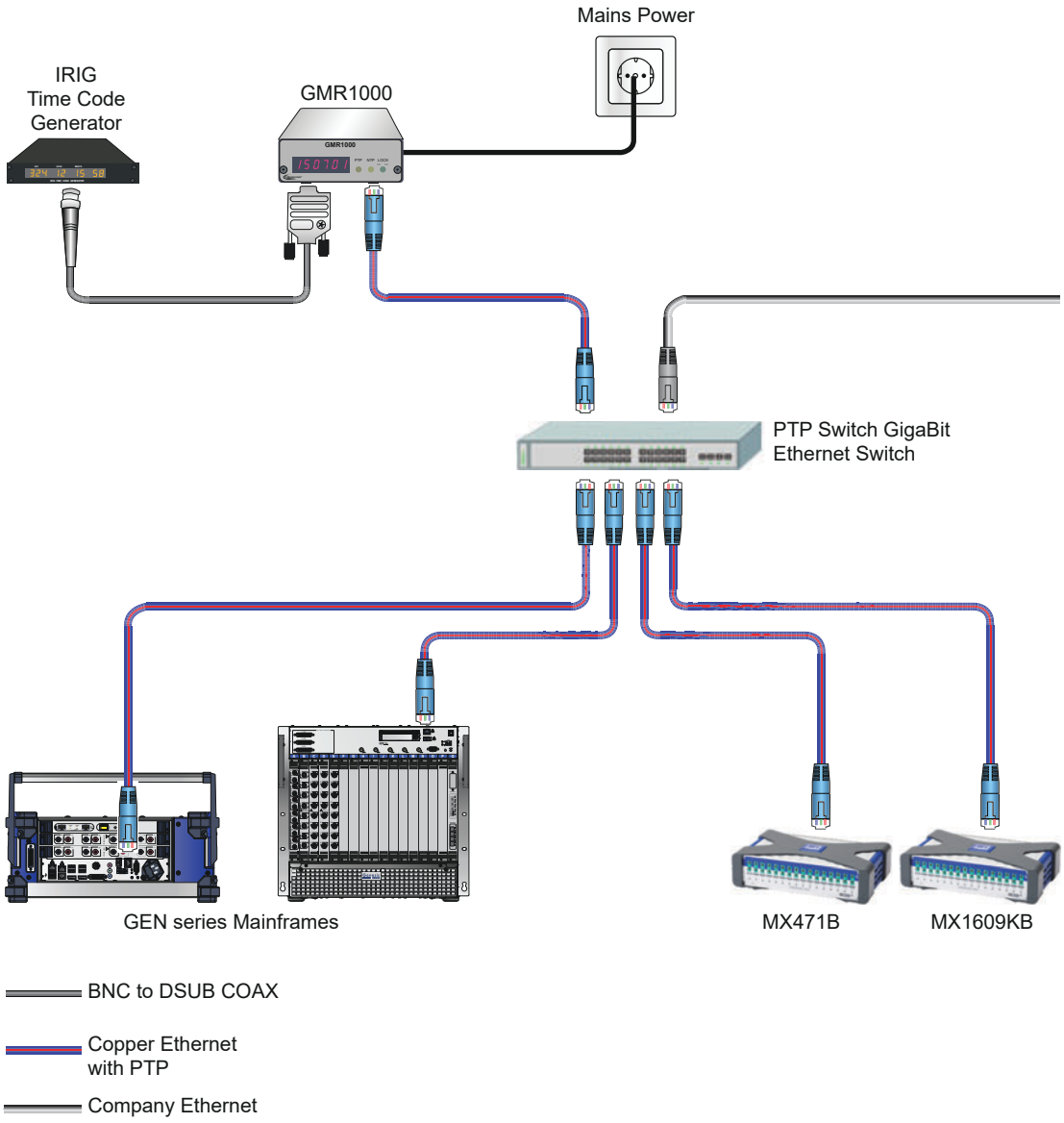


Figure 14.50: IRIG setup for tethered mainframes and QuantumX

14.4.2 Installation

When connecting the G001B option, please follow the steps described below.

1 Connect GMR1000 to power socket using the correct power adapter.

Figure 14.51: GMR1000

A Display information

B LOCK led

The **LOCK** led should light up, stay lit and after a while start to blink. After a while the red digits should start displaying information.

2 Connect the IRIG source to the GMR1000. After a few seconds, the **LOCK** led should blink green.

3 Connect the GMR1000 to the mainframe via Ethernet.

3a G001B: Direct connection setup.

- Connect the GMR1000 to mainframe PTP port 1 (RJ45) using a standard Ethernet cable.

3b G001B: Direct connection setup with optical Ethernet.

- Connect the mainframe PTP port 2 (SFP) to the media converter using the fiber cable.
- Connect the GMR1000 to the media converter using a standard Ethernet cable.

3C G001B: IRIG to PTP with tethered mainframes plus QuantumX.

- Connect the GEN series mainframe to the PTP aware switch using the port of choice PTP 1 (RJ45) or PTP 2 (SFP).
- Connect the GMR1000 to the PTP aware switch.

Note *The choice of mainframe PTP port impacts the later selection of Sync Source. Please match the selection to the actual selection here for proper operation.*

14.4.3 Using the GMR1000 module

The GMR1000 unit takes the IRIG signal as time source input and acts as a PTP master clock for the rest of the system (see Figure 14.52).

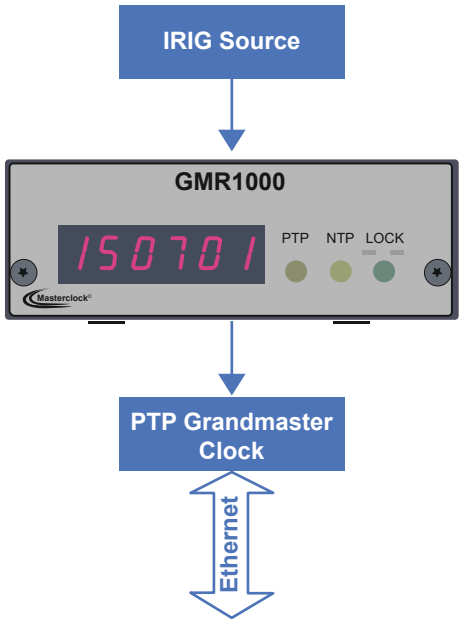


Figure 14.52: G001B architecture

Note *This means that most references in the system setup are **PTP** related, and not **IRIG** related.*

Perception setup

To perform time synchronized data acquisition using GEN series mainframes and the G001B option it is necessary to further setup the system. This section explains how to accomplish that using the **HBM Perception Data Acquisition** software.

Note *This section assumes you are familiar with basic operations in Perception such as connecting to data acquisition hardware and changing settings.*

Note *G001B requires usage of Perception version 7.20 or higher.*

1 Start Perception

2 Connect to the mainframe.

3 Open the settings sheet and select advanced settings:

3a In the main menu select **Settings**.

3b In the Settings menu select **Show Settings ►**.

3c In the submenu select:

- **Basic:** this will show only the relevant settings
- **Advanced:** this will show all settings

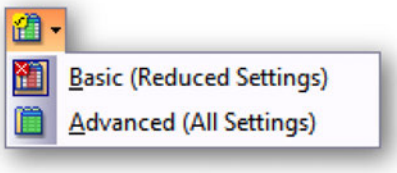


Figure 14.53: Perception settings sheet options

4 In the **Sync source** column select the required IRIG option.

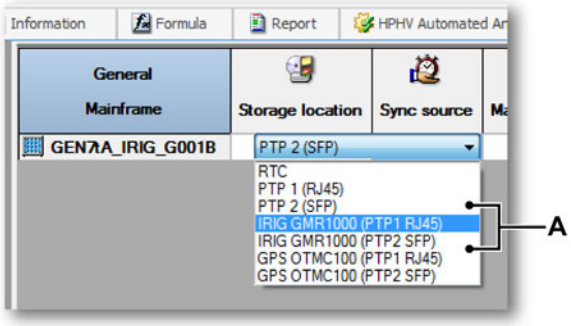


Figure 14.54: PTP selection

A **IRIG GMR1000 (PTP1 RJ45)** and **IRIG GMR1000 (PTP2 SFP)** options

Change the synchronization source to **IRIG GMR1000 (PTP1 RJ45)**.

5 The acquisition system tries to find and synchronize to the PTP signal. The system status goes through the following states:

- No signal
- Out of synchronization
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

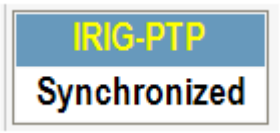


Figure 14.55: IRIG-PTP status - Synchronized

6 The GMR1000 does not act as a highly accurate PTP master in the network, therefore disable **Use Accurate Master** (see Figure 14.56).

Note *If **Use Accurate Master** is enabled and the GMR1000 becomes the PTP master, Perception will show a warning because the GMR1000 is not a clock class 7 or better PTP master.*

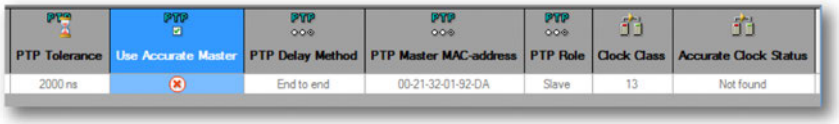


Figure 14.56: PTP - Use Accurate Master

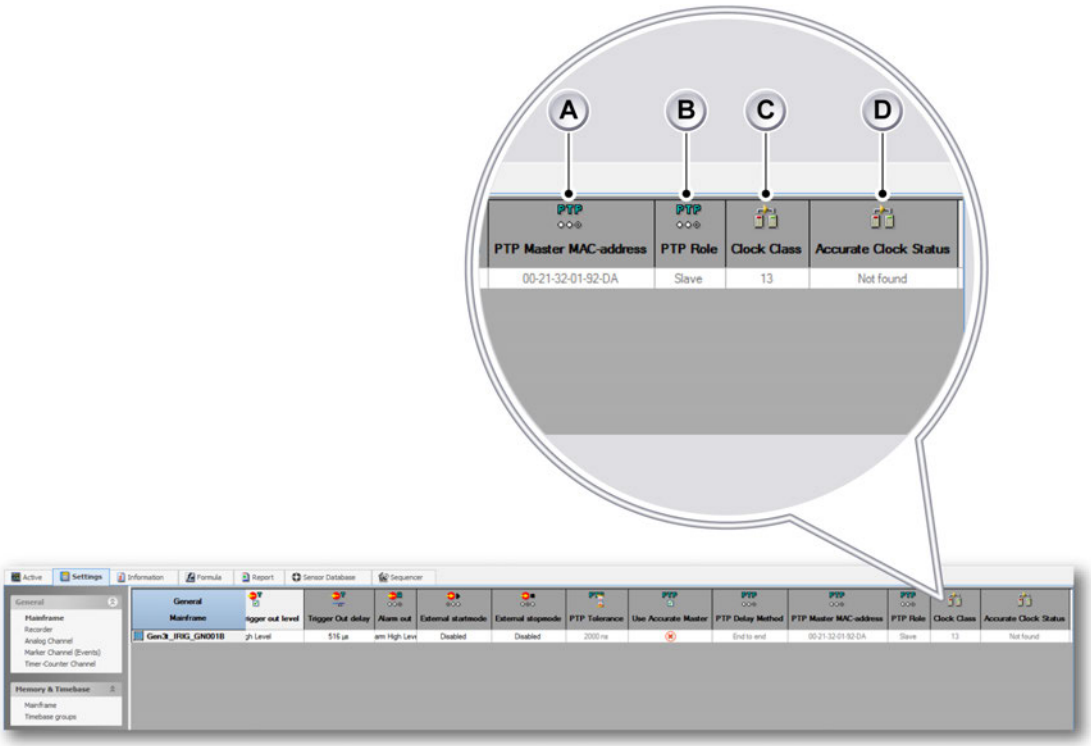


Figure 14.57: PTP synchronization status

Please verify the following settings:

A **PTP Master MAC-address:** Address of the GMR1000

B **PTP Role:** Slave

C **Clock Class:** 13

D **Accurate Clock Status:** Not found

Verify setup and installation

Once the setup is complete there are several steps that can be taken to verify if the setup was successful.

Status information

The overall system time base information is displayed in the status window. This will give a system wide overview showing the most imprecise time source from all connected mainframes.

Note *As all mainframes are expected to be on PTP, the status should show PTP, and should have the default colors blue and white (see figure below).*

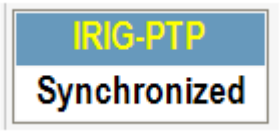


Figure 14.58: IRIG-PTP status - Synchronized

Note *In case the status shown is orange / red a problem has occurred, please refer to the “Troubleshooting” chapter (on page 331) for detailed information.*

System topology

An overview can be found in the system topology overview. The system topology will show the information per connected mainframe.

1 In the menu bar choose **Help ► System Topology** (see Figure 14.59).

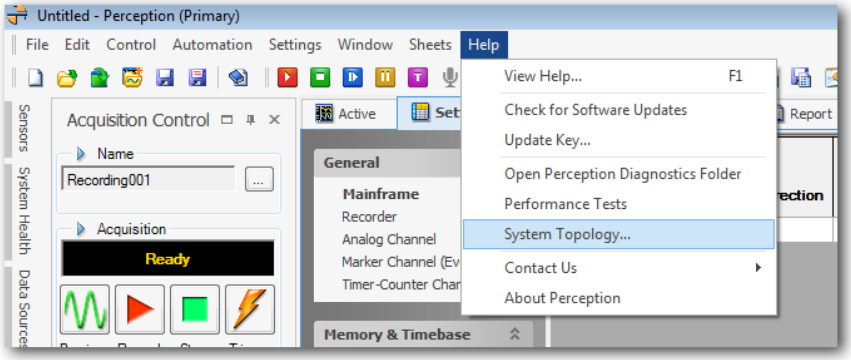


Figure 14.59: System Topology Help

2 The **System Topology** overview opens (see Figure 14.60):

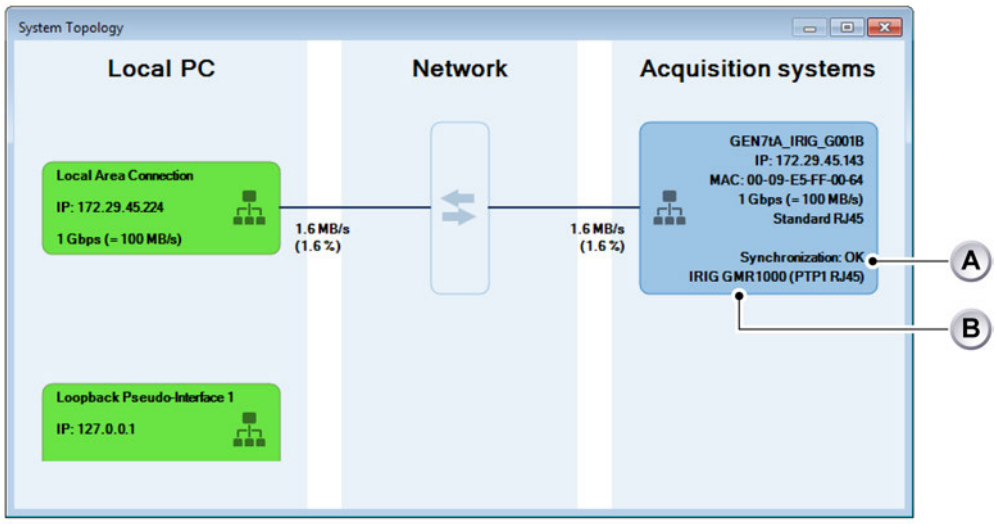


Figure 14.60: System Topology

In **System Topology** overview, please verify the following information:

A States that **Synchronization** is OK

B States that **IRIG GMR1000** is connected as selected (**PTP1 RJ45** for RJ45 connection as shown in Figure 14.60, **PTP2 SFP** if you are using the optical Ethernet).

Note *Network peripherals such as switches and routers are not visualized within the network topology overview.*

Recording information

When a recording is created using PTP time synchronization, the PTP master clock information is available in the recorded information in the Yt display in Perception (see Figure 14.61).

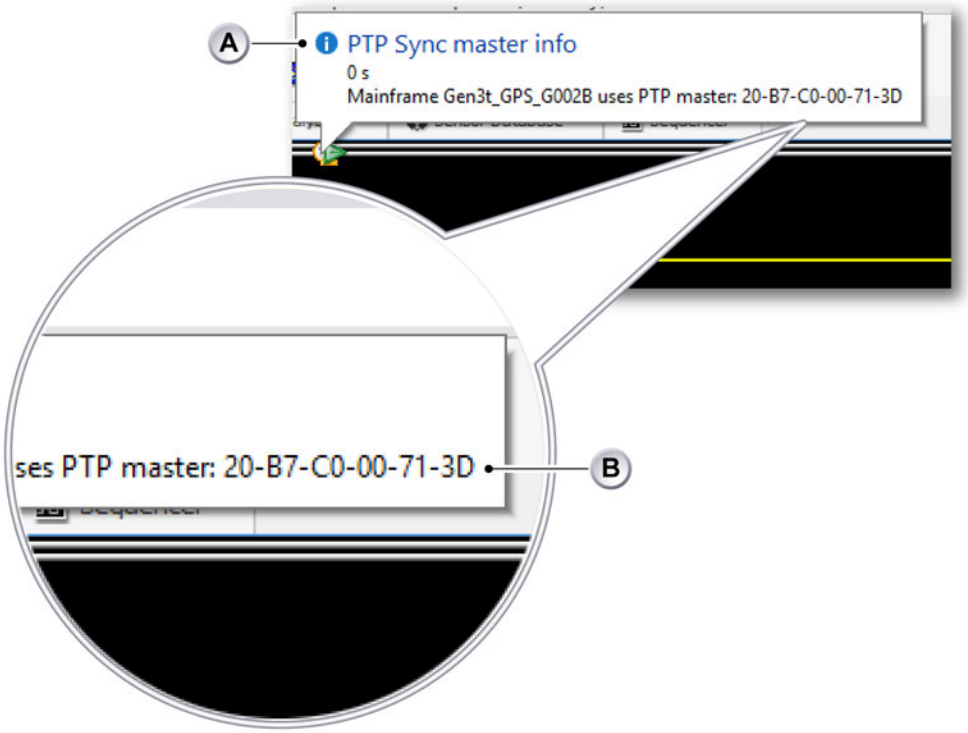


Figure 14.61: PTP synchronization master information

A PTP master clock information

B PTP master MAC adress

Note *Please refer to the “Trouble-shooting” chapter on page 331 in case this information is not shown or is not correct.*

14.4.4 Trouble-shooting guide for G001B

This document gives some hints on what to check if the GMR1000 does not work as expected. It will first explain how to use Perception to determine if there is a problem and then offer help on diagnosing and solving the issue.

In case this information does not solve the problem, call your local HBM Support group.

Note *The PTP settings used in this document are displayed only in the **Advanced** settings mode of Perception.*

To open the **Advanced** settings do the following:

1. Open the settings sheet
2. In the main menu select **Settings**.
3. In the Settings menu select **Show Settings ►**.
4. In the submenu select:
   - **Basic:** this will show only the relevant settings
   - **Advanced:** this will show all settings

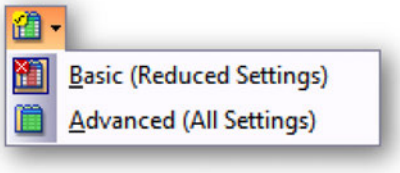


Figure 14.62: Perception settings sheet options

How to check synchronization

The synchronization status is displayed in the status window of Perception: When IRIG GMR1000 is selected, the system status goes through the following states:

- No signal
- Out of sync
- Synchronizing
- Coarse(1)
- Synchronized

(1) Coarse may not be shown if synchronization occurs quickly.

Note *The system status returns an overall status for all connected mainframes. To determine which mainframe(s) is causing problems, please see "Finding the system that is causing the problems" on page 334.*

The state remains at “NO GMR1000”	
Category	**Description**
Cause	This problem is caused because the mainframe is synchronizing to a PTP master other than the GMR1000.
Solution	Check the GMR1000 and network peripherals.
Recording	When starting a recording the mainframes that are in the state “NO GMR1000” try to follow the signal from the PTP grandmaster they did find. The time used in the recording is undetermined. The PTP settings can be used to determine the synchronization source. If the PTP Role is Master, the mainframe has become the master in the PTP network. If the PTP Role is Slave, the PTP Master MAC-address can be used to determine which node in the network is the PTP master. In-depth knowledge of networking is required to obtain this information.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

The state remains at “Coarse”	
Category	**Description**
Cause	A network switch is causing jitter on the PTP timestamps in the network.
Solution	**1** See "PTP capable switch" on page 837 **2** Increase the PTP Accuracy, see chapter "Checking the Perception setup" on page 334
Recording	When starting a recording the mainframes are typically **not** synchronized within the specified accuracy. The samples at the start of the recording are expected to be synchronous within 10 times the specified accuracy, but may drift apart as the recording proceeds depending on the cause of the problem.
Feedback	Typically, a notification appears and the recording contains a marker to point out the problem.

Finding the system that is causing the problems

The status described in the previous section is an overall system status showing the most important status in the system. To verify the synchronization details per mainframe, please refer to the chapter "System topology" on page 328.

Checking the Perception setup

The following settings can all be found in the Perception Settings (see Figure 14.63).

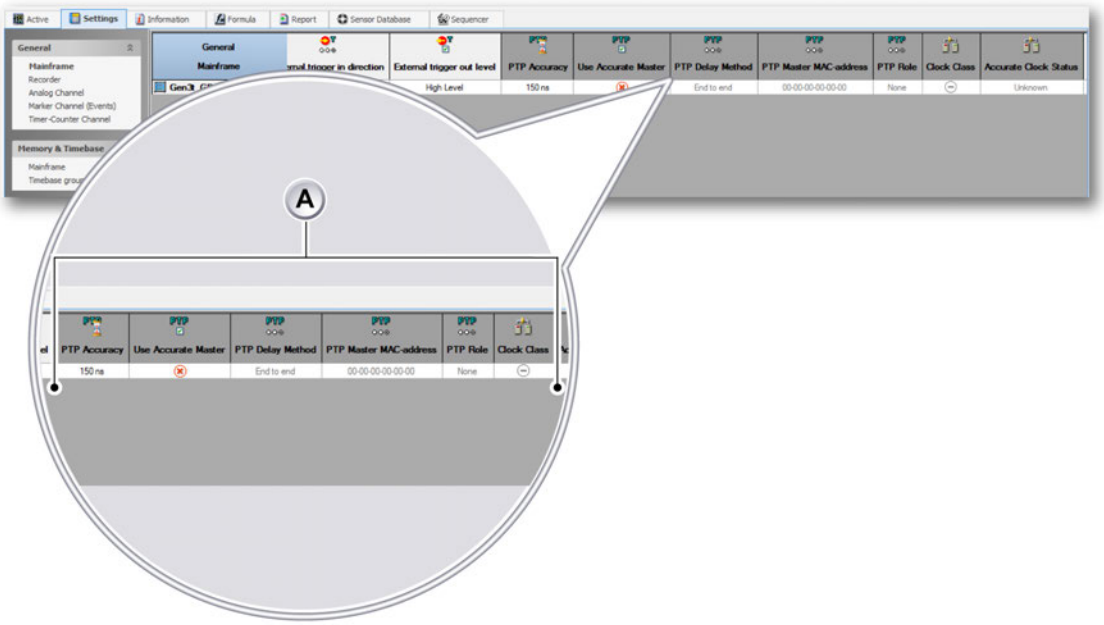


Figure 14.63: Perception General Mainframes settings

A PTP related settings in Perception General Mainframes settings

Sync source	
Network port used	**Sync source setting**
RJ45	IRIG GMR1000 (PTP1 RJ45)
Optical 1 Gbit	IRIG GMR1000 (PTP2 SFP)

PTP Accuracy
This is set to a fixed value because of the nature of the IRIG synchronization signal jitter. **Note** *This setting only needs to be changed if a network switch without PTP support is being used and more jitter is acceptable.* **Note** *Interaction between different time synchronization types in complex set-ups may induce a fixed accuracy.*

Use Accurate Master
Ensure that “accurate master”’ setting is disabled.

PTP Role (read-only)
Verify that the PTP Role is slave. If Master is listed in this column, the GEN series mainframe itself is the master rather than the GMR1000.

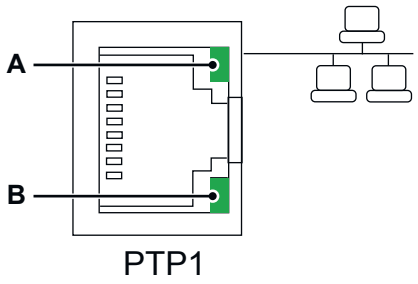
Clock Class
The clock class should be 13 (GPS clock class if the GPS antenna is synchronized).

Note *If the clock class is 14, IRIG is not locked and the GMR1000 runs on its internal clock.*
If the clock class is 52, the GMR1000 was never synchronized.

PTP Master MAC-address
This is the GMR1000 MAC-address, or the boundary clock MAC-address when boundary clocks are used.

Verify the GEN series network port

The following section explains how the LEDs on the ports can be used to diagnose system synchronization problems. The images herein are schematic, for actual port images and positioning of the ports in the system, refer to appendix “PTP Synchronization” on page 819.

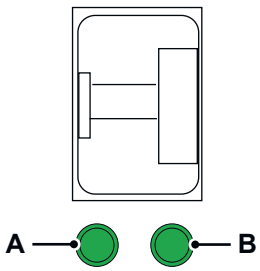


A Activity LED RJ 45 network (blinking)

B Link speed RJ45 network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	**1** Make sure the PoE injector is powered by checking the power LED. **2** Make sure PoE injector IN and OUT are correctly connected. **3** Replace the cables used to verify the cables are not causing the problem.(1)
100 or 10 Mbit/s network connection	ON	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
100 or 10 Mbit/s network connection	Blinking	OFF	This is expected, the GPS antenna typically runs on 100 Mbit/s.
1 Gbit/s network connection	ON	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.
1 Gbit/s network connection	Blinking	ON	The GPS antenna is not directly connected to the network port or another device is connected to this port. In case this port is used for PTP, please make sure that all network peripherals in between the port and the GPS antenna are PTP aware.

(1) **Note** *In case the problem remains unsolved, contact HBM service.*



PTP2

A Activity LED optical network

B Link speed LED optical network

Status	Activity LED	Speed LED	Description
No network connection	OFF	OFF	Refer to the “Verify SFP PoE injector” section (see details "Checking the SFP PoE injector" on page 339). If no problem is found, swap the SFP with the SFP in the PoE injector and retry. If a problem occurs now it is related to the SFP, contact HBM Service for information on how to replace it. **Note** *In case the problem remains unsolved, contact HBM service.*
100 or 10 Mbit/s network connection	ON	OFF	See section "Optical Network (SFP)" on page 813 for additional checks.
100 or 10 Mbit/s network connection	Blinking	OFF	See section "Optical Network (SFP)" on page 813 for additional checks.
1 Gbit/s network connection	ON	ON	This is expected.
1 Gbit/s network connection	Blinking	ON	This is expected.

Checking the SFP PoE injector

The “PoE injector LEDs trouble-shooting diagram” helps to determine the connection problems (see Figure 14.65).
The LED names that are referenced in the diagram can be found on the front of the device (see Figure 14.64).

PoE injector LEDs

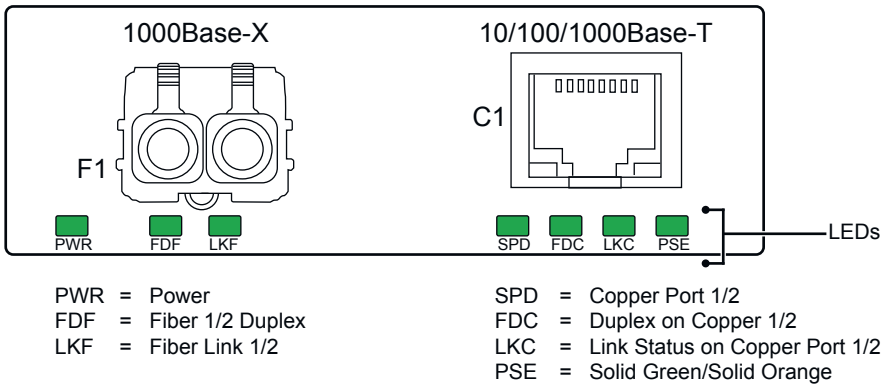


Figure 14.64: Power over Ethernet injector LEDs details

Checking the PoE injector LEDs

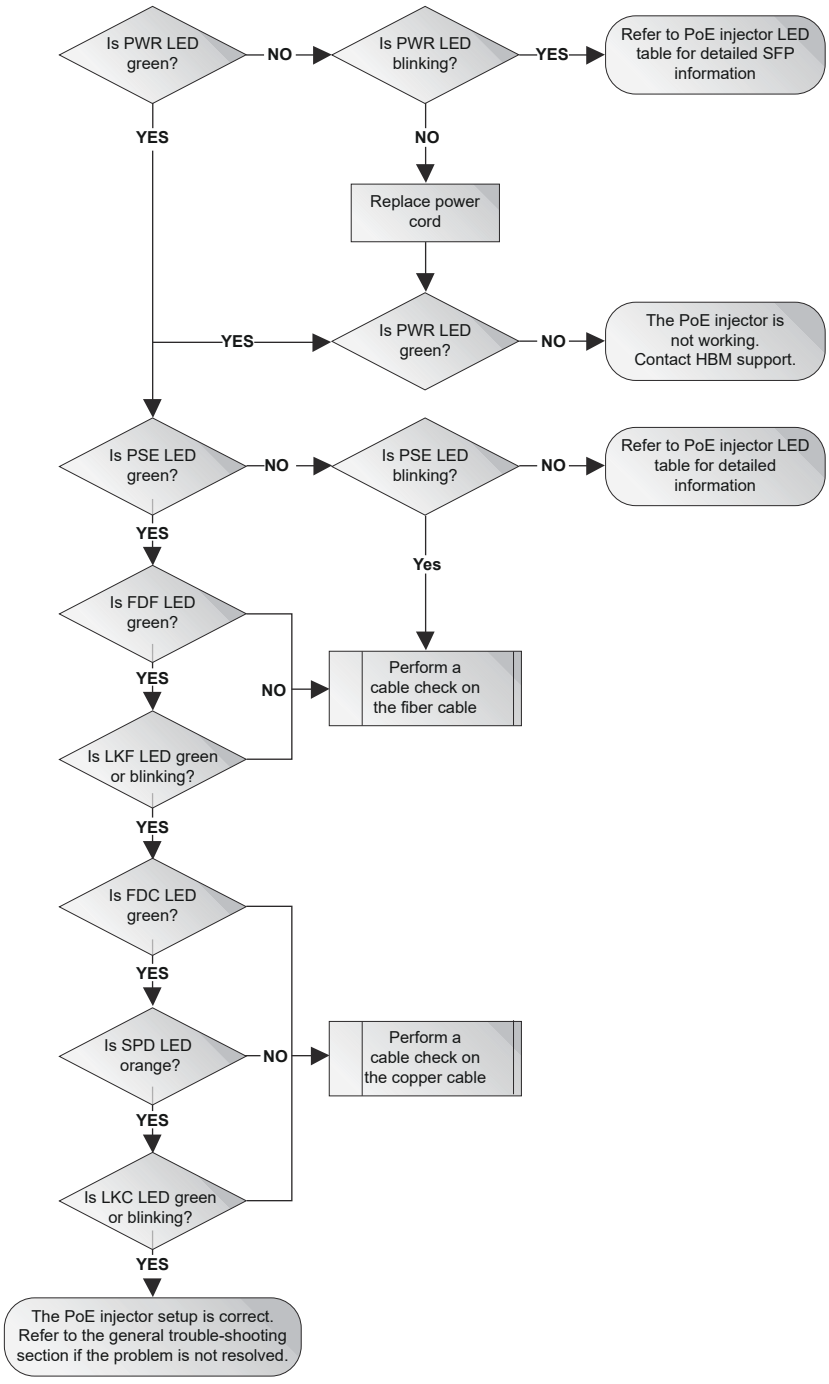


Figure 14.65: PoE injector LEDs trouble-shooting diagram

Checking PoE injector cables

When asked to check cables connected to the PoE injector, please use the following workflow to systematically rule out problems related to the network cables (see Figure 14.66).

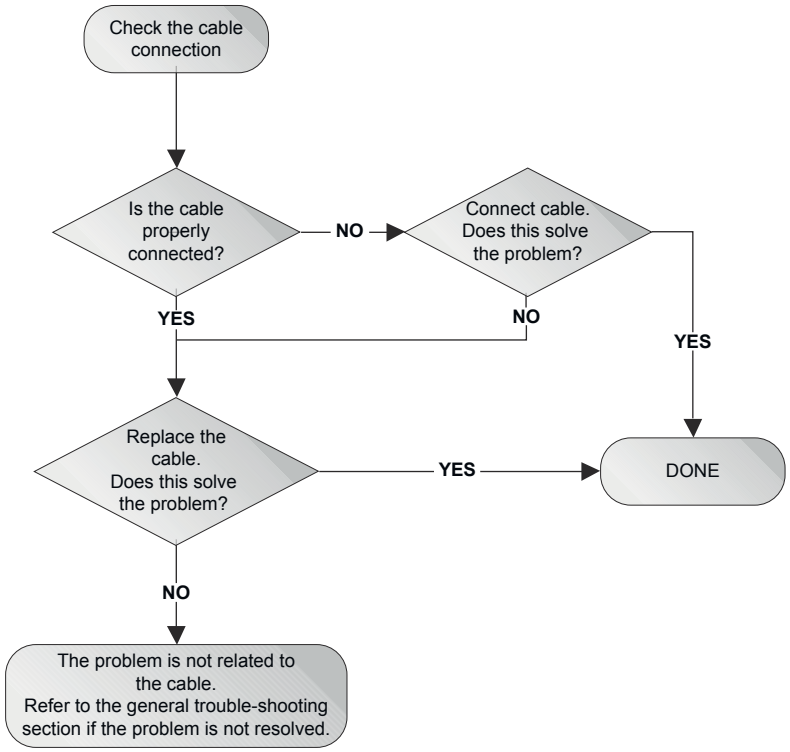


Figure 14.66: PoE injector cables trouble-shooting diagram

PoE injector settings

DIP switches can be used to configure settings on the PoE injector. All DIP switches should be in the factory default position. This means that all switches should be in the “up” position (see Figure 14.67).

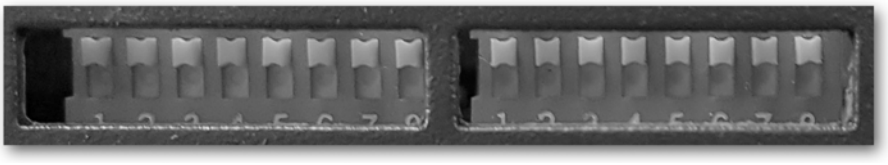


Figure 14.67: DIP switches on media converter

PoE injector LED status overview

The following tables give an overview of the LEDs' status for the PoE injector and can be used as reference. This information is an extract from the GPS antenna's manual, please refer to that manual directly for more detailed information.

Status LED

The Perle PoE/PoE +10/100/1000 rate Media convertors have status LEDs located on the front panel of the unit.

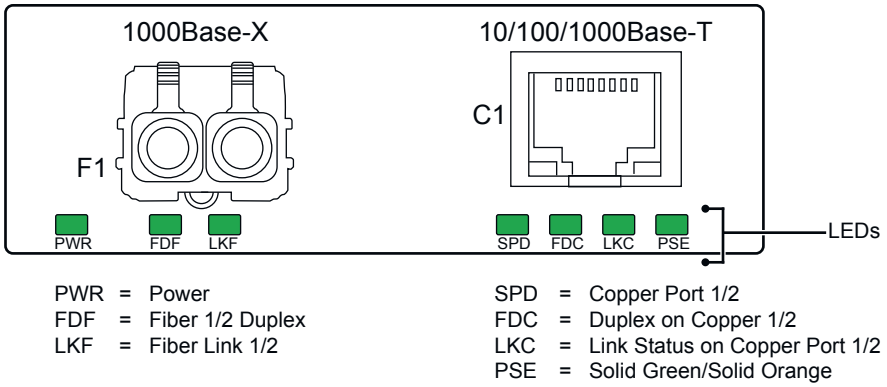


Figure 14.68: Power over Ethernet injector LEDs details

Status LED	Activity	Description
PWR	ON	Power is applied to the unit.
	Blinking (slow)	Loopback mode (one or both fiber interfaces are in loopback mode)
	Blinking (fast)	*Power ON* failure. See LED pattern table to determine pattern combination and failure cause*

***LED pattern**				
FDF	LKF	FDC	PSE	
OFF	OFF	ON	ON	SFP incompatible
All other LED patterns				Internal hardware failure

Status LED	Activity	Description
FDF-1/2 (Fiber 1/2 Duplex)	ON	Full Duplex
	OFF	Half Duplex

Status LED	Activity	Description
LKF-1/2 (Status on Fiber Link 1/2)	ON	Fiber Link is present
	OFF	No Fiber Link is present
	Blinking (slow)	Fiber Link appears functional - Fiber Link has been brought down by Smart Link pass-through
	Blinking (fast)	Fiber Link up and receiving data

Status LED	Activity	Description
SPD-(Copper port 1/2)	Green	1000 Mbps
	Orange	100 Mbps
	OFF	10 Mbps (if link is currently established)

Status LED	Activity	Description
FDC-1/2 (Duplex on Copper 1/2)	ON	Full Duplex mode
	OFF	Half Duplex mode

Status LED	Activity	Description
LKC-1/2 (Link status on Copper port 1/2)	ON	Copper link is present
	OFF	No Copper link is present
	Blinking (slow)	Copper link appears functional - Copper link has been brought down by Smart Link pass-through
	Blinking (fast)	Copper link up and receiving data

Status LED	Activity	Description
PSE-1/2	Solid green (Active)	The PSE has successfully detected a compliant PD and is applying power over the UTP
	Solid orange (Inactive)	The PSE is not active. The PSE has been configured to provide power, however ● Compliant is not detected - no power applied ● PSE has turned off power for Reset function
	OFF - (Disabled)	The PSE function is disabled in the configuration
	Error conditions A **blinking red light** is an error condition. The LED light will cycle with a three second stop interval between the error condition code.	
	Red (1 blink)	PD Capacitance too high
	Red (2 blinks)	PD Resistance too low or short circuit
	Red (3 blinks)	PD Resistance too high

Checking the GMR1000

The WinDiscovery tool from Masterclock© has to be installed on the PC, refer to the GMR1000 manual for detailed instructions on how to install and use the software.

1 Start the WinDiscovery tool from Masterclock©, this will show the devices on the network (see Figure 14.69).

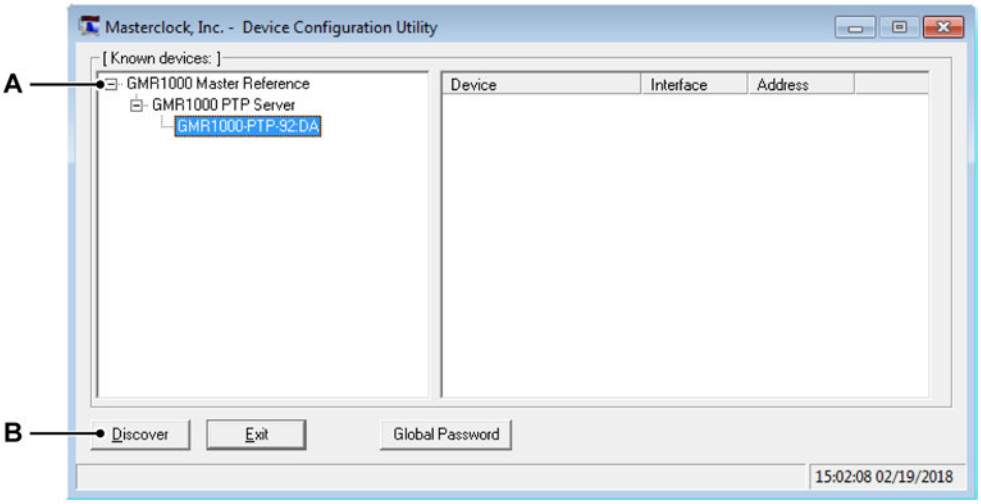


Figure 14.69: Device Configuration Utility tool - Detected devices

A List of detected devices

B Discover button

Note *In case no devices are shown, click the **Discover** button. If no devices are discovered, check that the PC running the tool is connected to the GMR1000 via Ethernet.*

1A The first time WinDiscovery is started, Windows® may show the firewall configuration window. Select both options as shown inFigure 14.70 and confirm with **Allow access** button.

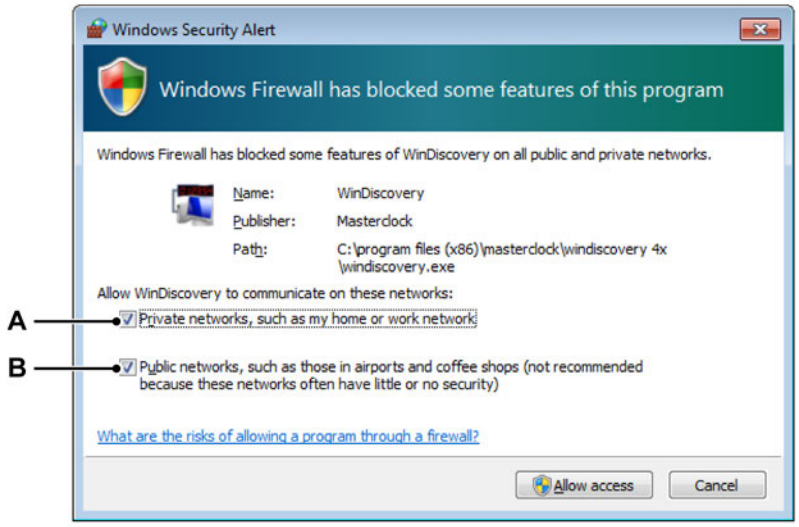


Figure 14.70: Windows® Security Alert settings

A Check box for private network(s)

B Check box for public networks

2 Expand the tree in the **Device Configuration Utility** until the specific device is found, which is part of the GMR1000 Master reference -> GMR1000 PTP Server family. Once found, click on the device, this will open the device settings window (see Figure 14.71).

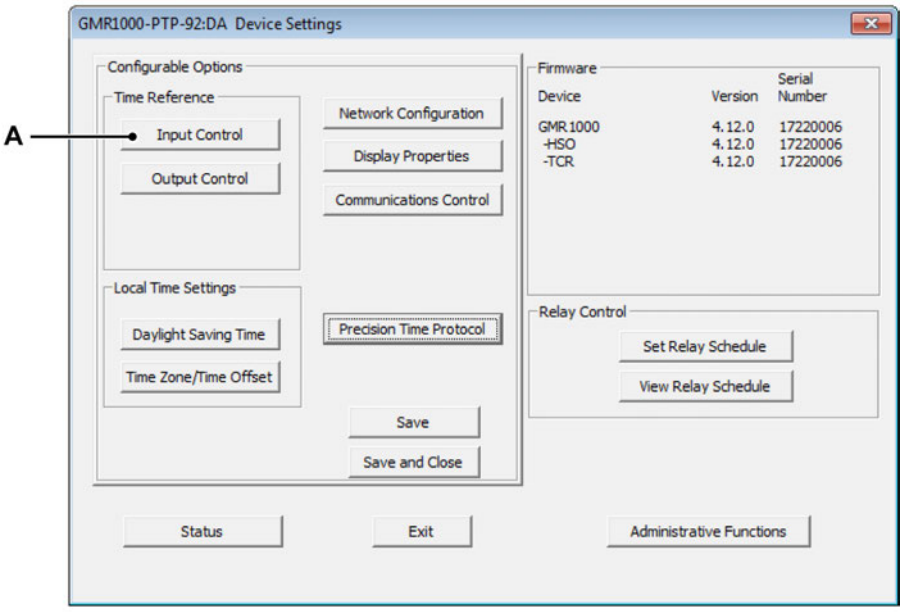


Figure 14.71: GMR1000 PTP Device settings

A Input Control

In the device settings, select the **Input Control (A)**.

3 In **Input Control A** dialog, select the **Time Code Reader** button.

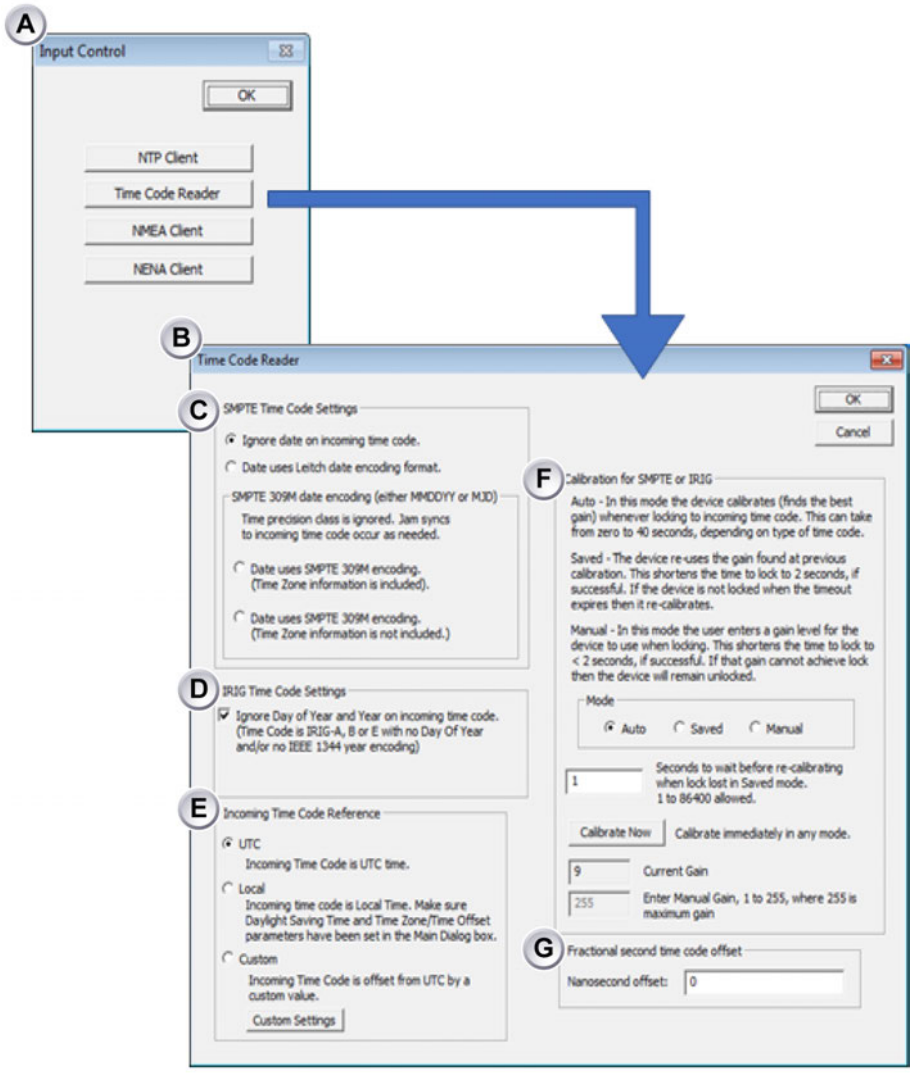


Figure 14.72: Input Control - Time Code Reader settings

A **Input Control** dialog

B **Time Code Reader** window

Make sure the settings are set as shown in Figure 14.72:

C **SMPTE Time Code Settings:** Select: **Ignore date on incoming time code.** option

D **IRIG Time Code Settings:** Select check box

E **Incoming Time Code Reference:** Select **UTC** option

F **Calibration for SMPTE ot IRIG:** Select **Auto** mode
Seconds to wait before re-calibrating... Set the value to: **1**

G **Fractional second time code offset: Naonosecond offset:** Should be **0**

Close the **Time Code Reader** and **Input Control** windows again.

4 In the GMR1000 PTP device settings window select the **Precision Time Protocol** button.

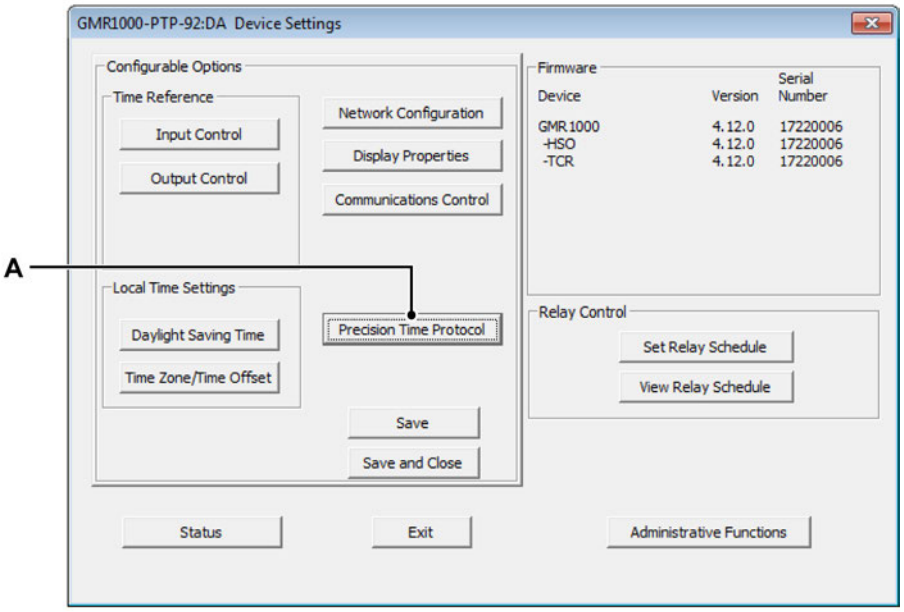


Figure 14.73: GMR1000 PTP Device settings

A Precision Time Protocol option

5 In **PTP- Precision Time Protocol** window make sure that the following settings are set:

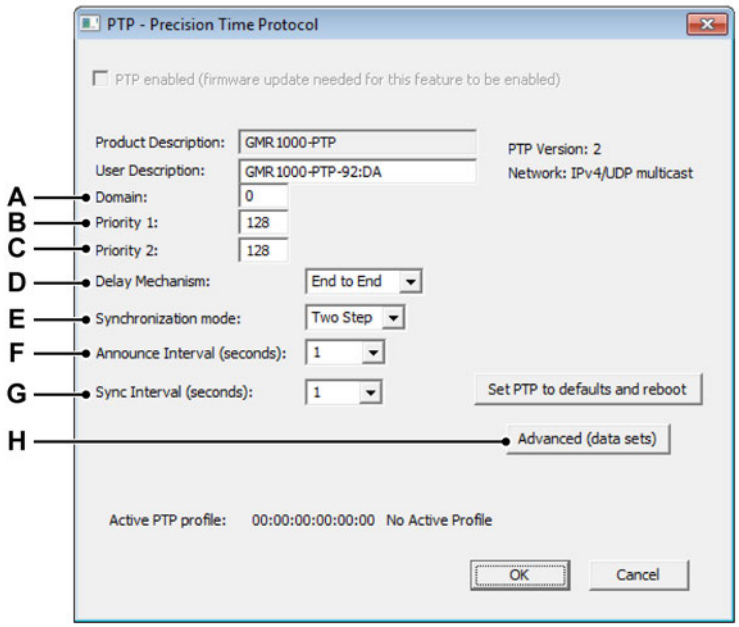


Figure 14.74: PTP - Precision Time Protocol

A	**Domain:**	Set the value to "0"
B	**Priority 1:**	Set the value to “128”
C	**Priority 2:**	Set the value to “128”
D	**Delay Mechanism:**	End to End
E	**Synchronization mode:**	Two Step
F	**Announce Interval (seconds):**	Set the value to “1”
G	**Sync Interval (seconds):**	Set the value to “1”

6 Click the **Advanced (data sets) button (H)** in PTP - Precision Time Protocol window (see Figure 14.74) to open the **PTP Avanced** settings (see Figure 14.75).
In **PTP Advanced** window make sure the followings settings are set:

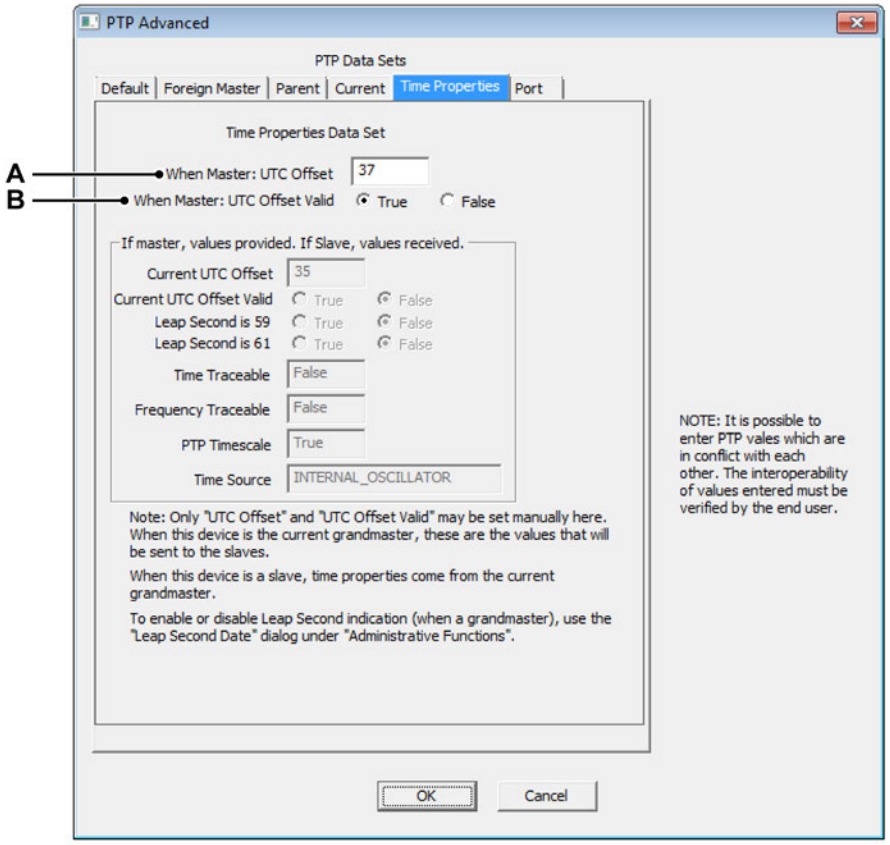


Figure 14.75: PTP Advanced - PTP Data Sets/Time Properties settings

Note *UTC Offset to TAI may differ, please enter the value that is currently correct.*

A	**When Master: UTC Offset**	Set the value to “37”
B	**When Master: UTC Offset Valid**	Select the option “True”

7 Finally, close the Advanced (data sets) and PTP - Precision Time Protocol windows. This will bring back the GMR1000 PTP device settings window (see Figure 14.76).

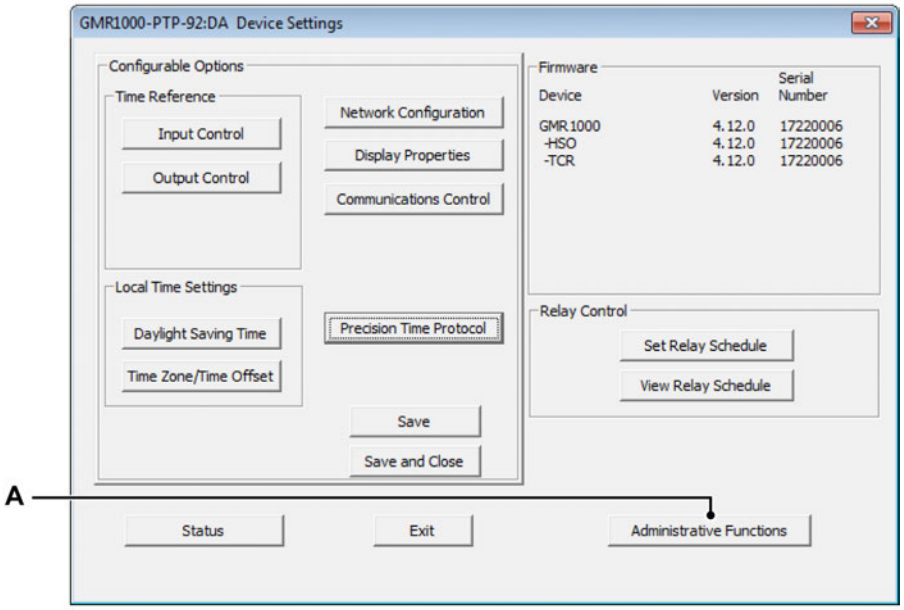


Figure 14.76: GMR1000 PTP Device settings

A Administrative Functions

8 As the IRIG signal contains no date, this needs to be entered manually. Open the **Administrative Functions** dialog with the **Administrative Functions (A)** button (see Figure 14.76).

9 Edit the date by clicking on the **Set Time/Date** button in the **Administrative Functions** dialog (see Figure 14.77).

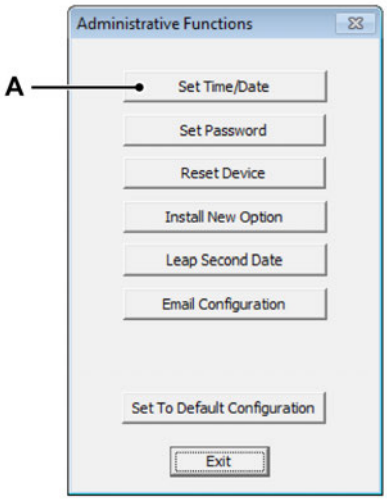


Figure 14.77: Administrative Functions - GMR1000

A Set Time/Date option

10 A message will be shown (see Figure 14.78).

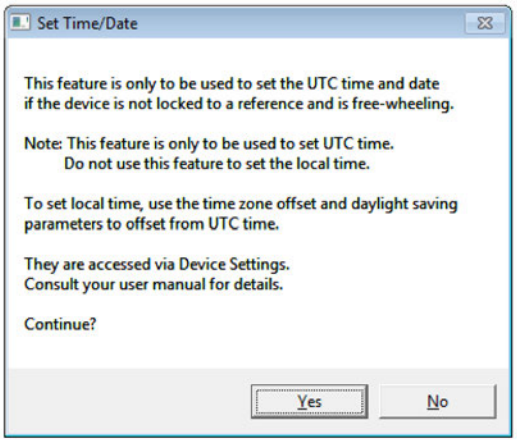


Figure 14.78: Set Time/Date

Confirm with **Yes**

11 Now the **Set Time and Date** window is shown (see Figure 14.79).

Note *Depending on the PC's settings, the **UTC Time and Date from the PC clock** or the **Custom** option button has to be clicked.*

If the PC's clock is set correctly select the **UTC Time and Date from the PC clock** option button (see Figure 14.79).

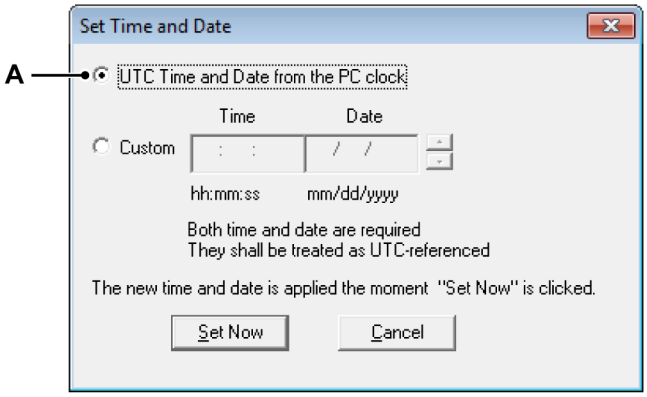


Figure 14.79: UTC Time and Date from the PC clock

A UTC Time and Date from the PC clock option

Otherwise select the **custom** time option button (see Figure 14.80).

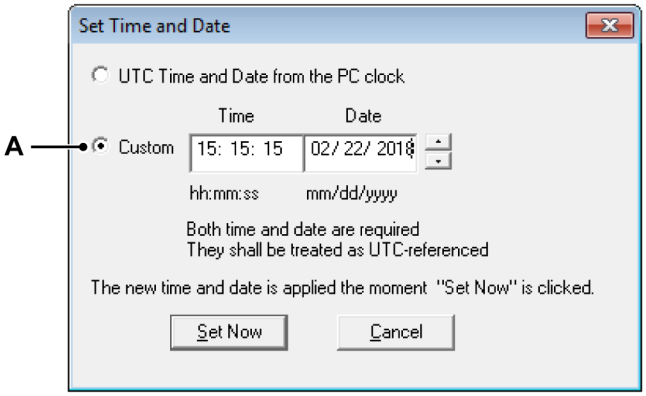


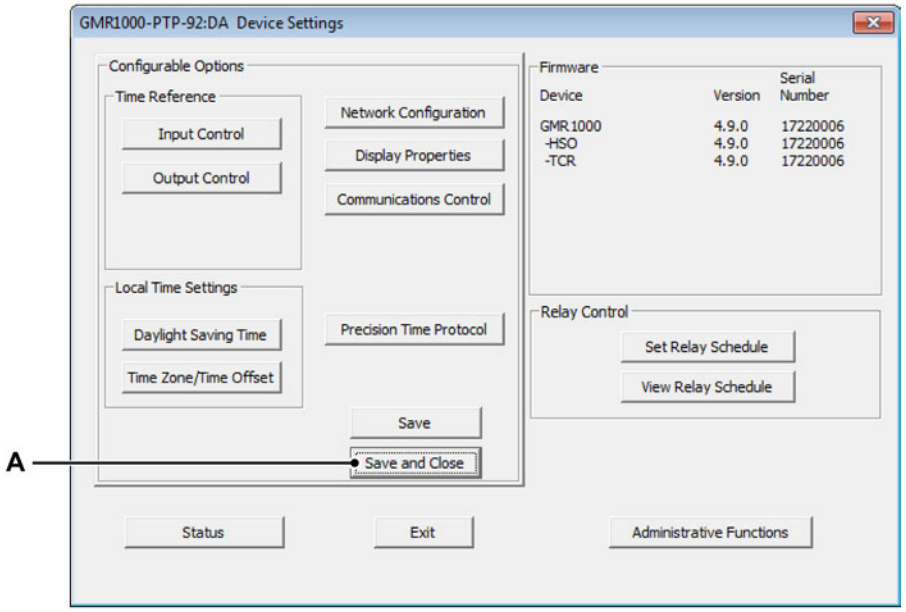
Figure 14.80: Setting the time to a custom value

A UTC Time and Date - Custom

Note *Enter any time as this will be overridden later by the IRIG source, but make sure the date entered is the correct date!*

Confirm the changes with **Set Now**.

12 Select the **Save and Close (A)** button to confirm the changes. After a few seconds, the GRM1000 will take over the time from the IRIG source again.



A Save and Close

15 Understanding Inputs and Usage of Probes

15.1 GEN series inputs

Note *Every manufacturer uses different names for similar or even identical types of inputs. Some of the terminology used is described in this section.*

Balanced Vs Unbalanced
A balanced input describes an input stage where both input terminals exhibit the same electrical behavior, such as resistance and capacitance. Unbalanced electrical input properties are different.

Symmetrical Vs Unsymmetrical
Symmetrical (similar to **balanced**) describes the input properties; if both input terminals are built up using the same component in a mirrored way, they are **symmetrical** (this will result in a **balanced input**).

Differential
A differential amplifier is a type of electronic amplifier that multiplies the difference between two inputs by a constant factor.
A differential amplifier is often treated as an isolated amplifier, which is incorrect.

Single-ended
A single-ended amplifier is a type of electronic amplifier that has the negative input connected to (measurement) ground.

Note *A differential amplifier can be turned into a single-ended one by connecting the negative input to ground.*

Isolated
An isolated amplifier is a type of electronic amplifier where both inputs are isolated from (earth) ground or which has infinite resistance to ground.

Note *Isolation can be combined with any of the amplifier variations mentioned above.*

15.1.1 Single-ended input

A single-ended input is not isolated and uses unbalanced inputs.

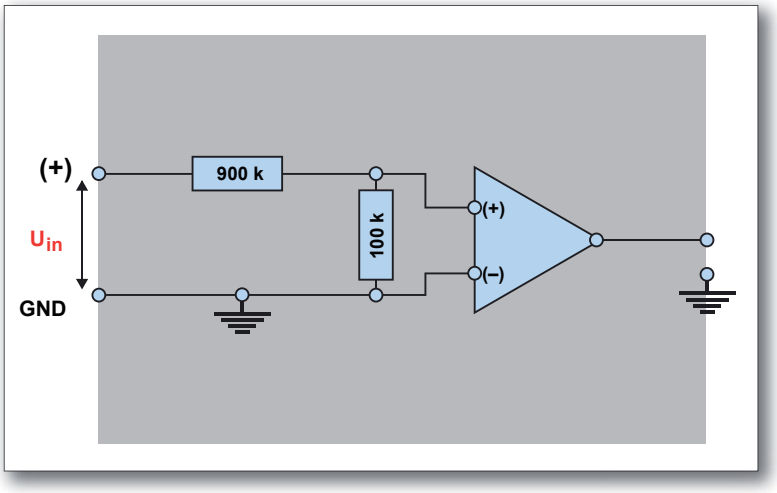


Figure 15.1: Single-ended amplifier

- One input is connected to ground
- Resistance / Capacitance from each terminal to ground is different
- Amplifier is typically found in oscilloscopes
  - Also used in GEN DAQ Basic amp, Liberty 8ch DC amp
  - Often identified by the use of a single METAL BNC connector per channel
- Can be used with standard passive probes (as with oscilloscopes)

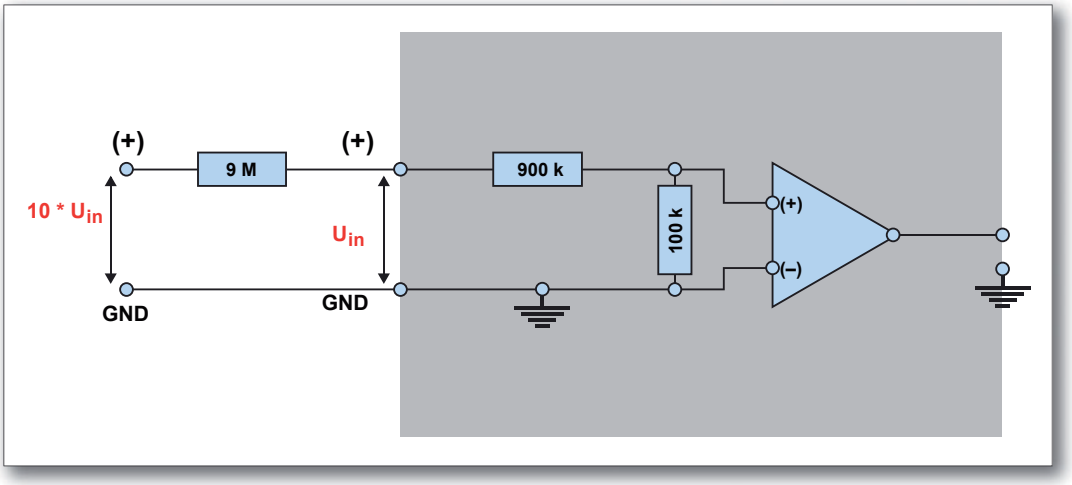


Figure 15.2: Single-ended amplifier with passive probe

- An inline resistor acts as a voltage divider using the input resistance of the amplifier
- The amplifier itself measures only $\mathbf{U_{in}}$; the **total** input range is $\mathbf{10 * U_{in}}$
- This can be done with any oscilloscope or the GEN DAQ Basic Amp
  - Oscilloscope probes are typically only +/- 2% to +/- 5% accurate
- The probes used need compensation. The compensation range needs to match the input amplifier's capacitance range.

15.1.2 Balanced differential input

A balanced differential input is not isolated and uses balanced inputs.

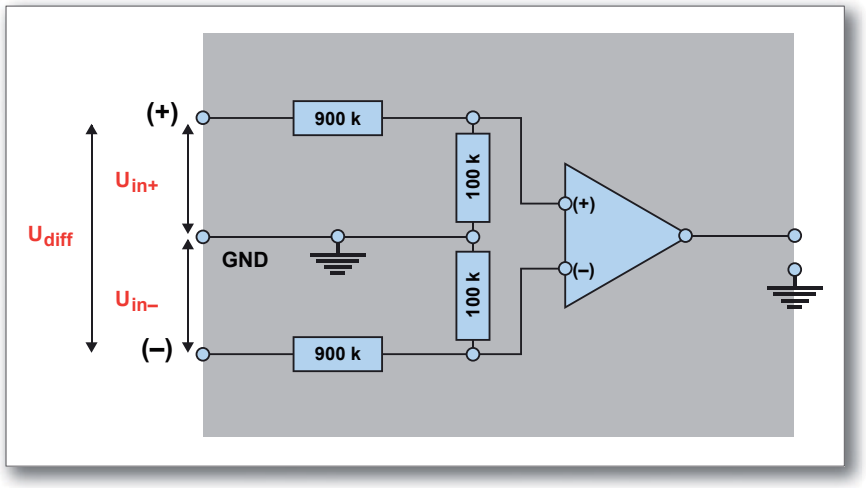


Figure 15.3: Balanced differential amplifier

- Resistance / Capacitance from each terminal to ground is identical
- There is NO ISOLATION
  - Used in some of the GEN DAQ acquisition cards
  - Often identified by the use of two METAL BNC connectors per channel
- Can be used with matched pair of probes only
  - Works with the same limitations as single probes, but is more tricky due to the necessary **balance** between probes
- The probes used need compensation. The compensation range needs to match the input amplifier's capacitance range

15.1.3 Isolated single-ended or Isolated unbalanced differential input

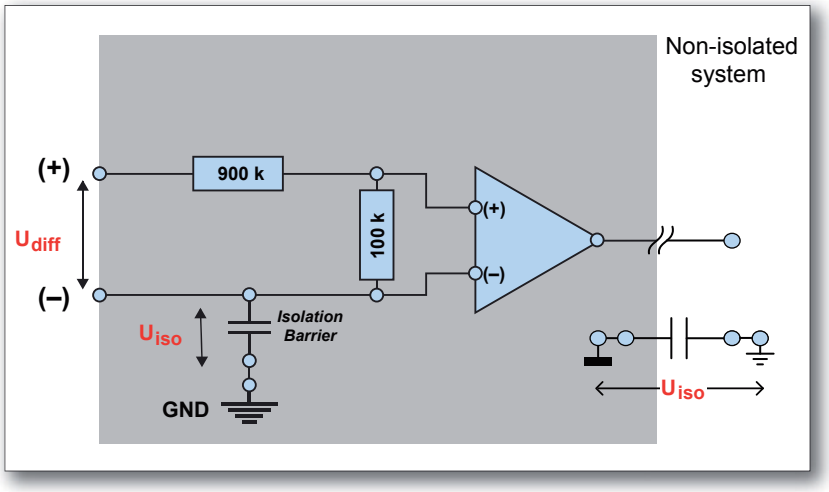


Figure 15.4: Isolated single-ended or Isolated unbalanced differential amplifier

- Also referred to as **unbalanced**, **isolated** or **unbalanced differential** amplifier
- None of the inputs are connected to ground for safety and to avoid ground loops
- Typically used in isolated DAQ systems
  - Often identified by the use of a single PLASTIC (isolated) BNC connector
  - Used in GEN DAQ ISOLATED Basic amp
- Can perform *DIFFERENTIAL MEASUREMENTS with different limitations and options, compared to a differential grounded amplifier*.

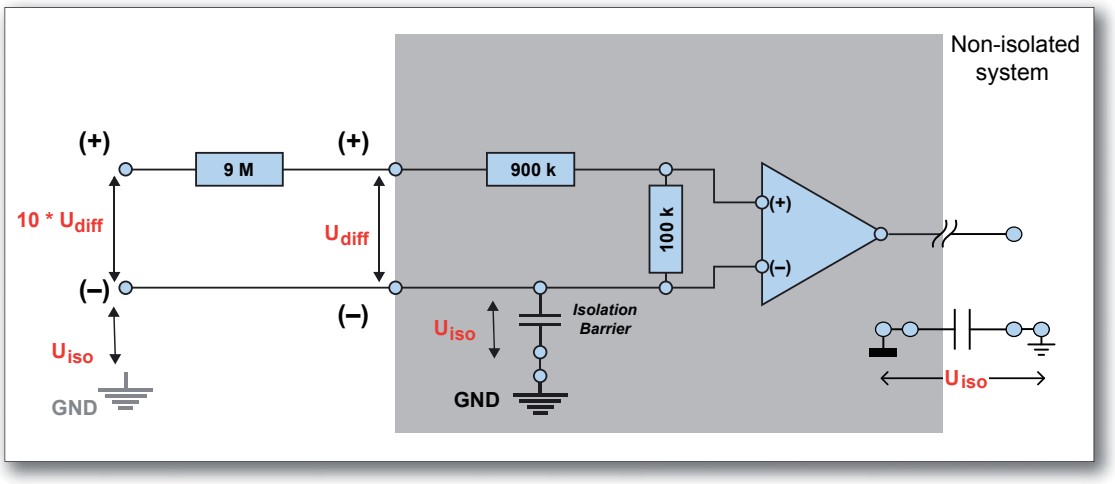


Figure 15.5: Isolated single-ended or Isolated unbalanced differential amplifier with passive probe

- Also referred to as **unbalanced**, **isolated** or **unbalanced differential** amplifier with probe
- None of the inputs are connected to ground
- The positive (system) input accepts ten times the input voltage of the amplifier
- The negative input has NOT CHANGED AT ALL
- The measurement range is increased from + to - inputs,
  BUT the isolation voltage from (-) to ground remains unchanged
  - Example is the GEN DAQ Basic XT Iso card with external Isolated passive probe
- The probes used need compensation. The compensation range needs to match the input amplifier's capacitance range

15.1.4 Isolated balanced differential input

An isolated balanced differential input is isolated and uses balanced inputs. Isolated measurement ground is not often available.

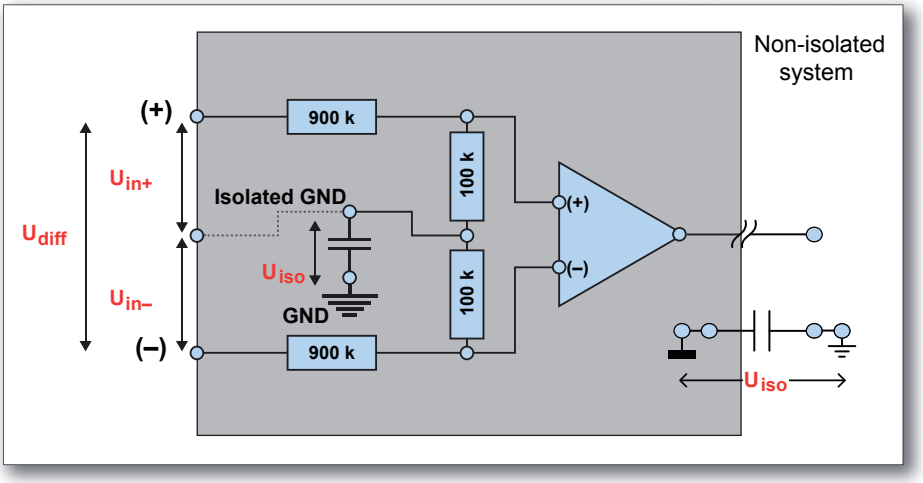


Figure 15.6: Isolated balanced differential amplifier

- Resistance / Capacitance from each terminal to isolated measurement ground is identical
- There is an ISOLATED MEASUREMENT GROUND
  - Used in GEN DAQ Universal amplifier
  - Typically identified by using two or three (isolated) connectors per channel

Note *The isolated ground is not accessible in some designs*

- Cannot be used with probes as there is no ground reference for probes to divide the voltage

Different amplifiers – Pros and Cons

Single-ended (to ground) amplifiers

- Cost effective and small
- High bandwidth
- Easy to use with probes
- Potential ground problems
- No safety problems
- No CMRR and no CMV

Single-ended isolated amplifier – unbalanced differential

- Can perform differential measurements
- Expensive and large
- Difficult to use with probes
- Limited CMRR, best CMV
- Avoids ground loops
- High level of safety

Differential amplifier (with common ground)

- Widely used in DAQ
- Good CMRR, limited CMV
- No (safety) isolation and potential ground loops will remain present

Differential amplifier with isolated common

- Safe
- Expensive and large
- Good CMRR, best CMV
- More difficult to use with probes

15.2 GEN series voltage probe types

HBM offers a variety of probes. Which probe is needed depends on the application and which instrument is being used. It is important to match the compensation of the probe to the instrument.

- **Passive, single-ended voltage probes**
  These probes can be used with single-ended or differential non-isolated amplifiers and increase the input range of the amplifier only in single-ended mode. They typically decrease the overall accuracy of the amplifier.
- **Passive, single-ended isolated voltage probes**
  These probes can be used with single-ended or differential isolated amplifiers and increase the input range of an isolated amplifier only in single-ended mode. They typically decrease the overall accuracy of the amplifier.
  It is important to understand that they increase only the range, not the isolation voltage.
- **Passive, differential matched isolated voltage probes**
  These probes can be used with differential isolated amplifiers and increase the input range of the amplifier in differential mode. They typically decrease the overall accuracy and the CMRR of the amplifier.
  They work with isolated and non-isolated variations of differential amplifiers.
  When used with isolated amplifiers, they increase only the range, not the isolation voltage.
- **Active differential voltage probes**
  These probes are self-contained, differential amplifiers to be used in front of an instrument using any amplifier in single-ended mode.
  The input range and accuracy depend on the type of active differential probe used and have no relation to the amplifier used. They usually operate from batteries; this causes some inconvenience.
- **Current clamps**
  Current clamps function more as transducers than probes, as they convert one physical quantity (current) into another one (usually voltage). They are used to perform non-invasive current measurements. This allows the current in a circuit to be measured without disturbing the circuit.

Note *There are other possibilities to measure current as well (current shunts, or Rogowski coils).*

15.2.1 Passive, single-ended voltage probes

Voltage probes divide a single-ended input signal by a specific factor.

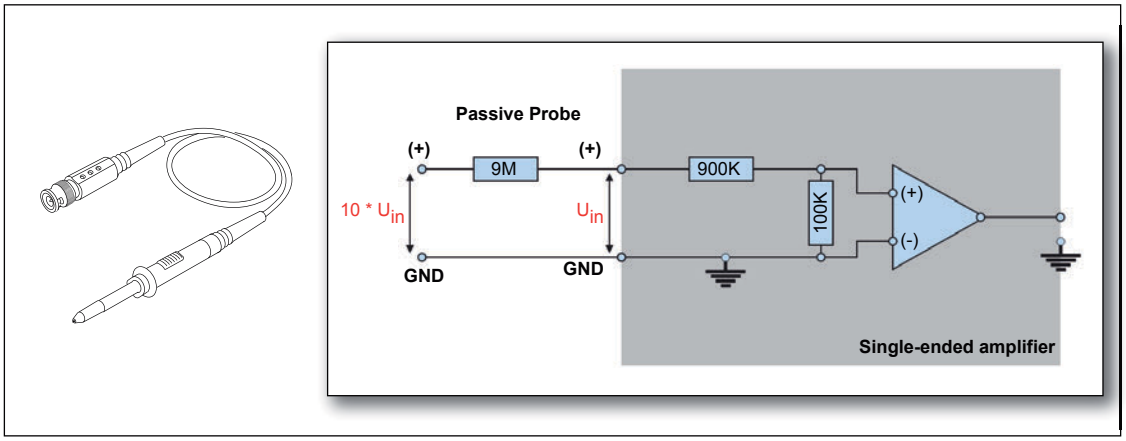


Figure 15.7: Typical example of a voltage probe

Theoretically, voltage probes are simply passive in-line resistors in series with the positive input of a single-ended amplifier. Together with the input resistor of the amplifier, they form a voltage divider so that the voltage in series with the amplifier itself is divided. As there is also a capacitive component in this divider, the input capacitance of the amplifier and the so-called “compensation range” of the probe need to match. Otherwise, signal distortion might occur.

By selecting a higher resistance probe, the divider ratio increases so that large input ranges can be achieved. Voltage probes do not provide or add either isolation or common mode voltage rejection. These probes can only be used in series with single-ended amplifiers.

Voltage probes typically decrease the overall accuracy of the system (caused by the inaccuracy of the input divider ratio formed by the external probe resistance and the internal amplifier resistance).

Table 15.1: Voltage probes overview table

Part number	Capacitive compensation range	Cable length	Divider factor	Bandwidth	Maximum input voltage
1-G901	7 - 75 pF	1.2 m	1 ± 2%	12 MHz	55 V RMS
			10 ± 2%	200 MHz	300 V RMS
1-G902	7 - 75 pF	3 m	1 ± 2%	12 MHz	55 V RMS
			10 ± 2%	200 MHz	300 V RMS
1-G903	7 - 45 pF	1.2 m	100 ± 2%	400 MHz	1 kV RMS
1-G904	10 - 50 pF	2 m	100 ± 2%	300 MHz	2 kV RMS 3 kV DC 3 kV pulse
1-G906	10 - 50 pF	3 m	1000 ± 2%	100 MHz	14 kV RMS 20 kV DC 40 kV pulse
1-G027-2	100 – 140 pF	3 m	1 ± 2%	2 MHz	55 V RMS
			10 ± 2%	50 MHz	300 V RMS

Table 15.2: Passive, single-ended voltage probe overview

Input card	1-G901	1-G902	1-G903	1-G904	1-G906	1-G027-2
GN110/GN111	✔	✔	✔	✔	✔	
GN112/GN113	✔	✔	✔	✔	✔	
GN114	✔	✔	✔	✔	✔	
GN610B/GN611B						
GN815/GN816						
GN840B						
GN1640B						
GN3210/GN3211	✔	✔				
GENIS-1T/GENIS-1TM	✔	✔	✔	✔	✔	

15.2.2 Passive, single-ended isolated voltage probes

Passive, single-ended isolated voltage probes divide an isolated input signal by a specific factor. They are designed in an “isolated way” (like plastic BNCs to prevent users from touching the connection) so they can be used in series with an isolated unbalanced amplifier. They are called “isolated voltage probes”, although the amplifier and not the probe adds the isolation.

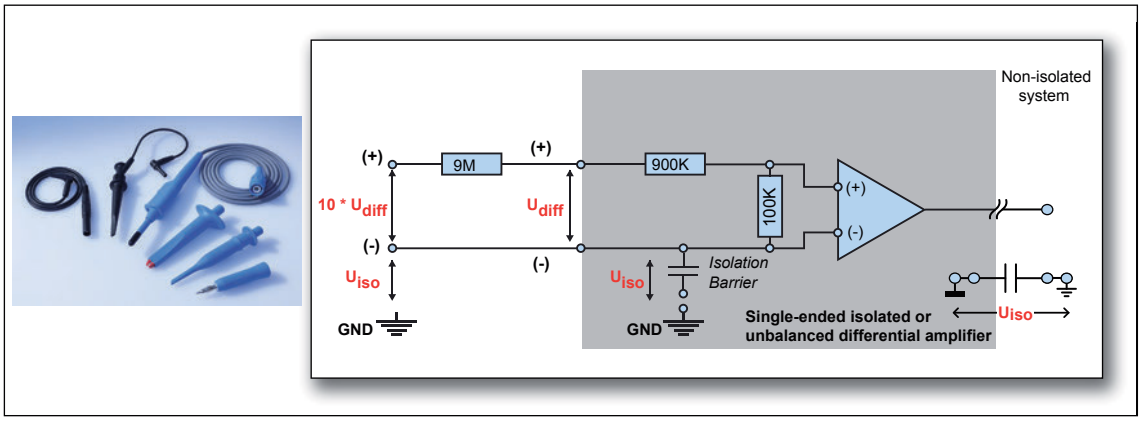


Figure 15.8: Typical example of an isolated voltage probe

Theoretically, voltage probes for isolated amplifiers are simply passive in-line resistors in series with the positive input of an isolated unbalanced amplifier as well.

Together with the input resistor of the amplifier, they form a voltage divider so that the voltage in front of the amplifier itself is divided. As there is also a capacitive component in this divider, the input capacitance of the amplifier and the so-called “compensation range” of the probe need to match. Otherwise, signal distortion might occur.

However, as the division only applies to the positive side of the amplifier input, the input range is increased while the isolation voltage remains the same as without a probe.

These probes can only be used in series with isolated unbalanced amplifiers.

Isolated voltage probes typically decrease the overall accuracy of the system (caused by the inaccuracy of the input divider ratio formed by the external probe resistance and the internal amplifier resistance).

Table 15.3: Voltage probes for ISOLATED amplifiers overview table

Part number	Capacitive compensation range	Cable length	Divider factor	Bandwidth	Maximum input voltage
1-G057	30 - 70 pF	1.2 m	100 ± 2%	50 MHz	3.5 kV RMS 1 kV RMS CAT II 600 V RMS CAT III

15.2.3 Passive, differential matched isolated voltage probes

Passive, differential matched isolated voltage probes are used in series with differential amplifiers and divide a differential input signal by a specific factor.

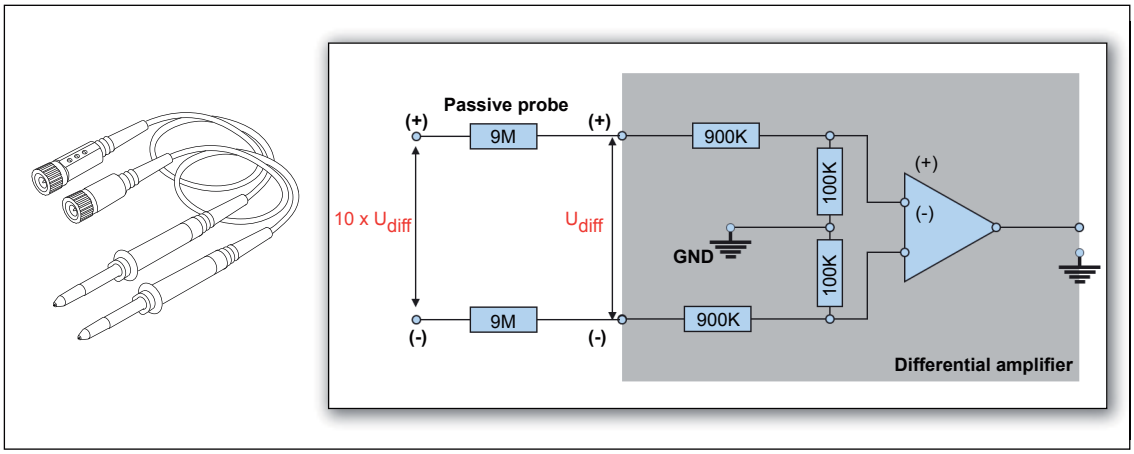


Figure 15.9: Typical example of a passive differential voltage probe

Passive, differential matched isolated voltage probes are – in theory – simply a pair of “normal” voltage probes.

They add passive in-line resistors in series with both the positive and the negative inputs of a differential amplifier. Together with the input resistor of the amplifier, they form a voltage divider on each input side so that the voltage in series with the amplifier itself is divided. As there is also a capacitive component in this divider, the input capacitance of the amplifier and the so-called “compensation range” of the probe need to match.

As two of these probes are used, one with each input terminal, the probes themselves need to “match” as closely as possible. Otherwise, the two input terminals are divided differently. Therefore, the probes are typically manufactured (and sold) in pairs and called “matched”. By selecting higher resistance probes, the divider ratio increases so that large input ranges are possible. Passive, differential matched isolated voltage probes typically decrease the overall accuracy and the CMRR of the system.

Table 15.4: Passive differential voltage probes overview table

Part number	Capacitive compensation range	Cable length	Divider factor	Bandwidth	Maximum input voltage
1-G025	100 – 140 pF	3 m	200 ± 2%	20 MHz	2.8 kV RMS 4 kV DC
1-G026-2	105 – 140 pF	3 m	10 ± 2%	100 MHz	400 V RMS 300 V RMS CAT II
1-G907	35 – 70 pF	3 m	10 ± 2%	100 MHz	300 V RMS CAT II

Table 15.5: Passive, single-ended isolated voltage probe overview

Input card	1-G025	1-G026-2	1-G907
GN110/GN111			
GN112/GN113			
GN114			
GN610B/GN611B			
GN815/GN816			
GN840B			
GN1640B			
GN3210/GN3211			✓
GENIS-1T/GENIS-1TM			

15.2.4 Active differential voltage probes

Active differential voltage probes are battery-powered, differential amplifiers in series with any input amplifier in single-ended mode.

Figure 15.10: Typical example of an active differential voltage probe

The achievable input range and accuracy depends on which active differential probe is used. Active differential probes can be used in series with virtually any amplifier, their performance typically is limited. The fact that they are usually battery-powerd may cause some inconvenience, as battery maintenance is required.

Active differential voltage probes typically decrease the overall accuracy of the system. The active output enables the use of the probe with (almost) any type of input.

Table 15.6: Active differential voltage probes

Part number	Capacitive compensation range	Cable length	Divider factor	Bandwidth	Maximum input voltage
1-G909	n/a	0.9 m	20 ± 2%	25 MHz	140 V RMS 140 V DC
			200 ± 2%	25 MHz	1.0 kV RMS 1.4 kV DC

15.2.5 Probe accessories

Probe accessories
1-G910 (LDS 040-747900)
Probe tip adapters with 4 mm safety-shrouded banana plugs. Include tip and ground lead adapters and two alligator clips with 1" jaw opening.
Use on probes G901 and G902 only.

G911 Probe Accessory Kit
1-G911 (LDS 869-925200)
Includes rigid probe tip, spring-loaded probe tip, insulating cap, ground lead, sprung hook, trimmer tool, and BNC adapter.
Use on probes G901 and G902 only.

15.3 Probe bandwidth calibration

A probe makes a physical and electrical connection between a test point or signal source and the instrument. Depending on the measurement needs, this connection can be made with something as simple as a length of wire or with something as sophisticated as an active differential probe.

For the purpose of this document, we only describe attenuating probes within two categories: 1X Probes and 10X Probes.

15.3.1 1X Probes

1X probes, also known as 1:1 (one-to-one) probes, simply connect the input of the instrument to the circuit being measured. They are designed for minimum loss and easy connection. Figure 15.11 shows the circuit diagram for an instrument input connected to a circuit under test. The circuit under test is modeled as a voltage source with a series resistor. The 1X probe (or cable) introduces a significant amount of capacitance that appears in parallel with the input of the instrument. A 1X probe may have around 40 to 60 pF of capacitance.

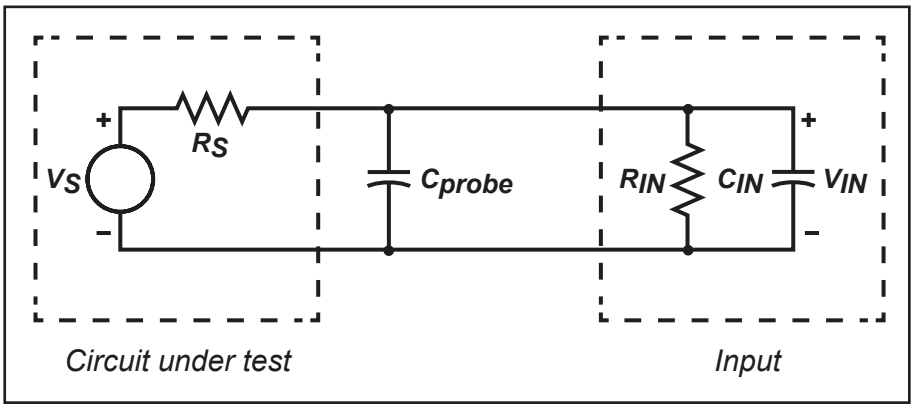


Figure 15.11: Input connection using a 1X probe

The impedance of the circuit and the input impedance of the instrument produce a lowpass filter. For very low frequencies, the capacitor acts as an open circuit and has little or no effect on the measurement. For high frequencies, the capacitor's impedance becomes significant and reduces the voltage detected by the instrument. Figure 15.12 shows this effect in the frequency domain. If the input is a sine wave, the amplitude tends to decrease with increasing frequency and the phase is shifted.

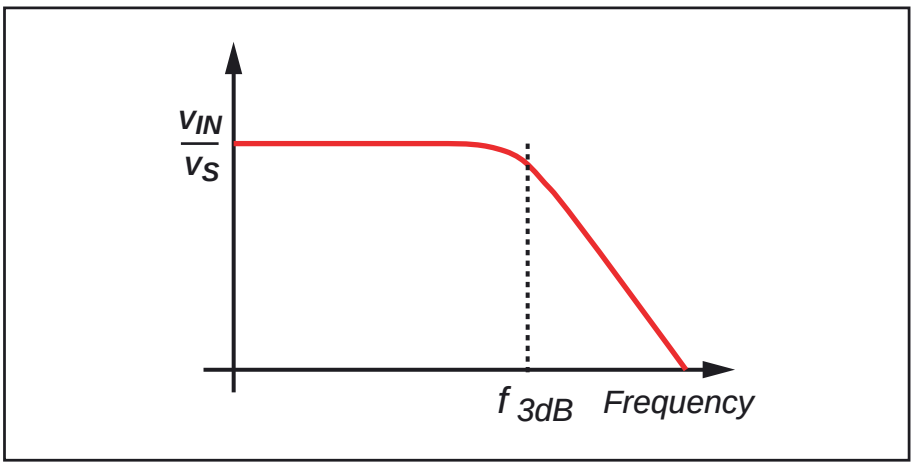


Figure 15.12: Frequency response with 1X probe

Example: Assuming that the voltage source has a 1 MΩ resistance and the 1X probe has a 50 pF capacitance (a 1X probe has no resistance by itself), the universal amplifier input would have a 1 MΩ resistance and a 100 pF capacitance.

This yields a -3dB point at:

(EQ1)

$$f(\text{-}3db) = \frac{1}{2\pi(R_s \| R_{IN})\ (C_{IN}+C_{probe})}$$

= 1 / (6.28 x 500 E+3 x 150 E-12) ≈ 2 kHz

The loading due to the input impedance of the instrument and the probe capacitance is twofold: resistive loading and capacitive loading.

The resistive loading actually reduces the voltage delivered to the instrument:

(EQ2)

$$V_{IN} = V_S\left(\frac{R_{IN}}{R_{IN}+R_S}\right)$$

The effect of the capacitive loading is more complex and results in an exponential response in the voltage:

(EQ3)

$$V_{IN}(t) = V_{MAX}\left[1 - e^{-t/(R_S C_{in\ +\ probe})}\right]$$

15.3.2 10X Probes

10X probes (also called 10:1 probes, divider probes, or attenuating probes) have a resistor and capacitor (in parallel) inserted into the probe.
Figure 15.13 shows the circuit diagram for the 10X probe connected to a high-impedance input of an instrument.

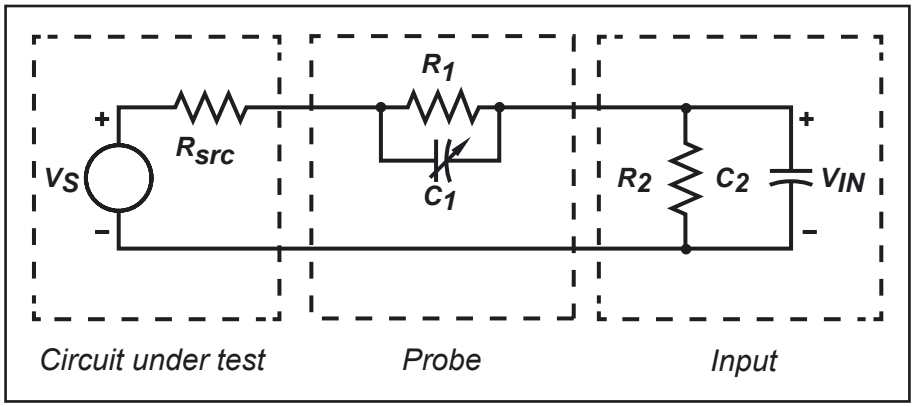


Figure 15.13: Input connection using a 10X probe

Assuming that R_{src} is low compared to R_1 and that $R_1 * C_1 = R_2 * C_2$, then the effect of both capacitors cancel each other out in this circuit. The capacitor is usually adjustable and can be tweaked for a nearly perfect match. In these conditions, the relationship of VS to VIN is:

(EQ 4)

$$V_{IN} = V_S\left(\frac{R_2}{R_1 + R_2}\right)$$

R_2 is the input resistance of the instrument's high input impedance (1 MΩ) and $R_1 = 9 * R_2$. Using the previous equation, this results in:

(EQ 5)

$$V_{IN} = \left(\frac{1}{10}\right)V_S$$

The final result is a probe / instrument input combination that has a much wider bandwidth than the 1X probe due to the effective cancellation of the two capacitors. However, the instrument now measures only one-tenth of the original voltage (hence the name 10X probe). The circuit being measured is affected with a load impedance of $R_1 + R_2 = 10$ MΩ, which is much higher than with the 1X probe.

IMPORTANT

To perform the compensation correctly, both impedances must have the same value, i.e. $R_1 * C_1 = R_2 * C_2$. In practice, $R_1 * C_1$ will never be equal to $R_2 * C_2$, but the values can be approximated. The probe's compensation capacitor is usually adjustable somewhere between 10 pF and 50 pF to compensate for the instrument's input capacitance. Since the Universal Amplifier has a 100 pF capacitance, the compensation cannot be performed correctly with standard probes. Therefore, the probe capacitance must be adapted to this situation. Various probe manufacturers offer the possibility to purchase probes with other compensation ranges on request.

15.3.3 Probes and differential measurements

Connecting the differential amplifier or probe to the signal source is generally a major source of error. To maintain the input match, both paths should be as identical as possible. Any cabling should be the same length for both inputs. If individual probes are used for each signal line, they should be the same model and have the same cable length. When measuring low-frequency signals with large common mode voltages, avoid the use of attenuating probes. At high gains, they simply cannot be used as it is impossible to balance their attenuation precisely. When attenuation is needed for high-voltage or high-frequency applications, special passive probes designed specifically for differential applications should be used. These probes have provisions for precisely trimming the DC attenuation and AC compensation. To get the best performance, a set of probes should be dedicated to each specific amplifier and calibrated with that amplifier using the procedure included with the probes.

15.4 Current shunt measurements

Special care must be taken with shunt measurements. Typical shunt measurements generate signals with an amplitude of only a few volts or even mV. To prevent interference from higher voltage signals (up to 100 V), the following guidelines apply:

- Use only coaxial cables for all measurements.
- If possible, place the instrument as close as possible to the test object to reduce the length of the coax cable.
- Physically separate the low voltage signal lines from the high voltage signal lines as much as possible. Do not combine them. When the high voltage signals include high frequency transients, these will easily cross over to the low voltage signals.

HINT/TIP

The GEN DAQ series instruments typically have a very high bandwidth. Potential higher frequency transients are measured as a result of the high bandwidth. Using other lower bandwidth equipment can not measure these results. Use the filter to reduce the bandwidth to a physically relevant value.

A Specifications

A.1 B3762-6.0 en (GEN3i Portable Data Recorder)

- **Built-in PC**
- **Robust and portable**
- **Three slots for any mix of acquisition cards**
- **Up to 96 analog channels**
- **200 MB/s continuous streaming**
- **Remote use from external PC**
- **Perception Advanced software for review and analysis**
- **Power failure data security**
- **Wake on LAN**
- **Master/Slave synchronization**
- **PTP time synchronization**
- **IRIG/GPS time synchronization (option)**
- **1 Gbit optical Ethernet (option)**
- **10 Gbit optical or electrical Ethernet with 400 MB/s continuous streaming (option)**

The GEN3i is a versatile portable data recorder. In addition, it provides all the features expected from a transient recorder. The hardware combines a full-featured, low-power, Intel Core™ i5 3rd generation Windows® PC with a large, high-resolution, touch screen and a robust three-slot acquisition unit. The GEN3i power failure data security feature enables recording file integrity during continuous recording minimizing data loss upon sudden power loss. As soon as power restores, GEN3i automatically reboots and resumes the recording with the setup used prior to power loss. GEN3i features five different Windows® languages and eight different Perception languages pre-installed.
Designed for operation in the field as well as in the laboratory, GEN3i features a unique, Instrument Panel touch interface, with one-touch access to all features for daily operation.
In addition, GEN3i includes the Perception Advanced for post-processing. With a single touch, the data recorder turns into a dedicated instrument for analysis and sophisticated reporting. If third party analysis is preferred, up to 20 export formats are available including MATLAB, DIAdem, MDF4/ASAM, UFF58 and more.

Block Diagram

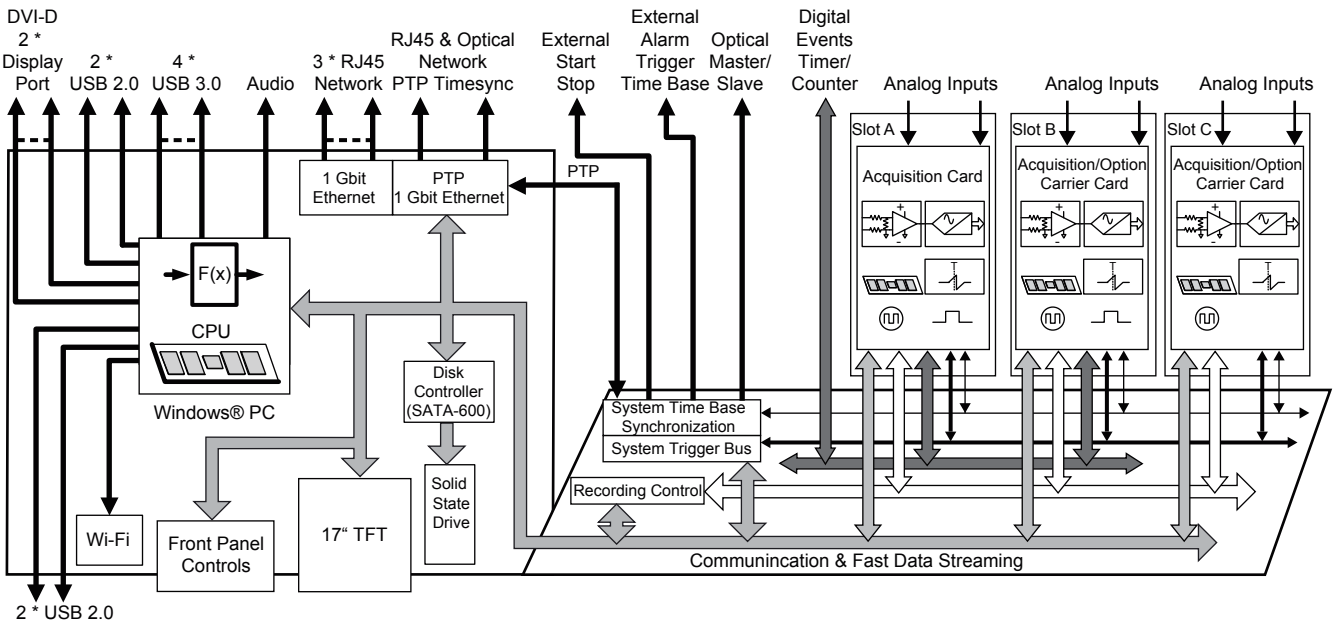


Figure A.1: Block diagram

Windows® PC	
Memory	8 GB; DDR3 RAM
Processor	Intel 3610ME, Core™ i5 3rd generation; 2 Core, 4 threads; 2.7 GHz, 3.3 GHz turbo
Ethernet	1 * RJ45 Ethernet connection with PTP V2 support; 1 Gbit/s 3 * RJ45 Ethernet connection without PTP V2 support; 1 Gbit/s 1 * SFP based optical Ethernet connection with PTP V2 support; 1 Gbit/s; supports 850 and 1310 nm SFP modules.
Wake on LAN	Supported on all Ethernet ports
Wireless LAN (WIFI)	Embedded 801.11b/g/n; 54, 100 and 300 Mbit/s; wireless LAN can be hardware disabled
USB connectors	USB 2.0, two in back + two in front USB 3.0, four in back (using selective SSD > 100 MB/s continuous streaming)
Internal storage PC disk	Solid State Drive (SSD), unformatted size 480 GB, 200 MB/s continuous streaming. The size of SSDs increases almost every year. Contact the local HBM support team or custom systems(1) for availability.
Display	TFT SXGA touch screen, 17” / 1280x1024 resolution
Video connection	2 * Display port and 1 * DVI-D connector; CRT 2048x1536 and DVI-D 1600x1200
Multiple monitors support	3; clone mode and extended mode
Speaker/Speaker Out	Internal speaker/jack plug 3.5 mm
Microphone	Jack plug 3.5 mm
Accessories	Protective carrying bag, USB keyboard and USB optical mouse
Front panel controls	4; direct recording control for Start/Stop/Pause/Trigger

(1) Contact custom systems at: customsystems@hbm.com

Software	
Instrument Panel/touch interface (Fully touch-optimized)	Setup of instrument, Acquisition control, Display data: live/review, Basic measurements, Export and archiving, Basic reporting
DAQ software	Perception Advanced package. Includes real-time live and recorded data review using y/t and x/y displays. Y/t displays support vertical, horizontal and slope cursors, trace and display markers as well as an interactive waveform calculator. On top Perception allows synchronized video playback. For data analysis Perception supports interactive user keys with macro support, Formula Database with waveform and math calculators. To create a report of the recorded and analysis data Perception supports adding additional meta data describing your test details, quick report to Microsoft Word® and Excel®, an advanced built-in report engine. If analysis in third party software is preferred 20 export format (Including MATLAB, DIAdem, MDF4/ASAM, UFF58 and more) are supported. For automated analysis, reporting or data exports Perception supports extensive automation and result logging features.
DAQ software options	Basic FFT, Sensor Database, User Definer Mode and Multi Mainframe Control.
DAQ software and Instrument Panel languages	English, German, French, Chinese, Japanese, Korean, Russian, Portuguese (Brazilian)
Operating system	Microsoft Windows® 10 PRO (Windows® 7 Ultimate for systems shipped before November 2016)
Languages installed in operating system	English, German, French, Chinese, Japanese Other languages can be downloaded and installed using "Windows® Update"

Acquisition System	
System Time Base and Synchronization Central time base for all acquisition cards	
Accuracy	± 3.5 ppm; aging after 10 years ± 10 ppm
Base	Binary, Decimal or External
Synchronization sources	IEEE1588:2008 PTP V2 (Precision Time Protocol) using an End-to-End protocol Master/Slave synchronization; Slave or Master mode on built-in connector Master output card (G083): Option to synchronize up to 16 Slave systems
PTP synchronization accuracy	± 150 ns; no Ethernet switch used When network switches are required, use only PTP aware switches that support End-to-End set-ups. Overall accuracy depends on PTP switch used.
Acquisition Slots Unused slots must be covered using the GEN DAQ blind panel. This closes the mainframe front panels for EMC/EMI and safety compliance and also regulates the internal airflow to cool the acquisition system correctly.	
Maximum slots	3
Acquisition cards	Any combination of GEN DAQ acquisition cards which support fast data streaming
Digital Event/Timer/Counter connector	1; Connected to slots A and B
Thermal control	Every acquisition card and the acquisition system monitors its own temperature and status. This is used to regulate fan speeds and reduce noise while optimizing airflow and power consumption.
Calibration	Any changes to the acquisition system configuration may change its internal thermal gradients. As accurate calibration relies on a steady and repeatable thermal environment, calibration is void if changes are made in the configuration. For information on calibration impact, please refer to the individual card specifications.

Connection Overview

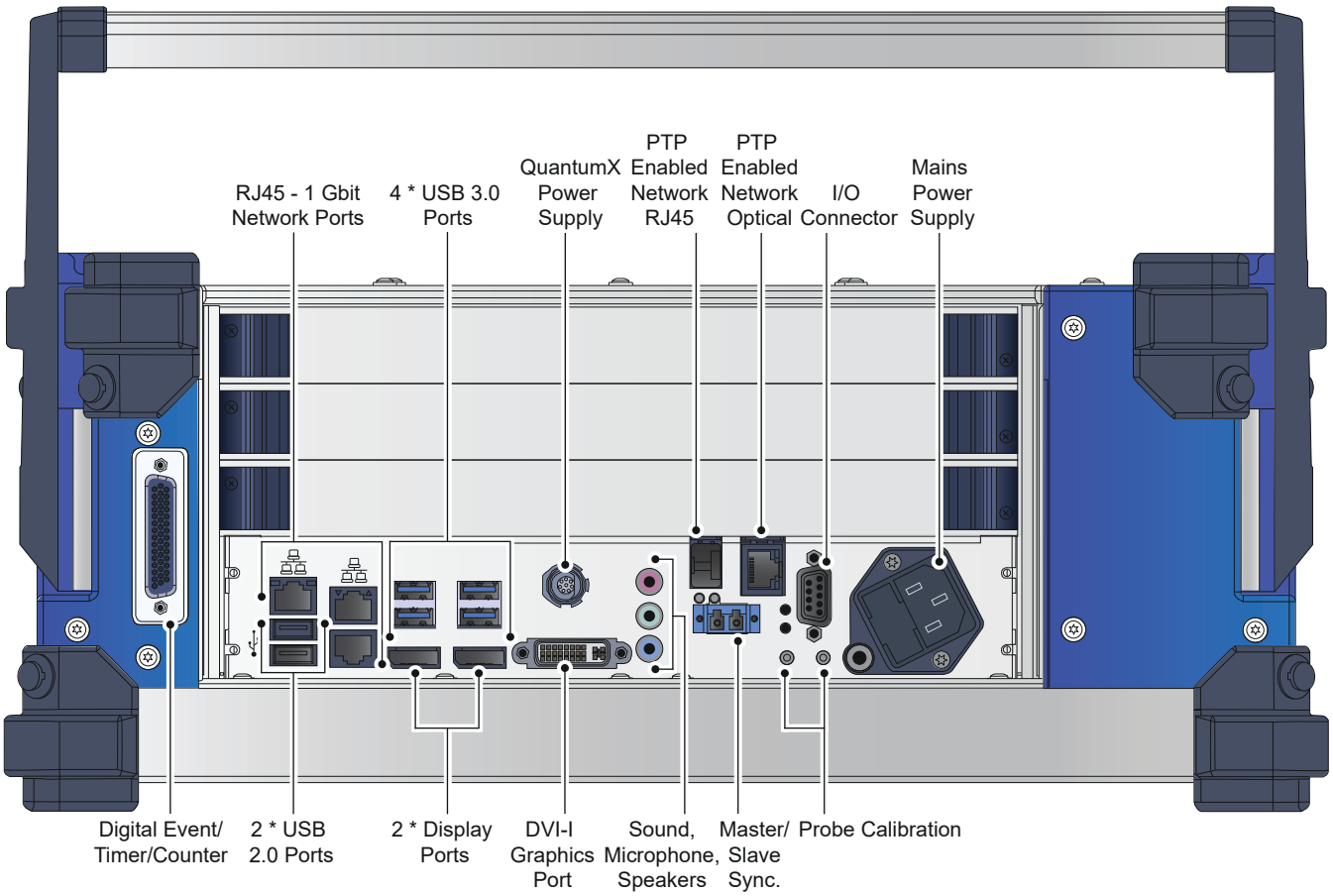


Figure A.2: Connection overview

GEN3i Stand-Alone Recorded Data Storage Overview

Using GEN3i in stand-alone mode allows for several storage options. The built-in SSD is directly controlled by the Windows® PC inside the GEN3i. As a result all storage options are Perception PC storage based. Continuous streaming throughput is tested by using 48 hours of circular recordings at specified data rates.

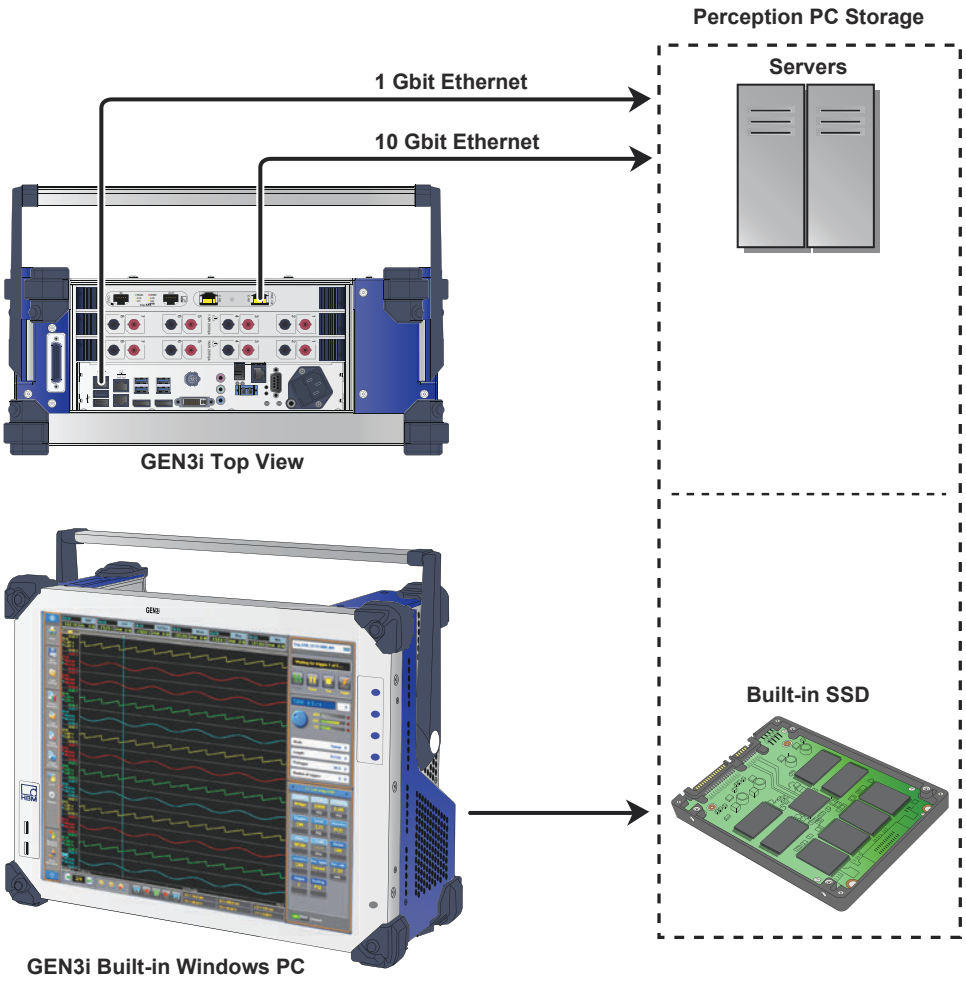


Figure A.3: Data storage overview

Maximum continuous data storage rates	Perception PC storage (GEN3i)
Built-in SSD	200 MB/s(2)
Server storage	
1 Gbit Ethernet (optical or electrical)	100 MB/s(3)
10 Gbit Ethernet (optical or electrical, option)	400 MB/s(1)(4)
Power failure data security	
Continuous recording	When storing continuous recorded data on the built-in SSD Perception secures all recorded data is stored on the SSD on regular intervals. The interval time depends on the continuous data storage rate used. A sudden power loss at higher continuous data storage rates results in more recording time loss just before the moment the power disappeared.
Sweep and dual rate recording	When storing sweeps and/or dual rate recordings the data storage behavior is heavily depending on the triggers detected by the system. Sudden bursts of triggers mean a lot of data to be stored. A power loss during or right after this trigger burst will result in much more data loss compared to a moment in time the system is waiting for triggers.

(1) Legacy cards do not support the enhanced fast streaming bus. The maximum aggregate storage rate for legacy cards is 200 MB/s.

(2) Tested using circular recording for 48 hours.

(3) Tested using circular recording for 48 hours. Test setup uses a Synology® DS212 configured with a two disk RAID 0 partition.

(4) Tested using circular recording for 48 hours. Test setup uses a Synology® DS3412 configured with a eight disk RAID 0 partition and a 10 Gbit Ethernet link.

GEN3i Remote Controlled Recorded Data Storage Overview

Using GEN3i in remote mode allows for several storage options. While in remote control, Perception on the GEN3i Windows® PC is closed. As a result all Solid State Drives (internal and removable) are not usable anymore.
Continuous streaming throughput is tested by using 48 hours of circular recordings at specified data rates.

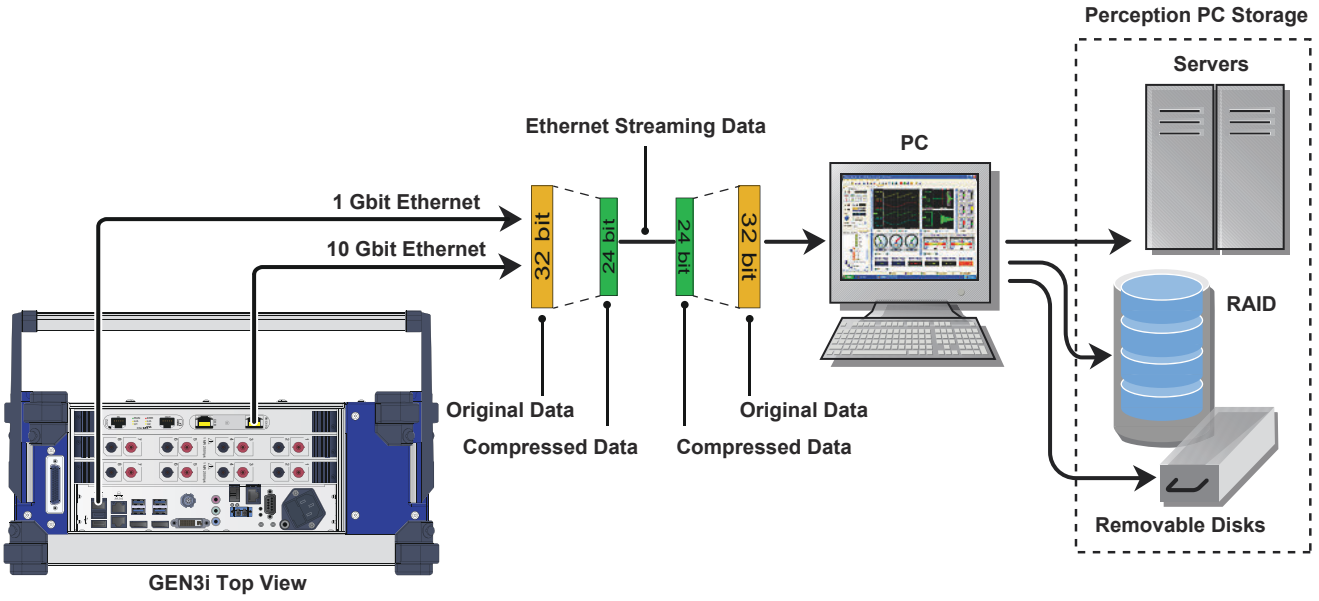


Figure A.4: Remote data storage overview

Maximum continuous data storage rates (tested using full disk circular recording for 48 hours)	**Perception PC storage**	
	Uncompressed	Compressed
1 Gbit Ethernet (optical or electrical)	100 MB/s(1)	Up to 175 MB/s(1)(2)
10 Gbit Ethernet (optical or electrical, option)	400 MB/s(3)	n/a
Built-in SSD	Not usable in this mode	Not usable in this mode

(1) Test setup uses a Windows® 7 PC with Intel i7 CPU and SSD with sustained write speeds exceeding 250 MB/s.

(2) Compression ratio is defined by the ADC channel width. For details, please refer to the "Streaming Compression Ratio" table (below). Rate is valid before decompressing storage data to maintain backward PNRF compatibility.

(3) Test setup uses a Windows® 7 PC with Intel i7 CPU and SSD with sustained write speeds exceeding 700 MB/s and a 10 Gbit Ethernet link.

Analog Channel Streaming Compression Ratio

Acquisition cards	**Sample width**	**Compression ratio**	
		16 bit storage	**32 bit storage**
GN610B, GN611B	18 bits	1 : 1	1.75 : 1
GN815, GN816	18 bits	1 : 1	1.75 : 1
GN840B, GN1640B	24 bits	1 : 1	1.33 : 1
GN1202B	14 bits	1 : 1	N/A
GN3210, GN3211	24 bits	1 : 1	1.33 : 1
GN8101B, GN8102B, GN8103B	14 bits	1 : 1	N/A

Master/Slave Synchronization

GEN series mainframes support a Master/Slave synchronization connector. The connector can be used as a single Master output or as a Slave input. The Master output function can be extended using the Master output card (G083).

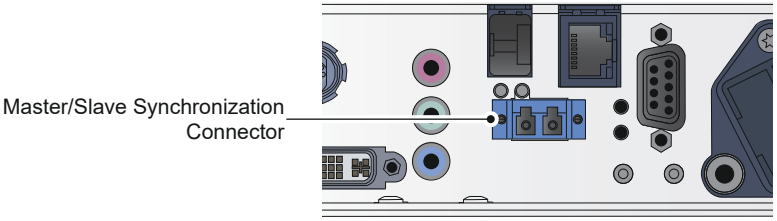


Figure A.5: Master/Slave synchronization connector

Mainframe to mainframe phase shift	± 150 ns RMS
LED signaling	Optical link synchronized, not connected, function disabled
Master mode	Basic and extended synchronization supported; Supports one Slave. Multiple Slave support by using one or more optional Master output cards (G083)
Slave mode	Basic and extended synchronization supported
Maximum number of mainframes	2; more mainframes supported when using one or more optional Master output cards (G083)
Time required to full synchronization after Master/Slave signal detected	
No recording active	Typically 1 minute
Recording or pause active	1 minute and an additional 25 s per ms recording time deviation from Master time
User notifications while recording	Time marks on Master/Slave signal lost/restored and Master/Slave time synchronized
Basic synchronization	
Cable length propagation delay	Automatic cable length detection and propagation delay compensation
First sample	Synchronizes the first sample in a continuous recording for each mainframe. Cable length propagation delay not compensated for at start of recording. First samples not recorded in the Slave mainframes, as defined by the propagation delays. Signal phase shifts are not introduced by this propagation delay.
Synchronized time base	Prevents frequency drift of the sample rates within each mainframe
Measured channel trigger exchange	Synchronously exchanges measured channel triggers connected to the Master/Slave trigger bus to/from each connected mainframe. Typically used for the sweep recording modes.
Compatibility	Basic synchronization features are backward compatible with GEN series Master/Slave card option for both Master and Slave modes
Extended synchronization	
Calculated channel trigger exchange	Additional trigger bus to synchronously exchange trigger conditions detected on real-time calculated (RTC) channels between mainframes. RTC channel triggers have a longer delay caused by the required calculation time prior to establishing a trigger.
Synchronous manual trigger	User action within Perception to trigger all mainframes synchronously
Synchronous recording actions	Start/Stop and Pause a recording across multiple mainframes, each of which is controlled by a separate instance of Perception. Stop recording is a non-synchronous action. Synchronously records distributed data with a mix of two GEN7i/t - GEN3i/t - GEN2i mainframes in Master/Slave setup while running Perception on each of the mainframes. A more typical Master/Slave setup would be to stop Perception on one system and use one instance of Perception application to control both systems.
Compatibility	Extended synchronization features are not supported by the legacy Master/Slave card option. A mixed system setup automatically works with basic synchronization.
Connection	
Optical wavelength	850 nm
Optical cable type	Multi Mode 50/125 µm
Optical data rate	2 Gbit/s
Maximum cable length	500 m
Connector type	Duplex LC

Synchronization Specification Overview

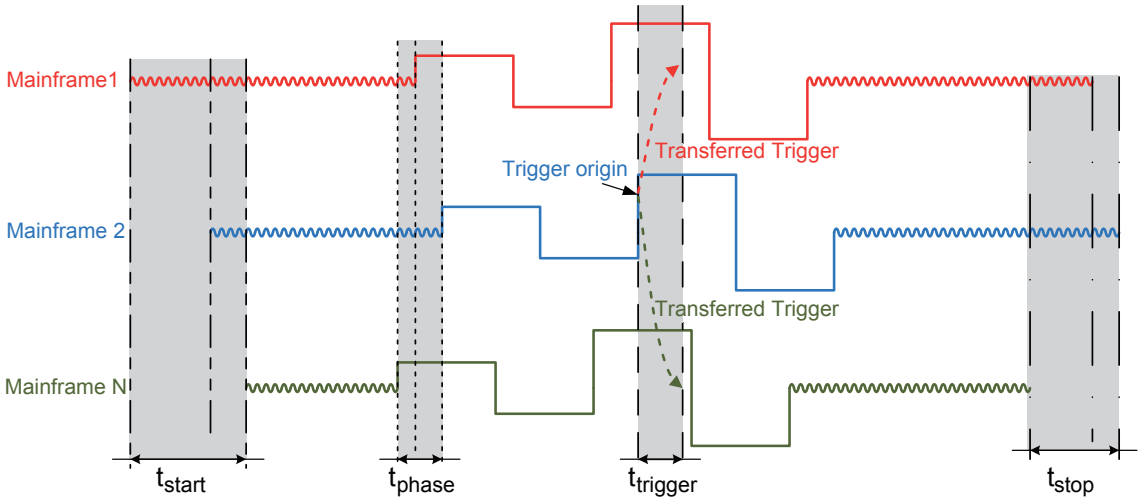


Figure A.6: Synchronization specification overview

Master to Slave and Slave to Slave timing	t_{phase} (1)	t_{start} (2)	t_{stop} (3)	$t_{trigger}$ (4) (5)
Synchronization source				
Master/Slave	≤ 150 ns	≤ cable delay	≤ 1 s	≤ 150 ns
PTP	≤ 150 ns	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)
GPS	≤ 1 µs	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)
IRIG	≤ (10 µs + cable delays)	≤ 1 s	≤ 1 s	≤ (516 µs + cable delays)
No synchronization source				
Mainframes connected by Perception simultaneously	≤ 1 s	≤ 1 s	≤ 1 s	≤ 1 s
Additional error after connection	≤ 0.5 s/hour	≤ 0.5 s/hour	≤ 0.5 s/hour	≤ 0.5 s/hour

(1) t_{phase} Maximum phase difference between signals. *(This specification is not affected by any of the other specifications).*

(2) t_{start} Maximum delay between the start of recording for each mainframe.

(3) t_{stop} Maximum delay between the stop of recording for each mainframe.

(4) $t_{trigger}$ Maximum delay to transfer a trigger from one mainframe to all other mainframes.

(5) **Note** on trigger exchange
Trigger exchange is included in the Master/Slave synchronization cable. All other synchronization modes require that the mainframes are connected from each External Trigger Out to each External Trigger In on all the mainframes in order to exchange triggers.

I/O Connector

PIN Signal
PIN 1 - External Time base In
PIN 2 - External Event Out
PIN 3 - External Trigger In
PIN 4 - Ground
PIN 5 - Ground
PIN 6 - External Start In
PIN 7 - External Trigger Out
PIN 8 - External Stop In
PIN 9 - Ground

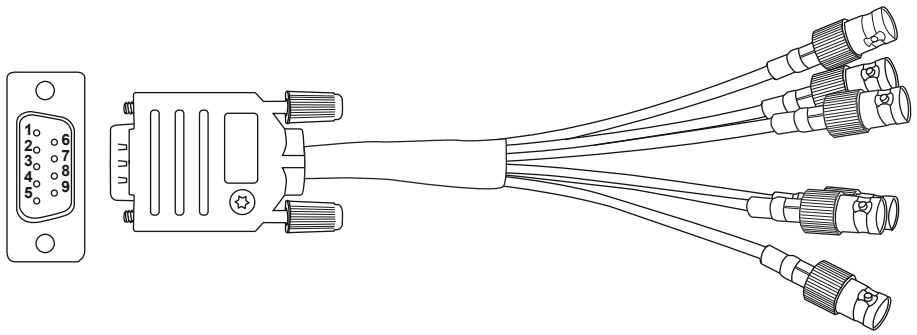


Figure A.7: Pin assignment and breakout cable

Connector type	TE (Tyco Electronics) connectivity: 2-5747706-0 (D-sub, 9-pin female)
Mating connector type	TE (Tyco Electronics) connectivity: 5-747904-5
Breakout cable (included)	
Cable type	Coax
Connector type	6; BNC female
Length	0.5 m (1.6 ft)
External Time base In	
Levels	TTL compatible, Low -30 V to 0.7 V, High 2 V to 30 V Input has an internal pull-up of 20 kΩ ± 1% to 5 V
Input overvoltage protection	± 30 V DC
Maximum frequency	5 MHz
Minimum pulse width	100 ns
Active edge	Rising
Rounding resolution	4.01 µs; 250 kS/s and 20 kS/s acquisition cards
	1.01 µs; 1 MS/s and 200 kS/s acquisition cards
	510 ns; 2 MS/s and 200 kS/s (GN611B/GN816) acquisition cards
	60 ns; 100 MS/s and 25 MS/s acquisition cards
Input to sample moment delay	350 – 400 ns, plus up to one full "rounding resolution"
External Trigger In	
Levels	TTL compatible, Low -30 V to 0.7 V, High 2 V to 30 V Input has an internal pull-up of 20 kΩ ± 1% to 5 V
Input overvoltage protection	± 30 V DC
Resolution	50 ns
Minimum pulse width	500 ns
Active edge	Rising or falling; software selectable
Delay	± 1 µs + up to one sample period (for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
Top Dead Center Rotational input	Used to indicate top dead center in rotational external time base
External Trigger Out	
Levels	TTL compatible; 0 V < Low < 0.6 V; 2 V < High < 5 V
Active level	High/Low/Hold High; software selectable
Pulse width	High or Low selected: 12.5 to 12.8 µs Hold High selected: Active from first trigger to end of recording
Maximum output current	50 mA, short circuit protected
Output impedance	49.9 Ω ± 1%
Short circuit protected	Continuous
Delay	User selectable; minimum value may vary for each acquisition card. Default 516 ± 1 µs (504 Binary sample rates) + up to one sample period; Filter set to wideband (1)

(1) If an analog and/or digital filter is used, extra delay will be added, depending on the type of filter and signal frequency.

I/O Connector	
External Event Out	
Levels	TTL compatible; 0 V < Low < 0.6 V; 2 V < High < 5 V
Function	Alarm or Recording Active output; software selectable
Active level	High/Low for Alarm output; software selectable Recording active High output
Pulse width	Alarm: Active from start of alarm condition until condition ends Recording: Active until recording stops
Maximum output current	50 mA, short circuit protected
Output impedance	49.9 Ω ± 1%
Short circuit protected	Continuous
Delay	User selected external trigger output delay - 1 µs
External Start In	
Levels	TTL compatible, Low -30 V to 0.7 V, High 2 V to 30 V Input has an internal pull-up of 20 kΩ ± 1% to 5 V
Input overvoltage protection	± 30 V DC
Minimum Pulse width	200 ns
Active edge	Rising/falling edge; software selectable
Start response time	Typically 1 s when system is completely idle
External Stop In	
Levels	TTL compatible, Low -30 V to 0.7 V, High 2 V to 30 V Input has an internal pull-up of 20 kΩ ± 1% to 5 V
Input overvoltage protection	± 30 V DC
Minimum Pulse width	200 ns
Active edge	Rising/falling edge; software selectable
Stop response time	Typically 1 s when system is recording without automation

Digital Event/Timer/Counter

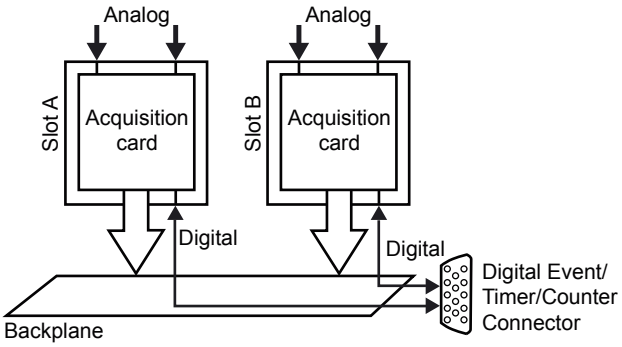


Figure A.8: Digital Event/Timer/Counter block diagram

Supported cards	See specifications of acquisition cards
Number of connectors	1
Connector type	44 pin, female D-type connector, AMP HD-22 series (Tyco/TE connectivity: 5748482-5)
Mating cable connector type	44 pin, male D-type connector, HDP-22 series (Tyco/TE connectivity: 1658680-1)
Output power	
Voltage	5 ± 0.5 V DC
Maximum current	0.5 A

Digital Event/Timer/Counter

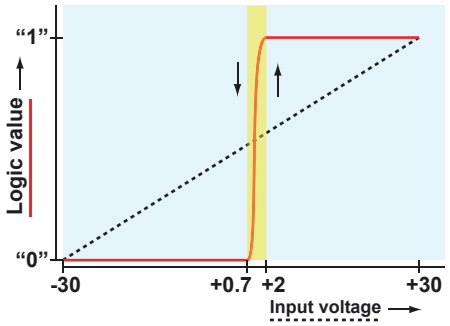
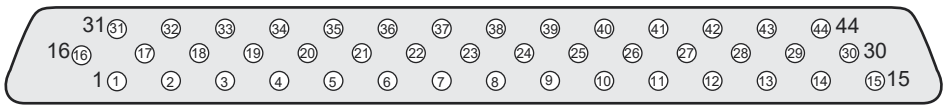
Event Inputs	
Number of event inputs	16 per card, 2 cards per connector
Levels	TTL Compatible, Low -30 V to 0.7 V, High 2 V to 30 V
	
Overvoltage protection	± 30 V DC
Timer/Counter	
Number of channels	Two per card, two cards per connector
Functions	See specifications of the acquisition cards that support these inputs
Outputs	
Number of outputs	Two per card, two cards per connector
Functions	See specifications of acquisition cards that support these outputs
Output levels	TTL compatible; 0 V < Low < 0.6V; 2 V < High < 5 V
Output resistance	49.9 Ω ± 1%
Maximum output current	50 mA, short circuit protected

Figure A.9: Logic threshold voltage levels

Digital Event/Timer/Counter Connector Pin Assignment



PIN 1 - Event Input 1A & Reset Timer/Counter 2A
PIN 2 - Event Input 2A & Direction Timer/Counter 2A
PIN 3 - Event Input 3A & Clock Timer/Counter 2A
PIN 4 - Event Input 4A
PIN 5 - Event Input 5A
PIN 6 - Event Input 6A
PIN 7 - Event Input 7A
PIN 8 - Event Input 8A
PIN 9 - Event Input 9A
PIN 10 - Event Input 10A & Reset Timer/Counter 1A
PIN 11 - Event Input 11A & Direction Timer/Counter 1A
PIN 12 - Event Input 12A & Clock Timer/Counter 1A
PIN 13 - Event Input 1B & Reset Timer/Counter 2B
PIN 14 - Event Input 2B & Direction Timer/Counter 2B
PIN 15 - Event Input 3B & Clock Timer/Counter 2B
PIN 16 - Event Input 4B
PIN 17 - Event Input 5B
PIN 18 - Event Input 6B
PIN 19 - Event Input 7B
PIN 20 - Event Input 8B
PIN 21 - Event Input 9B
PIN 22 - Event Input 10B & Reset Timer/Counter 1B
PIN 23 - Event Input 11B & Direction Timer/Counter 1B
PIN 24 - Event Input 12B & Clock Timer/Counter 1B
PIN 25 - Event Input 13B
PIN 26 - Event Input 14B
PIN 27 - Ground
PIN 28 - Ground
PIN 29 - Ground
PIN 30 - Ground
PIN 31 - Event Input 15B
PIN 32 - Event Input 16B
PIN 33 - Event Input 13A
PIN 34 - Event Input 14A
PIN 35 - Event Input 15A
PIN 36 - Event Input 16A
PIN 37 - Event Output 2B
PIN 38 - Event Output 1B
PIN 39 - Event Output 2A
PIN 40 - Event Output 1A
PIN 41 - Ground
PIN 42 - Ground
PIN 43 - +5 V Power
PIN 44 - +5 V Power

Figure A.10: Pin diagram for Digital Event/Timer/Counter connector

DC Power Output	
Connector type	ODU, G81L0C-P08LFG0-0000
Mating connector type	ODU, SX1LOC−P08MFG0−0000
Connector pinning	QuantumX compatible; only GND and PWR signals connected
Output Power	15 Watt
Output Voltage	> 11 V; Typically 11.5 V to 12 V
Maximum Output Current	1.4 A; Limited current and short circuit protected

PIN Signal
PIN 1 - Reserved/not connected
PIN 2 - Reserved/not connected
PIN 3 - GND
PIN 4 - Reserved/not connected
PIN 5 - Reserved/not connected
PIN 6 - Reserved/not connected
PIN 7 - PWR
PIN 8 - Reserved/not connected

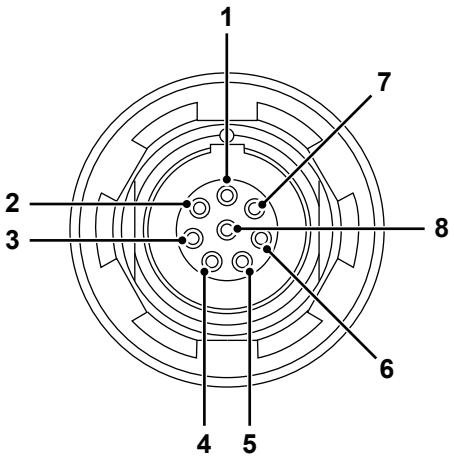


Figure A.11: Connector power output

Probe Calibration	
Pins	2; Signal and ground
Signal	~1 kHz square wave
Signal amplitude	0 V to 2 V using 1 MΩ load 0 V to 1 V using 50 Ω load

Power	
Power Inlet	47-63 Hz, 100-240 V AC
Total Power of unit (maximum)	250 VA, 300 VA peak

Physical, Weight and Dimensions	
Weight	
Mainframe	9 kg (20.9 lb), add ≈ 1 kg (2.2 lb) per acquisition card installed
Dimensions	
Height/Height with handle	342 mm/392 mm (13.5"/15.4")
Width	436 mm (17.2")
Depth	186 mm (7.3")
Acoustic Noise	The total A-weighted SPL 55 dBA @ 0.6 m maximum
Temperature Sensors	For temperature monitoring and air flow control
Cooling Fans	2
Handle	One handle used for carrying and tilting the unit to higher tilt angles
Tilting Feet	Two retractable feet for small tilt angles
Grounding	4 mm Banana plug
Casing	Aluminum/Plastic cover

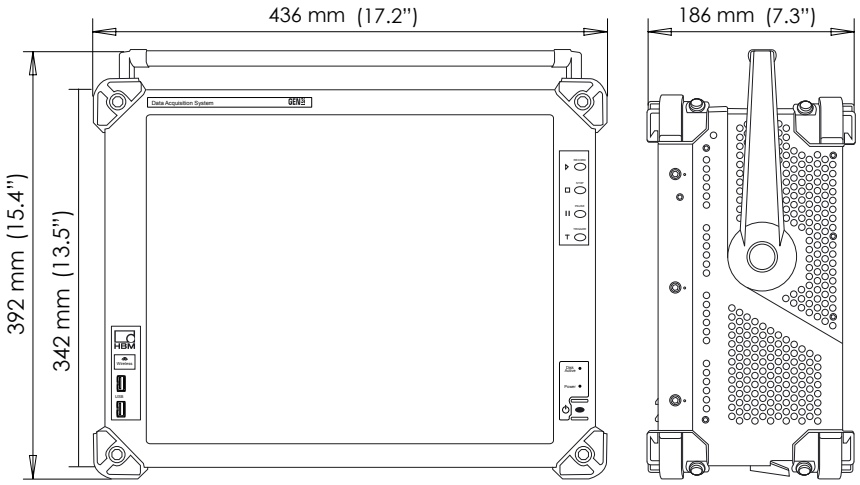


Figure A.12: GEN3i dimensions

Accessories	Soft carry case with strap for transportation included. The case has a hardened front and back for protection and two storage pouches for a mouse and keyboard

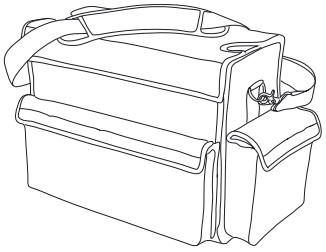


Figure A.13: Soft carry case

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC-60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC-60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC-60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

Supported Acquisition Cards

Model	Type	Isolation	Maximum sample rate/ (not multiplexed)	Resolution	Memory/card	Analog Channels	Digital events	Timer/Counter channels	Streaming support	Slot width
GN610B	Balanced Differential	yes	2 MS/s	18 bit	2 GB	6	16	2	fast	1
GN611B	Balanced Differential	yes	200 kS/s	18 bit	200 MB	6	16	2	fast	1
GN815	Unbalanced Differential/ IEPE	yes	2 MS/s	18 bit	2 GB	8	16	2	standard & fast	1
GN816	Unbalanced Differential/ IEPE	yes	200 kS/s	18 bit	200 MB	8	16	2	standard & fast	1
GN840B	Bridge/IEPE/Charge/ 4-20 mA/PT100/PT1000/ Thermocouples	yes	500 kS/s	24 bit	2 GB	8	16	2	fast	1
GN1202B	Multi Mode Optical Fiber	yes	100 MS/s	--(1)	8 GB	12	16	2	fast	1
GN1640B	Bridge/IEPE/Charge/ 4-20 mA/PT100/PT1000/ Thermocouples	yes	500 kS/s	24 bit	2 GB	16	16	2	fast	2
GN3210	Differential/IEPE/Charge	no	250 kS/s	24 bit	2 GB	32	16	2	standard	1
GN3211	Differential	no	20 kS/s	16 bit	200 MB	32	16	2	standard	1
GN8101B	Single-ended	no	250 MS/s	14 bit	8 GB	8	16	2	fast	1
GN8102B	Single-ended	no	100 MS/s	14 bit	8 GB	8	16	2	fast	1
GN8103B	Single-ended	no	25 MS/s	14 bit	8 GB	8	16	2	fast	1

(1) This card supports up to 12 optical fiber transmitter channels.

Optical Fiber Transmitter Channels

Transmitter

Every transmitter is a single channel unit. Every unit has an unbalanced differential input, amplifier, analog anti-alias filter and ADC with an optical data and control link to the receiver card. The receiver card has the recording logic, sample rate selection and memory.

Model	Receiver card	Power	Sample rate	Resolution	Isolation
GN110	GN1202B	Battery	100 MS/s	14 bit	User application defined
GN111	GN1202B	Battery	25 MS/s	15 bit	User application defined
GN112	GN1202B	120/240 V AC	100 MS/s	14 bit	1800 V RMS
GN113	GN1202B	120/240 V AC	25 MS/s	15 bit	1800 V RMS

Mainframe Feature Overview

	Tethered models				Integrated models	
	GEN2tB	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
Number of acquisition cards	2	3	7	17	3	7
Built-in TFT screen (resolution)	Not Supported				17" (1280x1024)	17" (1280x1024)
Built-in Windows® PC	Not Supported				Intel© i5, 8 GB RAM	Intel© i7, 16 GB RAM
Portable	ultra portable	portable	transporta-ble	Not Supported	portable	transporta-ble
Rack mount support (Option)	yes					
Built-in storage drive	option 500 GB	option 400 GB	Not Supported		480 GB	960 GB
Removable built-in storage drive	Not Supported		option 960 GB EXT4		Not Supported	option 960 GB NTFS
Built-in drive continuous streaming rate	200 MB/s		350 MB/s		200 MB/s	350 MB/s
1 GB Ethernet Continuous streaming rate	100 MB/s					
10 GB Ethernet Continuous streaming rate	NS(1)	400 MB/s				
IEEE1588:2008 PTP V2 support	yes					
Digital events	up to 32	up to 32	up to 96	up to 96	up to 32	up to 96
USB ports	1	0			8	
1 GB Ethernet (RJ45)	1				4	
Master/Slave synchronization connector	SFP option	Standard included				
DC power output (QuantumX compliant)	NS(1)	15 W	30 W	NS(1)	15 W	30 W
Mechanical	**GEN2tB**	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
Air filter	yes	no	yes		no	yes
Weight without acquisition cards (kg)	4.0	7	10.9	18.9	9	15.7
Dimensions (height / width / depth [mm])	96/375/320	342/436/186	293/448/343	450/446/517	342/436/186	350/446/386
19" Rack mount	option					
Shipping case	G098 option	G054 option	G086 option	no	G054 option	G077 option
Option overview	**GEN2tB**	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
CAN FD output	Option	NS(1)	Option	Not supported		
IRIG time synchronization (G001B)	option					
GPS time synchronization (G002B)	option					
Option carrier card support (G081)	option					
Master output card (G083)	option					
10 GB Ethernet optical (G064)	NS(1)	option				
10 GB Ethernet electrical (G084)	NS(1)	option				
EtherCAT®	NS(1)	option			Not Supported	
NAS (Network attached Storage)	**GEN2tB**	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
1 GB Ethernet Continuous streaming rate	50 MB/s	80 MB/s				
10 GB Ethernet Continuous streaming rate	NS(1)	150 MB/s				
Software	**GEN2tB**	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
Included Perception package	Standard				Advanced	Enterprise
Remote control	**GEN2tB**	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
GEN DAQ API (Perception not used)	yes				no	no
Perception RPC/COM API	yes					
Customer Special Perception extenstion	**GEN2tB**	**GEN3t**	**GEN7tA**	**GEN17tA**	**GEN3i**	**GEN7i**
Perception CSI	option					

(1) NS: Not supported

Perception Versions					
Features	**Free Viewer (no copy protection)**	**Viewer Enterprise**	**Standard (no copy protection)**	**Advanced**	**Enterprise**
True 64 bit support(1)	✓	✓	✓	✓	✓
Basic review, y/t and x/y displays	✓	✓	✓	✓	✓
Horizontal, vertical and slope cursors	✓	✓	✓	✓	✓
Trace and display markers	✓	✓	✓	✓	✓
Interactive waveform calculator	✓	✓	✓	✓	✓
Interactive user keys	✓	✓	✓	✓	✓
Quick report to Microsoft® Word and Excel	✓	✓	✓	✓	✓
Automation and log-file	✓	✓	✓	✓	✓
Export to ASCII, Excel, imPression, RTPro, TEAM data	✓	✓	✓	✓	✓
Analysis functions/Formula Database	✗	✓	✗	✓	✓
Advanced Report	✗	✓	✗	✓	✓
Advanced Export adds 15 additional formats MATLAB, DIAdem, Flexpro, Famos, UFF58 etc.	✗	✓	✗	✓	✓
Synchronized Video Playback	✗	✓	✗	✓	✓
Multiple Workbooks (Monitors)	✗	✓	✗	✓	✓
Information sheet to add recording meta data	✗	✓	✗	✓	✓
Single mainframe control	✗	✗	✓	✓	✓
Multiple mainframe control(2)	✗	✗	✗	✗	✓
Macro editor for user keys and automation	✗	✓	✗	✗	✓
Basic FFT	✗	✓	✗	✗	✓
Sensor Database	✗	✓	✗	✗	✓
User/Definer Mode	✗	✓	✗	✗	✓
Application packages					
Custom Software Interface	✗	Cost option	✗	Cost option	Cost option
STL Analysis (Short-Circuit Testing Liaison methods)	✗	Cost option	✗	Cost option	Cost option
HV-IA Lightning, Switching and Current impulse analysis (IEC60060-1 and IEC61083-2)	✗	Cost option	✗	Cost option	Cost option
eDrive electrical motor/inverter/generator and drive analysis	✗	Cost option	✗	✗	Cost option

(1) 32 bit versions available for legacy 32 bit Windows® PC support.

(2) The maximum number of mainframes Perception can control is calculated by using 25% of PC memory divided by 50 MB FIFO required per mainframe. Minimum suggested configuration is a PC with 64 bit Windows® and 8 GB of memory.

Perception Remote Control (Free of Charge)

Perception remote control is based on DCE/RPC network communication standards (Distributed Computing Environment/Remote Procedure Calls, free of charge). The source code supplied by HBM can be compiled on many different operating systems. For ease of use in the Microsoft®.NET environment a COM interface is created on top of the basic DCE/RPC interface. An extensive help file is available to explain interface calls offered in this API.

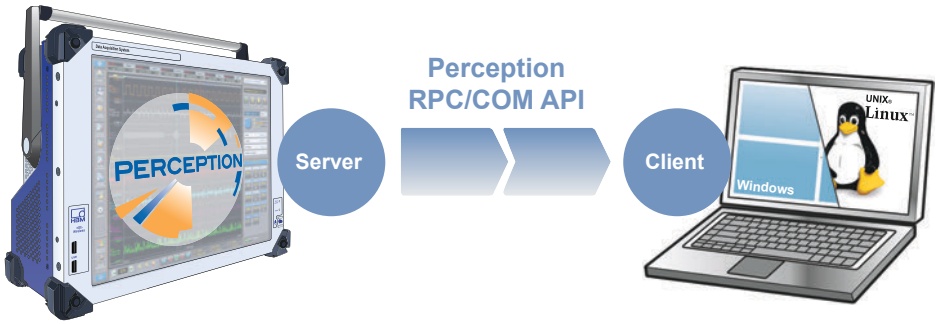


Figure A.14: Functional diagram DCE/RPC

Functions	Control Perception software from an external computer/application on Windows®, Linux, Unix or Mac OS X
COM interface	All RPC commands have a COM wrapper for easier Windows® software integration
Available basic commands	Load and save Perception setup files, Setup Recording, set and review Hardware Settings, Start/Stop/Pause/Trigger, monitor Live data
Examples (free of charge)	C++ and C# getting started example programs supplied for Windows®, source code included. Unsupported Linux getting started example by request only.
LabVIEW™ integration (free of charge)	LabVIEW™ RPC/COM getting started examples available on www.hbm.com
DIAdem™ integration (free of charge)	DIAdem™ RPC/COM getting started examples available on www.hbm.com

PNRF Recording File Reader (Free of Charge)

HBM maintained file reader to read the proprietary PNRF format. (Perception Native Recording File) Integrated by several industry standard analysis package suppliers. Available for all 3rd party software developers.

Figure A.15: Functional diagram PNRF Reader

Functions	Read PNRF, NRF and LRF recording files directly in your own application
COM interface	The PNRF reader comes as a COM interface and can be used from any application or programming language which supports COM automation
PNRF Software Development Kit (SDK)	Installs PNRF dll's and supplies Visual Basic, C# and C++ getting started examples
GlyphWorks® integration	PNRF SDK integrated and available directly from HBM nCode
MATLAB® integration	PNRF SDK installs both MATLAB® PNRF reader and getting started examples
LabVIEW™ integration	PNRF SDK integrated and available directly from National Instruments
DIAdem™ integration	PNRF SDK integrated and available directly from National Instruments
FlexPRO integration	PNRF SDK integrated and available directly from Weisang GmbH
jBEAM™ integration	PNRF SDK integrated and available directly from AMS
DynaWorks® integration	PNRF SDK integrated and available directly from Intespace

Perception CSI (Customer Software Interface)

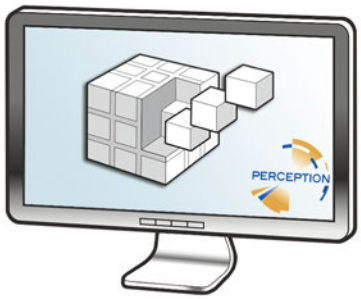


Figure A.16: Perception CSI building blocks

Functions	Create software extensions inside the Perception software by adding CSI user sheets, custom automation and extended analysis functions. Basic Windows C# sheet template included. Available for all languages that support Microsoft®.NET 4.
Available basic controls & commands	Access to every Perception part: Start/Stop/Pause and Trigger, Start Manager, Acquisition System, Hardware Settings, Displays, Meters, User Tables, Formulas, Calculations, Data Manager, Data Sources, User variables, Notifications, Logging, Conversion Functions, Automation Actions, Sheet Manager and more, to create a dedicated application GUI that hides the entire Perception standard GUI.
Examples (free of charge)	C# getting started example programs supplied, source code included

Perception API and CSI Training/Support Program

Figure A.17: Perception targeted training

HBM offers paid professional training and support programs on all API interfaces (PNRF reader, RPC and CSI). Training programs are based on C#, are on-site or are at a central HBM location. On-site training can be specific for each customer. Support can be the development of a fully customized software application or answering questions from software engineers.	
S-TRAIN1-GEN_PERC	First day on-site basic training on GEN DAQ/PERCEPTION. Example content: Basic usage, hardware setup, acquisition. Training can be customized for specific training needs.
S-TRAIN2-GEN_PERC	Second day on-site enhanced training on GEN DAQ/PERCEPTION. Training can be customized for specific training needs.
S-TRAIN1-eDRIVE	First day on-site basic training on eDrive application specifics. Example content: Basic usage, hardware setup, acquisition. Training can be customized for specific training needs.
S-TRAIN2-eDRIVE	Second day on-site enhanced training on eDrive application specifics. Training can be customized for specific training needs.
1-PERC-CSI-TRAIN	Two day on-site Perception CSI training for software programmers During the training software programmers learn how to get started using the CSI template, make changes to the Perception user interface, to add new mathematical routines to the Formula Database or to add User Keys etc. The exact training details can be fully customized to the programmers needs including reviews and examples how to create the exact CSI changes of choice. Basic Microsoft® Visual Studio software C# programming skills are required before joining this training. More dedicated detailed training is available on request.
1-PERC-CSI-PROJ	One day eMail/Phone support for Perception CSI or RPC programmers. Get support from a HBM senior software engineer. Support can range anywhere from answering "how-to" question, assisting in analysing any kind of (performance) issue to generating basic getting started example code fragments.

A.2 B04374_02_E00_00 (GEN series GN610B)

Capabilities Overview			
Model	GN610B		
Maximum sample rate per channel	2 MS/s		
Memory per card	2 GB		
Analog channels	6		
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter		
ADC resolution	18 bit		
Isolation	Channel to channel and channel to chassis		
Input type	Analog, isolated balanced differential		
Passive voltage/current probes	Special designed matching probes only (e.g. Elas HDP)		
Sensors	Not supported		
TEDS	Not supported		
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results		
Real-time formula database calculators (option)	Extensive set of user programmable math routines with triggering on calculated results		
Real-time calculated results output	Ethernet software API	EtherCAT®	CAN/CAN FD
Result blocks per second	2000	1000	500
Latency	Ethernet dependent	1 ms	CAN bus speed
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels		
Standard data streaming (CPCI up to 200 MB/s)	Not supported		
Fast data streaming (PCIe up to 1 GB/s)	Supported		
Slot width	1		

Block Diagram

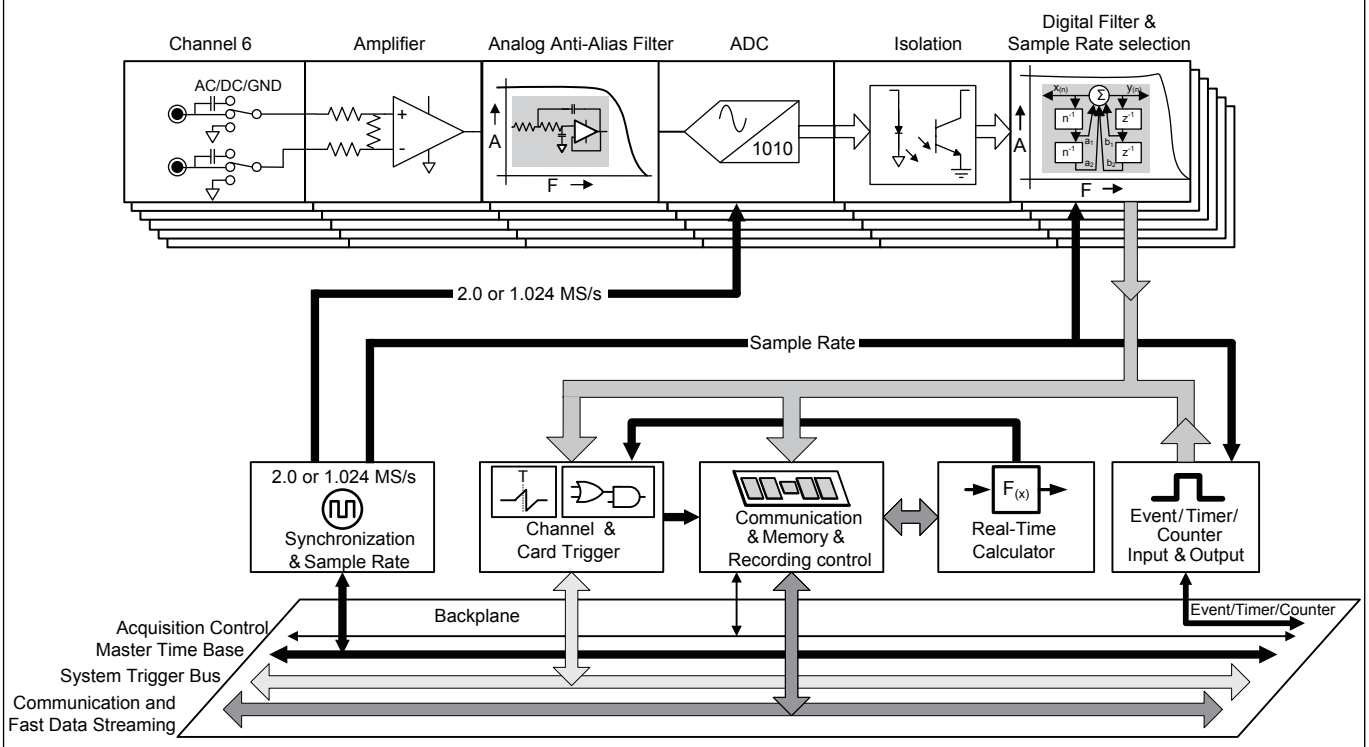


Figure A.18: Block Diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input Section		
Channels	6	
Connectors	Fully isolated 4 mm banana plugs (plastic), 2 per channel (red and black)	
Input type	Analog, isolated balanced differential	
Input impedance	2 * 1 MΩ ± 1% // 33 pF ± 10% ranges larger than ± 5 V. All other ranges 57 pF ± 10%	
Input coupling		
Coupling modes	AC, DC, GND	
AC coupling frequency	48 Hz ± 5 Hz (-3 dB)	

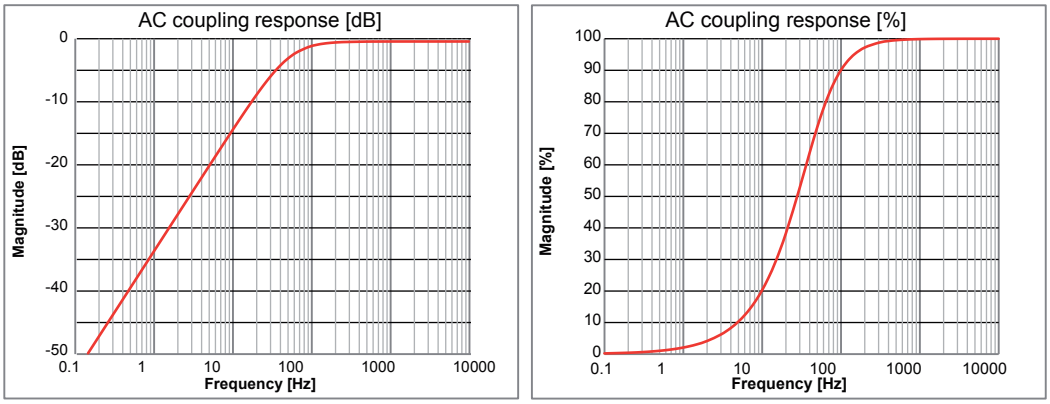
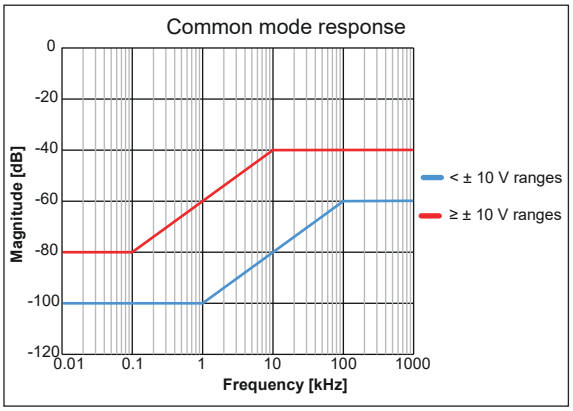


Figure A.19: Representative AC coupling response

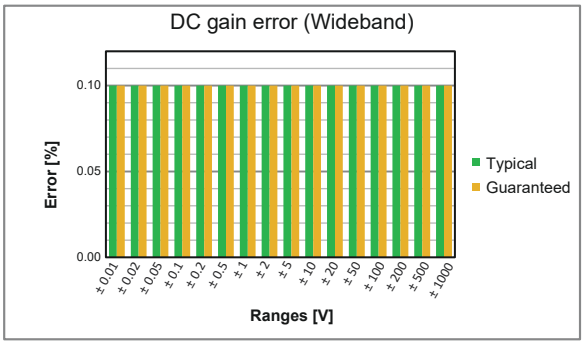
Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V, ± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1000 V	
Offset	± 50% in 1000 steps (0.1%); ± 1000 V range has fixed 0% offset	
Common mode (referred to system ground)		
Ranges	Less than ± 10 V	Larger than or equal to ± 10 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	7 V RMS	1000 V RMS

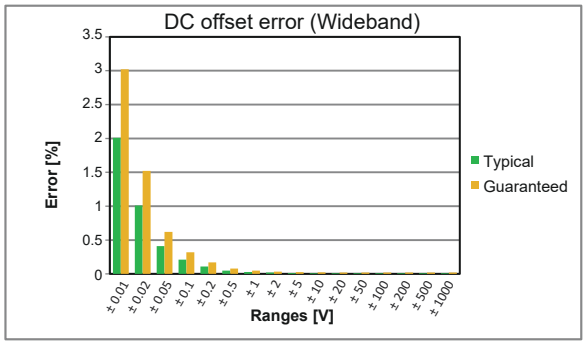


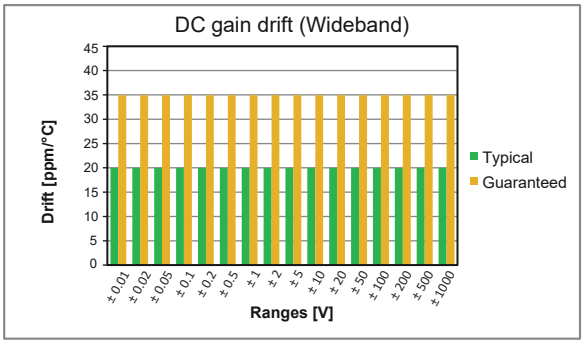
Input overload protection	
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage remains less than 200% of the selected input range or 1250 V, whichever value is the smallest.
Maximum nondestructive voltage	± 2000 V DC
Maximum overload without auto range	200% of selected range
Automatic auto range	When overload causes the amplifier to overheat, the amplifier increases its range in steps of a factor of 10 until the overload ceases. When the overload exceeds 1000 V, the input signal is disconnected and the amplifier input is grounded. When the temperature returns to normal, the range that was originally selected is restored. The automatic auto range cannot be turned off.
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

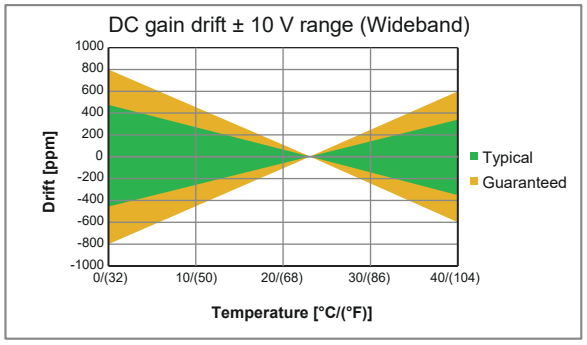
Voltage Specifications (Wideband)

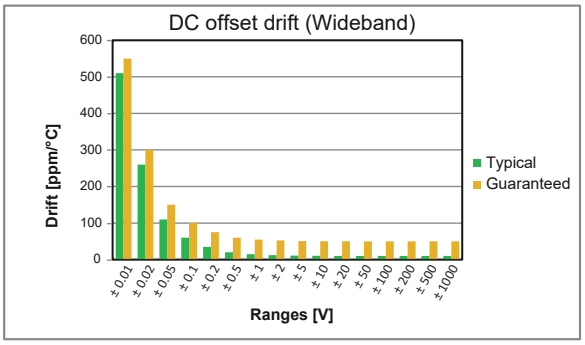
	Typical	Guaranteed
DC gain error	0.1% of reading	0.1% of reading
DC offset error	0.01% of Full Scale ± 400 µV	0.02% of Full Scale ± 600 µV
DC gain error drift	±20 ppm/°C (±12 ppm/°F)	±35 ppm/°C (±20 ppm/°F)
DC offset error drift	±(10 ppm + 10 µV)/°C (±(6 ppm + 6 µV)/°F)	±(50 ppm + 10 µV)/°C (±(28 ppm + 6 µV)/°F)
RMS Noise (50 Ω terminated)	0.02% of Full Scale ± 50 µV	0.03% of Full Scale ± 70 µV

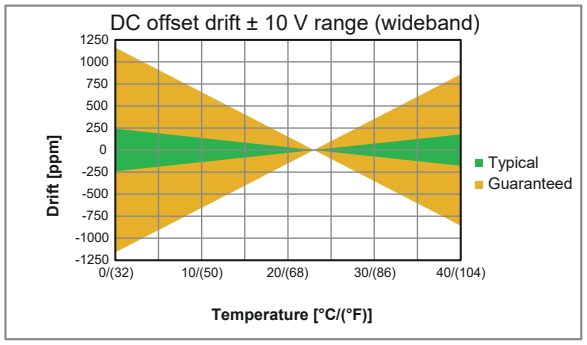












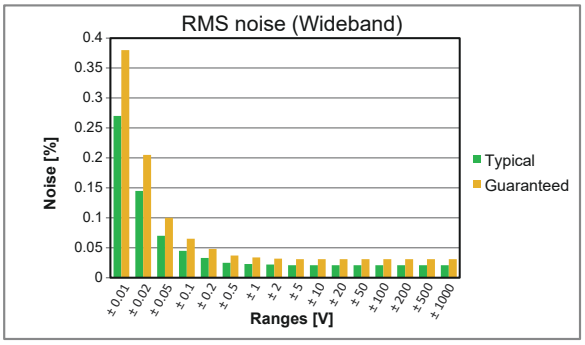
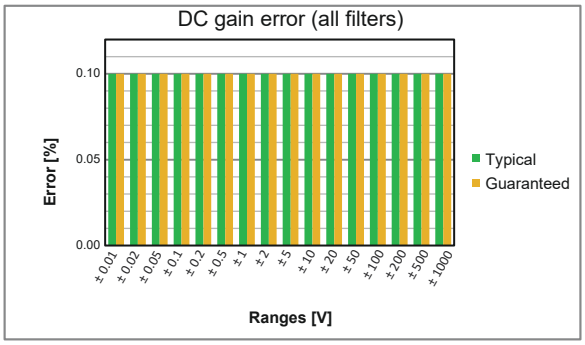
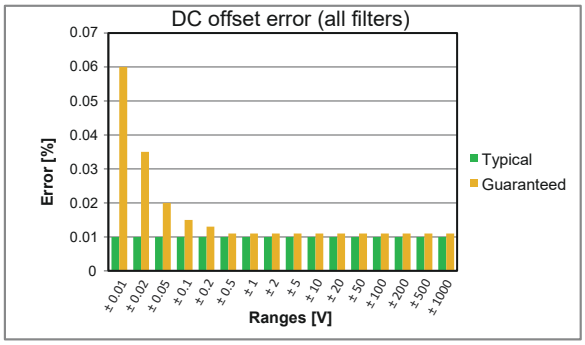


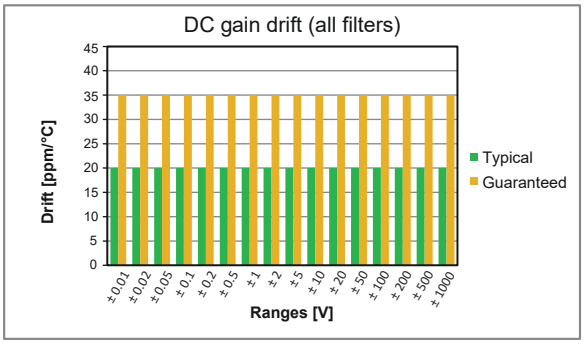
Figure A.20: Wideband voltage specification

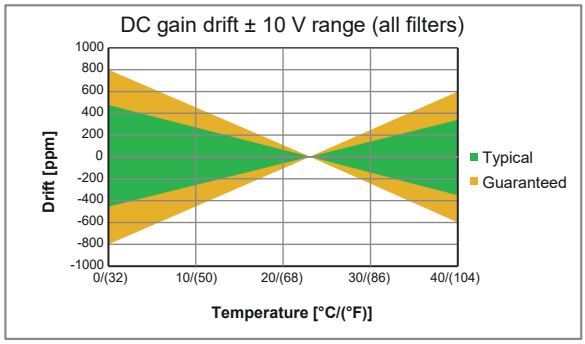
Voltage Specifications (All Filters Used)

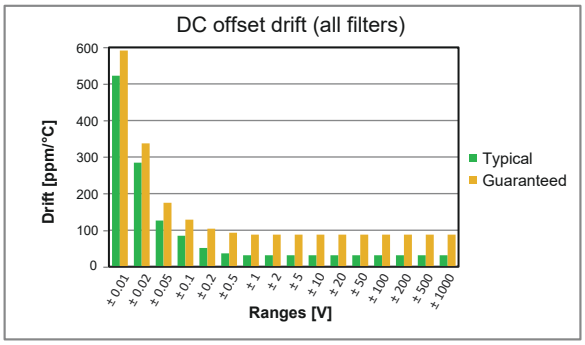
	Typical	Guaranteed
DC gain error	0.1% of reading	0.1% of reading
DC offset error	0.01% of Full Scale	0.01% of Full Scale ± 10 µV
DC gain error drift	±20 ppm/°C (±12 ppm/°F)	±35 ppm/°C (±20 ppm/°F)
DC offset error drift	±(30 ppm + 10 µV)/°C (±(17 ppm + 6 µV)/°F)	±(80 ppm + 10 µV)/°C (±(45 ppm + 6 µV)/°F)
RMS Noise (50 Ω terminated)	0.01% of Full Scale ± 20 µV	0.02% of Full Scale ± 20 µV

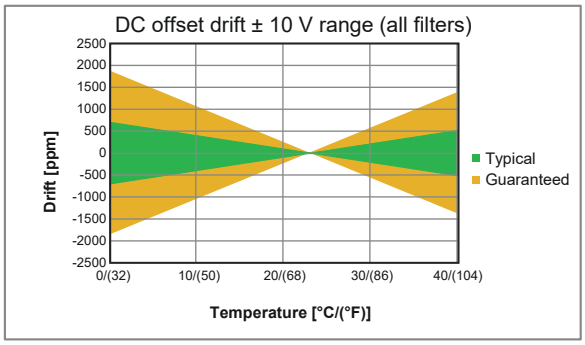












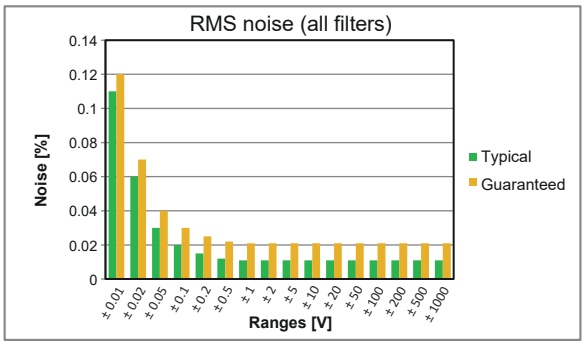


Figure A.21: All filters used voltage specification

Basic Power Accuracy

The GN610B/GN611B is calibrated and checked at 53 Hz voltage and current inputs using burden resistors. During calibration burden resistors are attached to three voltage channels to enable current measurements.
Specifications are given for the 2.5 Ω burden. Using the 1.0 Ω or 10.0 Ω burden will give different current ranges but identical results.

2.5 Ω	**Burden spans**	**1.264 A DC**	**800 mA DC**	**400 mA DC**	**160 mA DC**	**80 mA DC**	**40 mA DC**
0 - 100 Hz Sine wave CF: 1.41 Cos Phi : 1	**Burden ranges**	**440 mA RMS**	**280 mA RMS**	**140 mA RMS**	**56 mA RMS**	**28 mA RMS**	**14 mA RMS**
	IT200 ranges	N/A	200 A RMS(1)	140 A RMS	56 A RMS	28 A RMS	14 A RMS
	IT400 ranges	N/A	400 A RMS(1)	280 A RMS	112 A RMS	56 A RMS	28 A RMS
	IT700 ranges	700 A RMS(1)	490 A RMS	245 A RMS	98 A RMS	49 A RMS	24.5 A RMS
Voltage spans	**Voltage ranges**	Typical	Typical	Typical	Typical	Typical	Typical
40 V DC	**14.1 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
100 V DC	**35.3 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
200 V DC	**70.7 V RMS**	0.02% reading +0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
400 V DC	**141 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
1 kV DC	**353 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
2 kV DC	**707 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range

(1) With the right setup the LEM sensor can be used for this range, however this input range is not specified in the LEM current sensor data sheet.

Isolation

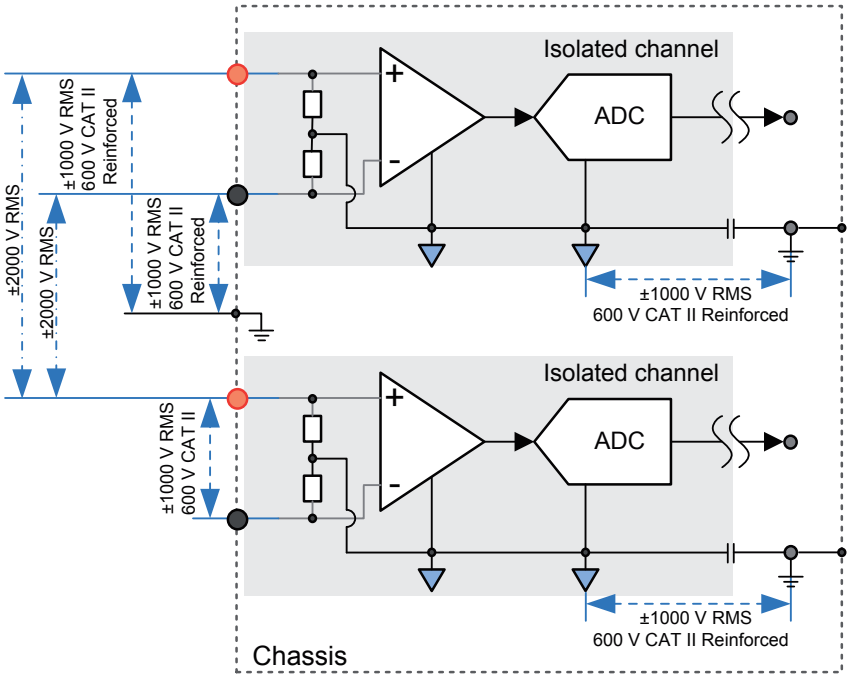


Figure A.22: Isolation 1kV card overview

		CAT II	CAT III
Channel to chassis (earth)	1000 V RMS	600 V RMS (1)	300 V RMS(1)
Channel to channel	2000 V RMS	(2)	(2)

(1) IEC61010-1 category voltage ratings are RMS voltages.

(2) Channel to channel CAT II and CAT III ratings are not a valid method to specify.

Isolation and Input Type Testing

IEC61010-1:2010 and IEC61010-2-030:2010 isolation tests	
Channel to channel	3510 V RMS and 4935 V DC for 5 s 3260 V RMS and 4596 V DC for 1 minute
Channel to chassis	3510 V RMS and 4935 V DC for 5 s 3260 V RMS and 4596 V DC for 1 minute
Channel to channel impulse	6400 V peak using a 2 Ω series resistor Rise time 1.2 µs, 50% amplitude reduction in 50 µs
Channel to chassis impulse	6400 V peak using a 2 Ω series resistor Rise time 1.2 µs, 50% amplitude reduction in 50 µs

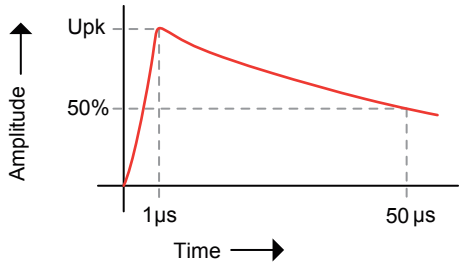


Figure A.23: Example of 1.2/50 µs impulse

Input impulse test	
Channel positive to negative input	4000 V peak using a 12 Ω series resistor, rise time 1.2 µs, 50% amplitude reduction in 50 µs

Analog to Digital Conversion	
Sample rate; per channel	0.1 S/s to 2 MS/s
ADC resolution; one ADC per channel	18 bit
ADC type	Successive Approximation Register (SAR); Analog Devices AD7986BCPZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm; aging after 10 years ± 10 ppm
Binary sample rate	Supported; calculating FFTs results in rounded BIN values
Maximum binary sample rate	1.024 MS/s
External time base frequency	0 S/s to 1 MS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

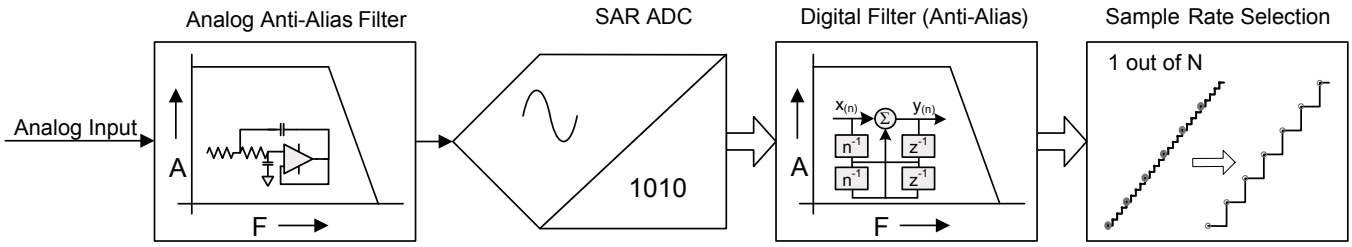


Figure A.24: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Wideband should not be used if working in a frequency domain with recorded data.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	Between 900 kHz and 1500 kHz (-3 dB)
0.1 dB passband flatness	DC to 160 kHz(1)

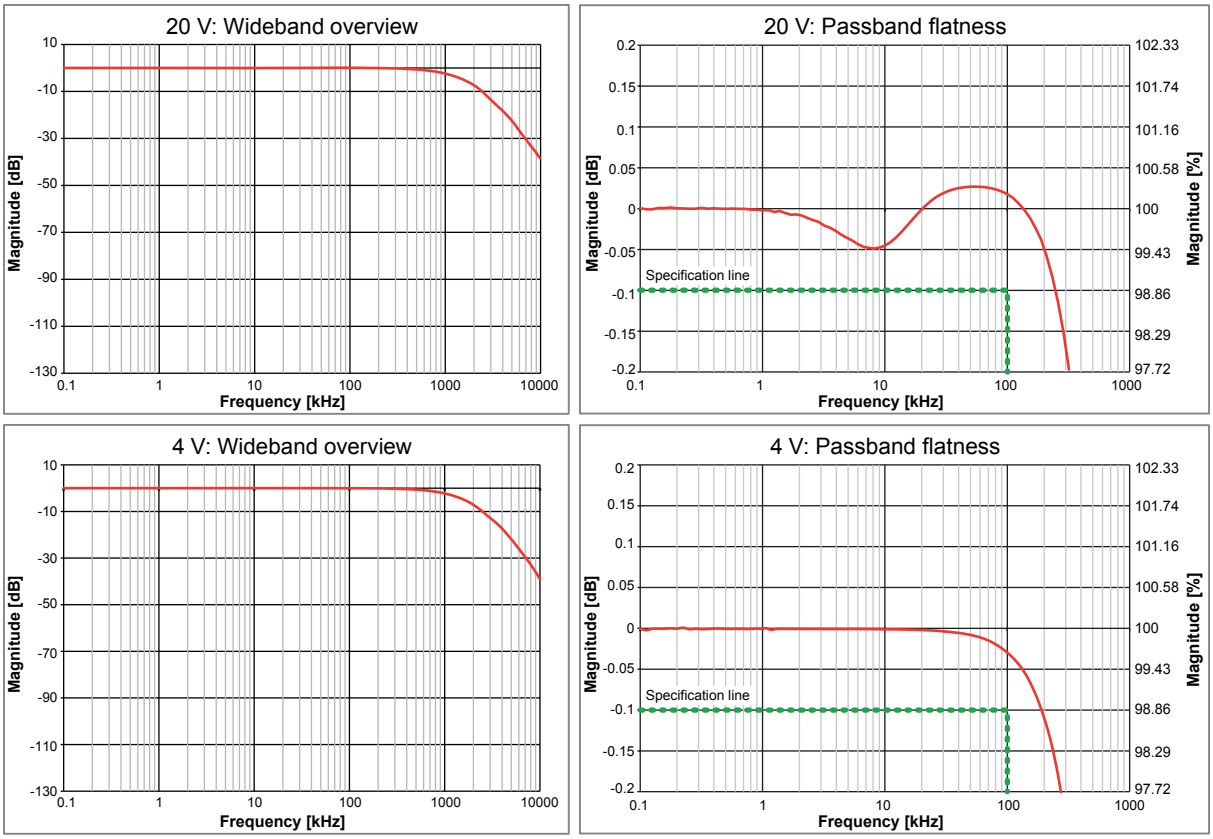
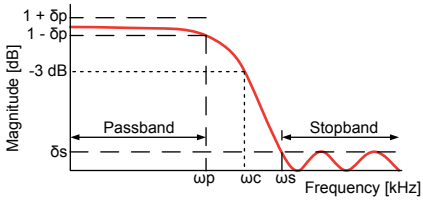


Figure A.25: Representative Wideband examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.26: Representative Bessel IIR examples

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.	
Analog anti-alias filter bandwidth	400 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	8-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	User selectable from 0.4 Hz to 200 kHz
Bessel IIR 0.1 dB passband (ωp)(1)	DC to 0.14 * ωc
Bessel IIR filter stopband attenuation (δs)	60 dB With the Bessel IIR filter bandwidth selection of ωc = 200 kHz, a peak of -55 dB occurs between 1.6 MHz and 1.8 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
Bessel IIR filter roll-off	48 dB/octave

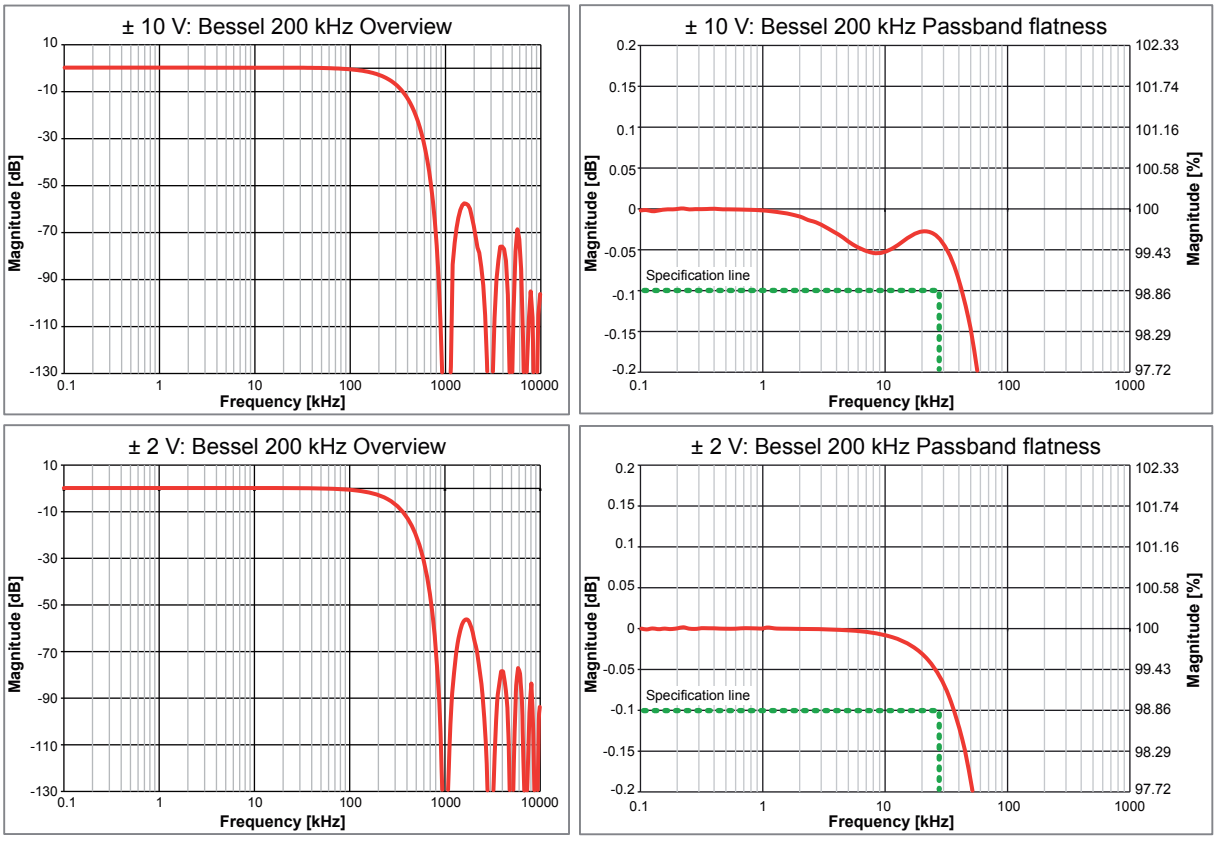
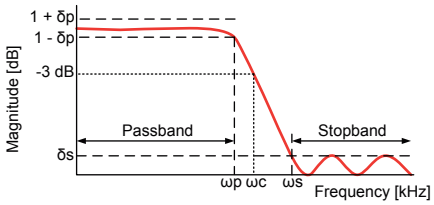


Figure A.27: Representative Bessel IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.28: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter.	
Analog anti-alias filter bandwidth	465 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Butterworth IIR filter characteristic	8-pole Butterworth style IIR
Butterworth IIR filter user selection	Auto tracking for sample rate divided by: 4(1), 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed
Butterworth IIR filter bandwidth (ωc)	User selectable from 1 Hz to 250 kHz
Butterworth IIR 0.1 dB passband (ωp)(2)	DC to 0.7 * ωc (for ωc > 100 kHz, DC to 0.6 * ωc, due to analog anti-alias filter bandwidth)
Butterworth IIR filter stopband attenuation (δs)	75 dB
Butterworth IIR filter roll-off	48 dB/octave

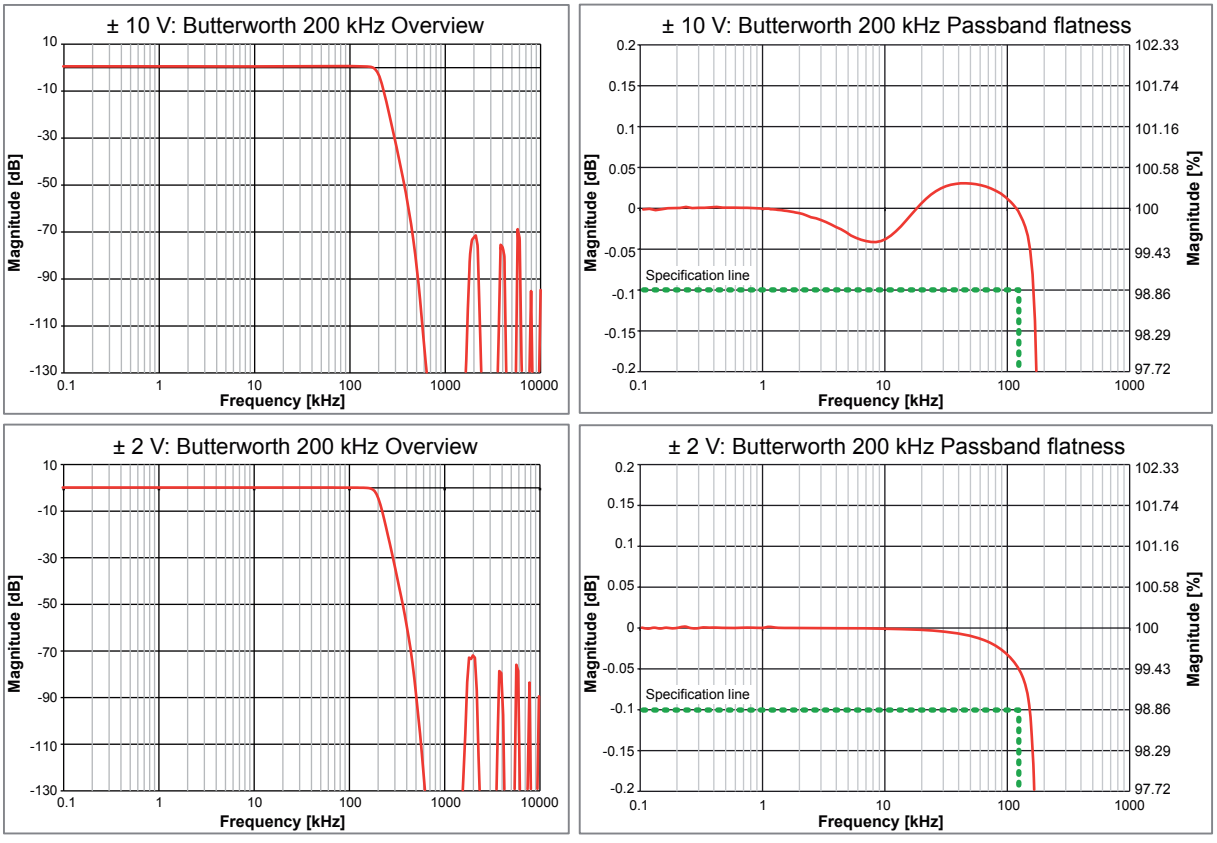
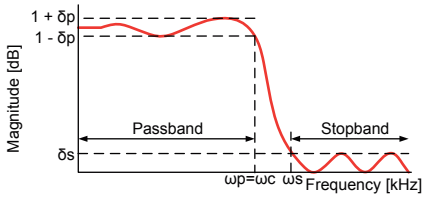


Figure A.29: Representative Butterworth IIR examples

(1) Division by 4 not possible for the 2 MS/s sample rate

(2) Measured using a Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.30: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter.

Analog anti-alias filter bandwidth	465 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Elliptic IIR filter characteristic	7-pole Elliptic style IIR
Elliptic IIR filter user selection	Auto tracking for sample rate divided by: 4(1), 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed
Elliptic IIR filter bandwidth (ωc)	1 Hz to 250 kHz
Elliptic IIR 0.1 dB passband (ωp)(2)	DC to ωc (for ωc > 100 kHz, DC to 0.7 * ωc due to analog anti-alias filter bandwidth)
Elliptic IIR filter stopband attenuation (δs)	75 dB
Elliptic IIR filter roll-off	72 dB/octave

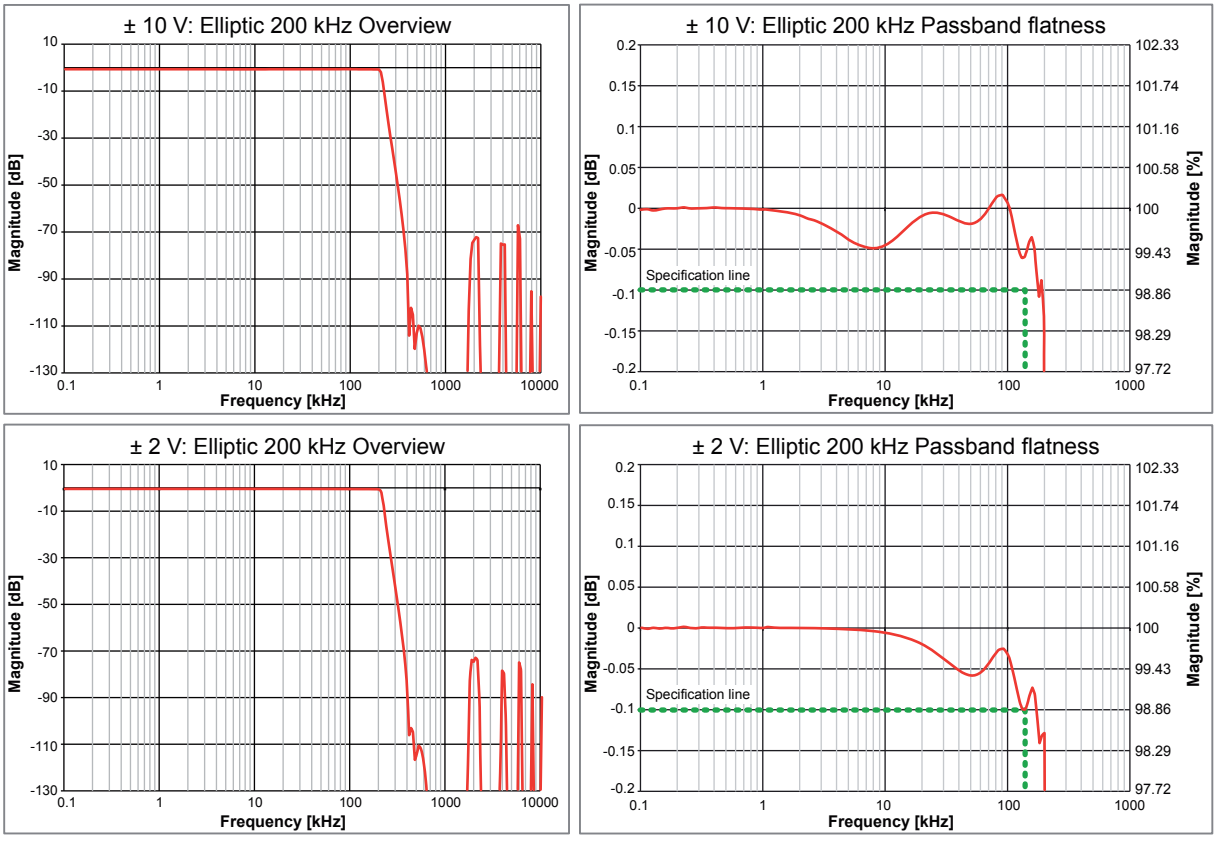


Figure A.31: Representative Elliptic IIR examples

(1) Division by 4 not possible for the 2 MS/s sample rate

(2) Measured using a Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match

Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths results in phase mismatches between channels. All specifications are typical static values and measured using a 100 kHz sine wave and 2 MS/s sample rate.

	Ranges < ±10V	Ranges ≥ ±10V	Combined ranges
Wideband			
Channels on card	0.1° (3 ns)	0.1° (3 ns)	0.1° (3 ns)
GN610B Channels within mainframe	0.1° (3 ns)	0.1° (3 ns)	0.1° (3 ns)
Bessel IIR, Filter frequency 200 kHz			
Channels on card	0.1° (3 ns)	0.1° (3 ns)	0.1° (3 ns)
GN610B Channels within mainframe	0.1° (3 ns)	0.1° (3 ns)	0.1° (3 ns)
Butterworth IIR, Filter frequency 200 kHz			
Channels on card	0.2° (6 ns)	0.2° (6 ns)	0.2° (6 ns)
GN610B Channels within mainframe	0.2° (6 ns)	0.2° (6 ns)	0.2° (6 ns)
Elliptic IIR, Filter frequency 200 kHz			
Channels on card	0.2° (6 ns)	0.2° (6 ns)	0.2° (6 ns)
GN610B Channels within mainframe	0.2° (6 ns)	0.2° (6 ns)	0.2° (6 ns)
GN610B channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)		

Channel to Channel Crosstalk

Channel to channel crosstalk is measured with a 50 Ω termination resistor on the input and uses sine wave signals on the channel above and below the channel being tested. To test Channel 2, Channel 2 is terminated with 50 Ω and Channels 1 and 3 are connected to the sine wave generator.

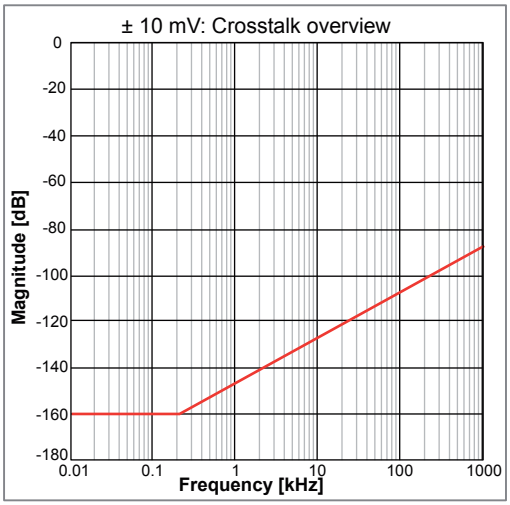


Figure A.32: Representative Channel to Channel crosstalk

On-board Memory

Per card	2 GB (1 GS @ 16 bits, 500 MS @ 18 bits storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	User selectable 16 or 18 bits 16 bits, 2 bytes/sample 18 bits, 4 bytes/sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

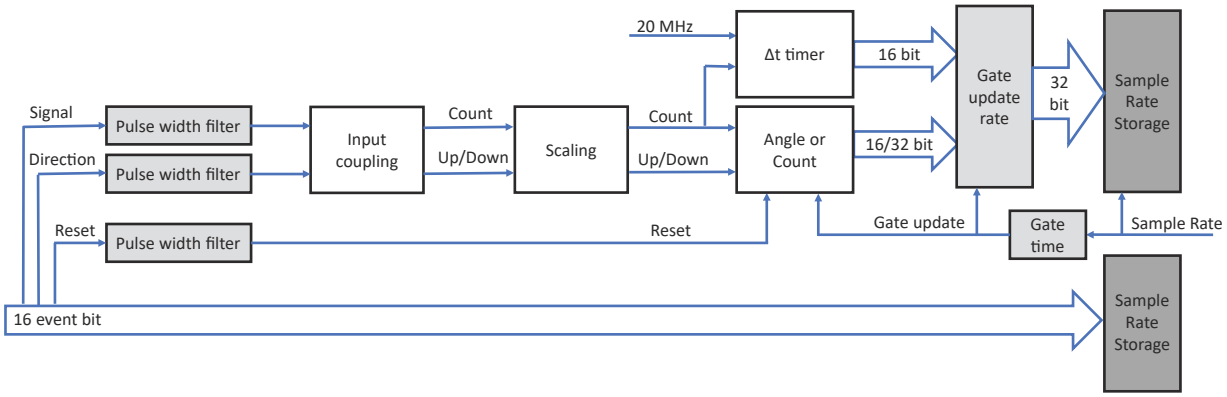


Figure A.33: Timer/Counter block diagram

Digital input events	16 per card			
Levels	TTL input level, user programmable invert level			
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs			
Overvoltage protection	± 30 V DC continuously			
Minimum pulse width	100 ns			
Maximum frequency	5 MHz			
Digital output events	2 per card			
Levels	TTL output levels, short circuit protected			
Output event 1	User selectable: Trigger, Alarm, set High or Low			
Output event 2	User selectable: Recording active, set High or Low			
Digital output event user selections				
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay			
Alarm	High when alarm condition of card is activated, low when not activated 200 µs ± 1 µs ± 1 sample period alarm event delay			
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns			
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation			
Timer/Counter	2 per card			
Levels	TTL input levels			
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs			
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)			
Measurement modes	Count (C) Angle (0 to 360 degrees) Frequency (Δcount / Δt) RPM (Δcount / Δt / 60 s)			
Δt timer measurement accuracy	50 ns (20 MHz)			
Gate time	1 to n samples (User selectable maximum Δt)			
Gate time and reading update rate	Gate time sets the maximum update rate of the measurement values			
Gate time and minimum frequency	Minimum measured frequency or RPM = 1 / gate time			
Gate time and frequency accuracy	Accuracy = 50 ns / gate time			
Gate time impact	**Gate time**	**1 us**	**10 us**	**100 us**
	Δt Error	5%	0.5%	0.05%
	Update rate	1 MS/s	100 kS/s	10 kS/s
RT-FDB options	RT-FDB timer based average enables the same gate time effect. RT-FDB cycle detect average enables a dynamic gate time effect.			

Input Coupling Uni- and Bi-directional Signal

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

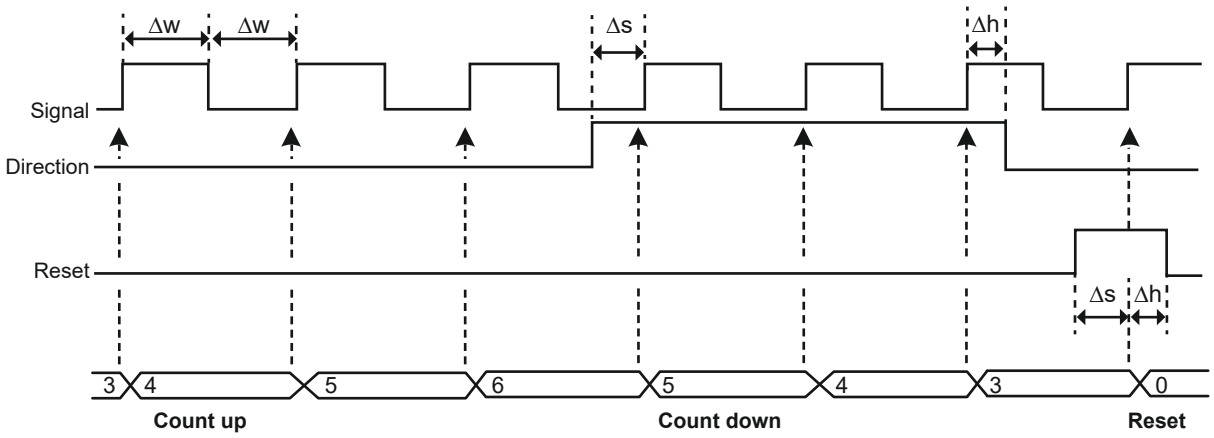


Figure A.34: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	4 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

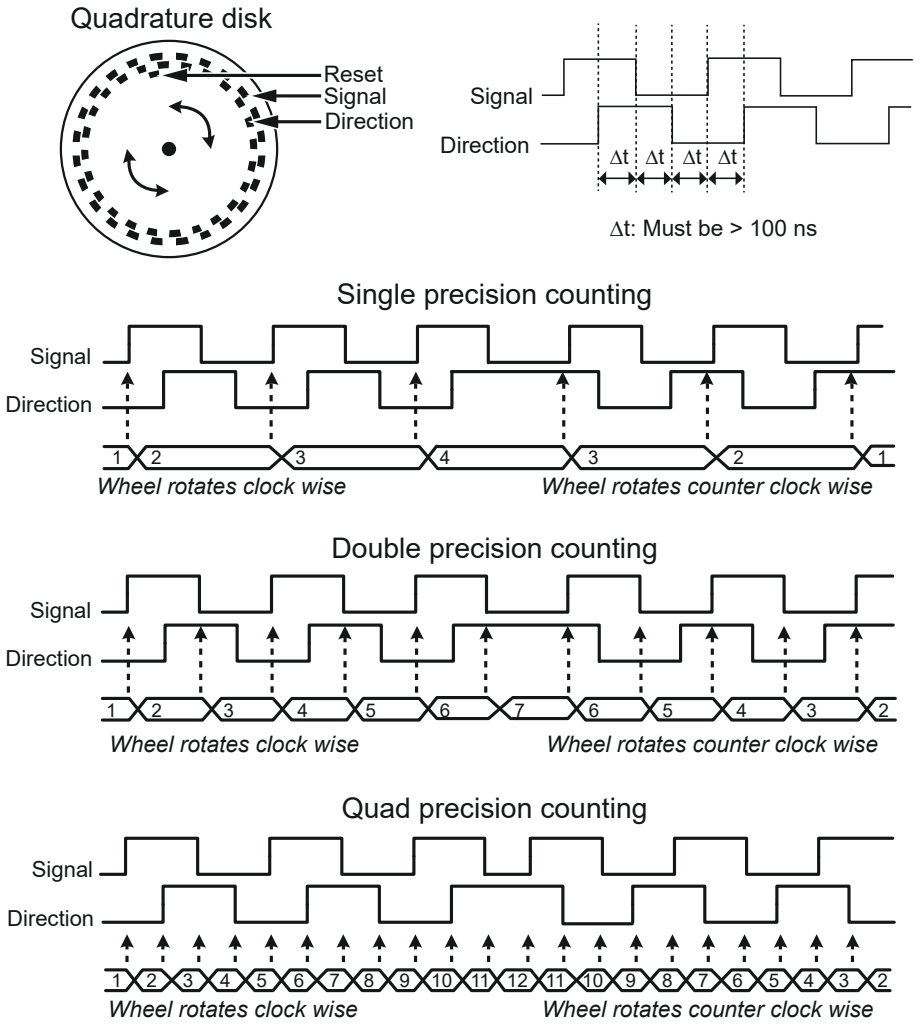


Figure A.35: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Count/Position	
Count/position mode is typically used for tracking movement of device under test. To reduce the sensitivity for count/position errors due to clock glitches use the minimum pulse width filter or enable the ABZ in stead of uni-/bi-polar input coupling .	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31}$ - 1; bi-directional count

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period (identical for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (10 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (9.76 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516 (504) µs for decimal (binary) time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators

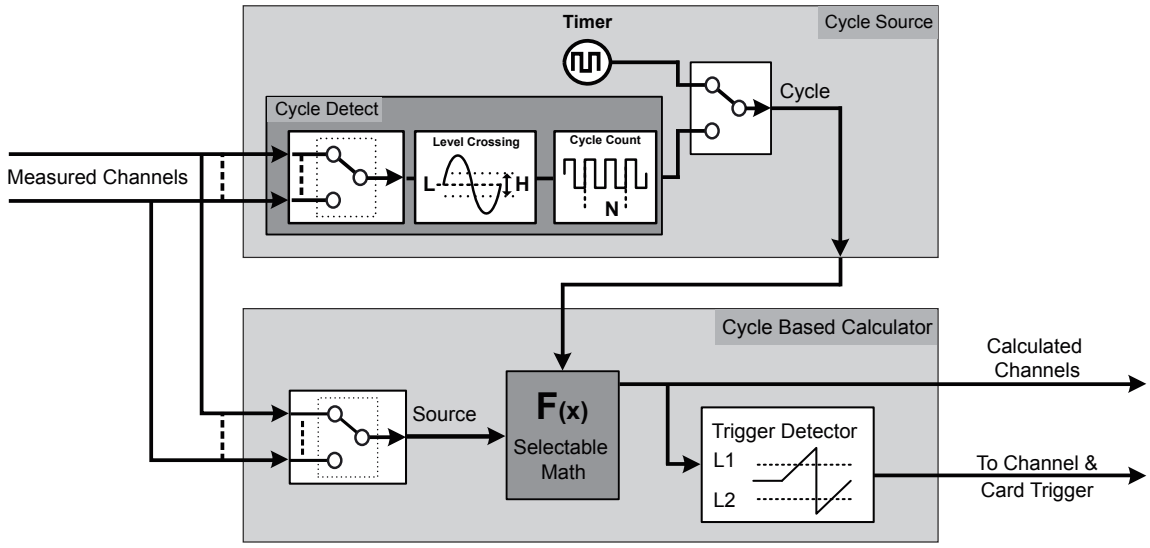


Figure A.36: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased
Cycle based calculator	
Number of calculators	32; at sample rates 200 kS/s or lower. At higher sample rates, the number of calculators is reduced to match the available DSP power
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and Crest Factor
Timer/Counter channel calculations	Frequency (to enable triggering), RPM of Angle
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)

The real-time formula database (RT-FDB) option offers an extensive set of math routines to enable almost any real-time mathematical challenge. The database structure enables the user to define a list of mathematical equations similar to the Perception review formula database.
The maximum supported sample rate is 2 MS/s.
The real-time formula database feature set is extended with higher Perception Versions. Different versions of Perception therefore can enable more or less features as described in this table.

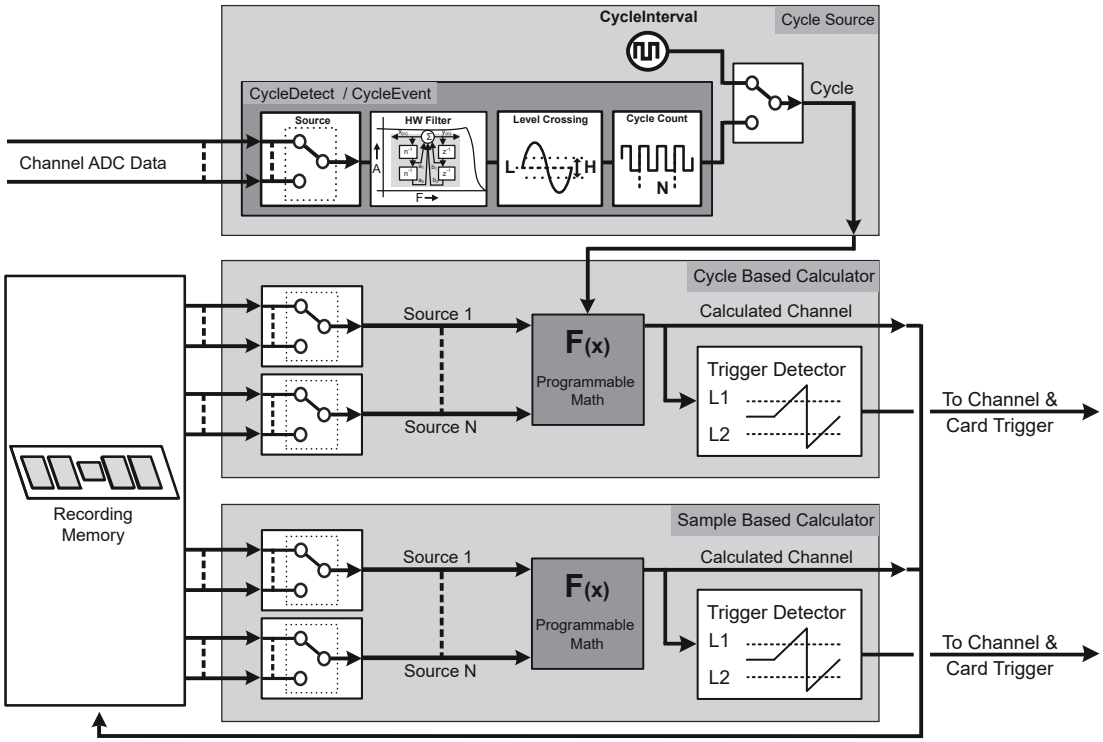


Figure A.37: Real-time formula database (RT-FDB) calculators

The real-time formula database supports the following list of calculations (Details of each calculation are described in the manual).

Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Basic calculations				
`+ (add)`	✓	✓	✓	✓(1)
`- (subtract)`	✓	✓	✓	✓(1)
`* (multiply)`	✓	✓	✓	✓(1)
`/ (divide)`	✓	✓	✓	✓(1)
Enhanced calculations				
`Abs`	✓	✓	✓	✓(1)
`Atan`	✓	✓	✓	✓(1)
`Atan2`	✓	✓	✓	✓(1)
`Cosine`	✓	✓	✓	✓(1)
`DegreesToRadians`	✓	✓	✓	✓(1)
`Min`	✓	✓	✓	✓(1)
`Max`	✓	✓	✓	✓(1)
`Modulo`	✓	✓	✓	✓(1)
`RadiansToDegrees`	✓	✓	✓	✓(1)
`Sine`	✓	✓	✓	✓(1)
`Sqrt`	✓	✓	✓	✓(1)
`Tan`	✓	✓	✓	✓(1)

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Boolean calculations				
`Equal`	✓	✓	✓	✓
`GreaterEqualThan`	✓	✓	✓	✓
`GreaterThan`	✓	✓	✓	✓
`LessEqualThan`	✓	✓	✓	✓
`LessThan`	✓	✓	✓	✓
`NotEqual`	✓	✓	✓	✓
`InsideBand`	✓	✓	✓	
`OutsideBand`	✓	✓	✓	
`And`	✓	✓	✓	✓
`Or`	✓	✓	✓	✓
`Xor`	✓	✓	✓	✓
`Not`	✓	✓	✓	✓
Cycle based calculations				
`CycleArea`		✓	✓	✓
`CycleBusDelay`		✓	✓	✓
`CycleCount`		✓	✓	✓
`CycleCrestFactor`		✓	✓	✓
`CycleEnergy`		✓	✓	✓
`CycleFundamentalPhase`		✓	✓	✓(2)
`CycleFundamentalRMS`		✓	✓	✓
`CycleFrequency`		✓	✓	✓
`CycleMax`		✓	✓	✓
`CycleMean`		✓	✓	✓
`CycleMin`		✓	✓	✓
`CyclePeak2Peak`		✓	✓	✓
`CyclePhase`		✓	✓	✓
`CycleRMS`		✓	✓	✓
`CycleRPM`		✓	✓	✓
`CycleSampleCount`		✓	✓	✓
`CycleTHD`(2)		✓	✓	✓(2)
Cycle source				
`CycleDetect`(4)		✓	✓	
`CycleEvent`		✓	✓	
`CycleInterval`		✓	✓	

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Hardware based signal filtering				
`HWFilter`(4)	✓		✓	
Software based signal filtering				
`FilterBesselBP`	✓		✓	
`FilterBesselHP`	✓		✓	
`FilterBesselLP`	✓		✓	
`FilterButterworthBP`	✓		✓	
`FilterButterworthHP`	✓		✓	
`FilterButterworthLP`	✓		✓	
`FilterChebyshevBP`	✓		✓	
`FilterChebyshevHP`	✓		✓	
`FilterChebyshevLP`	✓		✓	
Special category calculation				
`HarmonicsIEC61000`	✓		✓	
`Integrate`	✓		✓	
Signal transformation				
`DQZeroTransformation (Park)`(3)	✓		✓	✓(1)
`SpaceVectorTransformation`(3)	✓		✓	
`SpaceVectorInverse Transformation`(3)	✓		✓	
Signal generation				
`SineWave`	✓		✓	
`Ramp`	✓		✓	
Trigger functions				
`TriggerOnBooleanChange`			Trigger mark	
`TriggerOnLevel`			Trigger mark	

(1) Only cycle based results can be used for real-time output. Use the CycleMean calculation on recorded channel data or sample based results to enable the real-time output of this data.

(2) The time required to calculate the output depends on maximum cycle length and sample rate. Depending on the selected settings the output latency will increase. HBM refers to these calculations as not deterministic. All real-time output published values (deterministic and/or not deterministic) will always have the same latency.

(3) This formula is only available if the eDrive license is added to Perception.

(4) The output of HWFilter is used for CycleDetect.

Acquisition Modes

Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Acquisition Mode Details

16 Bit Resolution

Recording Mode	**Single Sweep Multiple Sweeps**			**Continuous**			**Dual Rate**		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	6 Ch	6 Ch & events	1 Ch	6 Ch	6 Ch & events	1 Ch	6 Ch	6 Ch & events
Max. sweep memory	1 GS	166 MS	142 MS	not used			800 MS	133 MS	113 MS
Max. sweep sample rate	2 MS/s			not used			2 MS/s		
Max. continuous FIFO	not used			1 GS	166 MS	142 MS	199 MS	33 MS	28 MS
Max. continuous sample rate	not used			2 MS/s			Sweep sample rate / 2		
Max. continuous streaming rate	not used			2 MS/s 4 MB/s	12 MS/s 24 MB/s	14 MS/s 28 MB/s	2 MS/s 4 MB/s	12 MS/s 24 MB/s	14 MS/s 28 MB/s

18 Bit Resolution

Recording Mode	**Single Sweep Multiple Sweeps**			**Continuous**			**Dual Rate**		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	6 Ch	6 Ch & events & Timer/ Counter	1 Ch	6 Ch	6 Ch & events & Timer/ Counter	1 Ch	6 Ch	6 Ch & events & Timer/ Counter
Max. sweep memory	500 MS	83 MS	55 MS	not used			400 MS	66 MS	44 MS
Max. sweep sample rate	2 MS/s			not used			2 MS/s		
Max. continuous FIFO	not used			500 MS	83 MS	55 MS	99 MS	16 MS	10 MS
Max. continuous sample rate	not used			2 MS/s			Sweep sample rate / 2		
Max. aggregate continuous streaming rate	not used			2 MS/s 8 MB/s	12 MS/s 48 MB/s	18 MS/s 72 MB/s	2 MS/s 8 MB/s	12 MS/s 48 MB/s	18 MS/s 72 MB/s

Single Sweep	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.3 B04375_02_E00_00 (GEN series GN611B)

Capabilities Overview			
Model	GN611B		
Maximum sample rate per channel	200 kS/s		
Memory per card	200 MB		
Analog channels	6		
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter		
ADC resolution	18 bit		
Isolation	Channel to channel and channel to chassis		
Input type	Analog, isolated balanced differential		
Passive voltage/current probes	Special designed matching probes only (e.g. Elas HDP)		
Sensors	Not supported		
TEDS	Not supported		
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results		
Real-time formula database calculators (option)	Extensive set of user programmable math routines with triggering on calculated results		
Real-time calculated results output	Ethernet software API	EtherCAT®	CAN/CAN FD
Result blocks per second	2000	1000	500
Latency	Ethernet dependent	1 ms	CAN bus speed
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels		
Standard data streaming (CPCI up to 200 MB/s)	Not supported		
Fast data streaming (PCIe up to 1 GB/s)	Supported		
Slot width	1		

Block Diagram

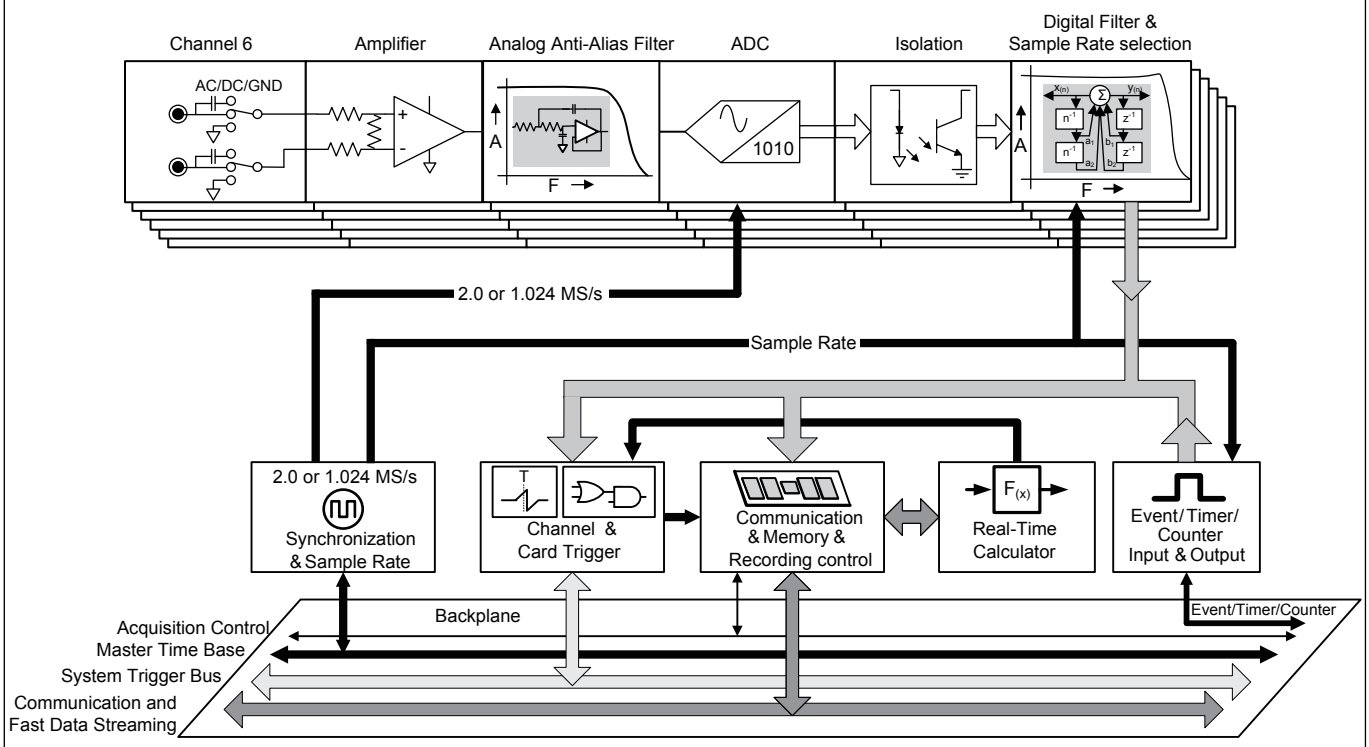


Figure A.38: Block Diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input Section		
Channels	6	
Connectors	Fully isolated 4 mm banana plugs (plastic), 2 per channel (red and black)	
Input type	Analog, isolated balanced differential	
Input impedance	2 * 1 MΩ ± 1% // 33 pF ± 10% ranges larger than ± 5 V. All other ranges 57 pF ± 10%	
Input coupling		
Coupling modes	AC, DC, GND	
AC coupling frequency	48 Hz ± 5 Hz (-3 dB)	

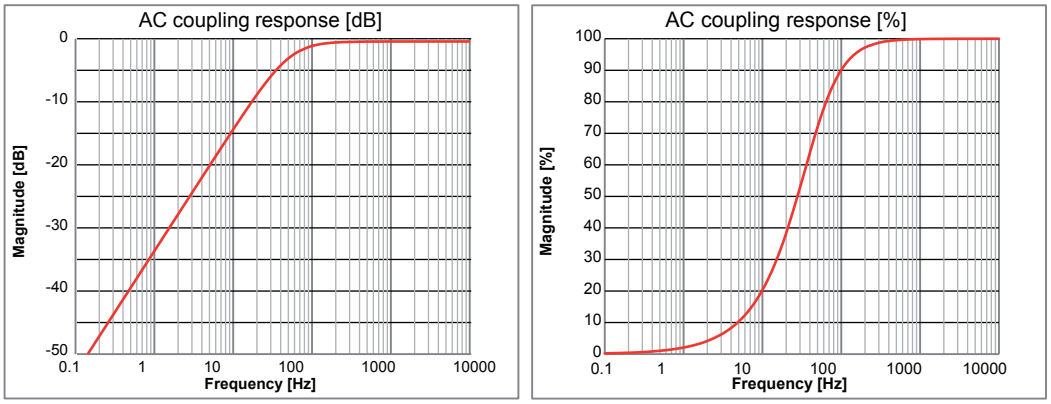
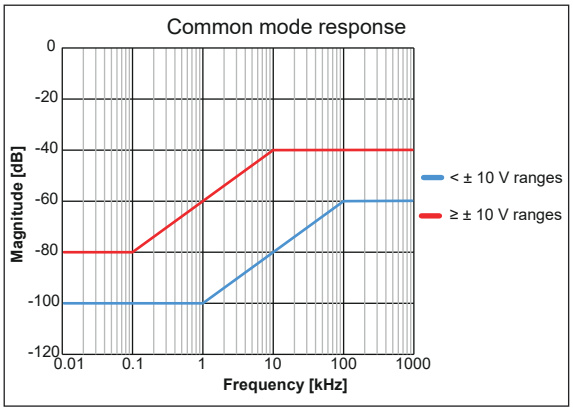


Figure A.39: Representative AC coupling response

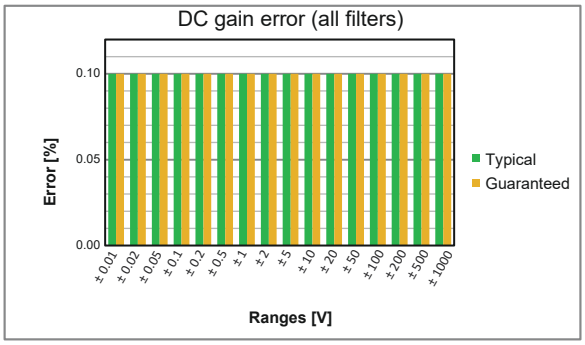
Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V, ± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1000 V	
Offset	± 50% in 1000 steps (0.1%); ± 1000 V range has fixed 0% offset	
Common mode (referred to system ground)		
Ranges	Less than ± 10 V	Larger than or equal to ± 10 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	7 V RMS	1000 V RMS

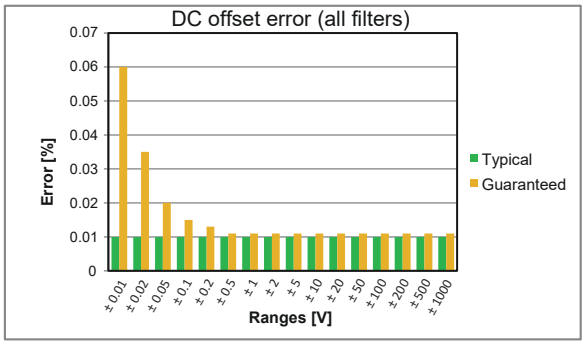


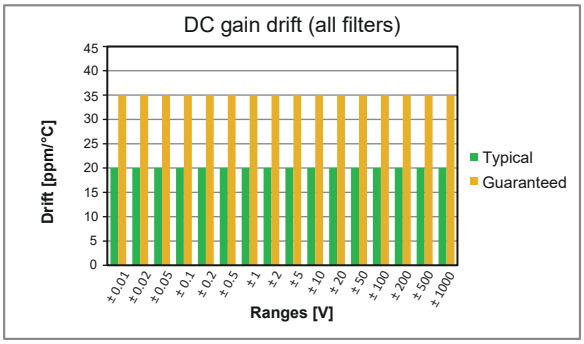
Input overload protection	
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage remains less than 200% of the selected input range or 1250 V, whichever value is the smallest.
Maximum nondestructive voltage	± 2000 V DC
Maximum overload without auto range	200% of selected range
Automatic auto range	When overload causes the amplifier to overheat, the amplifier increases its range in steps of a factor of 10 until the overload ceases. When the overload exceeds 1000 V, the input signal is disconnected and the amplifier input is grounded. When the temperature returns to normal, the range that was originally selected is restored. The automatic auto range cannot be turned off.
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

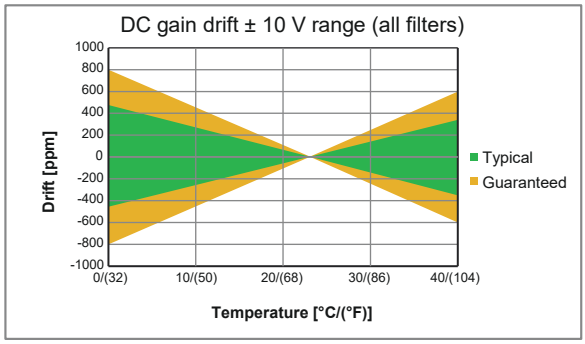
Voltage Specifications (All Filters Used)

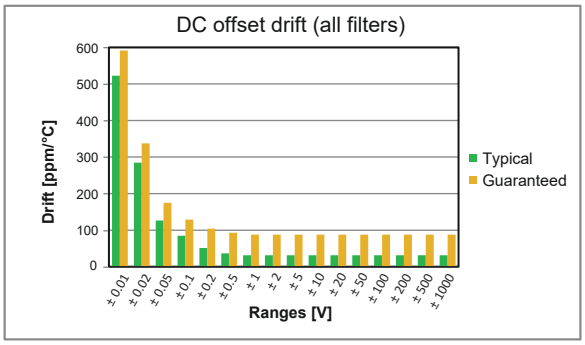
	Typical	Guaranteed
DC gain error	0.1% of reading	0.1% of reading
DC offset error	0.01% of Full Scale	0.01% of Full Scale ± 10 µV
DC gain error drift	±20 ppm/°C (±12 ppm/°F)	±35 ppm/°C (±20 ppm/°F)
DC offset error drift	±(30 ppm + 10 µV)/°C (±(17 ppm + 6 µV)/°F)	±(80 ppm + 10 µV)/°C (±(45 ppm + 6 µV)/°F)
RMS Noise (50 Ω terminated)	0.01% of Full Scale ± 20 µV	0.02% of Full Scale ± 20 µV

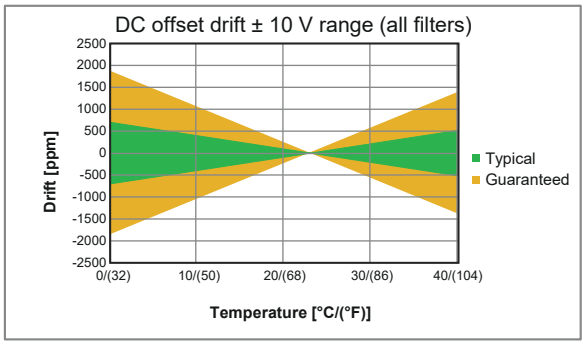












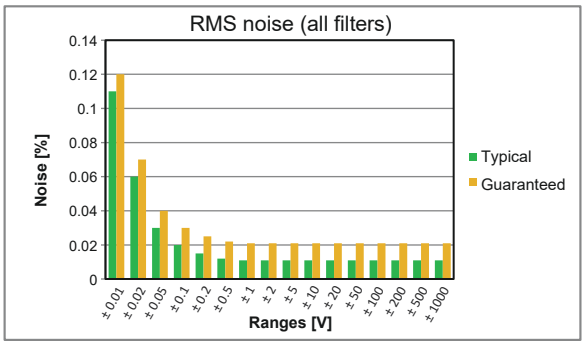


Figure A.40: All filters used voltage specification

Basic Power Accuracy

The GN610B/GN611B is calibrated and checked at 53 Hz voltage and current inputs using burden resistors. During calibration burden resistors are attached to three voltage channels to enable current measurements.
Specifications are given for the 2.5 Ω burden. Using the 1.0 Ω or 10.0 Ω burden will give different current ranges but identical results.

2.5 Ω	**Burden spans**	**1.264 A DC**	**800 mA DC**	**400 mA DC**	**160 mA DC**	**80 mA DC**	**40 mA DC**
0 - 100 Hz Sine wave CF: 1.41 Cos Phi : 1	**Burden ranges**	**440 mA RMS**	**280 mA RMS**	**140 mA RMS**	**56 mA RMS**	**28 mA RMS**	**14 mA RMS**
	IT200 ranges	N/A	200 A RMS(1)	140 A RMS	56 A RMS	28 A RMS	14 A RMS
	IT400 ranges	N/A	400 A RMS(1)	280 A RMS	112 A RMS	56 A RMS	28 A RMS
	IT700 ranges	700 A RMS(1)	490 A RMS	245 A RMS	98 A RMS	49 A RMS	24.5 A RMS
Voltage spans	**Voltage ranges**	Typical	Typical	Typical	Typical	Typical	Typical
40 V DC	**14.1 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
100 V DC	**35.3 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
200 V DC	**70.7 V RMS**	0.02% reading +0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
400 V DC	**141 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
1 kV DC	**353 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range
2 kV DC	**707 V RMS**	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.05% range	0.02% reading + 0.1% range	0.02% reading + 0.1% range	0.02% reading + 0.15% range

(1) With the right setup the LEM sensor can be used for this range, however this input range is not specified in the LEM current sensor data sheet.

Isolation

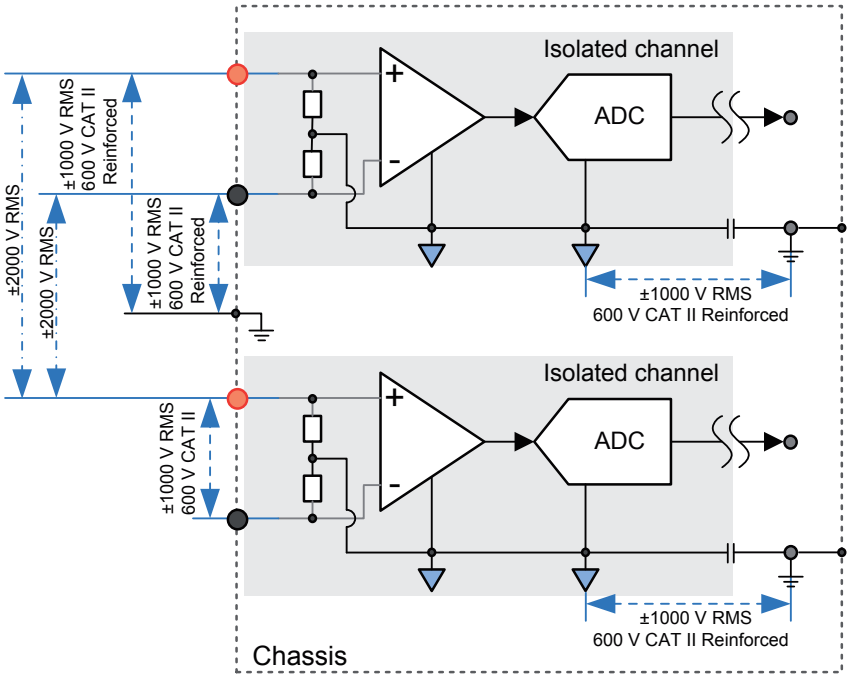


Figure A.41: Isolation 1kV card overview

		CAT II	CAT III
Channel to chassis (earth)	1000 V RMS	600 V RMS (1)	300 V RMS(1)
Channel to channel	2000 V RMS	(2)	(2)

(1) IEC61010-1 category voltage ratings are RMS voltages.

(2) Channel to channel CAT II and CAT III ratings are not a valid method to specify.

Isolation and Input Type Testing

IEC61010-1:2010 and IEC61010-2-030:2010 isolation tests	
Channel to channel	3510 V RMS and 4935 V DC for 5 s 3260 V RMS and 4596 V DC for 1 minute
Channel to chassis	3510 V RMS and 4935 V DC for 5 s 3260 V RMS and 4596 V DC for 1 minute
Channel to channel impulse	6400 V peak using a 2 Ω series resistor Rise time 1.2 µs, 50% amplitude reduction in 50 µs
Channel to chassis impulse	6400 V peak using a 2 Ω series resistor Rise time 1.2 µs, 50% amplitude reduction in 50 µs

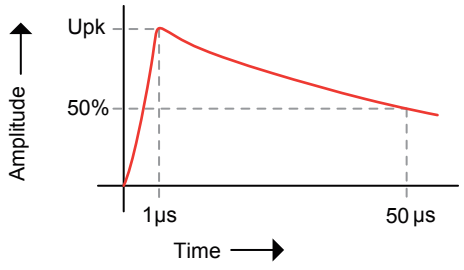


Figure A.42: Example of 1.2/50 µs impulse

Input impulse test	
Channel positive to negative input	4000 V peak using a 12 Ω series resistor, rise time 1.2 µs, 50% amplitude reduction in 50 µs

Analog to Digital Conversion	
Sample rate per channel	0.1 S/s to 200 kS/s
ADC resolution; one ADC per channel	18 bit
ADC type	Successive Approximation Register (SAR); Analog Devices AD7986BCPZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm; aging after 10 years ± 10 ppm
Binary sample rate	Supported; produces rounded BIN values when calculating FFTs
Maximum binary sample rate	204.8 kS/s
External time base frequency	0 S/s to 200 kS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

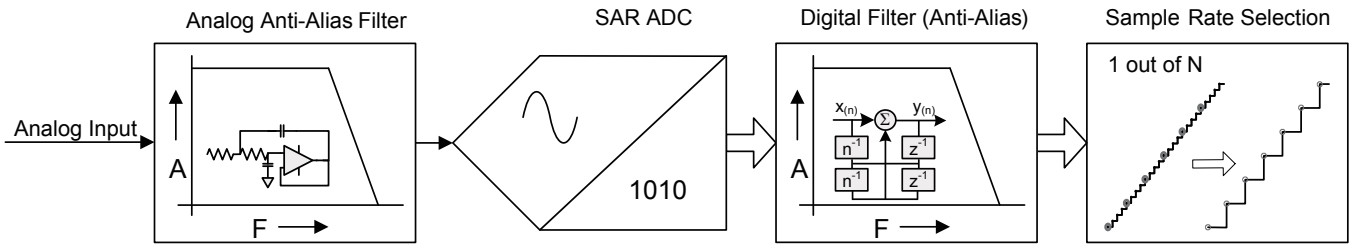
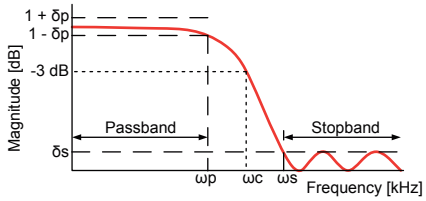


Figure A.43: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Bessel IIR	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.44: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.	
Analog anti-alias filter bandwidth	400 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	8-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	User selectable from 0.4 Hz to 20 kHz
Bessel IIR 0.1 dB passband (ωp)(1)	DC to 0.14 * ωc
Bessel IIR filter stopband attenuation (δs)	60 dB
Bessel IIR filter roll-off	48 dB/octave

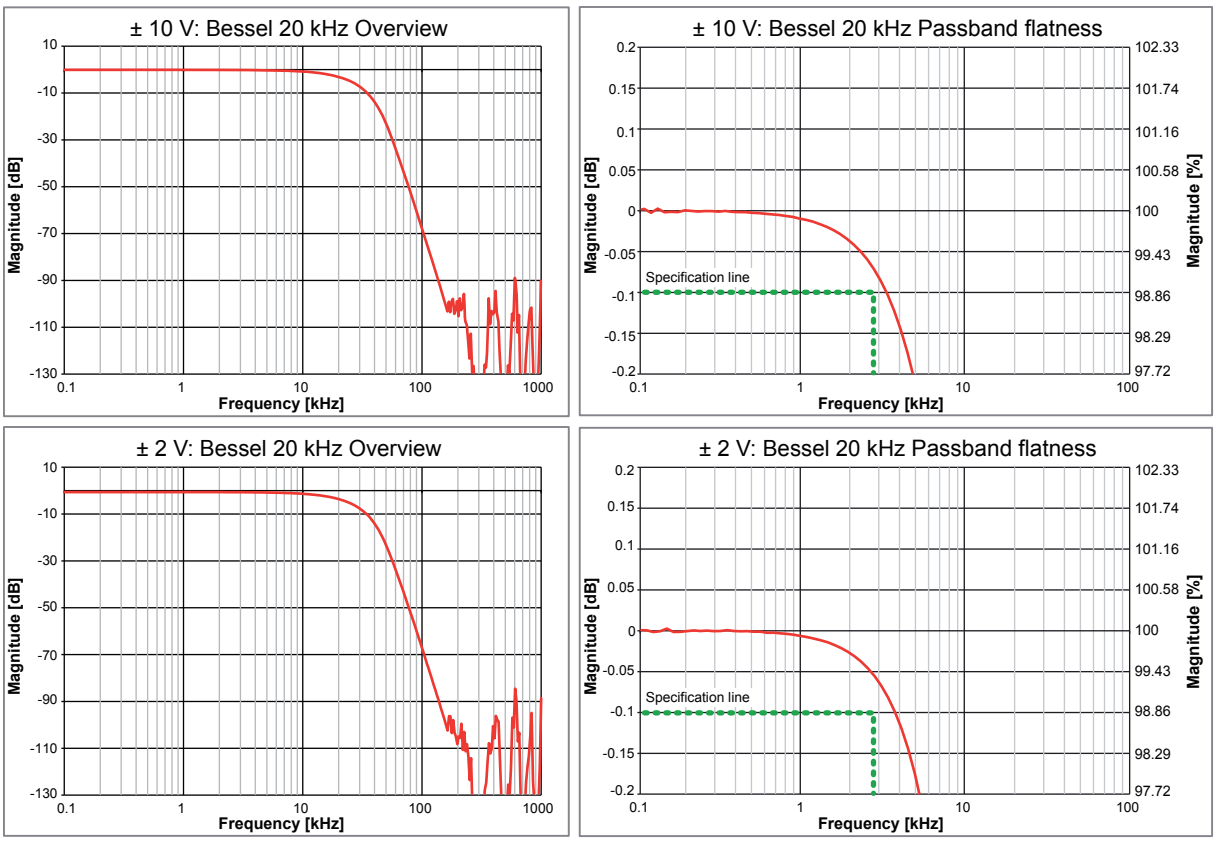
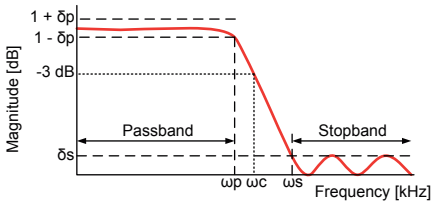


Figure A.45: Representative Bessel IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.46: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter.

Analog anti-alias filter bandwidth	465 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Butterworth IIR filter characteristic	8-pole Butterworth style IIR
Butterworth IIR filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Butterworth IIR filter bandwidth (ωc)	User selectable from 1 Hz to 50 kHz
Butterworth IIR 0.1 dB passband (ωp)(1)	DC to 0.7 * ωc
Butterworth IIR filter stopband attenuation (δs)	75 dB
Butterworth IIR filter roll-off	48 dB/octave

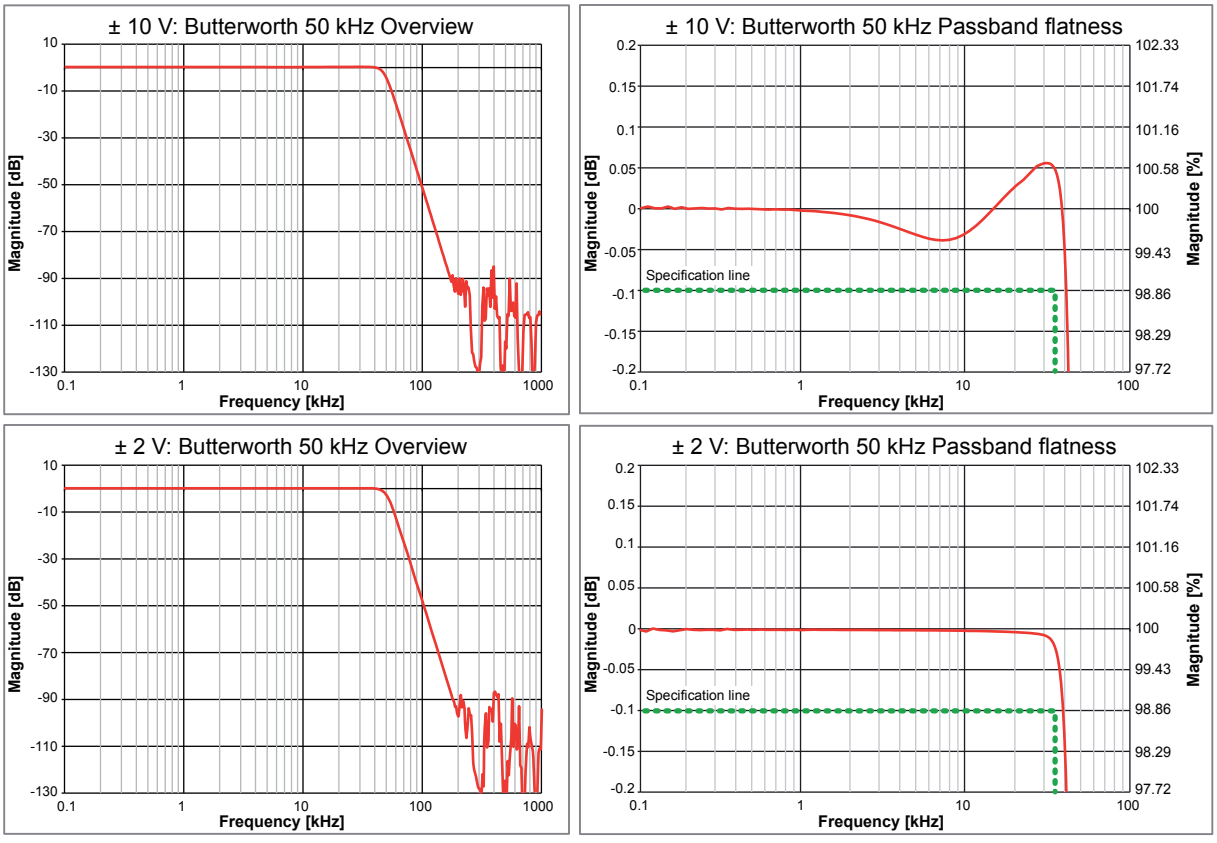
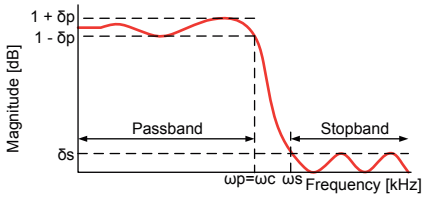


Figure A.47: Representative Butterworth IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.48: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter.	
Analog anti-alias filter bandwidth	465 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Elliptic IIR filter characteristic	7-pole Elliptic style IIR
Elliptic IIR filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Elliptic IIR filter bandwidth (ωc)	User selectable from 1 Hz to 50 kHz
Elliptic IIR 0.1 dB passband (ωp)(1)	DC to ωc
Elliptic IIR filter stopband attenuation (δs)	75 dB
Elliptic IIR filter roll-off	72 dB/octave

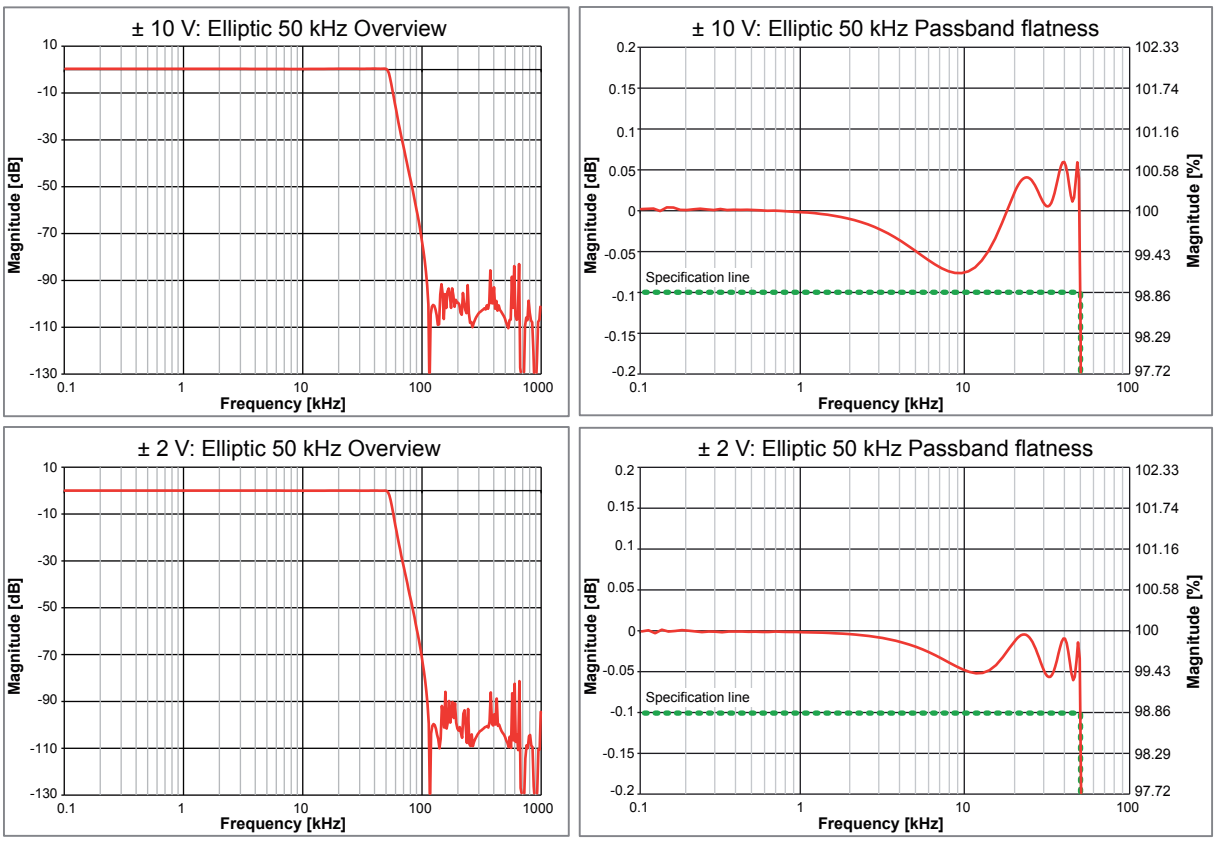


Figure A.49: Representative Elliptic IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match

Using different filter selections (Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths results in phase mismatches between channels. All specifications are typical static values and measured using a 10 kHz sine wave and 200 kS/s sample rate.

	< ±10V spans	≥ ±10V spans	Combined spans
Bessel IIR, Filter frequency 20 kHz			
Channels on card	0.01° (3 ns)	0.04° (13 ns)	0.27° (76 ns)
GN611B Channels within mainframe	0.01° (3 ns)	0.06° (17 ns)	0.27° (76 ns)
Butterworth IIR, Filter frequency 50 kHz			
Channels on card	0.02° (6 ns)	0.04° (13 ns)	0.27° (76 ns)
GN611B Channels within mainframe	0.02° (6 ns)	0.06° (17 ns)	0.27° (76 ns)
Elliptic IIR, Filter frequency 50 kHz			
Channels on card	0.02° (6 ns)	0.04° (13 ns)	0.27° (76 ns)
GN611B Channels within mainframe	0.02° (6 ns)	0.06° (17 ns)	0.27° (76 ns)
GN611B channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)		

Channel to Channel Crosstalk

Channel to channel crosstalk is measured with a 50 Ω termination resistor on the input and uses sine wave signals on the channel above and below the channel being tested. To test Channel 2, Channel 2 is terminated with 50 Ω and Channels 1 and 3 are connected to the sine wave generator.

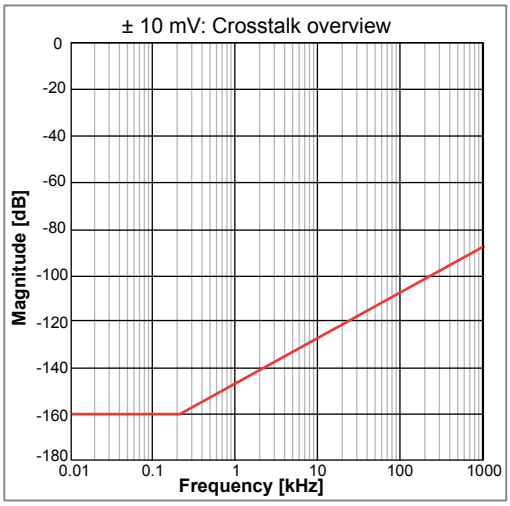


Figure A.50: Representative Channel to Channel crosstalk

On-board Memory

Per card	200 MB (100 MS @ 16 bits, 50 MS @ 18 bits storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	User selectable 16 or 18 bits 16 bits, 2 bytes/sample 18 bits, 4 bytes/sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

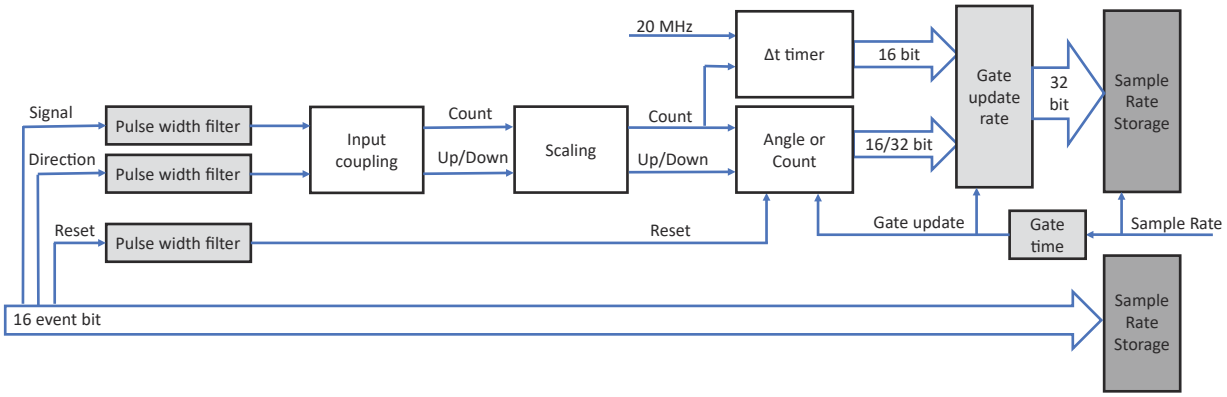


Figure A.51: Timer/Counter block diagram

Digital input events	16 per card			
Levels	TTL input level, user programmable invert level			
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs			
Overvoltage protection	± 30 V DC continuously			
Minimum pulse width	100 ns			
Maximum frequency	5 MHz			
Digital output events	2 per card			
Levels	TTL output levels, short circuit protected			
Output event 1	User selectable: Trigger, Alarm, set High or Low			
Output event 2	User selectable: Recording active, set High or Low			
Digital output event user selections				
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay			
Alarm	High when alarm condition of card is activated, low when not activated 200 µs ± 1 µs ± 1 sample period alarm event delay			
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns			
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation			
Timer/Counter	2 per card			
Levels	TTL input levels			
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs			
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)			
Measurement modes	Count (C) Angle (0 to 360 degrees) Frequency (Δcount / Δt) RPM (Δcount / Δt / 60 s)			
Δt timer measurement accuracy	50 ns (20 MHz)			
Gate time	1 to n samples (User selectable maximum Δt)			
Gate time and reading update rate	Gate time sets the maximum update rate of the measurement values			
Gate time and minimum frequency	Minimum measured frequency or RPM = 1 / gate time			
Gate time and frequency accuracy	Accuracy = 50 ns / gate time			
Gate time impact	**Gate time**	**1 us**	**10 us**	**100 us**
	Δt Error	5%	0.5%	0.05%
	Update rate	1 MS/s	100 kS/s	10 kS/s
RT-FDB options	RT-FDB timer based average enables the same gate time effect. RT-FDB cycle detect average enables a dynamic gate time effect.			

Input Coupling Uni- and Bi-directional Signal

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

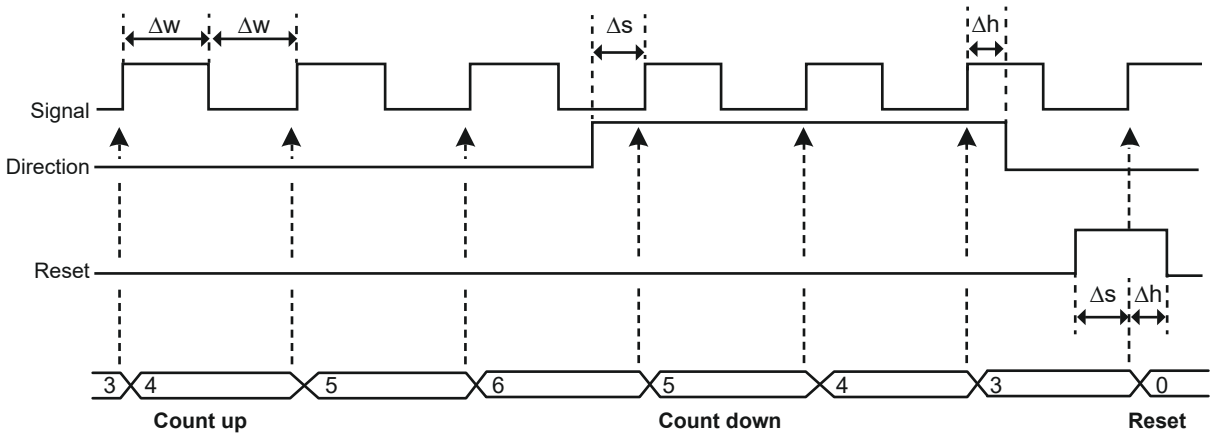


Figure A.52: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	4 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

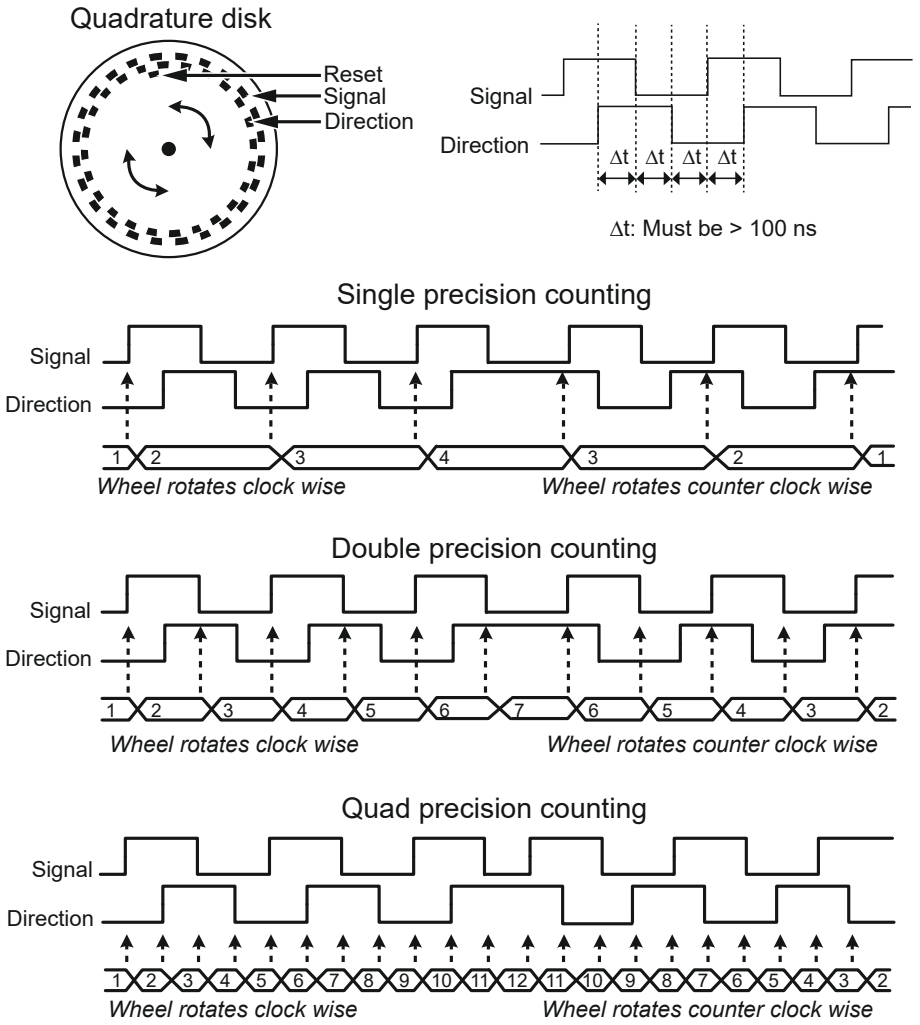


Figure A.53: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Count/Position	
Count/position mode is typically used for tracking movement of device under test. To reduce the sensitivity for count/position errors due to clock glitches use the minimum pulse width filter or enable the ABZ in stead of uni-/bi-polar input coupling .	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31} - 1$; bi-directional count

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period (identical for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (10 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (9.76 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516 (504) µs for decimal (binary) time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators

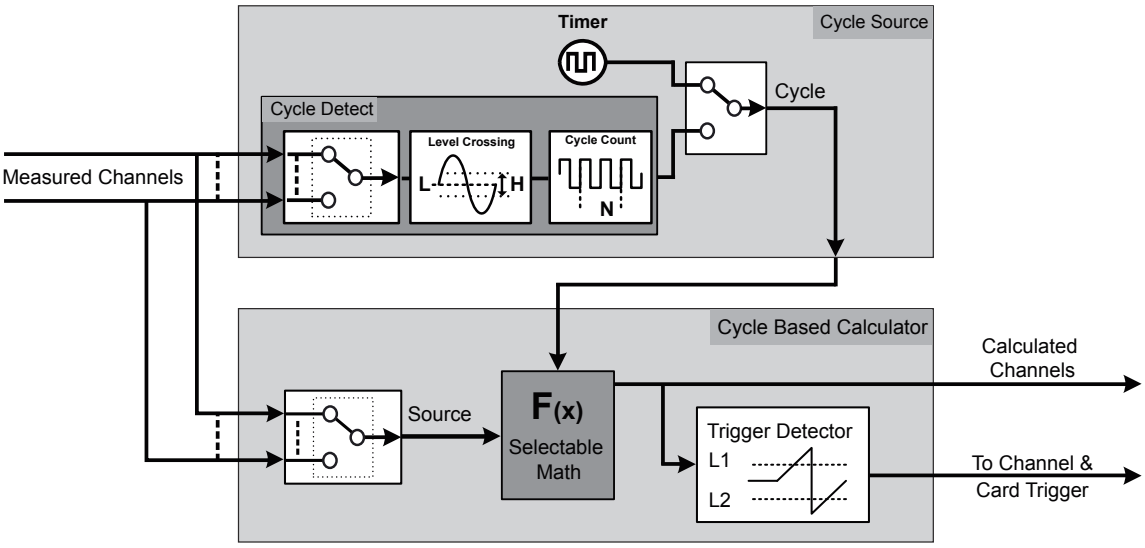


Figure A.54: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased
Cycle based calculator	
Number of calculators	32
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and Crest Factor
Timer/Counter channel calculations	Frequency (to enable triggering), RPM of Angle
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)

The real-time formula database (RT-FDB) option offers an extensive set of math routines to enable almost any real-time mathematical challenge. The database structure enables the user to define a list of mathematical equations similar to the Perception review formula database.
The maximum supported sample rate is 2 MS/s.
The real-time formula database feature set is extended with higher Perception Versions. Different versions of Perception therefore can enable more or less features as described in this table.

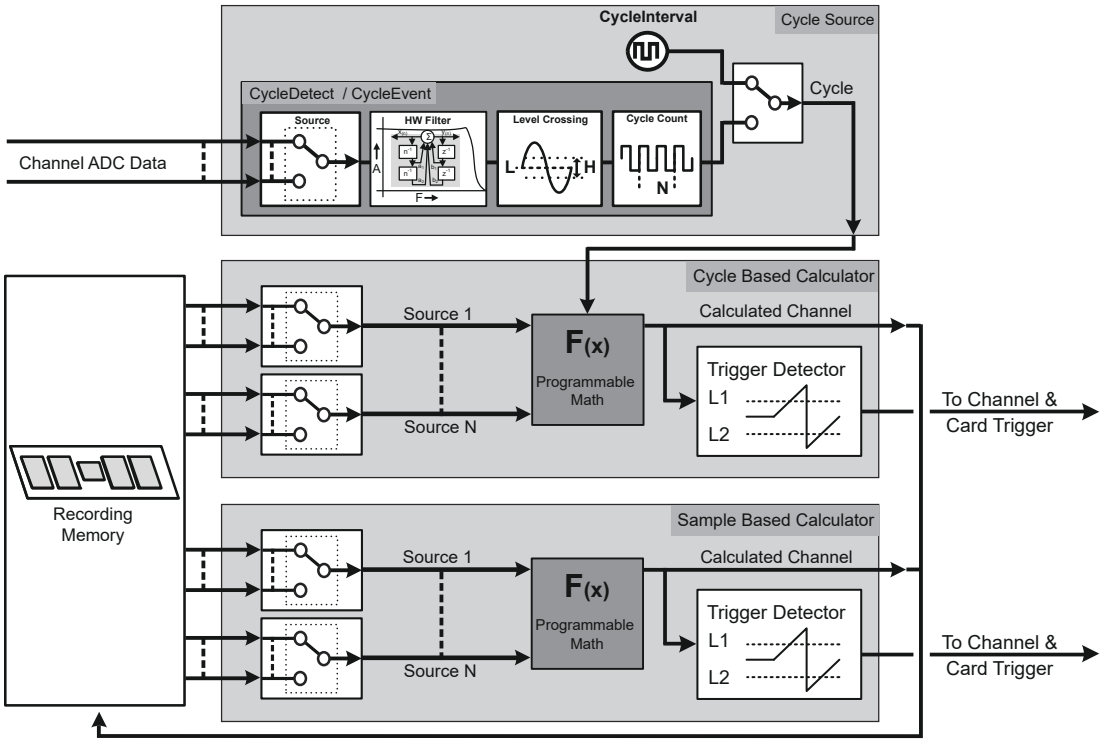


Figure A.55: Real-time formula database (RT-FDB) calculators

The real-time formula database supports the following list of calculations (Details of each calculation are described in the manual).

Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Basic calculations				
`+ (add)`	✓	✓	✓	✓(1)
`- (subtract)`	✓	✓	✓	✓(1)
`* (multiply)`	✓	✓	✓	✓(1)
`/ (divide)`	✓	✓	✓	✓(1)
Enhanced calculations				
`Abs`	✓	✓	✓	✓(1)
`Atan`	✓	✓	✓	✓(1)
`Atan2`	✓	✓	✓	✓(1)
`Cosine`	✓	✓	✓	✓(1)
`DegreesToRadians`	✓	✓	✓	✓(1)
`Min`	✓	✓	✓	✓(1)
`Max`	✓	✓	✓	✓(1)
`Modulo`	✓	✓	✓	✓(1)
`RadiansToDegrees`	✓	✓	✓	✓(1)
`Sine`	✓	✓	✓	✓(1)
`Sqrt`	✓	✓	✓	✓(1)
`Tan`	✓	✓	✓	✓(1)

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Boolean calculations				
`Equal`	✓	✓	✓	✓
`GreaterEqualThan`	✓	✓	✓	✓
`GreaterThan`	✓	✓	✓	✓
`LessEqualThan`	✓	✓	✓	✓
`LessThan`	✓	✓	✓	✓
`NotEqual`	✓	✓	✓	✓
`InsideBand`	✓	✓	✓	
`OutsideBand`	✓	✓	✓	
`And`	✓	✓	✓	✓
`Or`	✓	✓	✓	✓
`Xor`	✓	✓	✓	✓
`Not`	✓	✓	✓	✓
Cycle based calculations				
`CycleArea`		✓	✓	✓
`CycleBusDelay`		✓	✓	✓
`CycleCount`		✓	✓	✓
`CycleCrestFactor`		✓	✓	✓
`CycleEnergy`		✓	✓	✓
`CycleFundamentalPhase`		✓	✓	✓(2)
`CycleFundamentalRMS`		✓	✓	✓
`CycleFrequency`		✓	✓	✓
`CycleMax`		✓	✓	✓
`CycleMean`		✓	✓	✓
`CycleMin`		✓	✓	✓
`CyclePeak2Peak`		✓	✓	✓
`CyclePhase`		✓	✓	✓
`CycleRMS`		✓	✓	✓
`CycleRPM`		✓	✓	✓
`CycleSampleCount`		✓	✓	✓
`CycleTHD`(2)		✓	✓	✓(2)
Cycle source				
`CycleDetect`(4)		✓	✓	
`CycleEvent`		✓	✓	
`CycleInterval`		✓	✓	

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Hardware based signal filtering				
`HWFilter`(4)	✓		✓	
Software based signal filtering				
`FilterBesselBP`	✓		✓	
`FilterBesselHP`	✓		✓	
`FilterBesselLP`	✓		✓	
`FilterButterworthBP`	✓		✓	
`FilterButterworthHP`	✓		✓	
`FilterButterworthLP`	✓		✓	
`FilterChebyshevBP`	✓		✓	
`FilterChebyshevHP`	✓		✓	
`FilterChebyshevLP`	✓		✓	
Special category calculation				
`HarmonicsIEC61000`	✓		✓	
`Integrate`	✓		✓	
Signal transformation				
`DQZeroTransformation (Park)` (3)	✓		✓	✓(1)
`SpaceVectorTransformation`(3)	✓		✓	
`SpaceVectorInverse Transformation`(3)	✓		✓	
Signal generation				
`SineWave`	✓		✓	
`Ramp`	✓		✓	
Trigger functions				
`TriggerOnBooleanChange`			Trigger mark	
`TriggerOnLevel`			Trigger mark	

(1) Only cycle based results can be used for real-time output. Use the CycleMean calculation on recorded channel data or sample based results to enable the real-time output of this data.

(2) The time required to calculate the output depends on maximum cycle length and sample rate. Depending on the selected settings the output latency will increase. HBM refers to these calculations as not deterministic. All real-time output published values (deterministic and/or not deterministic) will always have the same latency.

(3) This formula is only available if the eDrive license is added to Perception.

(4) The output of HWFilter is used for CycleDetect.

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Acquisition Mode Details

16 Bit Resolution

Recording Mode	Single Sweep Multiple Sweeps			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	6 Ch	6 Ch & events	1 Ch	6 Ch	6 Ch & events	1 Ch	6 Ch	6 Ch & events
Max. sweep memory	100 MS	16 MS	14 MS	not used			80 MS	13 MS	11 MS
Max. sweep sample rate	200 kS/s			not used			200 kS/s		
Max. continuous FIFO	not used			100 MS	16 MS	14 MS	18 MS	3 MS	2.5 MS
Max. continuous sample rate	not used			200 kS/s			Sweep sample rate / 2		
Max. aggregate continuous streaming rate	not used			0.2 MS/s 0.4 MB/s	1.2 MS/s 2.4 MB/s	1.4 MS/s 2.8 MB/s	0.2 MS/s 0.4 MB/s	1.2 MS/s 2.4 MB/s	1.4 MS/s 2.8 MB/s

18 Bit Resolution

Recording Mode	Single Sweep Multiple Sweeps			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	6 Ch	6 Ch & events & Timer/ Counter	1 Ch	6 Ch	6 Ch & events & Timer/ Counter	1 Ch	6 Ch	6 Ch & events & Timer/ Counter
Max. sweep memory	50 MS	8 MS	5 MS	not used			40 MS	6.5 MS	4 MS
Max. sweep sample rate	200 kS/s			not used			200 kS/s		
Max. continuous FIFO	not used			50 MS	8 MS	5 MS	9 MS	1.5 MS	1 MS
Max. continuous sample rate	not used			200 kS/s			Sweep sample rate / 2		
Max. aggregate continuous streaming rate	not used			0.2 MS/s 0.8 MB/s	1.2 MS/s 4.8 MB/s	1.8 MS/s 7.2 MB/s	0.2 MS/s 0.8 MB/s	1.2 MS/s 4.8 MB/s	1.8 MS/s 7.2 MB/s

Single Sweep	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.4 B03997_02_E00_00 (GEN series GN815)

Capabilities Overview	
Model	GN815
Maximum sample rate per channel	2 MS/s
Memory per card	2 GB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	18 bit
Isolation	Channel to channel and channel to chassis
Input type	Analog, isolated, unbalanced differential
Passive voltage/current probes	Passive, singled-ended voltage probes
Sensors	IEPE
TEDS	Class 1, IEPE sensors
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Not supported
Real-time calculated results output	Not supported
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels
Standard data streaming (CPCI up to 200 MB/s)	Supported
Fast data streaming (PCIe up to 1 GB/s)	Supported
Slot width	1

Supported Sensors and Probes		
Perception input type	**Sensor/probe types**	**Remarks**
Basic voltage	Single ended voltage input Passive single ended probes Active differential probes Current probes External current burdens	Isolated BNC input
Basic sensor	Not supported	
Bridge	Not supported	
Charge	Not supported	
IEPE	IEPE vibration sensors ICP® Accelerometers 2, 4, 6 or 8 mA @ ≥ 23 V	TEDS class I Automatic sensor connected, open or shorted diagnostics Isolated input
Current loop	Not supported	
Thermocouple	Not supported	
Resistance thermometers	Not supported	

Block Diagram

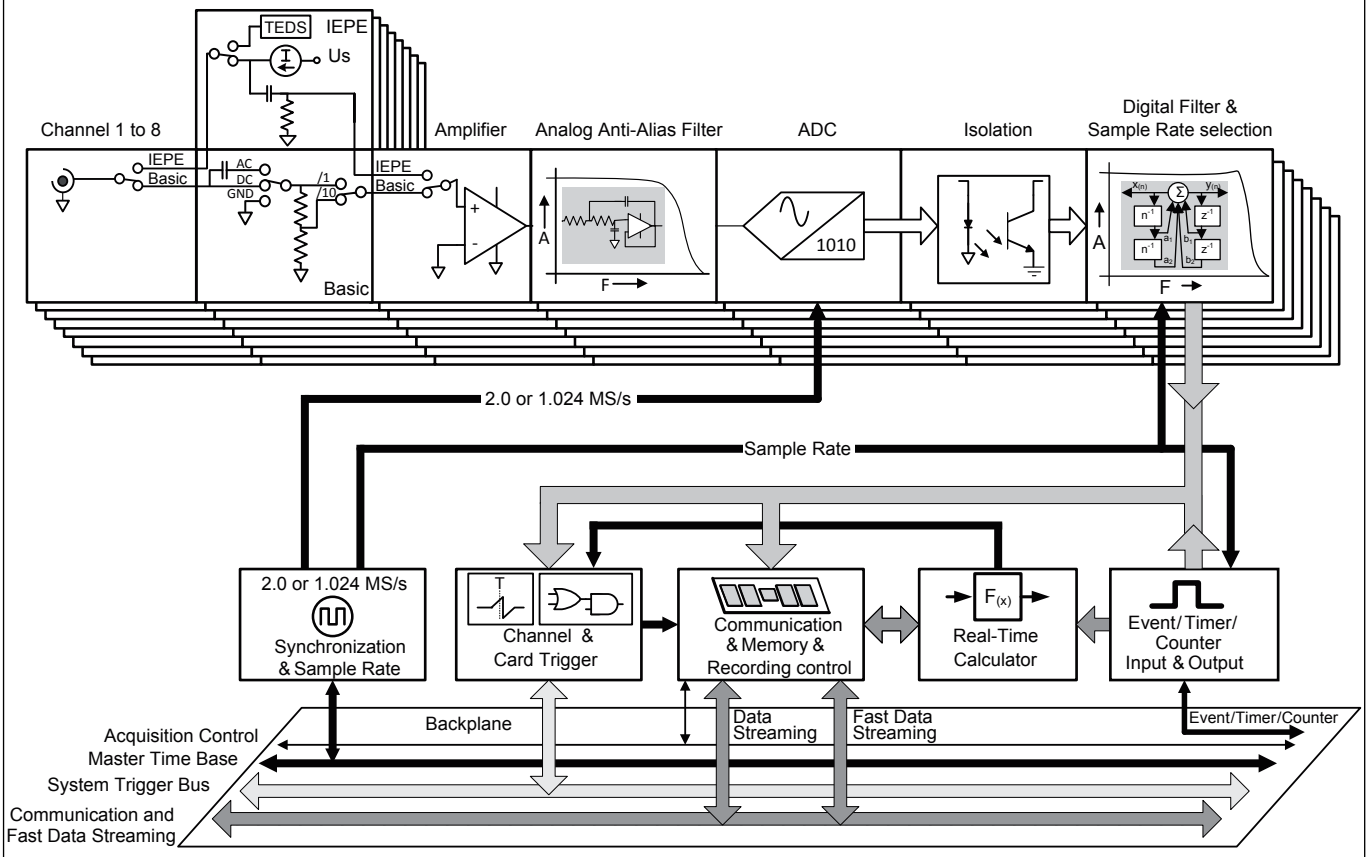


Figure A.56: Block Diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.

If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.

Recalibration after configuration changes is therefore highly recommended.

Analog Input Section		
Channels	8	
Connectors	Isolated metal BNC	
Input type	Analog, isolated, unbalanced differential	
Input impedance	1 MΩ ± 1% // 58 pF ± 10% ranges larger than ± 1 V. All other ranges 66 pF ± 10%	
Input coupling		
Coupling modes	AC, DC, GND	
AC coupling frequency	1.6 Hz ± 10%; - 3 dB	

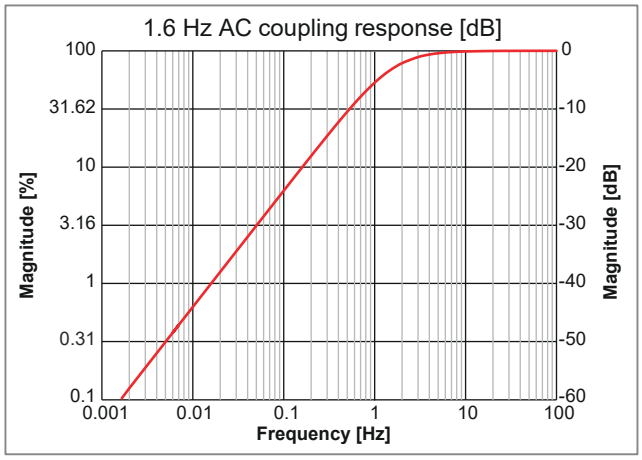


Figure A.57: Representative AC coupling response

Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V, ± 50 V	
Offset	± 50% in 1000 steps (0.1%); ± 50 V range has fixed 0% offset	
Common mode (referred to system ground)		
Ranges	Less than ± 2 V	Larger than or equal to ± 2 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	33 V RMS	33 V RMS

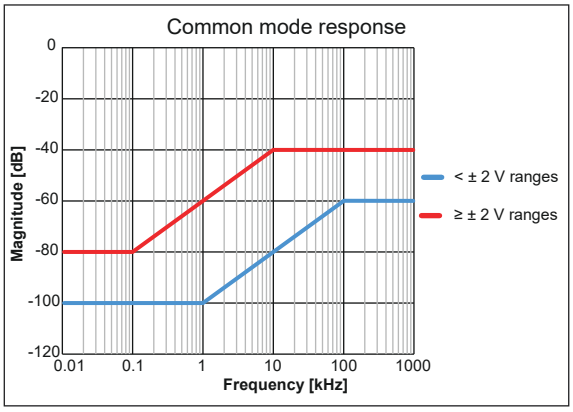


Figure A.58: Representative common mode response

Input overload protection	
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage remains less than 200% of the selected input range or 70 V, whichever value is the smallest.
Maximum nondestructive voltage	± 70 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

Voltage Specifications (Wideband)		
	Typical	**Guaranteed**
DC gain error	Not available	0.035% of reading ± 35 µV
DC Offset error	Not available	0.01% of Full Scale ± 200 µV
RMS Noise (50 Ω terminated)	Not available	0.025% of Full Scale ± 50 µV
Gain error drift	Not available	± 25 ppm/°C (± 14 ppm/°F)
Offset error drift	Not available	±(45 ppm + 5 µV)/°C (±(25 ppm + 3 µV)/°F)

Voltage Specifications (Filters Used)		
	Typical	**Guaranteed**
DC gain error	Not available	0.035% of Full Scale ± 35 µV
DC Offset error	Not available	0.01% of Full Scale ± 35 µV
RMS Noise (50 Ω terminated)	Not available	0.015% of Full Scale ± 20 µV
Gain error drift	Not available	± 25 ppm/°C (± 14 ppm/°F)
Offset error drift	Not available	±(45 ppm + 5 µV)/°C (±(25 ppm + 3 µV)/°F)

IEPE Sensor	
Input ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Overvoltage protection	- 1 V to 22 V
IEPE gain error	0.1% ± 250 µV
IEPE gain error drift	± 25 ppm/°C (± 14 ppm/°F)
IEPE compliance voltage	≥ 23 V
Excitation current	2, 4, 6, 8 mA, software selectable
Excitation current accuracy	± 5%
Coupling time constant	1.5 s
Lower bandwidth	-3 dB @ 0.11 Hz
Maximum cable length	100 m (RG-58)
TEDS support	Yes; class 1
Sensor diagnostics	Sensor connected, open or shorted
Supported sensors	IEPE vibration sensors ICP® Accelerometers

Isolation

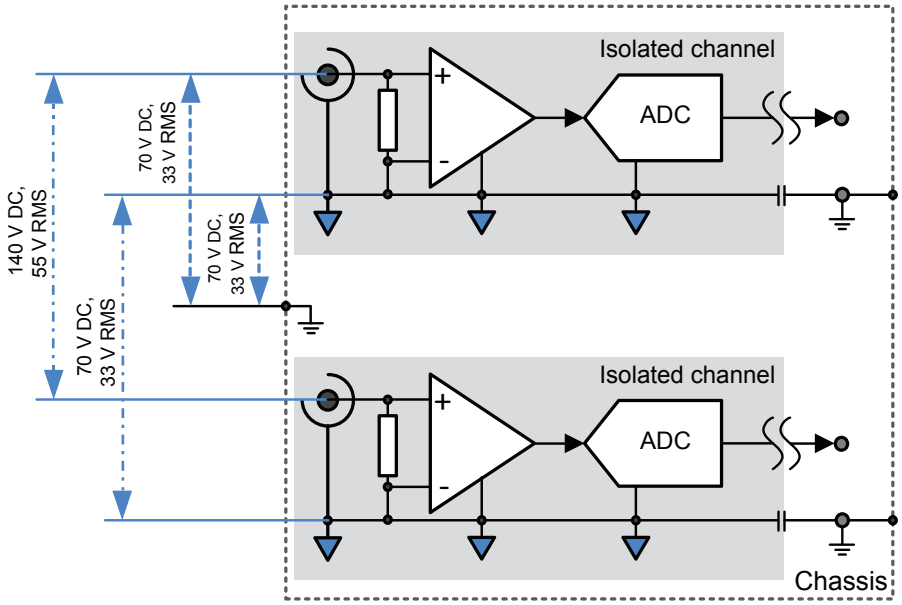


Figure A.59: Isolation schematic

Channel to chassis (earth)	33 V RMS, ± 70 V DC
Channel to channel (Isolated GND to isolated GND)	33 V RMS, ± 70 V DC
Input signal-to-input signal	55 V RMS, ± 140 V DC

Analog to Digital Conversion

Sample rate; per channel	0.1 S/s to 2 MS/s
ADC resolution; one ADC per channel	18 bit
ADC type	Successive Approximation Register (SAR); Analog Devices AD7986BCPZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; calculating FFTs results in rounded BIN values
Maximum binary sample rate	1.024 MS/s
External time base frequency	0 S/s to 1 MS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ±30 ppm.

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

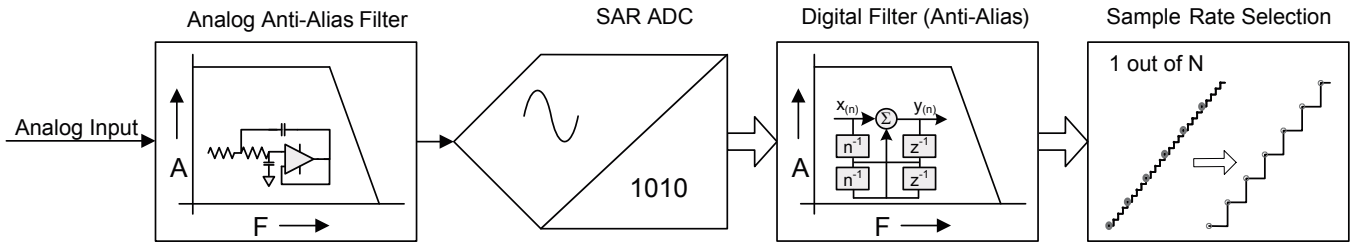


Figure A.60: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Wideband should not be used if working in a frequency domain with recorded data.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	Between 950 kHz and 1300 kHz (-3 dB)
0.1 dB passband flatness	DC to 200 kHz(1)

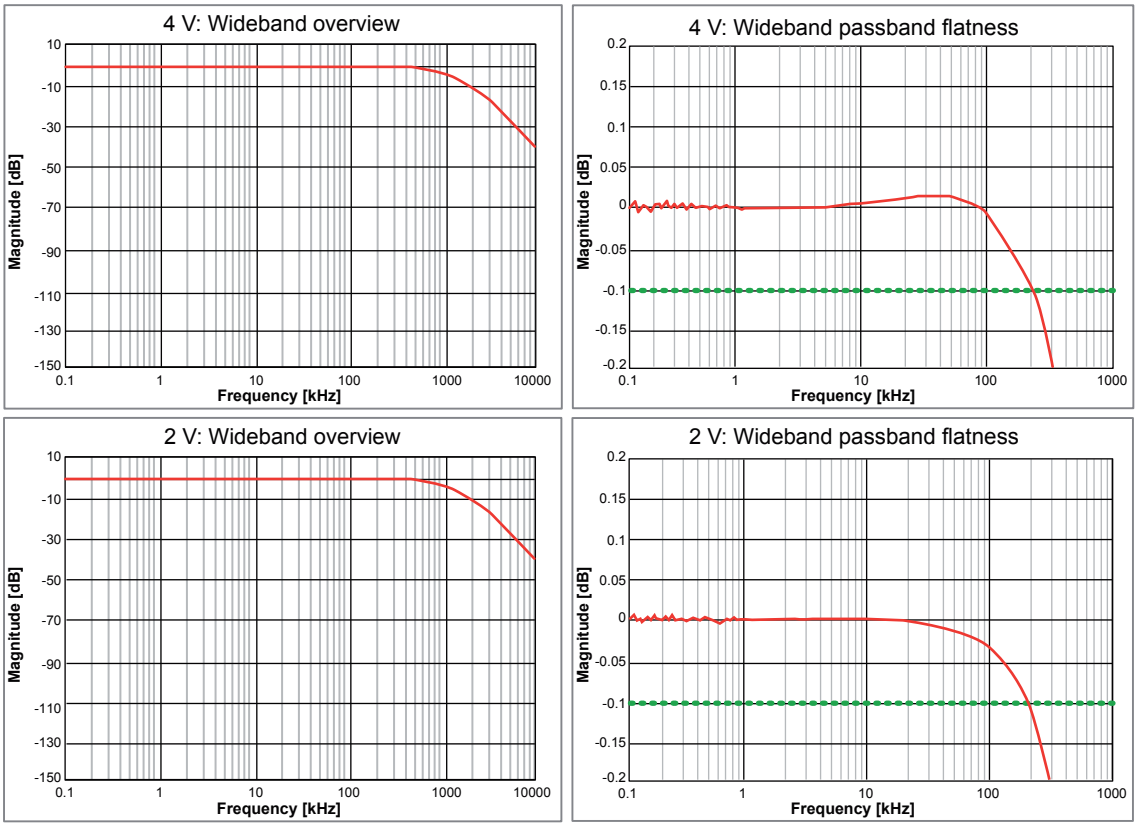
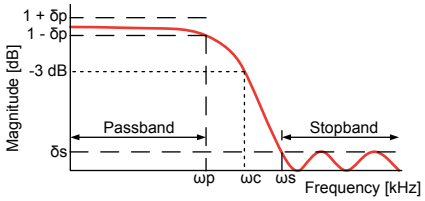


Figure A.61: Representative Wideband examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.62: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-alias filter bandwidth	390 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	8-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	User selectable from 0.4 Hz to 200 kHz
Bessel IIR 0.1 dB passband (ωp)(1)	DC to 35 kHz @ ωc = 200 kHz(1)
Bessel IIR filter stopband attenuation (δs)	60 dB With the Bessel IIR filter bandwidth selection of ωc = 200 kHz, a peak of -55 dB occurs between 1.6 MHz and 1.8 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
Bessel IIR filter roll-off	48 dB/octave

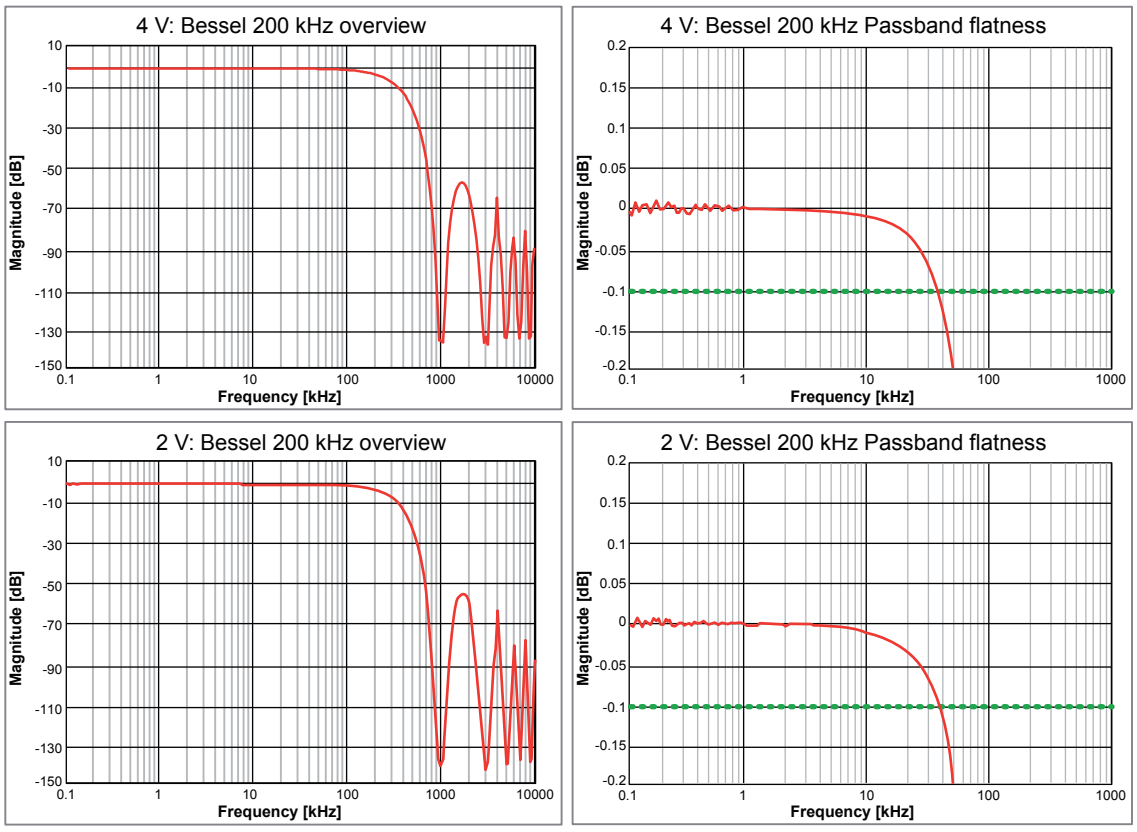
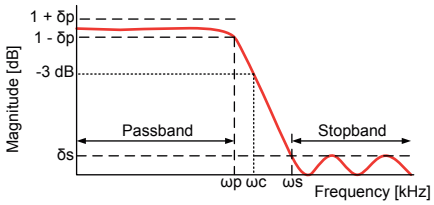


Figure A.63: Representative Bessel IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.64: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter.	
Analog anti-alias filter bandwidth	460 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Butterworth IIR filter characteristic	8-pole Butterworth style IIR
Butterworth IIR filter user selection	Auto tracking for sample rate divided by: 4(1), 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Butterworth IIR filter bandwidth (ωc)	User selectable from 1 Hz to 250 kHz
Butterworth IIR 0.1 dB passband (ωp)(2)	DC to 150 kHz @ ωc = 200 kHz(2)
Butterworth IIR filter stopband attenuation (δs)	75 dB With the Butterworth IIR filter bandwidth selection of ωc = 250 kHz, a peak of -60 dB occurs between 1.8 MHz and 2.2 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -75 dB.
Butterworth IIR filter roll-off	48 dB/octave

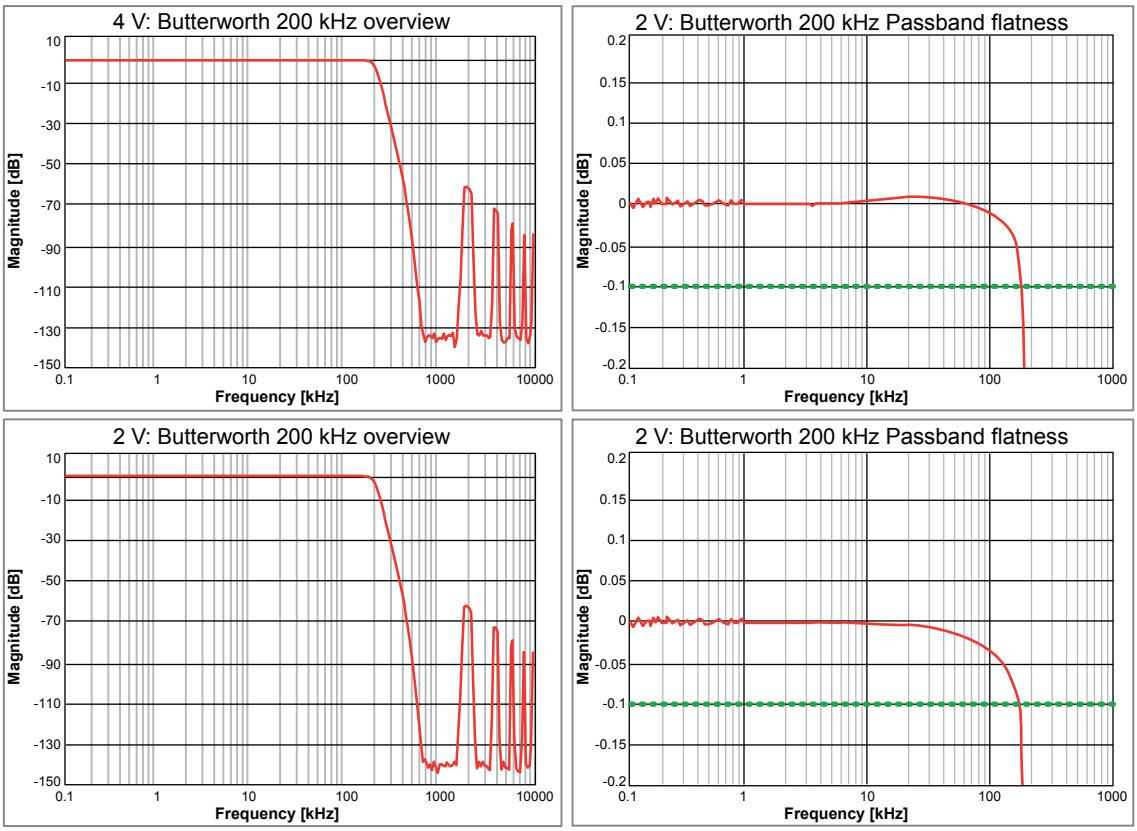
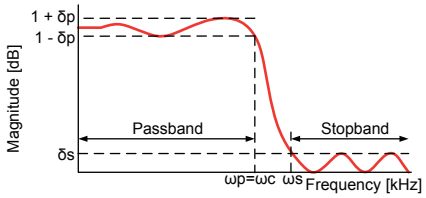


Figure A.65: Representative Butterworth IIR examples

(1) Division by 4 not possible for the 2 MS/s sample rate

(2) Measured using a Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.66: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter.

Analog anti-alias filter bandwidth	460 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Elliptic IIR filter characteristic	7-pole Elliptic style IIR
Elliptic IIR filter user selection	Auto tracking for sample rate divided by: 4(1), 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Elliptic IIR filter bandwidth (ωc)	User selectable from 1 Hz to 250 kHz
Elliptic IIR 0.1 dB passband (ωp)(2)	DC to ωc
Elliptic IIR filter stopband attenuation (δs)	75 dB With the Elliptic IIR filter bandwidth selection of ωc = 250 kHz, a peak of -60 dB occurs between 1.8 MHz and 2.2 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -75 dB.
Elliptic IIR filter roll-off	72 dB/octave

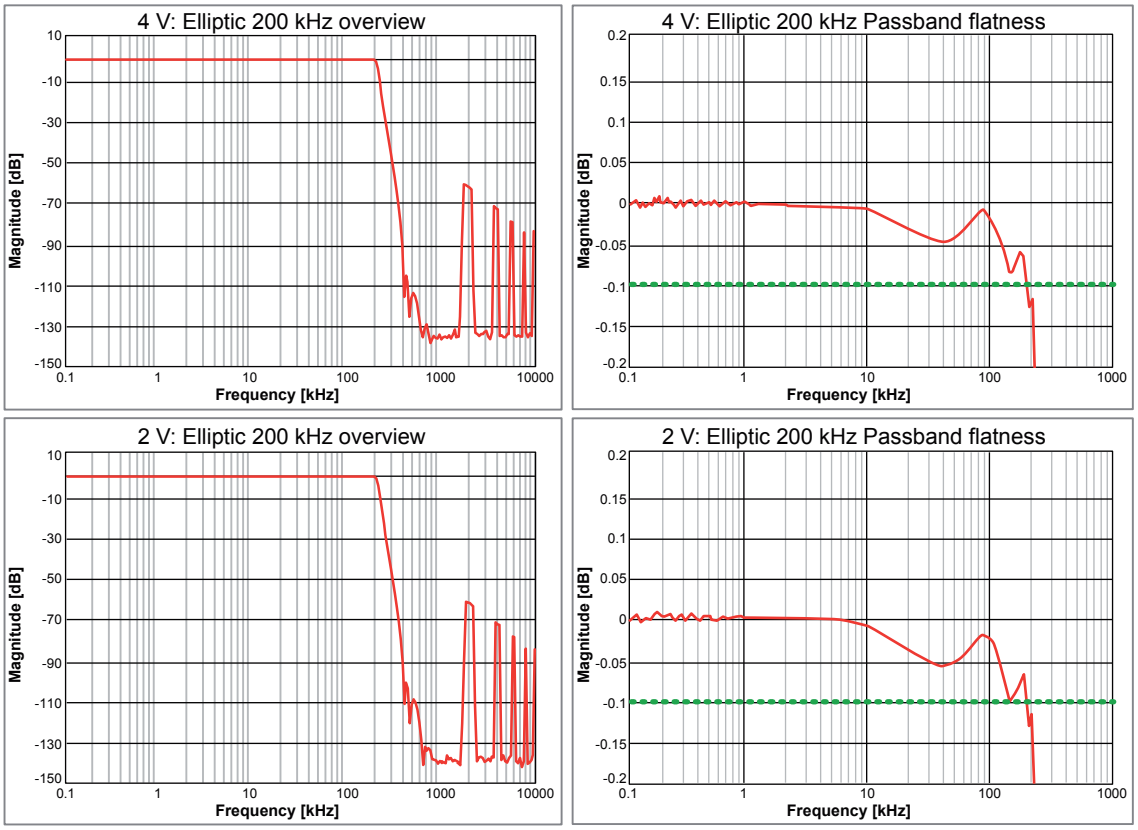


Figure A.67: Representative Elliptic IIR examples

(1) Division by 4 not possible for the 2 MS/s sample rate

(2) Measured using a Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match

Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths results in phase mismatches between channels.

Wideband	100 kHz Sine wave	800 kHz Sine wave
Channels on card	0.5 deg (14 ns)	2.0 deg (7 ns)
GN815 Channels within mainframe	0.5 deg (14 ns)	2.0 deg (7 ns)
Bessel IIR, Filter frequency 200 kHz @ 2 MS/s		
Channels on card	0.5 deg (14 ns)	
GN815 Channels within mainframe	0.5 deg (14 ns)	
Butterworth IIR, Filter frequency 200 kHz @ 2 MS/s		
Channels on card	0.5 deg (14 ns)	
GN815 Channels within mainframe	0.5 deg (14 ns)	
Elliptic IIR, Filter frequency 200 kHz @ 2 MS/s		
Channels on card	0.5 deg (14 ns)	
GN815 Channels within mainframe	0.5 deg (14 ns)	
GN815 channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)	

Channel to Channel Crosstalk

Channel to channel crosstalk is measured with a 50 Ω termination resistor on the input and uses sine wave signals on the channel above and below the channel being tested. To test Channel 2, Channel 2 is terminated with 50 Ω, while Channels 1 and 3 are connected to the sine wave generator.

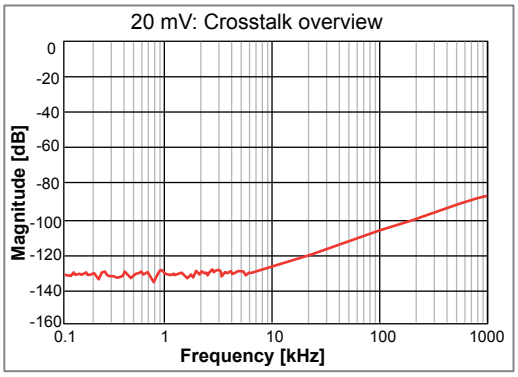


Figure A.68: Representative crosstalk overview

On-board Memory

Per card	2 GB (1 GS @ 16 bits, 500 MS @ 18 bits storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	User selectable 16 or 18 bits 16 bits, 2 bytes/sample 18 bits, 4 bytes/sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

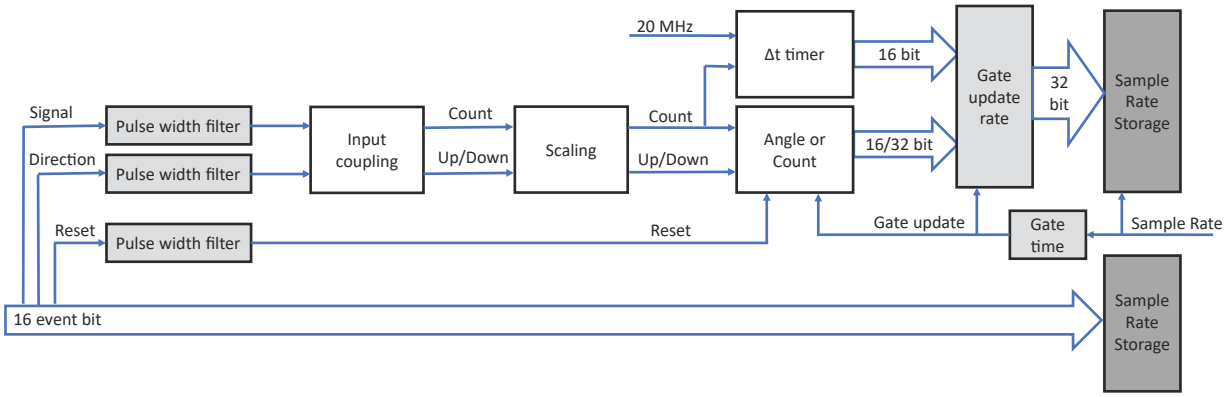


Figure A.69: Timer/Counter block diagram

Digital input events	16 per card			
Levels	TTL input level, user programmable invert level			
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs			
Overvoltage protection	± 30 V DC continuously			
Minimum pulse width	100 ns			
Maximum frequency	5 MHz			
Digital output events	2 per card			
Levels	TTL output levels, short circuit protected			
Output event 1	User selectable: Trigger, Alarm, set High or Low			
Output event 2	User selectable: Recording active, set High or Low			
Digital output event user selections				
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay			
Alarm	High when alarm condition of card is activated, low when not activated 200 µs ± 1 µs ± 1 sample period alarm event delay			
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns			
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation			
Timer/Counter	2 per card			
Levels	TTL input levels			
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs			
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)			
Measurement modes	Count (C) Angle (0 to 360 degrees) Frequency (Δcount / Δt) RPM (Δcount / Δt / 60 s)			
Δt timer measurement accuracy	50 ns (20 MHz)			
Gate time	1 to n samples (User selectable maximum Δt)			
Gate time and reading update rate	Gate time sets the maximum update rate of the measurement values			
Gate time and minimum frequency	Minimum measured frequency or RPM = 1 / gate time			
Gate time and frequency accuracy	Accuracy = 50 ns / gate time			
Gate time impact	**Gate time**	**1 us**	**10 us**	**100 us**
	Δt Error	5%	0.5%	0.05%
	Update rate	1 MS/s	100 kS/s	10 kS/s
RT-FDB options	RT-FDB timer based average enables the same gate time effect. RT-FDB cycle detect average enables a dynamic gate time effect.			

Input Coupling Uni- and Bi-directional

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

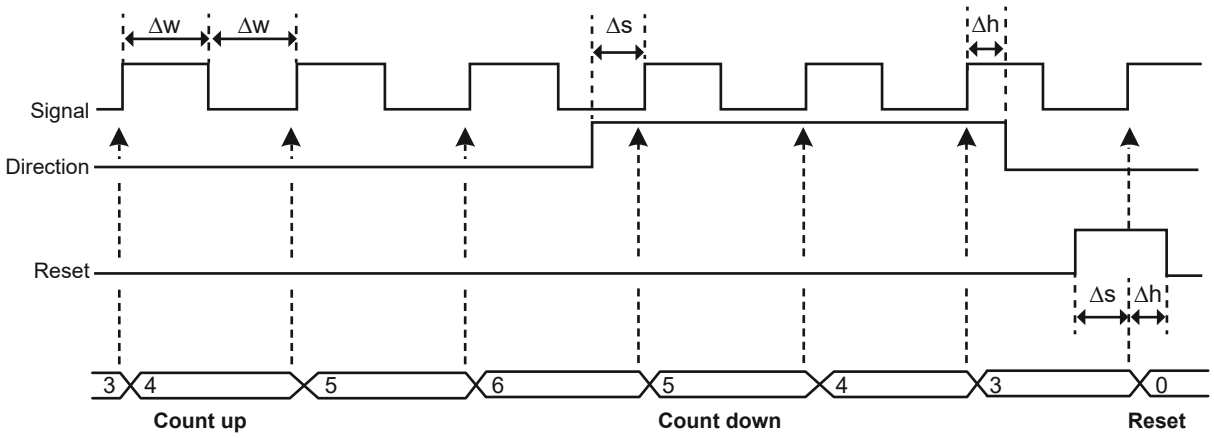


Figure A.70: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Maximum input signal frequency	5 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

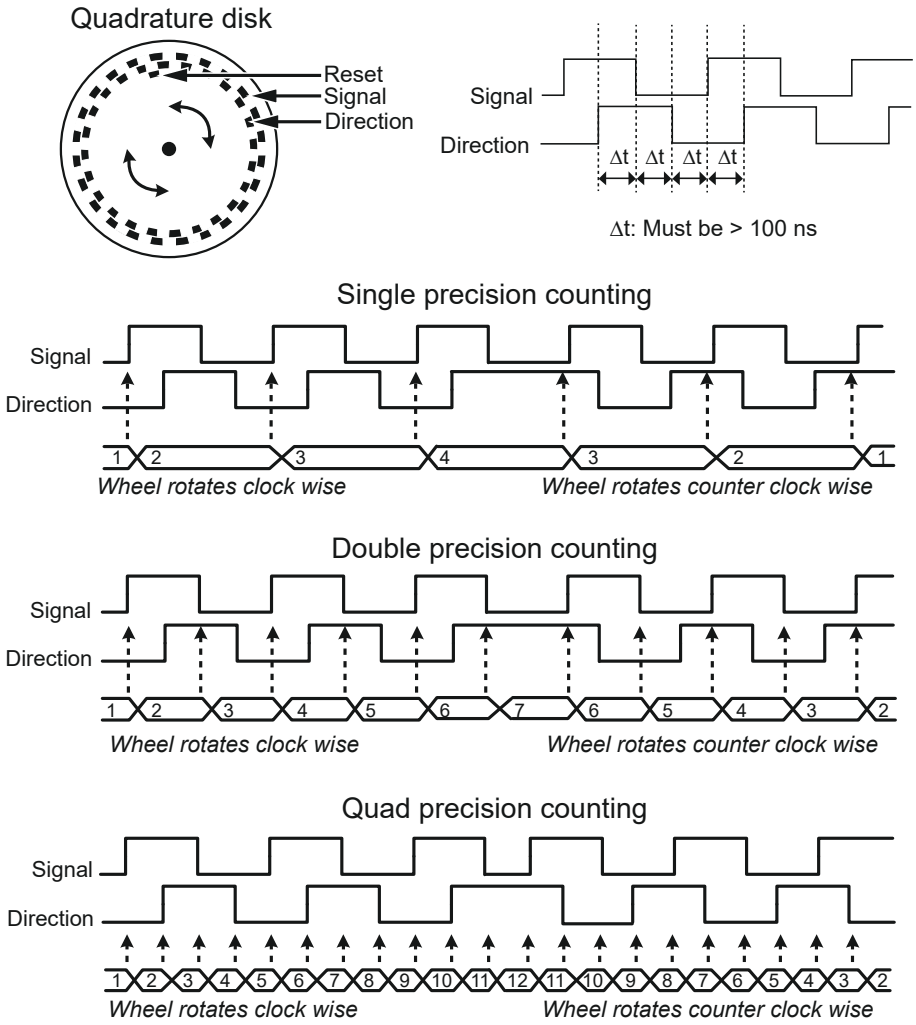


Figure A.71: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Uni-and Bi-directional Count	
Counter mode is typically used for tracking movement of device under test. When possible use the quadrature modes as these are less sensitive to counting errors.	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31} - 1$; bi-directional count

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period (identical for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (10 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (9.76 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516 (504) µs for decimal (binary) time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators

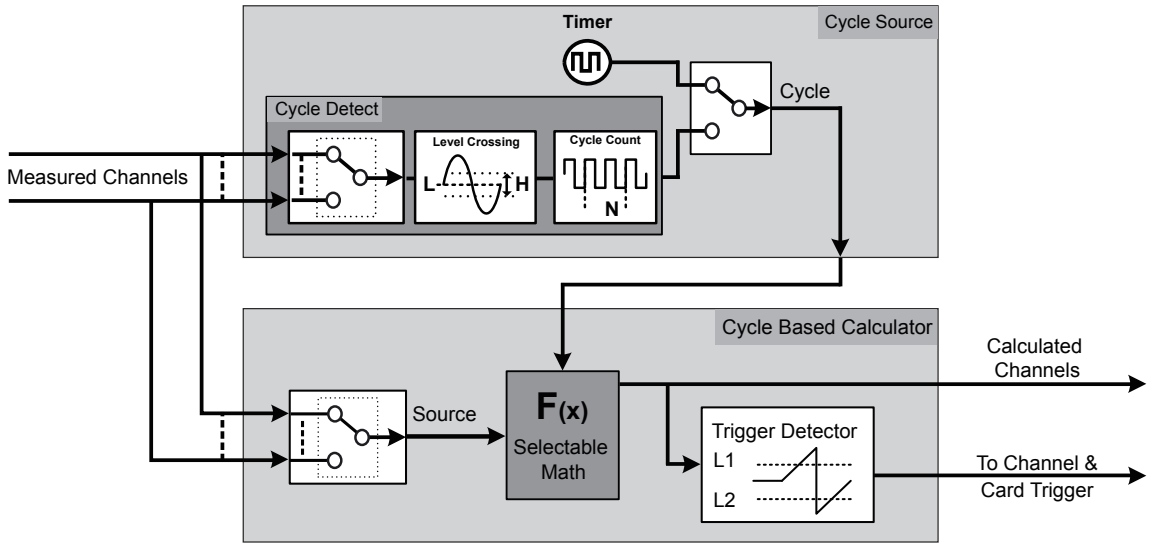


Figure A.72: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased.
Cycle based calculator	
Number of calculators	32; at sample rates 200 kS/s or lower. At higher sample rates, the number of calculators is reduced to match the available DSP power.
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software.
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and Crest Factor
Timer/Counter channel calculations	Frequency (to enable triggering). RPM of Angle.
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period.
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level.
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms.

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Acquisition Modes

Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Acquisition Mode Details

16 Bit Resolution

Recording Mode	Single Sweep Multiple Sweeps			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	8 Ch	8 Ch & events	1 Ch	8 Ch	8 Ch & events	1 Ch	8 Ch	8 Ch & events
Max. sweep memory	954 MS	119 MS	106 MS	not used			762 MS	95 MS	84 MS
Max. sweep sample rate	2 MS/s			not used			2 MS/s		
Max. continuous FIFO	not used			954 MS	119 MS	106 MS	190 MS	23 MS	21 MS
Max. continuous sample rate	not used			2 MS/s			Sweep sample rate / 2		
Max. continuous streaming rate	not used			2 MS/s 4 MB/s	16 MS/s 32 MB/s	18 MS/s 36 MB/s	1 MS/s 2 MB/s	8 MS/s 16 MB/s	9 MS/s 18 MB/s

18 Bit Resolution

Recording Mode	Single Sweep Multiple Sweeps			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	8 Ch	8 Ch & events & Timer/ Counter	1 Ch	8 Ch	8 Ch & events & Timer/ Counter	1 Ch	8 Ch	8 Ch & events & Timer/ Counter
Max. sweep memory	477 MS	59 MS	43 MS	not used			381 MS	47 MS	34 MS
Max. sweep sample rate	2 MS/s			not used			2 MS/s		
Max. continuous FIFO	not used			477 MS	59 MS	43 MS	95 MS	11 MS	8 MS
Max. continuous sample rate	not used			2 MS/s			Sweep sample rate / 2		
Max. aggregate continuous streaming rate	not used			2 MS/s 8 MB/s	16 MS/s 64 MB/s	22 MS/s 88 MB/s	1 MS/s 4 MB/s	8 MS/s 32 MB/s	11 MS/s 44 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 10 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.5 B03998_02_E00_00 (GEN series GN816)

Capabilities Overview	
Model	GN816
Maximum sample rate per channel	200 kS/s
Memory per card	200 MB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	18 bit
Isolation	Channel to channel and channel to chassis
Input type	Analog, isolated, unbalanced differential
Passive voltage/current probes	Passive, singled-ended voltage probes
Sensors	IEPE
TEDS	Class 1, IEPE sensors
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Not supported
Real-time calculated results output	Not supported
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels
Standard data streaming (CPCI up to 200 MB/s)	Supported
Fast data streaming (PCIe up to 1 GB/s)	Supported
Slot width	1

Supported Sensors and Probes		
Perception input type	**Sensor/probe types**	**Remarks**
Basic voltage	Single ended voltage input Passive single ended probes Active differential probes Current probes External current burdens	Isolated BNC input
Basic sensor	Not supported	
Bridge	Not supported	
Charge	Not supported	
IEPE	IEPE vibration sensors ICP® Accelerometers 2, 4, 6 or 8 mA @ ≥ 23 V	TEDS class I Automatic sensor connected, open or shorted diagnostics Isolated input
Current loop	Not supported	
Thermocouple	Not supported	
Resistance thermometers	Not supported	

Block Diagram

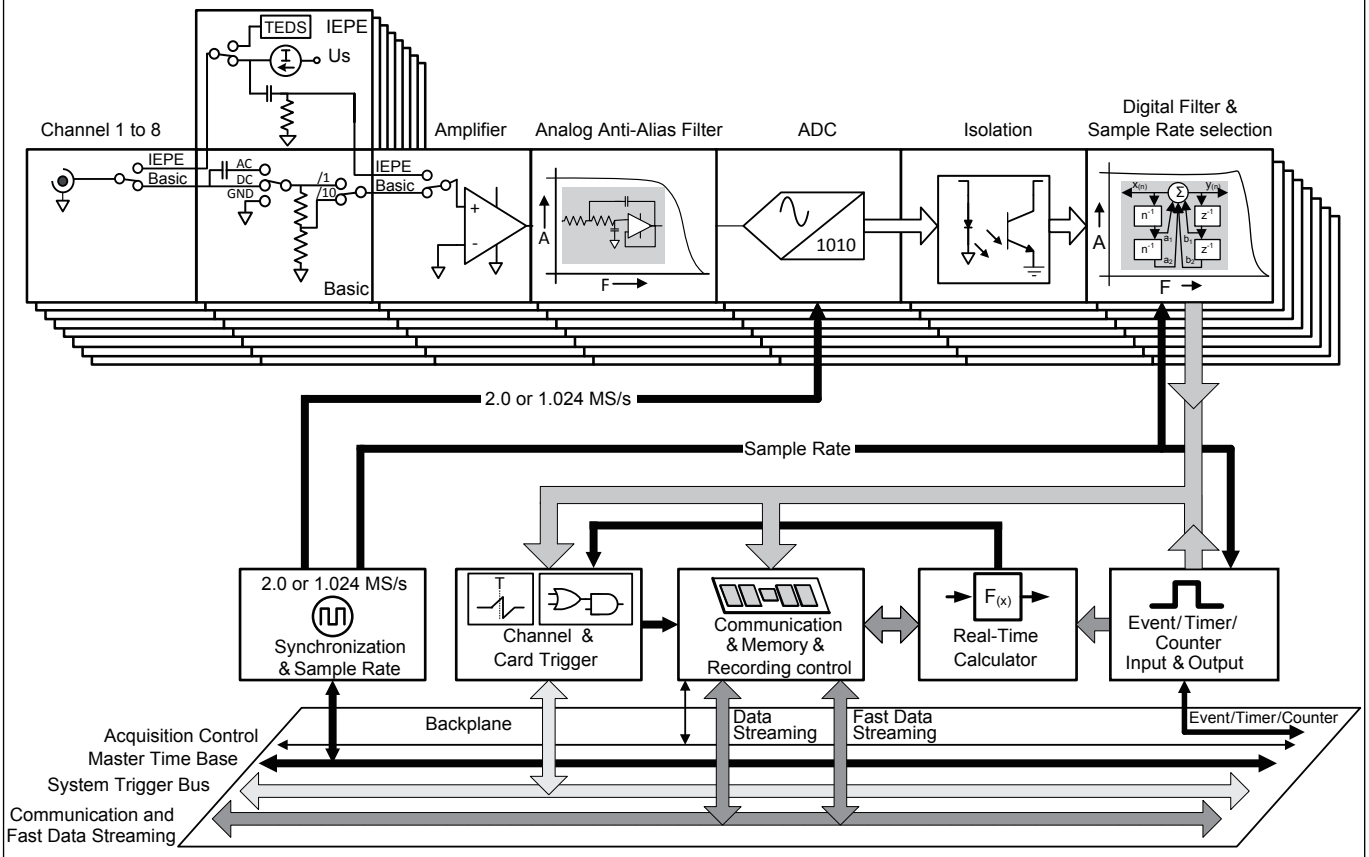


Figure A.73: Block Diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.

If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.

Recalibration after configuration changes is therefore highly recommended.

Analog Input Section		
Channels	8	
Connectors	Isolated metal BNC	
Input type	Analog, isolated, unbalanced differential	
Input impedance	1 MΩ ± 1% // 58 pF ± 10% ranges larger than ± 1 V. All other ranges 66 pF ± 10%	
Input coupling		
Coupling modes	AC, DC, GND	
AC coupling frequency	1.6 Hz ± 10%; - 3 dB	

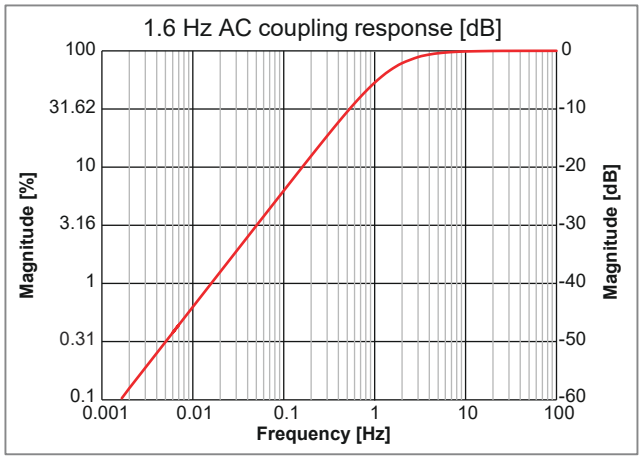


Figure A.74: Representative AC coupling response

Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V, ± 50 V	
Offset	± 50% in 1000 steps (0.1%); ± 50 V range has fixed 0% offset	
Common mode (referred to system ground)		
Ranges	Less than ± 2 V	Larger than or equal to ± 2 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	33 V RMS	33 V RMS

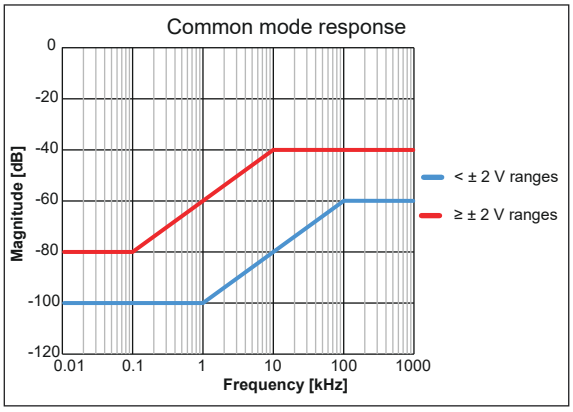


Figure A.75: Representative common mode response

Input overload protection	
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage remains less than 200% of the selected input range or 70 V, whichever value is the smallest.
Maximum nondestructive voltage	± 70 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

Voltage Specifications (Filters Used)		
	Typical	**Guaranteed**
DC gain error	Not available	0.035% of Full Scale ± 35 µV
DC Offset error	Not available	0.01% of Full Scale ± 35 µV
RMS Noise (50 Ω terminated)	Not available	0.015% of Full Scale ± 20 µV
Gain error drift	Not available	± 25 ppm/°C (± 14 ppm/°F)
Offset error drift	Not available	±(45 ppm + 5 µV)/°C (±(25 ppm + 3 µV)/°F)

IEPE Sensor	
Input ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Overvoltage protection	- 1 V to 22 V
IEPE gain error	0.1% ± 250 µV
IEPE gain error drift	± 25 ppm/°C (± 14 ppm/°F)
IEPE compliance voltage	≥ 23 V
Excitation current	2, 4, 6, 8 mA, software selectable
Excitation current accuracy	± 5%
Coupling time constant	1.5 s
Lower bandwidth	-3 dB @ 0.11 Hz
Maximum cable length	100 m (RG-58)
TEDS support	Yes; class 1
Sensor diagnostics	Sensor connected, open or shorted
Supported sensors	IEPE vibration sensors ICP® Accelerometers

Isolation

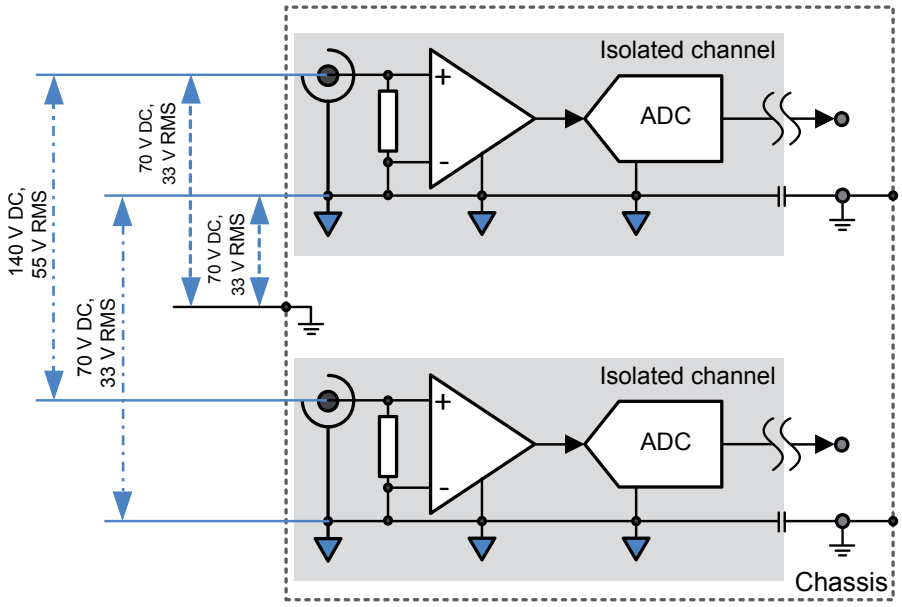


Figure A.76: Isolation schematic

Channel to chassis (earth)	33 V RMS, ± 70 V DC
Channel to channel (Isolated GND to isolated GND)	33 V RMS, ± 70 V DC
Input signal-to-input signal	55 V RMS, ± 140 V DC

Analog to Digital Conversion	
Sample rate; per channel	0.1 S/s to 200 kS/s
ADC resolution; one ADC per channel	18 bit
ADC type	Successive Approximation Register (SAR); Analog Devices AD7986BCPZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; calculating FFTs results in rounded BIN values
Maximum binary sample rate	204.8 kS/s
External time base frequency	0 S/s to 200 kS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ±30 ppm.

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

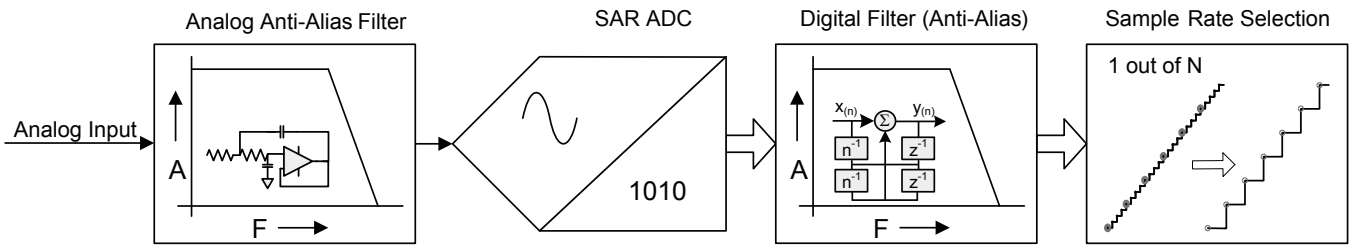
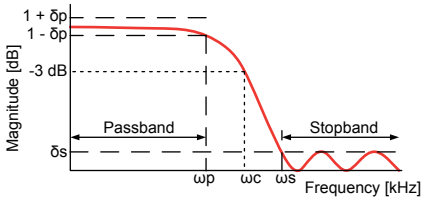


Figure A.77: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Bessel IIR	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.78: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-alias filter bandwidth	390 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	8-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	User selectable from 0.4 Hz to 20 kHz
Bessel IIR 0.1 dB passband (ωp)(1)	DC to 3.5 kHz @ ωc = 20 kHz
Bessel IIR filter stopband attenuation (δs)	75 dB
Bessel IIR filter roll-off	48 dB/octave

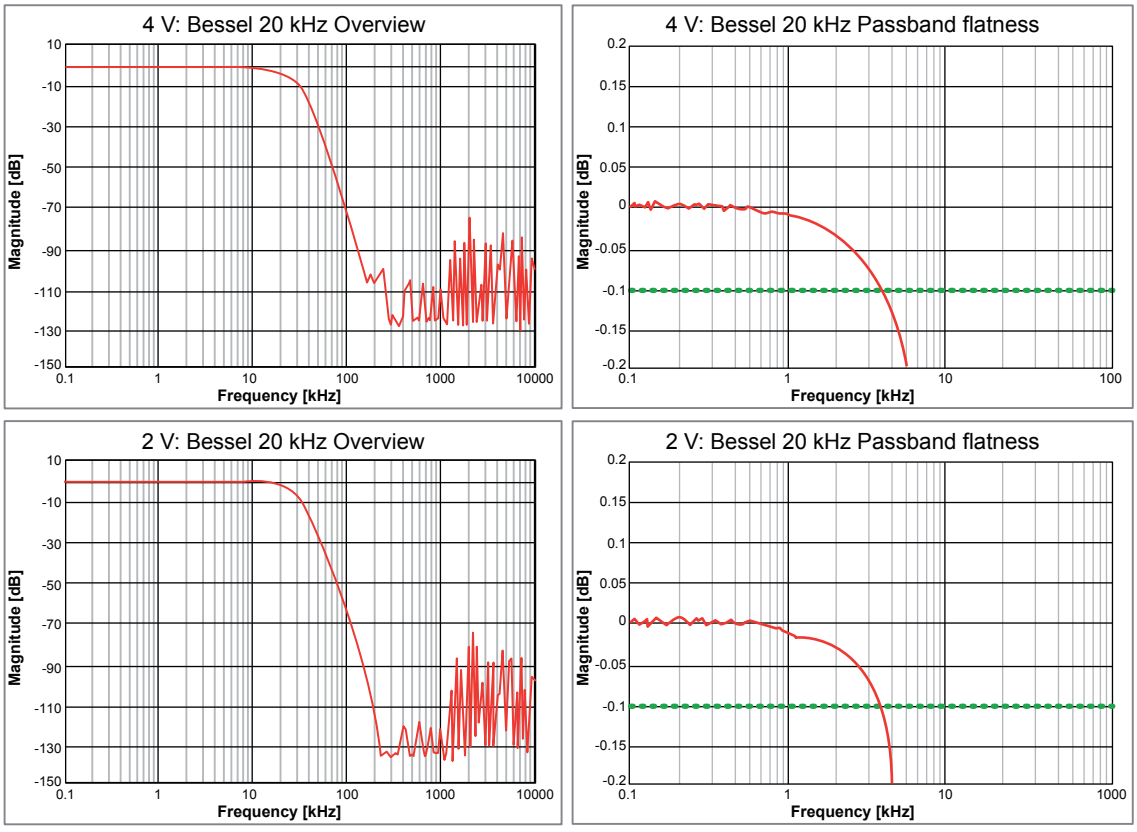
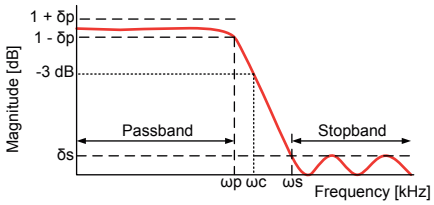


Figure A.79: Representative Bessel IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.80: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter.	
Analog anti-alias filter bandwidth	460 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Butterworth IIR filter characteristic	8-pole Butterworth style IIR
Butterworth IIR filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Butterworth IIR filter bandwidth (ωc)	User selectable from 1 Hz to 50 kHz
Butterworth IIR 0.1 dB passband (ωp)(1)	DC to 35 kHz @ ωc = 50 kHz(1)
Butterworth IIR filter stopband attenuation (δs)	75 dB
Butterworth IIR filter roll-off	48 dB/octave

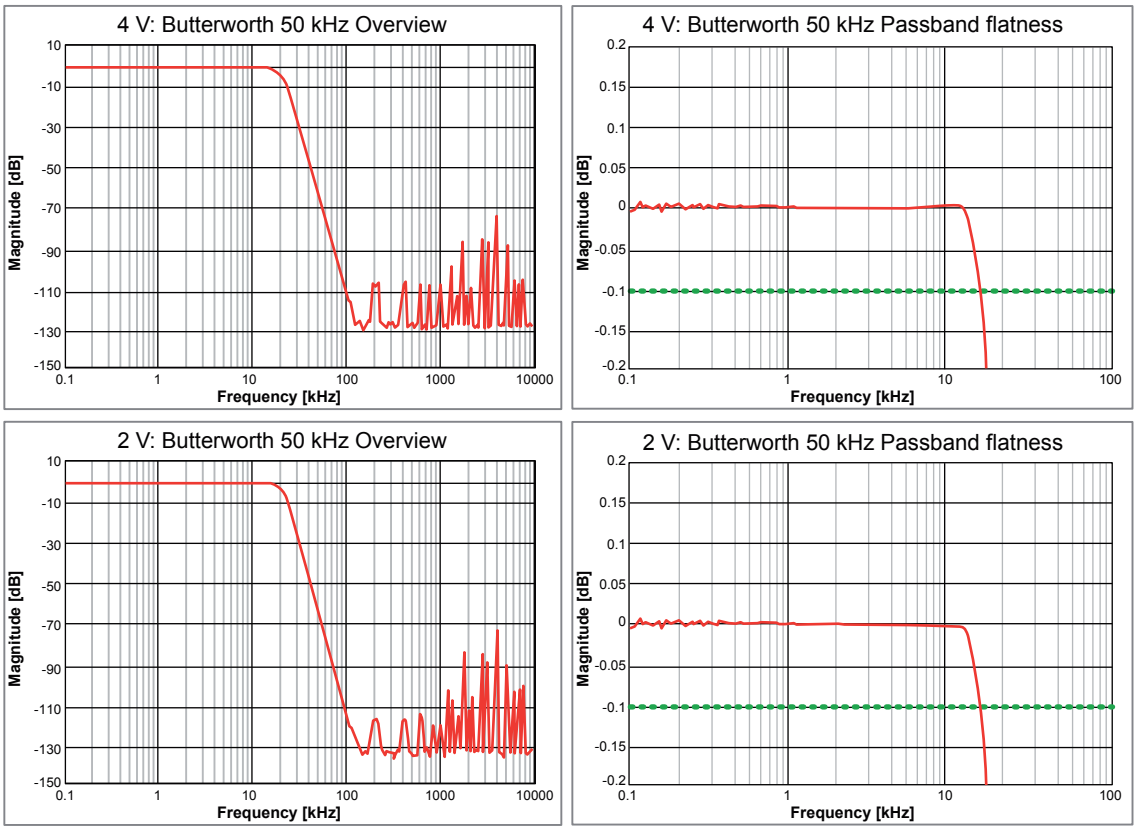
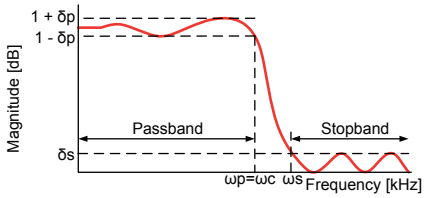


Figure A.81: Representative Butterworth IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.82: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Elliptic IIR filter.

Analog anti-alias filter bandwidth	460 kHz ± 25 kHz (-3 dB)
Analog anti-alias filter characteristic	7-pole Butterworth, extended passband response
Elliptic IIR filter characteristic	7-pole Elliptic style IIR
Elliptic IIR filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Elliptic IIR filter bandwidth (ωc)	User selectable from 1 Hz to 50 kHz
Elliptic IIR 0.1 dB passband (ωp)(1)	DC to ωc
Elliptic IIR filter stopband attenuation (δs)	75 dB
Elliptic IIR filter roll-off	72 dB/octave

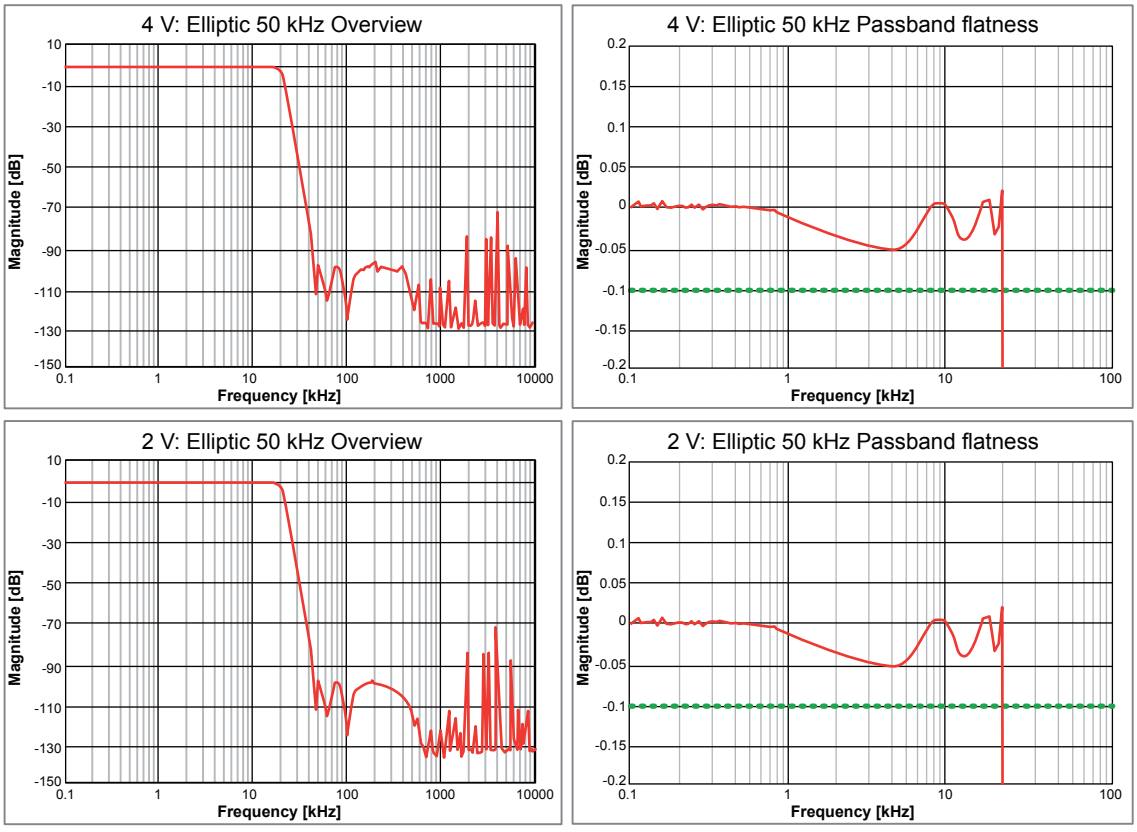


Figure A.83: Representative Elliptic IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths results in phase mismatches between channels.	
Bessel IIR, Filter frequency 20 kHz @ 200 kS/s; 10 kHz Sine wave	
Channels on card	0.5 deg (0.14 µs)
GN816 Channels within mainframe	0.5 deg (0.14 µs)
Butterworth IIR, Filter frequency 20 kHz @ 200 kS/s; 10 kHz Sine wave	
Channels on card	0.5 deg (0.14 µs)
GN816 Channels within mainframe	0.5 deg (0.14 µs)
Elliptic IIR, Filter frequency 20 kHz @ 200 kS/s; 10 kHz Sine wave	
Channels on card	0.5 deg (0.14 µs)
GN816 Channels within mainframe	0.5 deg (0.14 µs)
GN816 channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

Channel to Channel Crosstalk

Channel to channel crosstalk is measured with a 50 Ω termination resistor on the input and uses sine wave signals on the channel above and below the channel being tested. To test Channel 2, Channel 2 is terminated with 50 Ω, while Channels 1 and 3 are connected to the sine wave generator.

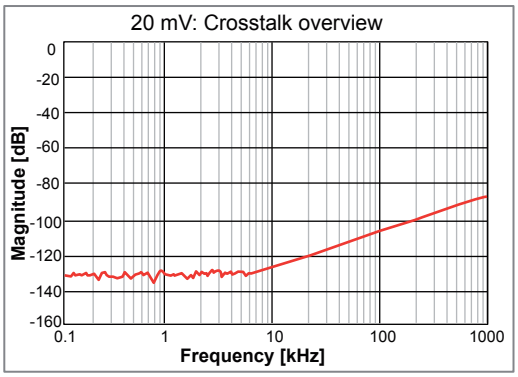


Figure A.84: Representative crosstalk overview

On-board Memory	
Per card	200 MB (100 MS @ 16 bits storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	User selectable 16 or 18 bits 16 bits, 2 bytes/sample 18 bits, 4 bytes/sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

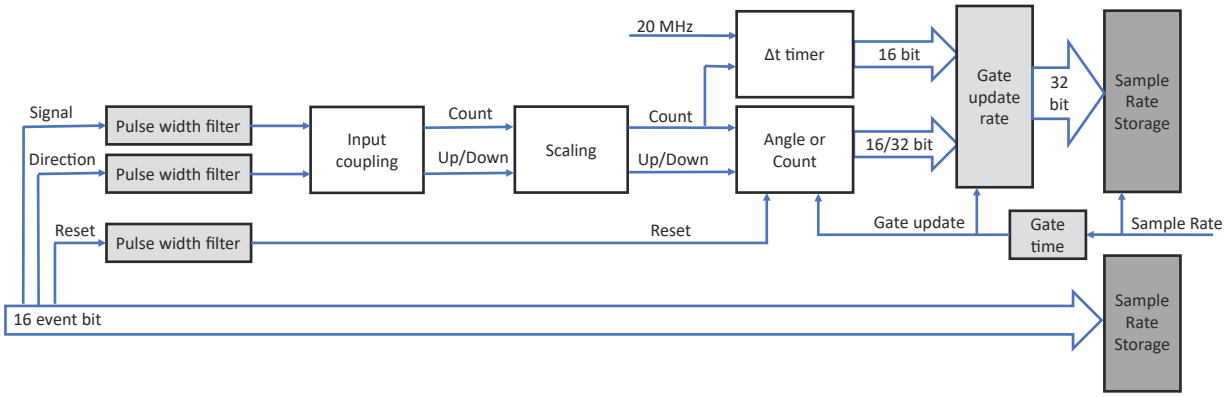


Figure A.85: Timer/Counter block diagram

Digital input events	16 per card			
Levels	TTL input level, user programmable invert level			
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs			
Overvoltage protection	± 30 V DC continuously			
Minimum pulse width	100 ns			
Maximum frequency	5 MHz			
Digital output events	2 per card			
Levels	TTL output levels, short circuit protected			
Output event 1	User selectable: Trigger, Alarm, set High or Low			
Output event 2	User selectable: Recording active, set High or Low			
Digital output event user selections				
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay			
Alarm	High when alarm condition of card is activated, low when not activated 200 µs ± 1 µs ± 1 sample period alarm event delay			
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns			
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation			
Timer/Counter	2 per card			
Levels	TTL input levels			
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs			
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)			
Measurement modes	Count (C) Angle (0 to 360 degrees) Frequency (Δcount / Δt) RPM (Δcount / Δt / 60 s)			
Δt timer measurement accuracy	50 ns (20 MHz)			
Gate time	1 to n samples (User selectable maximum Δt)			
Gate time and reading update rate	Gate time sets the maximum update rate of the measurement values			
Gate time and minimum frequency	Minimum measured frequency or RPM = 1 / gate time			
Gate time and frequency accuracy	Accuracy = 50 ns / gate time			
Gate time impact	**Gate time**	**1 us**	**10 us**	**100 us**
	Δt Error	5%	0.5%	0.05%
	Update rate	1 MS/s	100 kS/s	10 kS/s
RT-FDB options	RT-FDB timer based average enables the same gate time effect. RT-FDB cycle detect average enables a dynamic gate time effect.			

Input Coupling Uni- and Bi-directional Signal

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

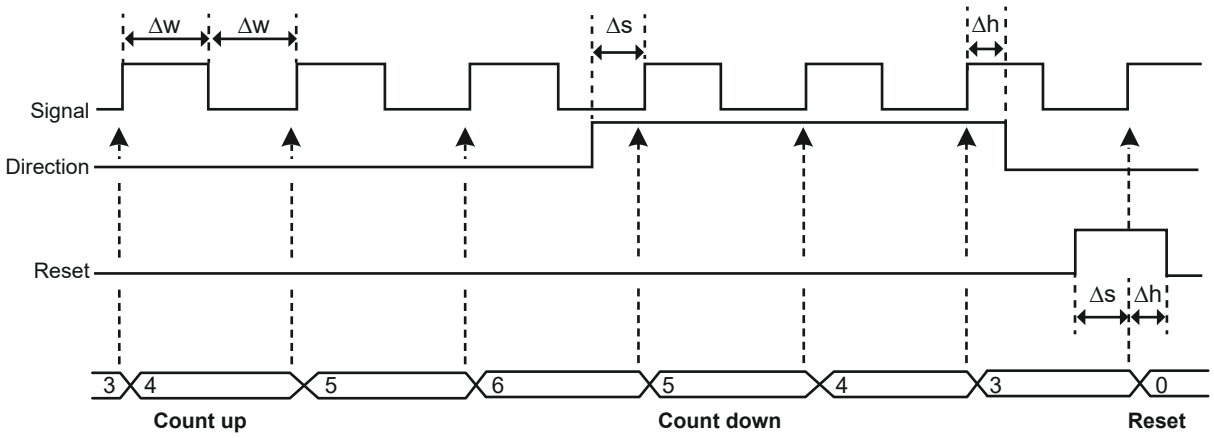


Figure A.86: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	4 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

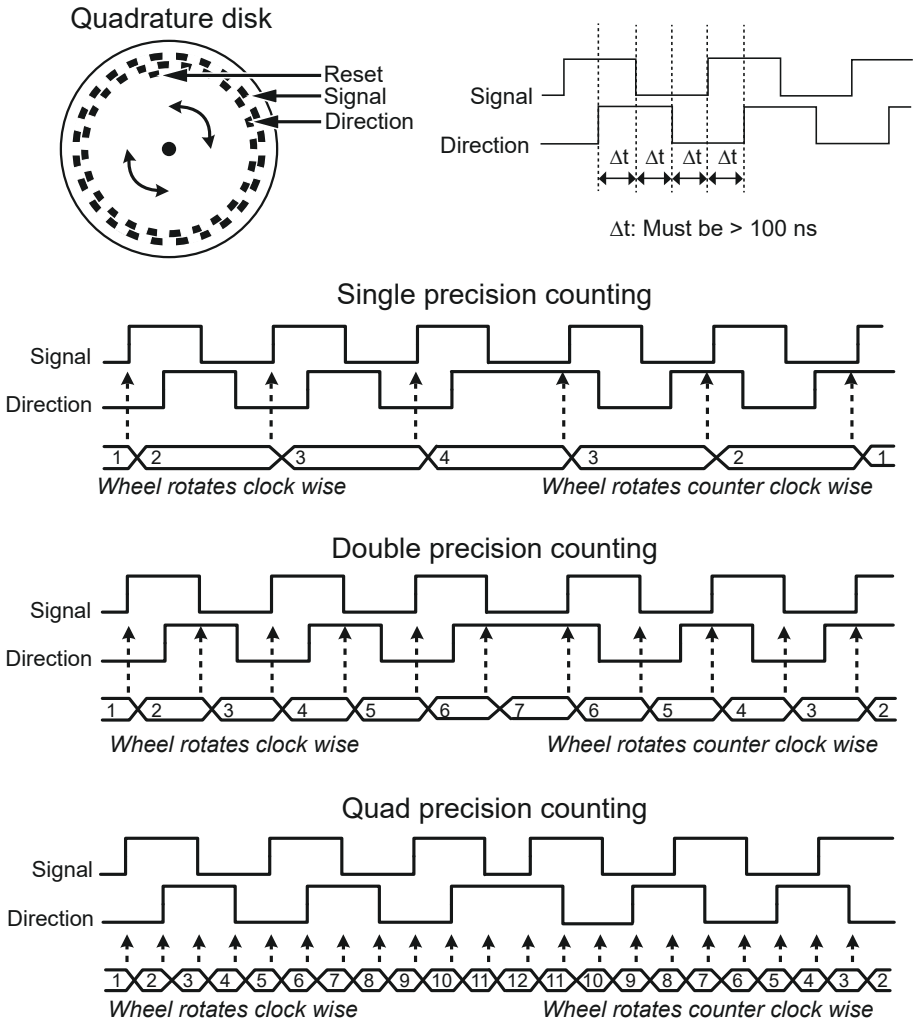


Figure A.87: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Count/Position	
Count/position mode is typically used for tracking movement of device under test. To reduce the sensitivity for count/position errors due to clock glitches use the minimum pulse width filter or enable the ABZ in stead of uni-/bi-polar input coupling .	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31}$ - 1; bi-directional count

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period (identical for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (10 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (9.76 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516 (504) µs for decimal (binary) time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators (Perception V6.72 and higher)

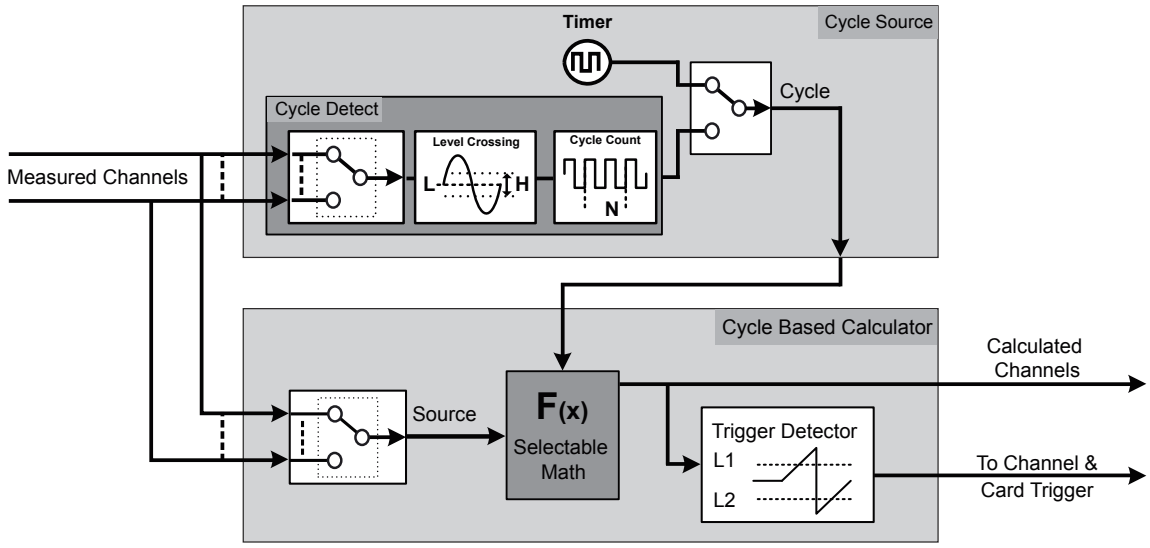


Figure A.88: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased.
Cycle based calculator	
Number of calculators	32
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software.
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and MeanOfMultiplication
Timer/Counter channel calculations	Frequency (to enable triggering). RPM of Angle.
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period.
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level.
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms.

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Acquisition Modes

Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Acquisition Mode Details

16 Bit Resolution

Recording Mode	Single Sweep Multiple Sweeps			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	8 Ch	8 Ch & events	1 Ch	8 Ch	8 Ch & events	1 Ch	8 Ch	8 Ch & events
Max. sweep memory	100 MS	12 MS	10.5 MS	not used			80 MS	9.5 MS	8 MS
Max. sweep sample rate	200 kS/s			not used			200 kS/s		
Max. continuous FIFO	not used			100 MS	12 MS	10.5 MS	20 MS	2 MS	2 MS
Max. continuous sample rate	not used			200 kS/s			Sweep sample rate / 2		
Max. aggregate continuous streaming rate	not used			0.2 MS/s 0.4 MB/s	1.6 MS/s 3.2 MB/s	1.8 MS/s 3.6 MB/s	0.1 MS/s 0.2 MB/s	0.8 MS/s 1.6 MB/s	0.9 MS/s 1.8 MB/s

18 Bit Resolution

Recording Mode	Single Sweep Multiple Sweeps			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	8 Ch	8 Ch & events & Timer/ Counter	1 Ch	8 Ch	8 Ch & events & Timer/ Counter	1 Ch	8 Ch	8 Ch & events & Timer/ Counter
Max. sweep memory	50 MS	6 MS	4 MS	not used			40 MS	4.5 MS	3 MS
Max. sweep sample rate	200 kS/s			not used			200 kS/s		
Max. continuous FIFO	not used			50 MS	6 MS	4 MS	10 MS	1 MS	0.7 MS
Max. continuous sample rate	not used			200 kS/s			Sweep sample rate / 2		
Max. aggregate continuous streaming rate	not used			0.2 MS/s 0.8 MB/s	1.6 MS/s 6.4 MB/s	2.2 MS/s 8.8 MB/s	0.1 MS/s 0.4 MB/s	0.8 MS/s 3.2 MB/s	1.1 MS/s 4.4 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 10 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.6 B04170_02_E00_00 (GEN series GN840B, GN1640B)

Capabilities Overview	
Model	GN840B, GN1640B
Maximum sample rate per channel	500 kS/s
Memory per card	2 GB
Analog channels	8 for GN840B and 16 for GN1640B
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	24 bit
Isolation	33 V RMS, ± 70 V DC, channel to channel and channel to chassis
Input type	Analog isolated balanced differential
Passive voltage/current probes	Active single ended and differential probes
Sensors	Quarter, half and full strain gauges/ bridges. Force, pressure, MEMS-type accelerometers and potentiometric displacement transducers. IEPE, piezoelectric, Pt10, Pt100, Pt500, Pt1000, Pt2000, 4…20 mA sensors Thermocouples types K, J, T, B, E, N, R, S and C
TEDS	Class 1, 2 and Class 3 (pending IEEE acceptance)
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Extensive set of user programmable math routines
Digital Event/Timer/Counter	Supported; 16 digital events and 2 Timer/Counter channels
Standard data streaming (CPCI up to 200 MB/s)	Not supported
Fast data streaming (PCIe up to 1 GB/s)	Supported
Slot width	1 for GN840B 2 for GN1640B

Real-time Calculated Results Output			
	Ethernet GEN DAQ API	EtherCAT®	CAN/CAN FD
Results per block	240	240	240
Result blocks per second	2000	1000	500
Latency	Ethernet dependent	1 ms	CAN bus speed

Mainframe Support

	GEN2tB	GEN3t	GEB7tA	GEN17tA	GEN3i	GEN7i	GEN2i(4)	GEN5i(4)	GEN7t(4)	GEN16t(4)
GN840B/GN1640B	Yes						No			
GEN DAQ API	Yes				Yes(1)		No			
EtherCAT®	No	Yes			No		No			
CAN/CAN FD	Yes	No	Yes(2)	Yes(3)	No		No			

(1) Close Perception to enable GEN DAQ API access.

(2) Early shipments have no access to an USB port. Contact support-edaq-gen@hbm.com for an user installed upgrade.

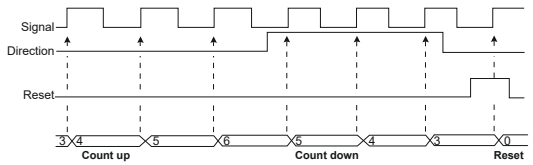
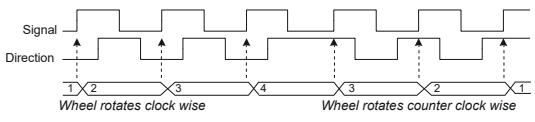
(3) Requires custom system modification.

(4) Mainframe replaced by newer version.

Supported Analog Sensors and Probes

Amplifier mode	Supported analog sensors and probes	Features, Cabling and Accessories
Basic voltage	• Electrical voltages single ended and differential • Active single ended probes • Active differential probes	• ± 1 mV up to ± 10.0 V • Isolated voltage input • 14 pin ODU connector • DIN rail mounted dual BNC breakout 1-G090 • ODU to BNC cable 1-KAB433-2
Basic sensor	• (Damped) Piezoresistive accelerometers • Potentiometric displacement transducers • Voltage output sensors using DC voltage excitation like Force, Pressure, MEMS-type and Kulite sensors	• ± 0.2 mV/V up to ± 500 mV/V • Basic sensor mode is a simplified bridge GUI • Sensor impedance from 17 Ω to 10 kΩ • ± 0.5 V to ± 5.0 V DC sensor supply voltage • DIN rail mounted push-pull breakout 1-G088 • Breakout cable with open ends 1-KAB183-x
Bridge	• Quarter, half and full strain gauges/ bridges • Strain gauge based sensors: load cells, force transducers, torque transducers and pressure transducers	• ± 0.2 mV/V up to ± 500 mV/V • No external support tools required • Bipolar ± 0.5 V to ± 5.0 V DC excitation voltage • 2 * 10 kΩ built in half bridge completion resistors • 120 Ω and 350 Ω built in quarter bridge completion • 3 wire quarter bridge support • Built in 100 kΩ shunt resistor • DIN rail mounted push-pull breakout: 1-G088 • Breakout cable with open ends 1-KAB183-x
Charge	• Piezo-electric sensors	• ± 1 nC up to ± 10 µC • AC input coupled • ODU to BNC cable 1-KAB433-2
IEPE	• IEPE based sensors like accelerometers, microphones and pressure transducers • ICP® Accelerometers	• ± 1 mV up to, ± 10.0 V • IEPE current: 2, 4, 6 or 8 mA @ ≥ 23 V • TEDS class I • Sensor connected, open or shorted diagnostics • DIN rail mounted dual BNC breakout : 1-G090 • ODU to BNC cable 1-KAB433-2
Current loop	• Electrical current 4 to 20 mA • Sensors with to 20 mA output	• Built in burden resistor • DIN rail mounted dual BNC breakout : 1-G090 • ODU to BNC cable 1-KAB433-2
Thermocouple	• Thermocouples types K, J, T, B, E, N, R, S and C	• Digital cold junction compensation • DIN rail mounted cold junction plug: 1-G089 • Thermocouple bandwidth up to 10 kHz
Resistance thermometers	• Resistive Temperature Detectors (RTD) • Pt10, Pt100, Pt500, Pt1000 and Pt2000	• 3 and 4 wire support • DIN rail mounted push-pull breakout : 1-G088 • Breakout cable with open ends 1-KAB183-x

Supported Digital Sensors (TTL Level Input)

Timer counter Input type	Measurement mode	Features
Uni and Bi-directional clock 	• Angle • Frequency / RPM • Count/position	• Count frequency up to 5 MHz • Input signal minimum width setting • Several reset options • RT-FDB can add a calculated Frequency/RPM channel based on the angle measurement
ABZ Incremental Encoder (Quadrature) 	• Angle • Frequency / RPM • Count/position	• Count frequency up to 2 MHz • Single, dual and quad precision count • Input signal minimum width setting • Transition tracking to avoid count drift • Several reset options • RT-FDB can add a calculated Frequency/RPM channel based on the angle measurement

Block Diagram

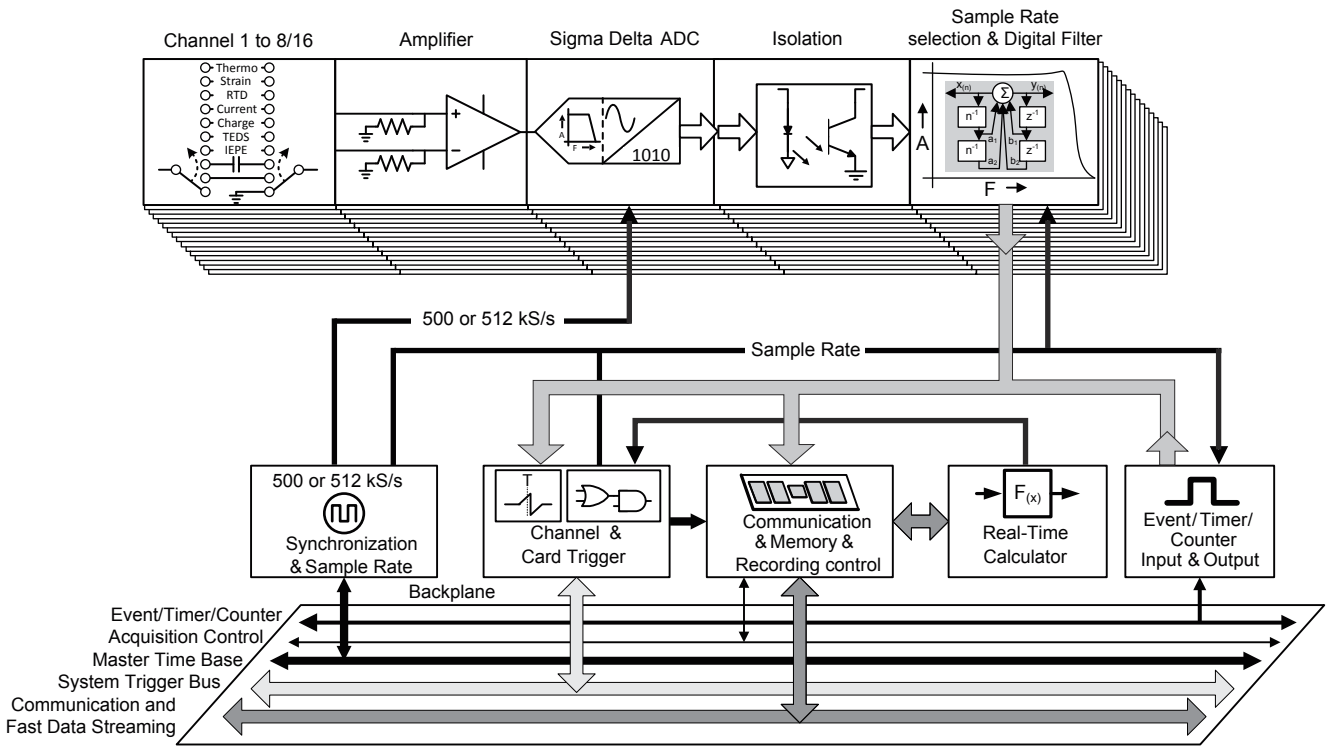


Figure A.89: Block Diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input Section		
Input type	Analog isolated balanced differential	
Impedance	2 * 10 MΩ ± 1% // 45 pF ± 10% (Differential)	
Input coupling	Single-ended positive, single-ended negative and differential	
Signal input coupling		
Coupling modes	AC/DC/GND	
AC coupling frequency	1.6 Hz ± 10%; -3 dB	

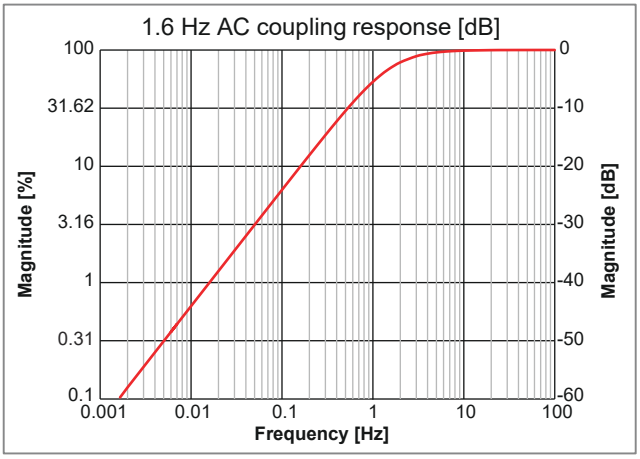


Figure A.90: Representative AC coupling response

Ranges	± 1 mV, ± 10 mV, ± 0.1 V, ± 1.0 V, ± 10.0 V	
Offset	± 50% in 1000 steps (0.1%). For all ranges except ± 10 V range (20 V span).	
Common mode (referred to system ground/earth)		
Ranges	Less than or equal to ± 100m V	Larger than or equal to ± 1 V
Rejection (CMR)	> 100 dB @ 80 Hz (105 dB typical)	> 80 dB @ 80 Hz (95 dB typical)
Maximum common mode voltage	7 V RMS	7 V RMS

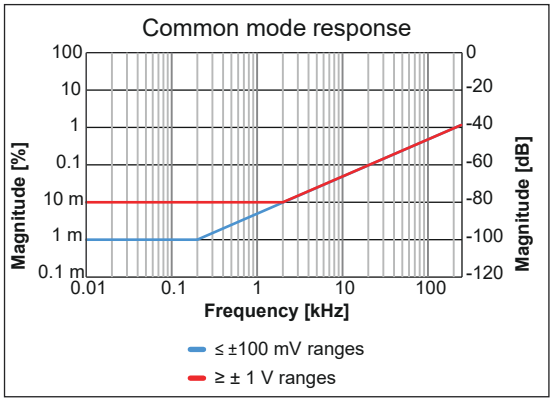
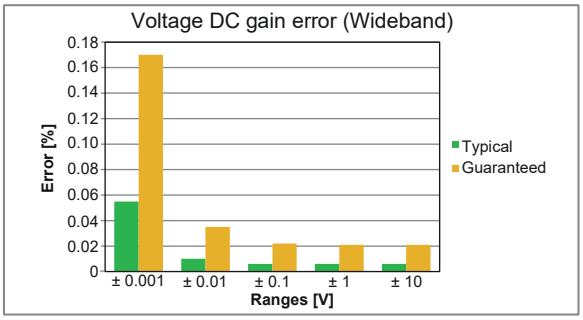


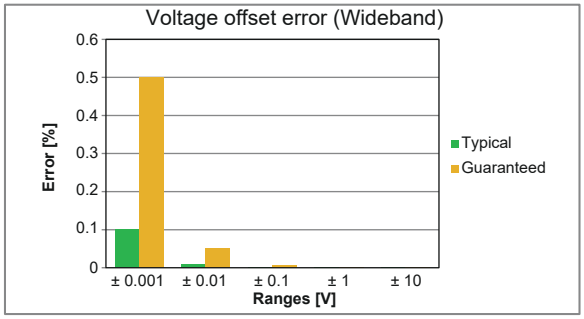
Figure A.91: Representative common mode response

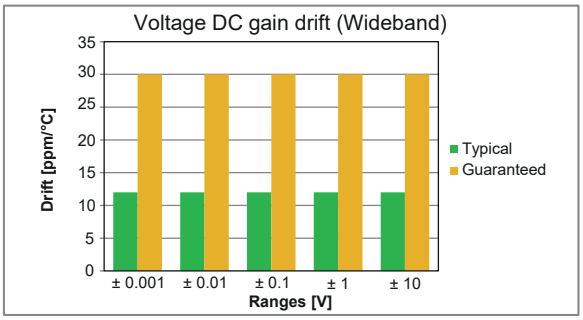
Input overload protection	
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage is between -12 V and +15 V in respect to channel ground.
Maximum nondestructive voltage	± 25 V DC

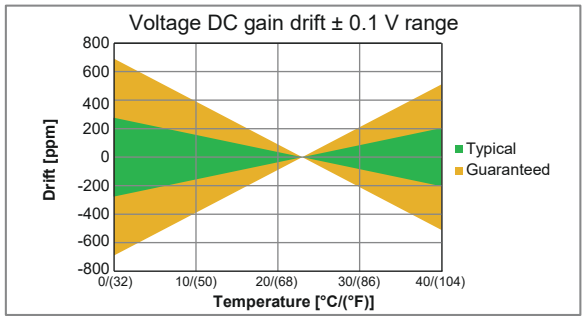
Basic Voltage Specifications

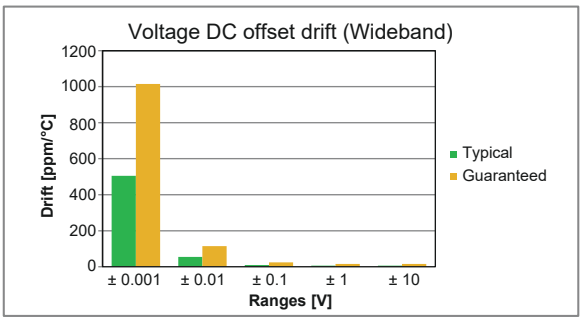
Wideband	Typical	Guaranteed
DC gain error	0.005% of reading ± 1 µV	0.02% of reading ± 3 µV
DC offset error	0.0002% of Full Scale ± 2 µV	0.001% of Full Scale ± 10 µV
DC gain error drift	12 ppm / °C (7 ppm / °F)	30 ppm / °C (17 ppm / °F)
DC offset error drift	± (5 ppm + 1 µV) / °C (± (3 ppm + 1 µV) / °F)	± (15 ppm + 2 µV) / °C (± (9 ppm + 2 µV) / °F)
RMS noise (50 Ω terminated)	0.001% of Full Scale ± 15 µV	0.002% of Full Scale ± 20 µV

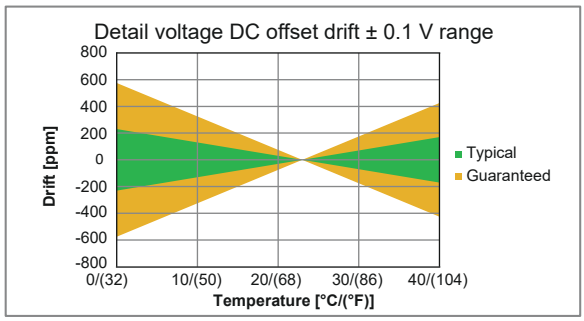












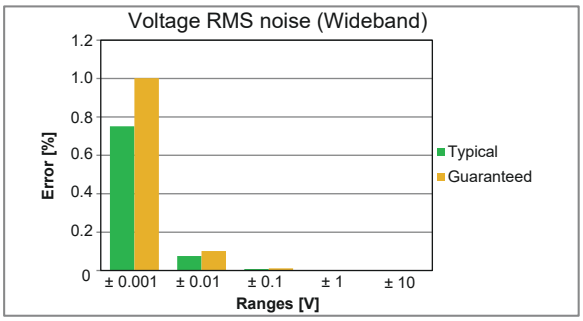


Figure A.92: Wideband voltage specification

Basic Voltage Mode

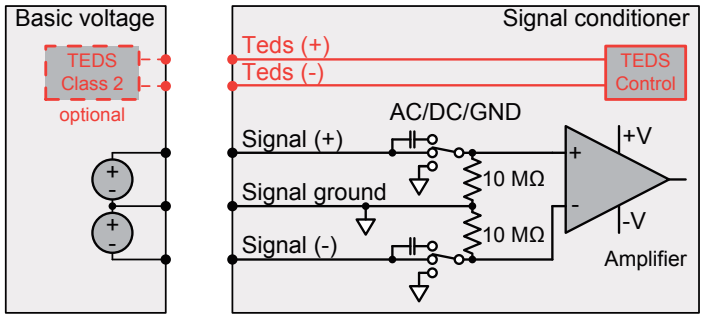


Figure A.93: Basic mode block diagram

Input type	Analog isolated balanced differential
Input coupling	Single-ended positive, single-ended negative and differential
Signal input coupling	
Coupling modes	AC/DC/GND
AC coupling frequency	1.6 Hz, ± 10%; -3 dB
Supported probes	Passive single-ended probes Passive differential probes Active differential probes

Basic Voltage Wiring Diagram

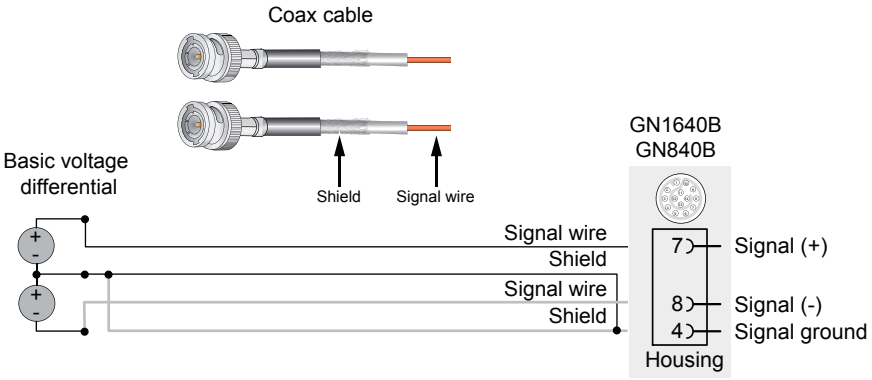


Figure A.94: Recommended basic voltage differential connection

Bridge Mode

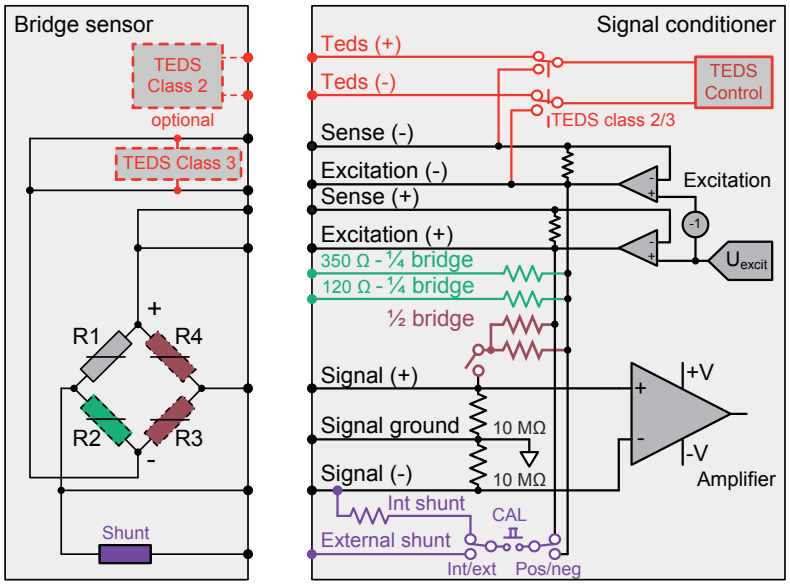


Figure A.95: Bridge mode block diagram

Supported sensors	Quarter, half and full strain gauges/ bridges. Strain gauge based sensors: load cells, force transducers, torque transducers and pressure transducers.			
Quarter bridge connection	Three wire support; the third wire keeps the measurement wire current free eliminating wire resistance errors through the measurement wire			
Built in quarter bridge completion resistor	120 Ω and 350 Ω, 0.1% 2 ppm/°C, wired to separate connector pin			
Built in half bridge completion resistors	2 times 10 kΩ, 0.05% 2 ppm/°C tracking			
Bridge excitation modes	Constant voltage			
Constant voltage excitation				
Excitation voltage inaccuracy	± 0.25%			
Bipolar excitation voltage	**± 0.5 V @ 30 mA**	**± 1 V @ 30 mA**	**± 2 V @ 30 mA**	**± 5 V @ 30 mA**
Transducer impedance	16.7 Ω to 10 kΩ	33.3 Ω to 10 kΩ	66.7 Ω to 10 kΩ	166.7 Ω to 10 kΩ
Measuring ranges (mV/Volt excitation)(1)	± 2 mV/V	± 1 mV/V	± 0.5 mV/V	± 0.2 mV/V
	± 20 mV/V	± 10 mV/V	± 5 mV/V	± 2 mV/V
	± 200 mV/V	± 100 mV/V	± 50 mV/V	± 20 mV/V
			± 500 mV/V	± 200 mV/V
Excitation voltage sense	2 separate connector pins available, wiring required (no internal bypass)			
Maximum cable length	100 m (328 ft), cable impedance ≤ 0.2 Ω/m (0.06 Ω/ ft)			
Bridge balance				
Operation principal	Bridge in-balance measured and software compensated by means of auto zero			
Auto zero	Parallel execution of auto zero on all channels on multiple cards reducing zero time significantly			
Bridge shunt (Sensor quick test)				
Bridge shunt resistor selection	Software selectable 2 sources 1 built-in shunt resistors, or external shunt			
Bridge shunt method	Software selectable to positive or negative excitation voltage			
External shunt	1 separate connector pin to wire shunt out to sensor connection points			
Built-in shunt resistor				
Type	Metal foil			
Shunt resistor	100 kΩ, 0.1% 5 ppm/°C			
TEDS support	Class 2 and 3 (no software support at release date)			

(1) Used amplifier range = mV/V range * Excitation voltage level

Bridge Wiring Diagrams

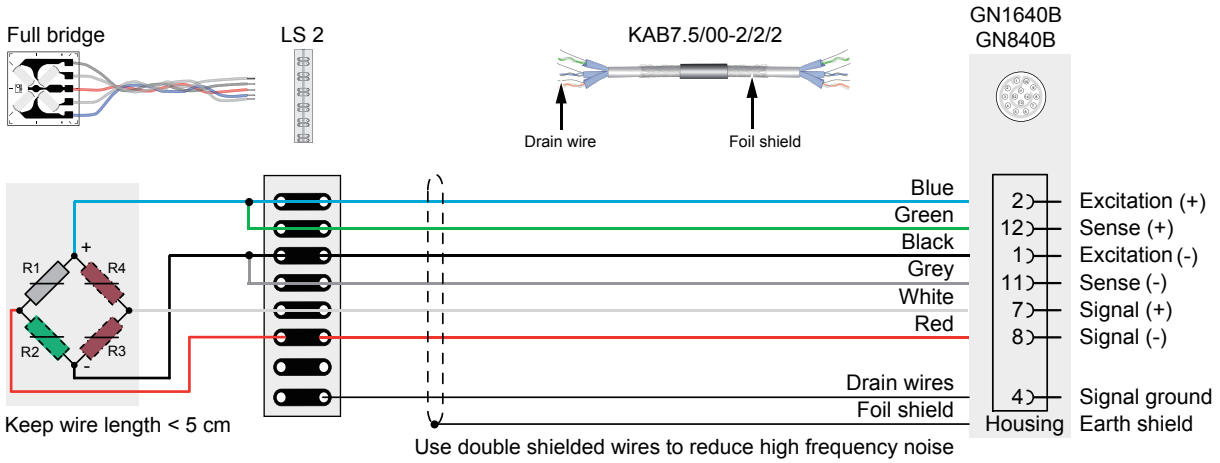


Figure A.96: Recommended 6 wire full bridge connection (more options are available)

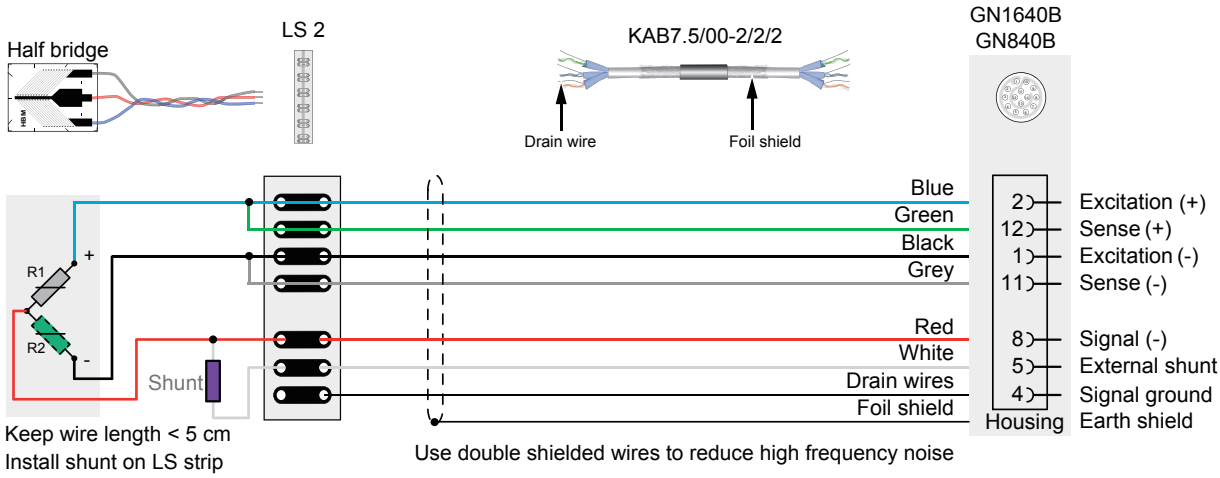


Figure A.97: Recommended 6 wire half bridge with shunt resistor connection (more options are available)

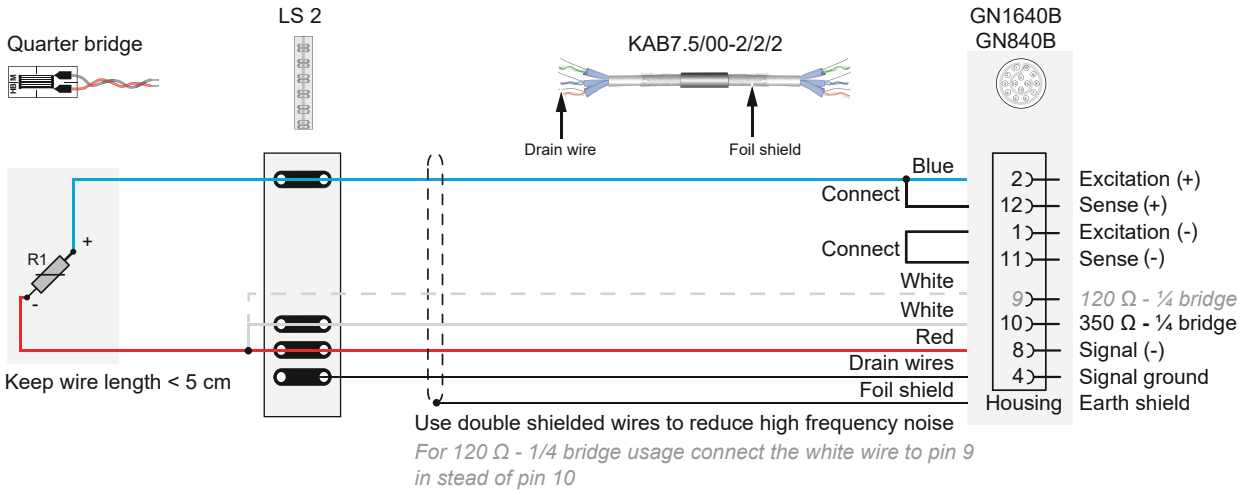


Figure A.98: Recommended 3 wire 350 Ω quarter bridge connection (more options are available)

Basic Sensor Mode

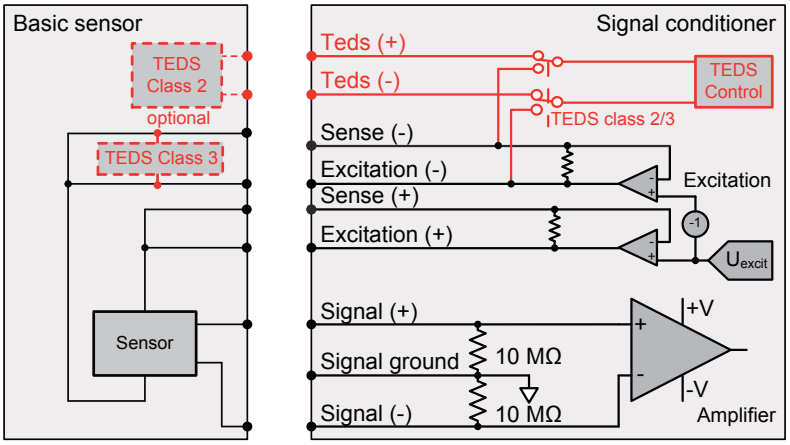


Figure A.99: Basic sensor mode block diagram

Supported sensors	(Damped) Piezoresistive accelerometers Potentiometric Displacement transducers Voltage output sensors using DC voltage excitation like Force, Pressure, MEMS-type and Kulite sensors			
Sensor excitation modes	Constant voltage			
Constant voltage excitation				
Excitation voltage inaccuracy	± 0.25%			
Bipolar excitation voltage	**± 0.5 V @ 30 mA**	**± 1 V @ 30 mA**	**± 2 V @ 30 mA**	**± 5 V @ 30 mA**
Transducer impedance	16.7 Ω to 10 kΩ	33.3 Ω to 10 kΩ	66.7 Ω to 10 kΩ	166.7 Ω to 10 kΩ
Measuring ranges (mV/Volt excitation)(1)	± 2 mV/V	± 1 mV/V	± 0.5 mV/V	± 0.2 mV/V
	± 20 mV/V	± 10 mV/V	± 5 mV/V	± 2 mV/V
	± 200 mV/V	± 100 mV/V	± 50 mV/V	± 20 mV/V
			± 500 mV/V	± 200 mV/V
Excitation voltage sense	2 separate connector pins available, wiring required (no internal bypass)			
Maximum cable length	100 m (328 ft), cable impedance ≤ 0.2 Ω/m (0.06 Ω/ ft)			
TEDS support	Class 2 and 3 (no software support at release date)			

(1) Used amplifier range = mV/V range * Excitation voltage level

Basic Sensor Mode Wire Diagram

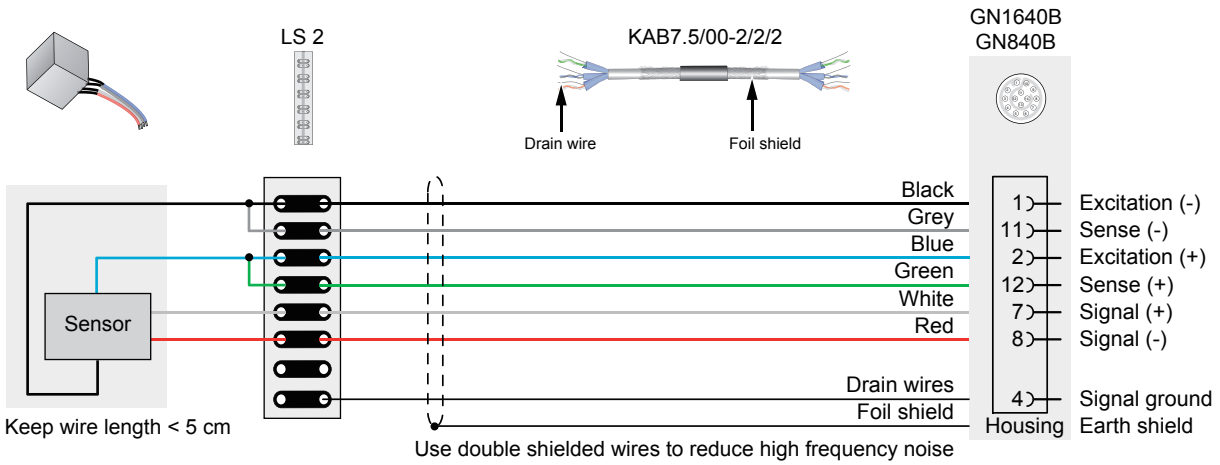


Figure A.100: Recommended 6 wire basic sensor connection (more options are available)

Integrated Electronic PiezoElectric (IEPE)

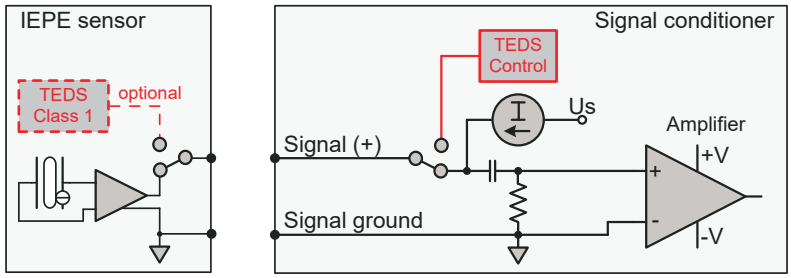


Figure A.101: IEPE mode block diagram

Input ranges	± 1 mV, ± 10 mV, ± 100 mV, ± 1 V, ± 10 V
Over voltage protection	- 15 V to + 26 V
IEPE compliance voltage (Us)	≥ 24 V
IEPE gain error drift	Typical: ± 15 ppm/°C (9 ppm/°F), maximum: ± 35 ppm/°C (20 ppm/°F)
Excitation current (I)	2, 4, 6, 8 mA, software selectable
Excitation current accuracy	± 5%
Coupling time constant	1.5 s
-3 dB high pass bandwidth limit	0.1 Hz ± 20%
Maximum cable length	100 m (RG-58)
Wire diagnostics	Open and shorted IEPE wiring detected
TEDS support	Class 1, including software selectable auto detect the presence of an attached sensor

IEPE Mode Wire Diagram

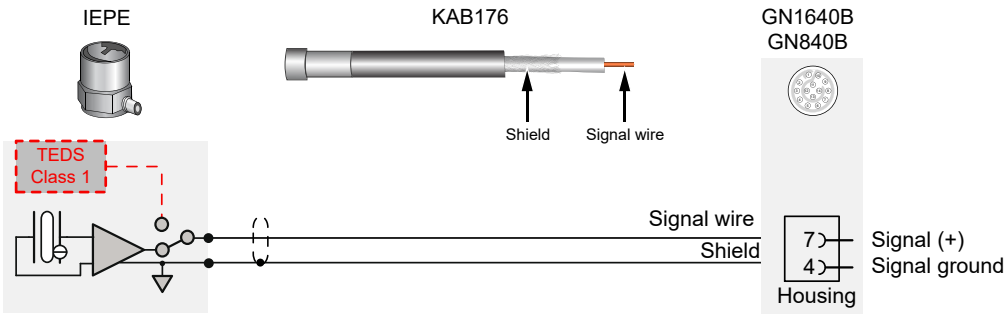


Figure A.102: Recommended IEPE connection

Voltage IEPE Gain

Wideband	Typical	Guaranteed
Voltage IEPE gain error	0.02% of reading ± 5 µV	0.05% of reading ± 20 µV

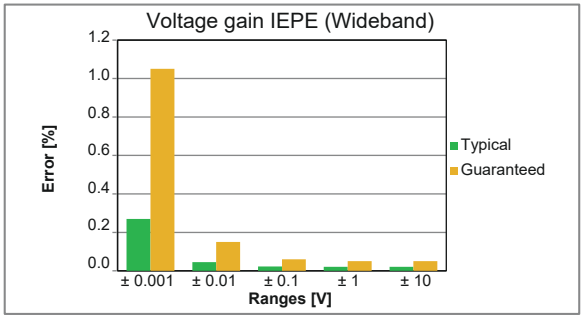


Figure A.103: Wideband IEPE specification

Piezoelectric (Charge) Mode

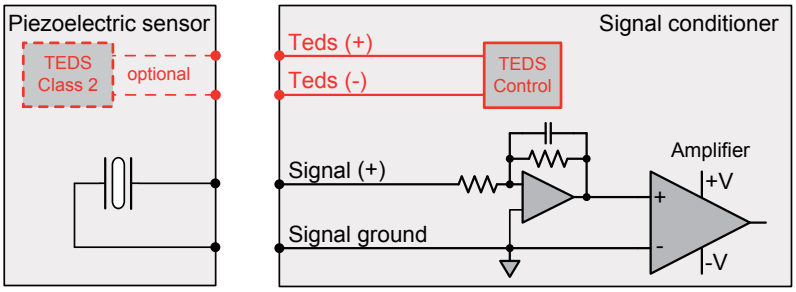


Figure A.104: Piezoelectric mode block diagram

Input ranges	± 1 nC, ± 10 nC, ± 100 nC, ± 1 µC, ± 10 µC
Input coupling	AC coupled only
Over voltage protection	± 25 V
Piezoelectric gain error	Typical: ± 1% of reading Guaranteed: ± 2% of reading
Piezoelectric gain error drift	Typical: ± 20 ppm/°C (± 12 ppm/°F) Guaranteed: ± 65 ppm/°C (± 36 ppm/°F)
-3 dB high pass bandwidth limit	1 Hz ± 20%
-3 dB low pass bandwidth limit	33 kHz ± 10% when a 650 pF source capacity is used 106 kHz ± 10% when a 100 pF source capacity is used
TEDS support	Class 2 (no software support at release date)

Piezoelectric Mode Wire Diagram

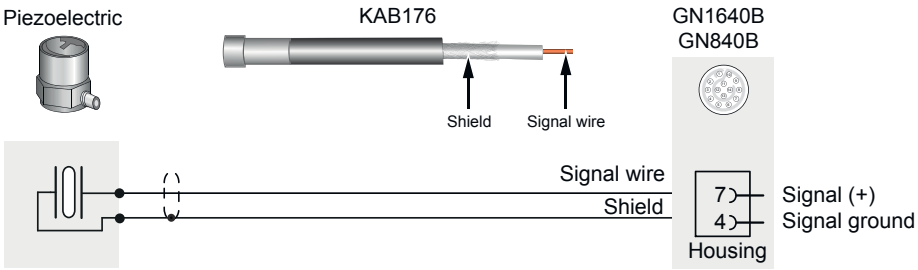


Figure A.105: Recommended piezoelectric connection

Resistive Temperature Detectors (RTD)

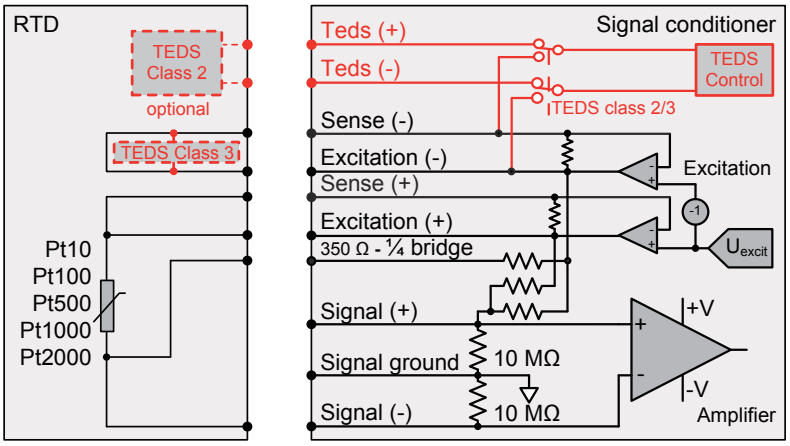


Figure A.106: RTD mode block diagram

Supported sensors	Pt10, Pt100, Pt500, Pt1000 and Pt2000		
Type	3 wire and 4 wire possible		
Inaccuracy	Temperature range	Typical inaccuracy(1)(2)	Guaranteed inaccuracy(1)(2)
Pt10	-200 °C to 0 °C (-328 °F to +32 °F)	± 2.2 °C°C	± 11 °C
	0 °C to +850 °C (+32 °F to +1562 °F)	± (2.2 °C + 0.07% of reading [°C])	± (11 °C + 0.35% of reading [°C])
Pt100	-200 °C to 0 °C (-328 °F to +32 °F)	± 0.25 °C	± 1.1 °C
	0 °C to +850 °C (+32 °F to +1562 °F)	± (0.25 °C + 0.04% of reading [°C])	± (1.1 °C + 0.055% of reading [°C])
Pt500	-200 °C to 0 °C (-328 °F to +32 °F)	± 0.1 °C	± 0.35 °C
	0 °C to +850 °C (+32 °F to +1562 °F)	± (0.1 °C + 0.2% of reading [°C])	± (0.35 °C + 1% of reading [°C])
Pt1000	-200 °C to 0 °C (-328 °F to +32 °F)	± 0.2 °C	± 0.9 °C
	0 °C to +850 °C (+32 °F to +1562 °F)	± (0.2 °C + 0.4% of reading [°C])	± (0.9 °C + 2% of reading [°C])
Pt2000	-200 °C to 0 °C (-328 °F to +32 °F)	± 0.35 °C	± 1.7 °C
	0 °C to +850 °C (+32 °F to +1562 °F)	± (0.35 °C + 0.8% of reading [°C])	± (1.7 °C + 3.9% of reading [°C])
Maximum cable length	100 m		
Measurement range	-200 °C to 850 °C (-328 °F to 1562 °F)		
TEDS support	Class 2 and 3 (no software support at release date)		

(1) Linearization curve IEC 60751 (α=0.00385 Ω/Ω/°C) according the International Temperature Scale of 1990 (ITS-90).

(2) Measured with Meatest M632 precision resistance decade.

RTD Wire Diagram

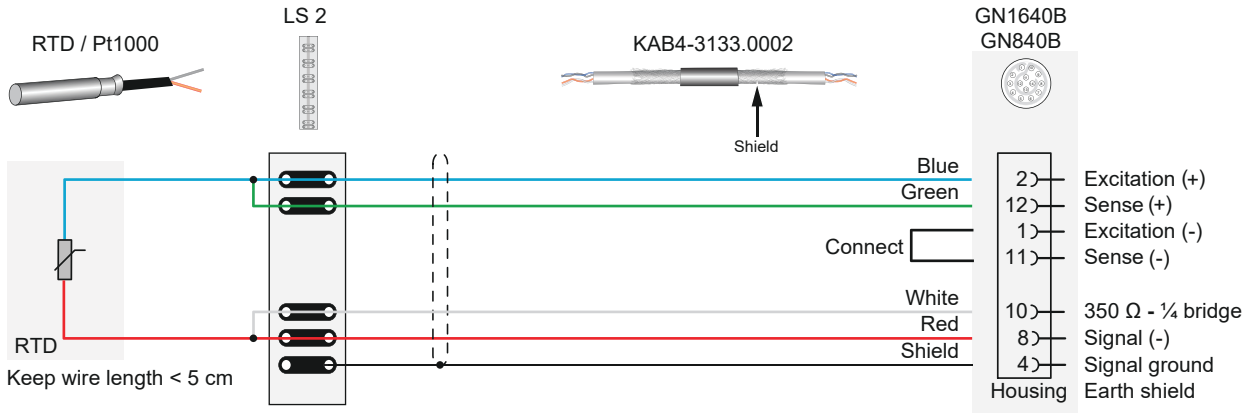


Figure A.107: Recommended 4 wire RTD connection (more options are available)

Current Loop Mode

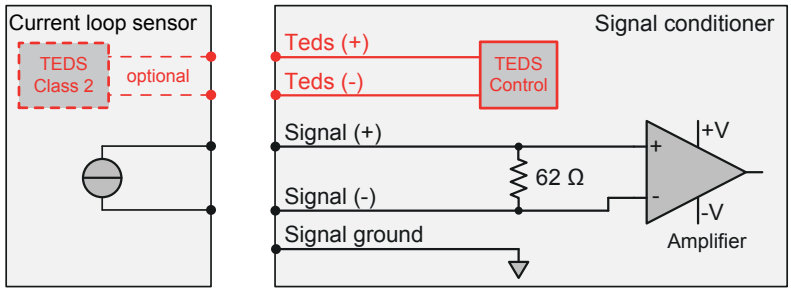


Figure A.108: Current loop mode block diagram

Resistance value (typical)	62 Ω
Input fuse	0.1 A (self-resettable)
Cable length	100 m Max.
Range	± 20 µA, ± 0.2 mA, ± 2 mA, ± 20 mA (0 to 40 mA with offset used)
TEDS support	Class 2 (no software support at release date)

Current Loop Wire Diagram

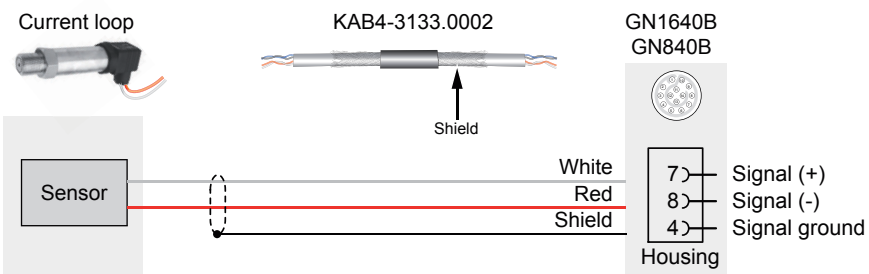
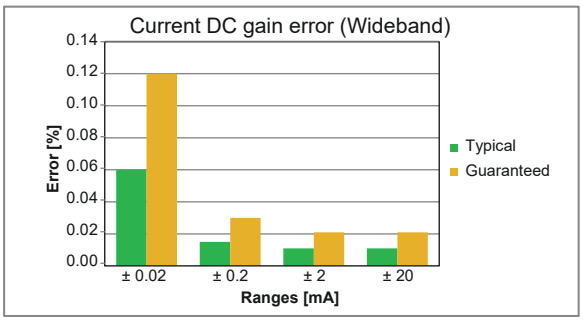
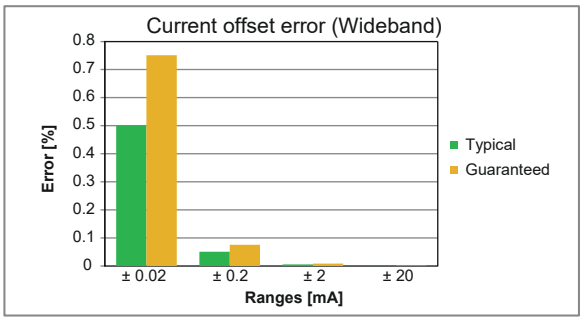


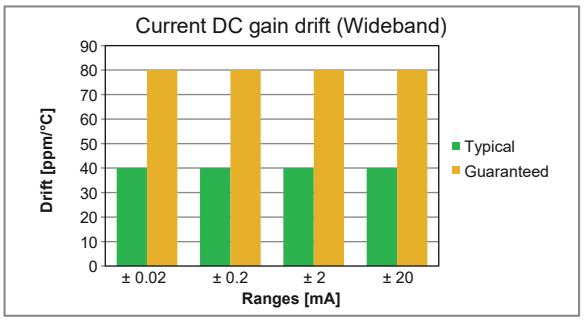
Figure A.109: Recommended current loop connection

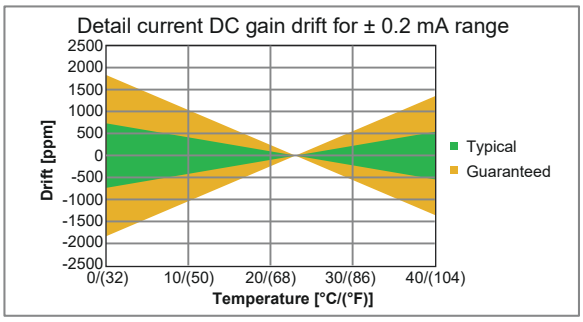
Current Loop Specifications

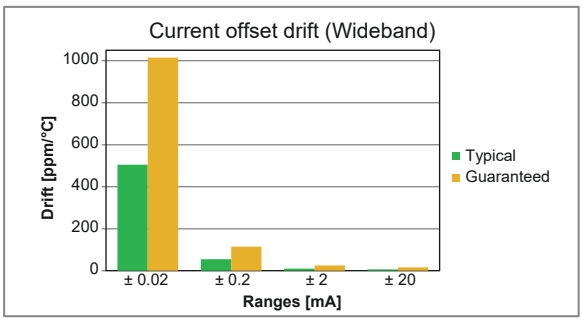
Wideband	Typical	Guaranteed
Current loop DC gain error	0.01% of reading ± 20 nA	0.03% of reading ± 100 nA
Current loop offset error	0.0001% of Full Scale ± 200 nA	0.001% of Full Scale ± 300 nA
Current loop DC gain error drift	40 ppm / °C (23 ppm / °F)	80 ppm / °C (45 ppm of Full Scale / °F)
Current loop offset error drift	± (5 ppm + 20 nA) / °C (± (3 ppm + 12 nA) / °F)	± (15 ppm + 40 nA) / °C (± (9 ppm + 23 nA) / °F)











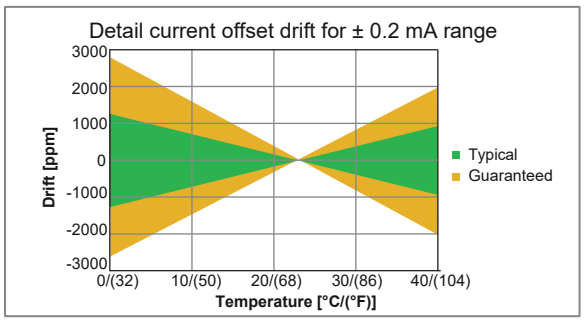


Figure A.110: Wideband current loop specification

Thermocouple Mode

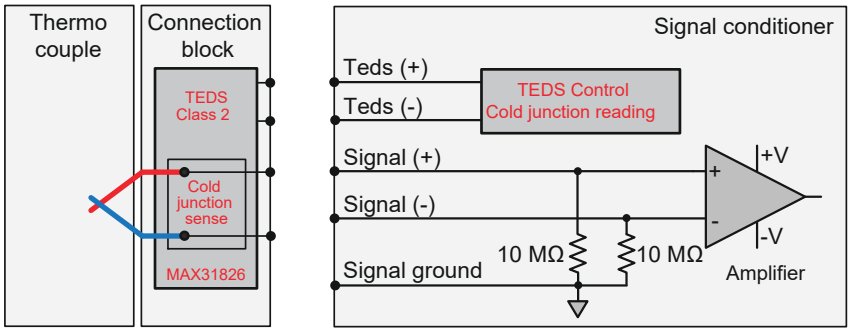


Figure A.111: Thermocouple mode block diagram

Linearization for thermocouples	K, J, T, B, E, N, R, S, C
Cold junction compensation	Digital 1-wire readout of MAX31826 or DS18S20 digital thermometer
Filter types	Bessel, Butterworth and Elliptic
Filter frequencies	10 kHz, 5 kHz, 2.5 kHz, 2 kHz, 1 kHz, 500 Hz, 250 Hz,200 Hz, 100 Hz, 50 Hz, 25 Hz, 20 Hz, 10 Hz, 5 Hz, 2.5 Hz, 2 Hz, 1 Hz, 0.5 Hz, 0.25 Hz Bessel filter additionally supports 0.2 Hz and 0.1 Hz
Thermocouple sample rate	Sample rate depends on filter frequency used. See table: “Thermocouple Update Rates”
Connector cable	Connection box
TEDS support	Class 2 (no software support at release date)

Types	**Temperature range**	**Typical(1)**	**Guaranteed(1)**
Type B	From 100° C to 200° C (212° F to 392° F)	± 1.4° C (± 2.52° F)	± 7° C (± 12.6° F)
	From 200° C to 500° C (392° F to 932° F)	± 0.75° C (± 1.35° F)	± 3.5° C (± 6.3° F)
	From 500 °C to 1820° C (932° F to 3308° F)	± 0.5° C (± 0.9° F)	± 2°C (± 3.6° F)
Type C	From 0° C to 1000° C (32° F to 1832° F)	± 0.6° C (± 1.08° F)	± 1.5° C (± 2.7° F)
	From 1000° C to 2315° C (1832° F to 4199° F)	± 1.5° C (± 2.7° F)	± 3°C (± 5.4° F)
Type E	From -200 °C to 900° C (-328° F to 1652° F)	± 0.4°C (± 0.72° F)	± 0.8°C (± 1.44° F)
Type J	From -210° C to 1200° C (-346° F to 2192° F)	± 0.5° C (± 0.9° F)	± 1°C (± 1.8° F)
Type K	From -200° C to 1372° C (-328° F to 2501.6° F)	± 0.6° C (± 1.08° F)	± 1°C (± 1.8° F)
Type N	From -250°C to -100°C (-418° F to -148° F)	± 1.25°C (± 2.25° F)	± 2.5°C (± 4.5° F)
	From -100°C to 1300°C (-148° F to 2372° F)	± 0.5° C (± 0.9° F)	± 1°C (± 1.8° F)
Type R	From -50° C to 0° C (-58° F to 32° F)	± 1°C (± 1.8° F)	± 2°C (± 3.6° F)
	From 0° C to 1100° C (32° F to 2012° F)	± 0.5° C (± 0.9° F)	± 1°C (± 1.8° F)
	From 1100° C to 1768° C (2012° F to 3214.4° F)	± 0.7°C (± 1.26° F)	± 1.4°C (± 2.52° F)
Type S	From -50° C to 0° C (-58° F to 32° F)	± 1°C (± 1.8° F)	± 2°C (± 3.6° F)
	From 0° C to 1100° C (32° F to 2012° F)	± 0.5° C (± 0.9° F)	± 1°C (± 1.8° F)
	From 1100° C to 1768° C (2012° F to 3214.4° F)	± 0.7°C (± 1.26° F)	± 1.4°C (± 2.52° F)
Type T	From -260°C to -100°C (-436° F to -148° F)	± 2°C (± 3.6° F)	± 4°C (± 7.2° F)
	From -100° C to 400° C (-148° F to 752° F)	± 0.3°C (± 0.54° F)	± 0.6°C (± 1.08° F)

(1) Measured using Bessel filter at 5 Hz bandwidth.

Thermocouple Wire Diagram

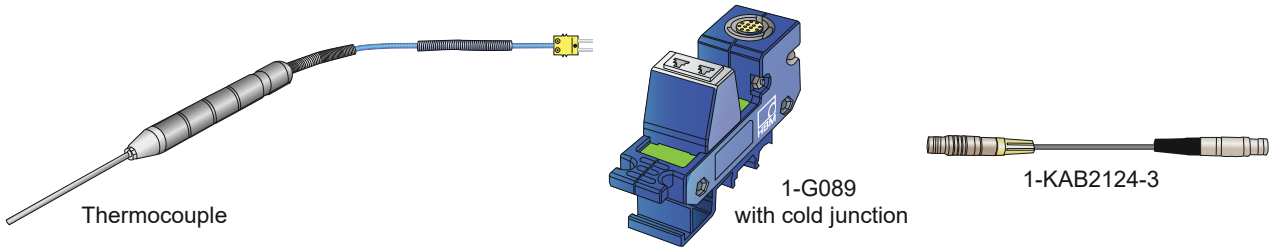


Figure A.112: Recommended thermocouple tools

Thermocouple Update Rates

Limited update rate	**GN840B/GN1640B Sample rate**		
Filter cut off	1 S/s to 500 S/s	1 kS/s to 5 kS/s	5 kS/s to 500 kS/s
0.25 Hz	500 Hz	500 Hz	500 Hz
0.5 Hz	500 Hz	500 Hz	500 Hz
1 Hz	500 Hz	5 kHz	5 kHz
2 Hz	500 Hz	5 kHz	5 kHz
2.5 Hz	500 Hz	5 kHz	5 kHz
5 Hz	500 Hz	5 kHz	5 kHz
10 Hz	500 Hz	5 kHz	50 kHz
20 Hz	500 Hz	5 kHz	50 kHz
25 Hz	500 Hz	5 kHz	50 kHz
50 Hz	500 Hz	5 kHz	50 kHz
100 Hz	500 Hz	5 kHz	500 kHz
200 Hz	-	5 kHz	500 kHz
250 Hz	-	5 kHz	500 kHz
500Hz	-	5 kHz	500 kHz
1000 Hz	-	5 kHz	500 kHz
2000 Hz	-	-	500 kHz
2500 Hz	-	-	500 kHz
5000 Hz	-	-	500 kHz
10000 Hz	-	-	500 kHz

Isolation

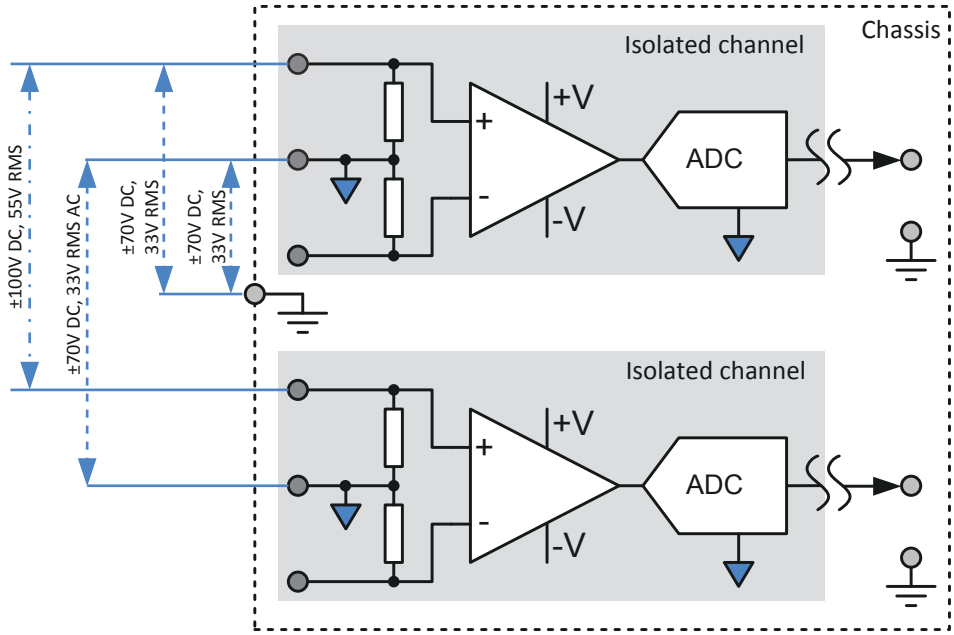


Figure A.113: Isolation schematic

Channel to chassis (earth)	33 V RMS, ± 70 V DC
Channel to channel (Isolated GND to isolated GND)	33 V RMS, ± 70 V DC
Input signal-to-input signal	55 V RMS, ± 100 V DC

GN1640B/GN840B Connector and Pinning

Mating connector	HBM 1-CON-P1007; ODU SX2B0C-P14MFG0-0001 (male)
Connectors	ODU GX2B0C-P14QF00-0002 (female)

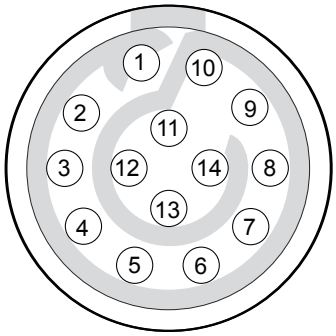


Figure A.114: Cable connector soldering view

GN1640B/GN840B	KAB183 colors	Pin number
Excitation (-) / TEDS class 3 (-)	Black	1
Excitation (+)	Blue	2
Reserved	White/Black	3
Signal ground	Red/Black	4
External shunt	Pink/Black	5
Reserved	Yellow/Black	6
Signal (+)	White	7
Signal (-)	Red	8
120 Ω -¼ bridge	Brown	9
350 Ω -¼ bridge	Yellow	10
Sense (-) / TEDS class 3 +	Grey	11
Sense (+)	Green	12
TEDS class 2 (-)	Grey/Black	13
TEDS class 2 (+)	Green/Black	14

Analog to Digital Conversion	
Sample rate; per channel	0.1 S/s to 500 kS/s
ADC resolution; one ADC per channel	24 bit
ADC Type	Sigma Delta (Σ-Δ) ADC; Texas Instruments® ADS127L01
Time base accuracy	Defined by mainframe: ± 3.5 ppm; aging after 10 years ± 10 ppm
Binary sample rate	Supported; when calculating FFT's produces rounded/integer BIN sizes
Maximum binary sample rate	512 kS/s
External time base sample rate	0 S/s to 250 kS/s
External time base level	TTL
External time base minimum pulse width	200 ns

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

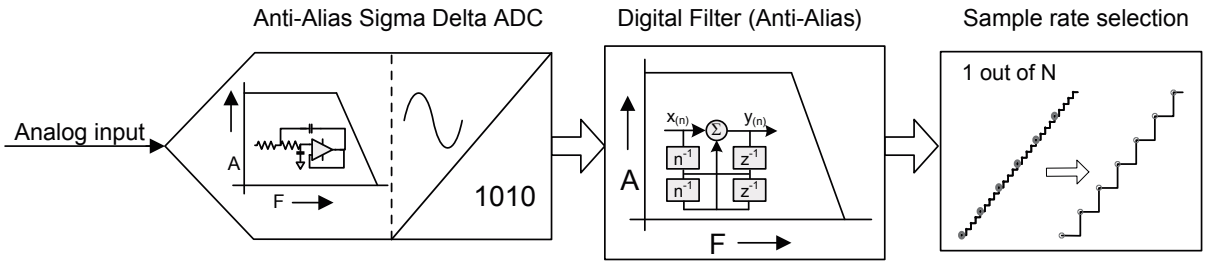


Figure A.115: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter integrated inside the Sigma Delta Analog to Digital Converter (ADC) always sampling at a fixed sample rate. This setup avoids the need for other analog anti-alias filters.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Sigma Delta Wideband	When Sigma Delta wideband is selected there is always the anti-alias filter built-in the Sigma Delta ADC (no digital filter) in the signal path. Therefore there is always anti-alias protection when wideband is selected.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. Best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. Best used when working in the frequency domain. When working in the time domain this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter to prevent aliasing at lower sample rates. Best used when working in the frequency domain. When working in the time domain this filter is best used for signals that are (close to) sine waves.
Elliptic Bandpass IIR	When Elliptic Bandpass IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Elliptic Bandpass IIR filter. Elliptic Bandpass filters are best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Bandwidth and Filter Characteristic Selection versus Sample Rate

The digital filter before decimation guarantees a superior phase match, ultra-low noise and alias free result.

	AA-filter(1)	Digital lowpass filters (alias free)					Digital bandpass(2)	
	Sigma Delta	Butterworth IIR Elliptic IIR	Bessel IIR Butterworth IIR Elliptic IIR	Bessel IIR Butterworth IIR Elliptic IIR	Bessel IIR Butterworth IIR Elliptic IIR	Bessel IIR	Elliptic IIR	
User selectable sample rates		**1/4 Fs**	**1/10 Fs**	**1/20 Fs**	**1/40 Fs**	**1/100 Fs**	**Highpass**	**Lowpass**
500 kS/s	ΣΔ Wideband	125 kHz	50 kHz	25 kHz	12.5 kHz	5 kHz	50 Hz, 100 Hz, 200 Hz, 500 Hz	1 kHz, 2 kHz, 5 kHz, 10 kHz, 12.5 kHz, 25 kHz, 50 kHz, 100 kHz
400 kS/s	ΣΔ Wideband	100 kHz	40 kHz	20 kHz	10 kHz	4 kHz		
250 kS/s	ΣΔ Wideband	62.5 kHz	25 kHz	12.5 kHz	6.25 kHz	2.5 kHz		
200 kS/s	ΣΔ Wideband	50 kHz	20 kHz	10 kHz	5 kHz	2 kHz		
125 kS/s	ΣΔ Wideband	25 kHz	12.5 kHz	6.25 kHz	2.5 kHz	1.25 kHz		
100 kS/s	ΣΔ Wideband	20 kHz	10 kHz	5 kHz	2 kHz	1 kHz		
50 kS/s	ΣΔ Wideband	12.5 kHz	5 kHz	2.5 kHz	1.25 kHz	500 Hz		
40 kS/s	ΣΔ Wideband	10 kHz	4 kHz	2 kHz	1 kHz	400 Hz		
25 kS/s	ΣΔ Wideband	6.25 kHz	2.5 kHz	1.25 kHz	625 Hz	250 Hz		
20 kS/s	ΣΔ Wideband	5 kHz	2 kHz	1 kHz	500 Hz	200 Hz		
12.5 kS/s	ΣΔ Wideband	2.5 kHz	1.25 kHz	625 Hz	312.5 Hz	125 Hz		
10 kS/s	ΣΔ Wideband	2 kHz	1 kHz	500 Hz	250 Hz	100 Hz		
5 kS/s	ΣΔ Wideband	1.25 kHz	500 Hz	250 Hz	125 Hz	50 Hz		
4 kS/s	ΣΔ Wideband	1 kHz	400 Hz	200 Hz	100 Hz	40 Hz		
2.5 kS/s	ΣΔ Wideband	625 Hz	250 Hz	125 Hz	62.5 Hz	25 Hz		
2 kS/s	ΣΔ Wideband	500 Hz	200 Hz	100 Hz	50 Hz	20 Hz		
1.25 kS/s	ΣΔ Wideband	312.5 Hz	125 Hz	62.5 Hz	31.25 Hz	12.5 Hz		
1 kS/s	ΣΔ Wideband	250 Hz	100 Hz	50 Hz	25 Hz	10 Hz		
500 S/s	ΣΔ Wideband	125 Hz	50 Hz	25 Hz	12.5 Hz	5 Hz		
400 S/s	ΣΔ Wideband	100 Hz	40 Hz	20 Hz	10 Hz	4 Hz		
250 S/s	ΣΔ Wideband	62.5 Hz	25 Hz	12.5 Hz	6.25 Hz	2.5 Hz		
200 S/s	ΣΔ Wideband	50 Hz	20 Hz	10 Hz	5 Hz	2 Hz		
125 S/s	ΣΔ Wideband	31.25 Hz	12.5 Hz	6.25 Hz	3.125 Hz	1.25 Hz		
100 S/s	ΣΔ Wideband	25 Hz	10 Hz	5 Hz	2.5 Hz	1 Hz		
50 S/s	ΣΔ Wideband	12.5 Hz	5 Hz	2.5 Hz	1.25 Hz	0.5 Hz		
40 S/s	ΣΔ Wideband	10 Hz	4 Hz	2 Hz	0.5 Hz	0.4 Hz		
25 S/s	ΣΔ Wideband	6.25 Hz	2.5 Hz	1.25 Hz	0.625 Hz	0.25 Hz		
20 S/s	ΣΔ Wideband	5 Hz	2 Hz	0.5 Hz	0.5 Hz	0.2 Hz		
12.5 S/s	ΣΔ Wideband	3.125 Hz	1.25 Hz	0.625 Hz	0.3125 Hz	0.125 Hz		
10 S/s	ΣΔ Wideband	2.5 Hz	1 Hz	0.5 Hz	0.25 Hz	0.1 Hz		

(1) Sigma Delta ΣΔ Wideband prevents aliasing before the digitization of the signal.

(2) Digital bandpass filters are selectable in all sample rates.

Sigma Delta Wideband (Analog Anti-Alias)

When Sigma Delta wideband is selected there is always the anti-alias filter built-in the Sigma Delta ADC (no digital filter) in the signal path. Therefore there is always anti-alias protection when Sigma Delta wideband is selected.

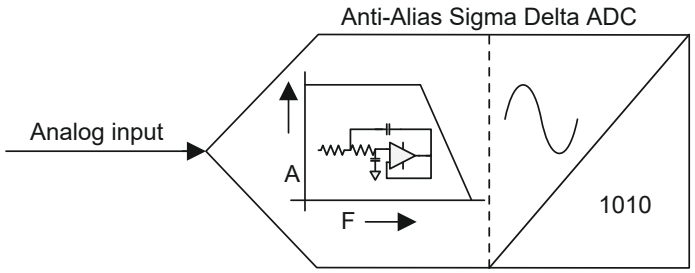


Figure A.116: Anti-alias filter built-in (Sigma Delta ADC)

Wideband -3 dB bandwidth(1)	DC to 211 kHz DC to 56 kHz for ± 1 mV range due to high amplifier gain
0.1 dB passband flatness(1)	DC to 150 kHz DC to 7 kHz for ± 1 mV range due to high amplifier gain

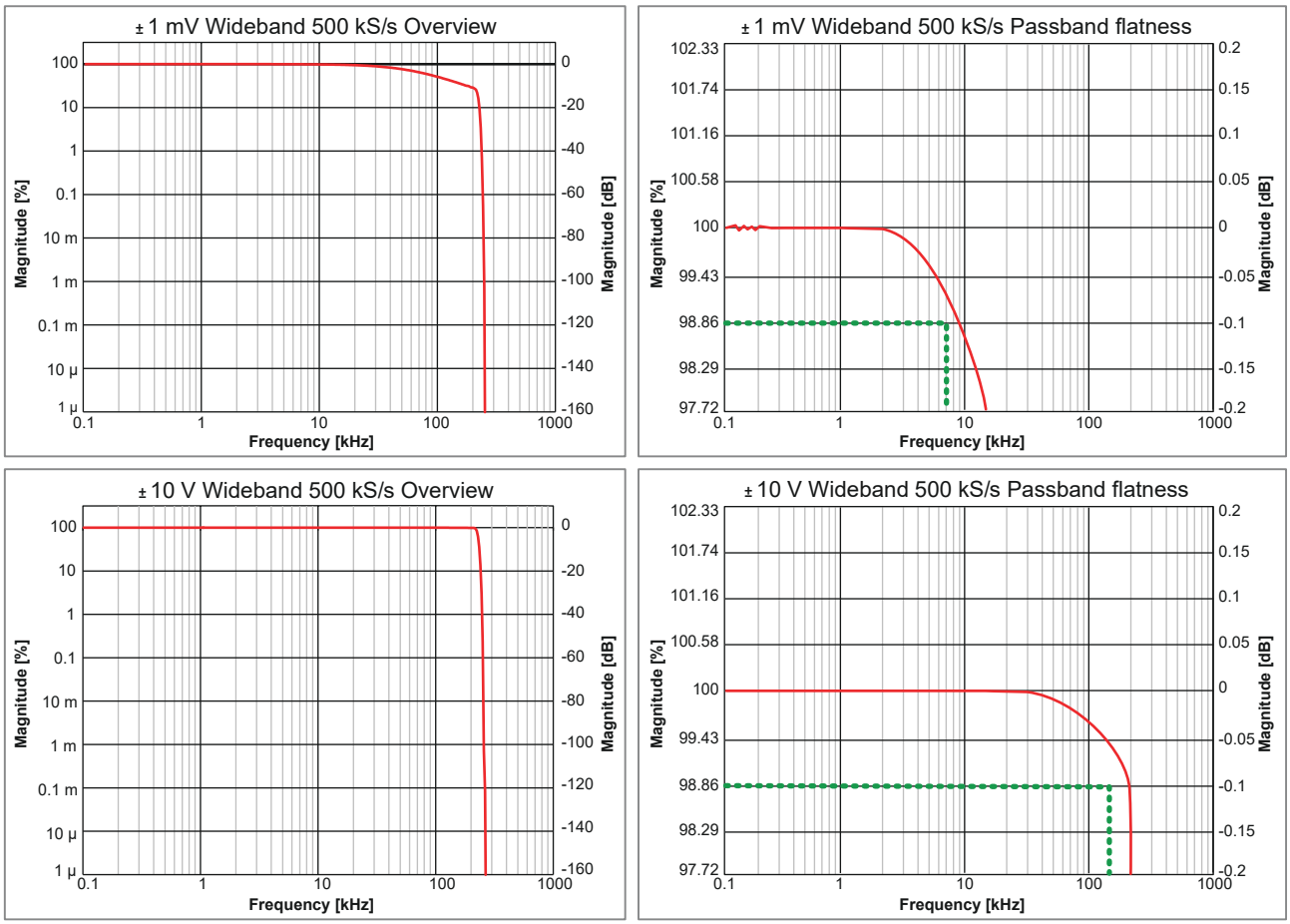
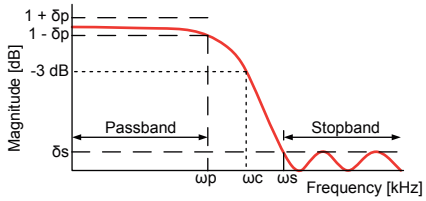


Figure A.117: Representative Wideband examples

(1) Measured using a Fluke 5730A calibrator, DC normalized

Bessel IIR filter (Digital Anti-Alias)



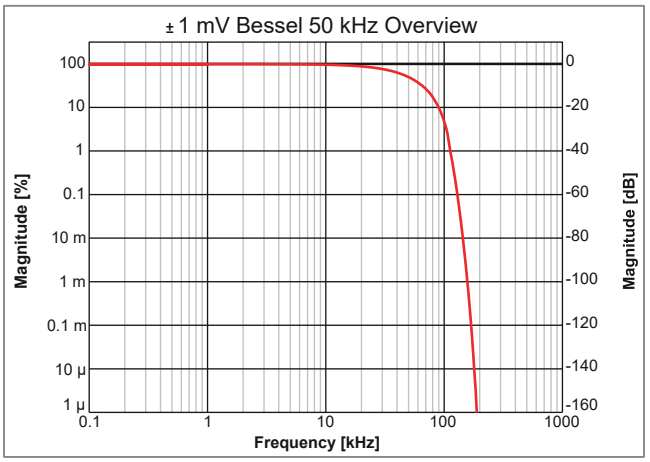
δp: Passband ripple
δs: Stopband attenuation

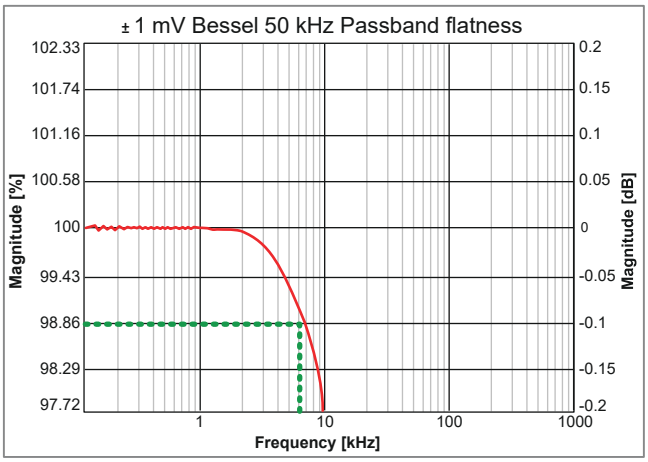
ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

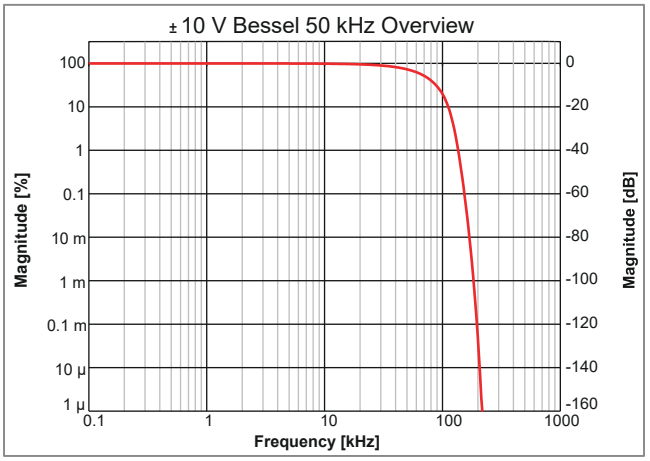
Figure A.118: Representative Bessel IIR examples

When Bessel IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Bessel IIR filter.

Analog anti-alias filter	The Sigma Delta ADC anti-alias filter
Bessel IIR filter	
Characteristic	12-pole Bessel style IIR
User selection	Auto tracking to sample rate divided by: 10, 20, 40, 100 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	User selectable from 1 Hz to 50 kHz
0.1 dB passband flatness (ωp)(1)	DC to 0.18 * ωc. Limited to 6 kHz for ± 1 mV range
Stopband	-180 dB (-160 dB for ± 1 mV range)
Roll-off	-72 dB/octave







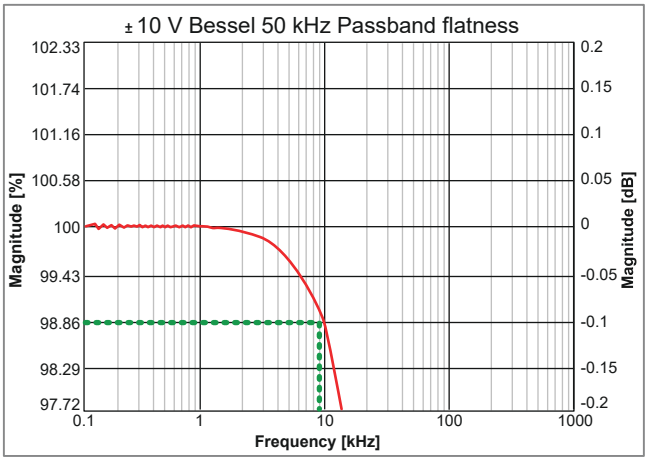
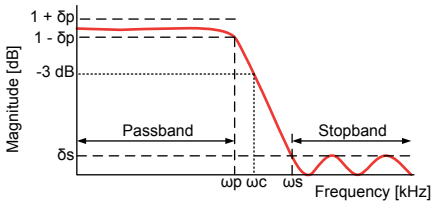


Figure A.119: Representative Bessel IIR examples

(1) Measured using Fluke 5730A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



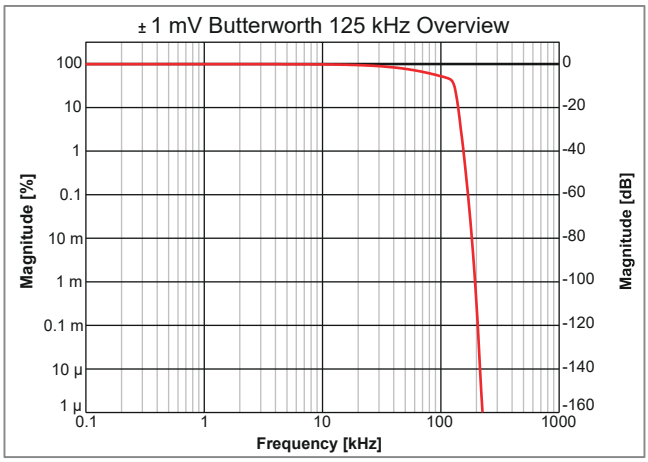
δp: Passband ripple
δs: Stopband attenuation

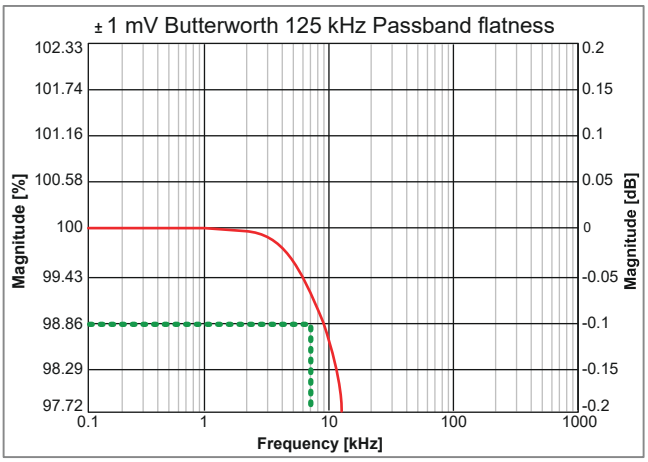
ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

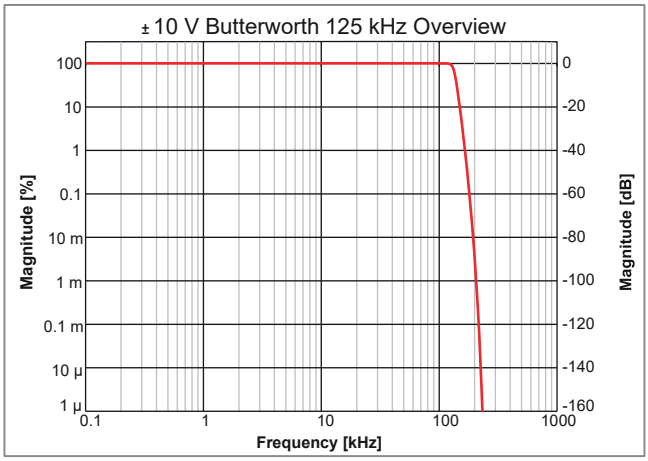
Figure A.120: Representative Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Butterworth IIR filter.

Analog anti-alias filter	The Sigma Delta ADC anti-alias filter
Butterworth IIR filter	
Characteristic	12-pole Butterworth style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed.
Bandwidth (ωc)	User selectable from 2.5 Hz to 125 kHz
0.1 dB passband ripple (ωp)	DC to 0.8 * ωc. Limited to 7 kHz for ± 1 mV range
Stopband attenuation (δs)	-180 dB (-160 dB for ± 1 mV range)
Roll-off	-72 dB/octave







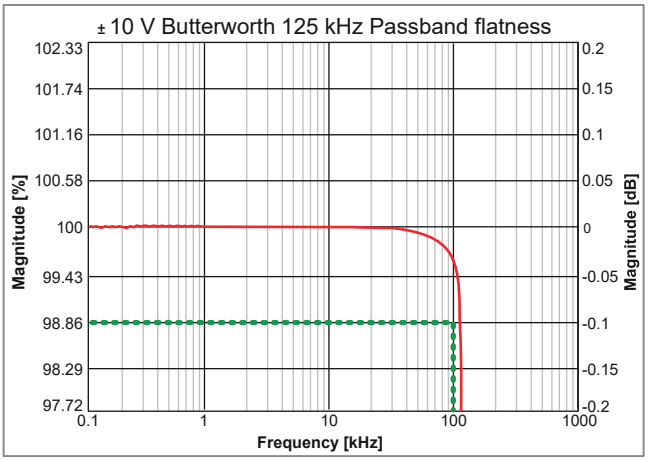
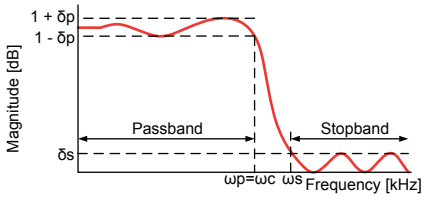


Figure A.121: Representative Butterworth IIR examples

(1) Measured using Fluke 5730A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.122: Representative Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	The Sigma Delta ADC anti-alias filter
Elliptic IIR filter	
Characteristic	11-pole Elliptic style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	User selectable from 2.5 Hz to 125 kHz
0.1 dB passband ripple (ωp)	DC to ωc. For ωc = 125 kHz, DC to 100 kHz due to amplifier bandwidth When using the range ± 1 mV for ωc > 10 kHz, DC to 7 kHz due to amplifier bandwidth
Stopband attenuation (δs)	-180 dB (-160 dB for ± 1 mV range)
Roll-off	-100 dB/octave

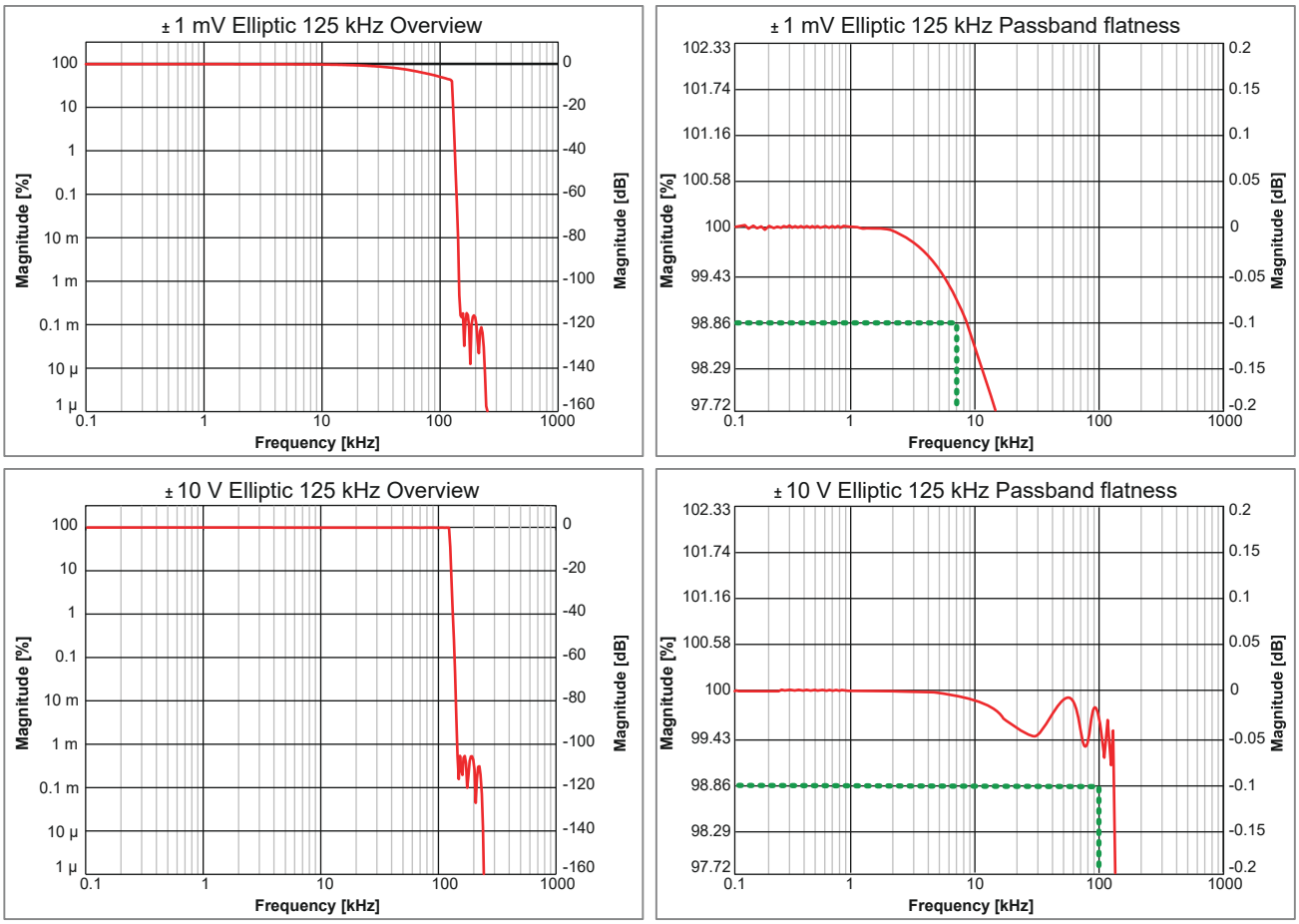
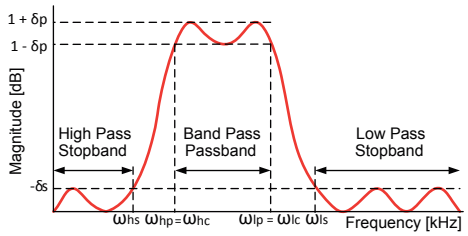


Figure A.123: Representative Elliptic IIR examples

(1) Measured using Fluke 5730A calibrator, DC normalized

Elliptic IIR Bandpass Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.124: Representative Digital Elliptic IIR Bandpass Filter

When Elliptic IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	The Sigma Delta ADC anti-alias filter
Elliptic IIR Bandpass filter	
Characteristic	12th order Elliptic style IIR
User selection	Fixed high pass frequencies to be combined with fixed low pass frequencies
High pass bandwidth (ωhc)	500 Hz, 200 Hz, 100 Hz, 50 Hz
High pass stopband frequency (ωhs)	Approximately ωhc / 2.5
Low pass bandwidth (ωlc)	125 kHz, 100 kHz, 50 kHz, 25 kHz, 12.5 kHz, 10 kHz, 5 kHz, 2 kHz, 1 kHz
Low pass stopband frequency (ωls)	Approximately 1.5 to 2.5 * ωc
0.1 dB passband flatness (ωp)(1)	ωhc to ωlc, limited to 7 kHz for ± 1 mV range
High pass stopband attenuation (δhs)	- 90 dB
Low pass stopband attenuation (δls)	-180 dB (-160 dB for ± 1 mV range)

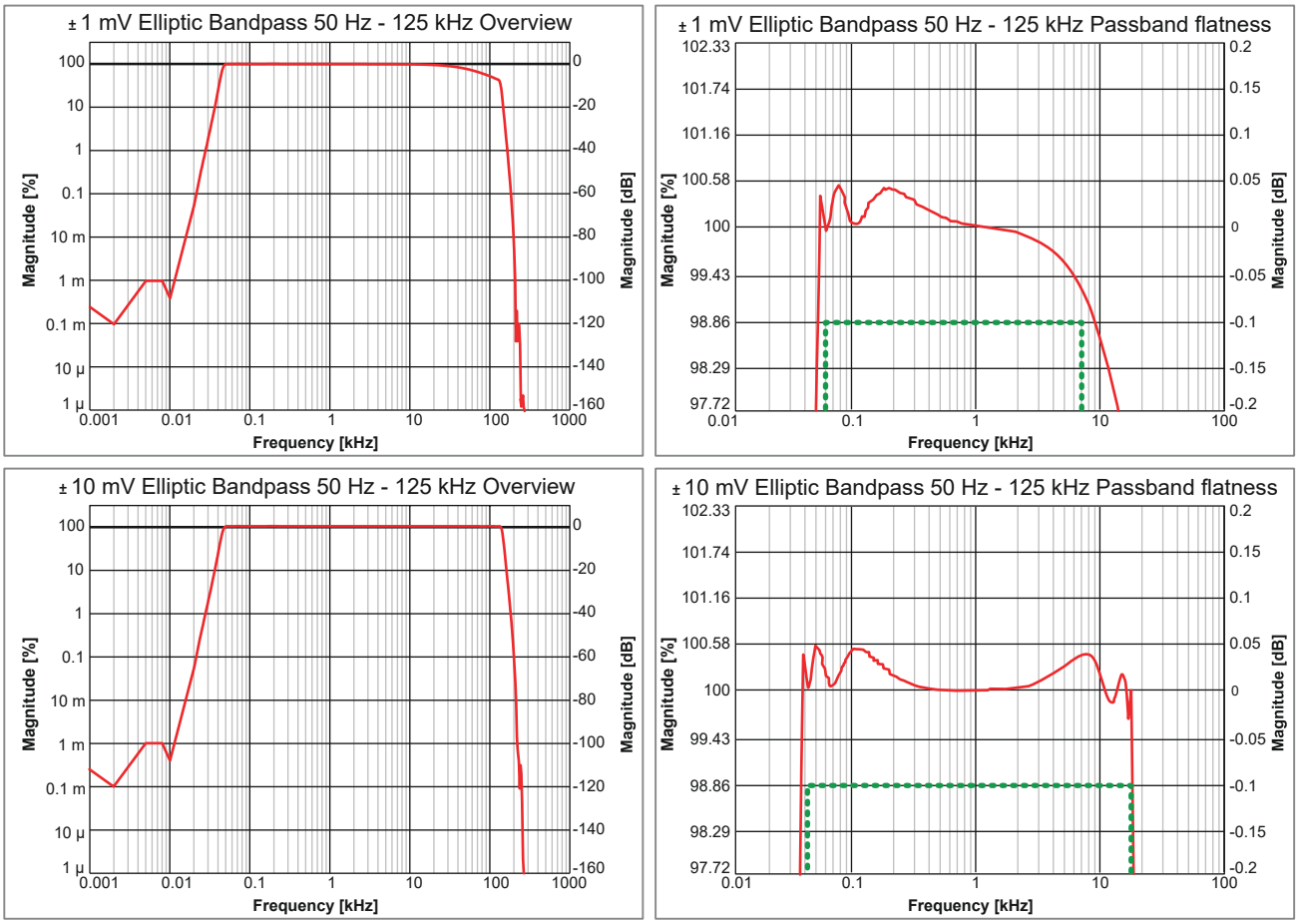


Figure A.125: Representative Elliptic IIR Bandpass examples

(1) Measured using Fluke 5730A calibrator, DC normalized

Channel to Channel Phase Match

Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths results in phase mismatches between channels. Specifications valid for channel to channel and card to card, all specifications are typical statistical values and measured using a 500 kS/s sample rate with sine wave ranging from 100 Hz to 100 kHz or filter frequency, whichever is reached first.

	Range ±1 mV	Ranges ≥ ±10 mV	Ranges combined
Wideband	200 ns	30 ns	200 ns
Bessel IIR	100 ns	30 ns	100 ns
Butterworth IIR	100 ns	30 ns	100 ns
Elliptic IIR	110 ns	30 ns	110 ns
Elliptic IIR Bandpass	80 ns	30 ns	80 ns
GN840B/GN1640B channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)		

Channel to Channel Crosstalk

Channel to channel crosstalk is measured with a 50 Ω termination resistor on the input and uses sine wave signals on the channel above and below the channel being tested. To test Channel 2, Channel 2 is terminated with 50 Ω and Channels 1 and 3 are connected to the sine wave generator.

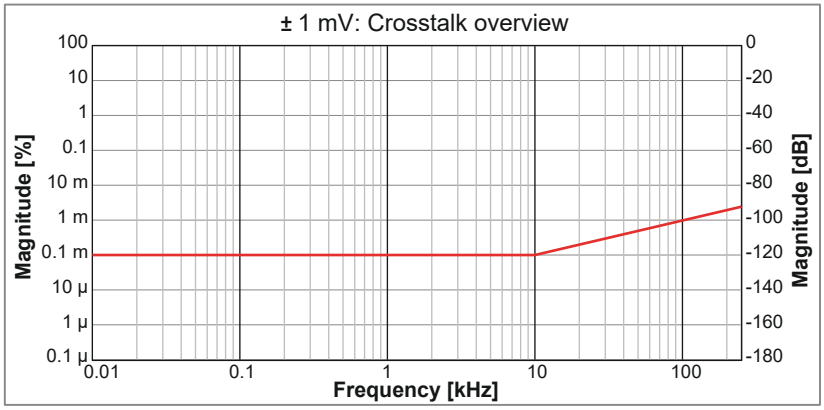


Figure A.126: Representative Channel to Channel crosstalk

On-board Memory

Per card	2 GB (1 GSample @ 16 bits, 500 MS @ 24 bits storage)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered and not recording
Storage sample size	16 bits, 2 bytes / sample 24 bits, 4 bytes / sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

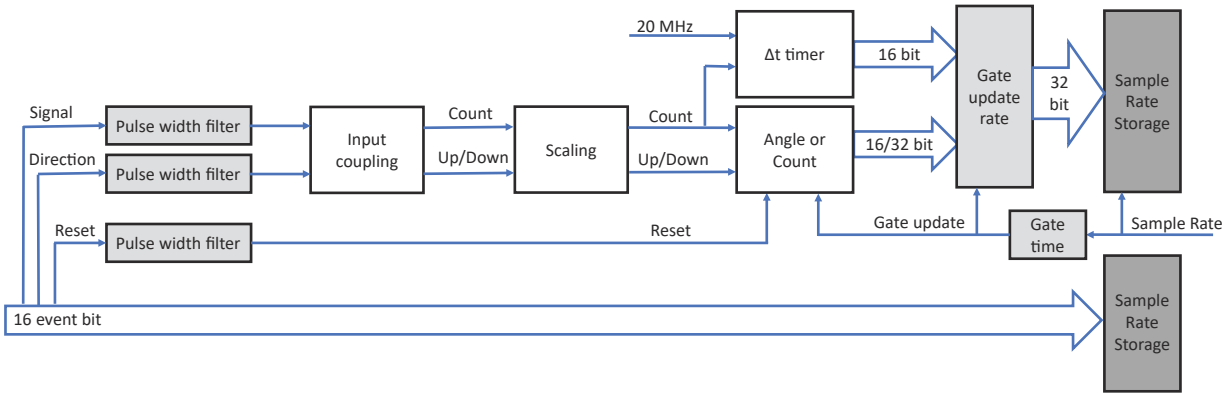


Figure A.127: Timer/Counter block diagram

Digital input events	16 per card			
Levels	TTL input level, user programmable invert level			
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs			
Overvoltage protection	± 30 V DC continuously			
Minimum pulse width	100 ns			
Maximum frequency	5 MHz			
Digital output events	2 per card			
Levels	TTL output levels, short circuit protected			
Output event 1	User selectable: Trigger, Alarm, set High or Low			
Output event 2	User selectable: Recording active, set High or Low			
Digital output event user selections				
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay			
Alarm	High when alarm condition of card is activated, low when not activated 200 µs ± 1 µs ± 1 sample period alarm event delay			
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns			
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation			
Timer/Counter	2 per card			
Levels	TTL input levels			
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs			
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)			
Measurement modes	Count (C) Angle (0 to 360 degrees) Frequency (Δcount / Δt) RPM (Δcount / Δt / 60 s)			
Δt timer measurement accuracy	50 ns (20 MHz)			
Gate time	1 to n samples (User selectable maximum Δt)			
Gate time and reading update rate	Gate time sets the maximum update rate of the measurement values			
Gate time and minimum frequency	Minimum measured frequency or RPM = 1 / gate time			
Gate time and frequency accuracy	Accuracy = 50 ns / gate time			
Gate time impact	**Gate time**	**1 us**	**10 us**	**100 us**
	Δt Error	5%	0.5%	0.05%
	Update rate	1 MS/s	100 kS/s	10 kS/s
RT-FDB options	RT-FDB timer based average enables the same gate time effect. RT-FDB cycle detect average enables a dynamic gate time effect.			

Input Coupling Uni- and Bi-directional Signal

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

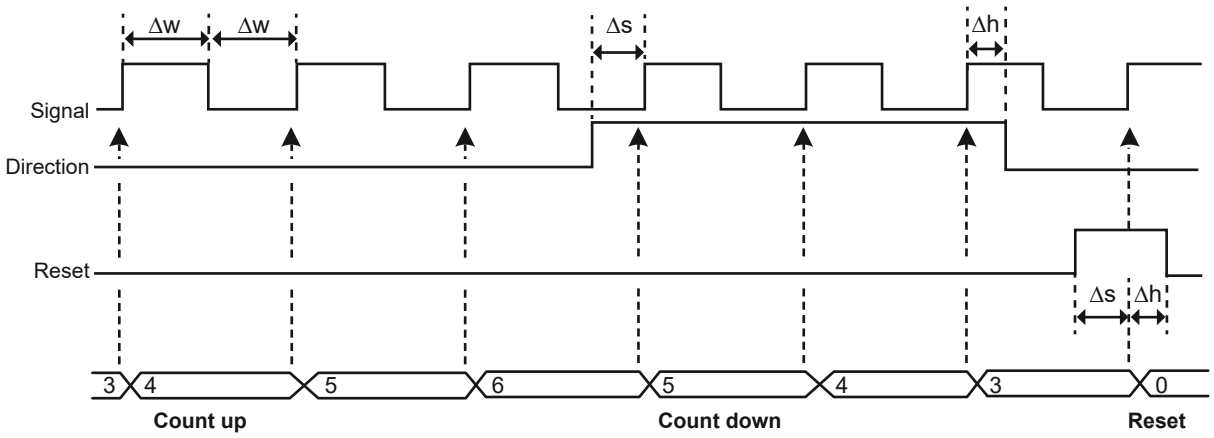


Figure A.128: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	4 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

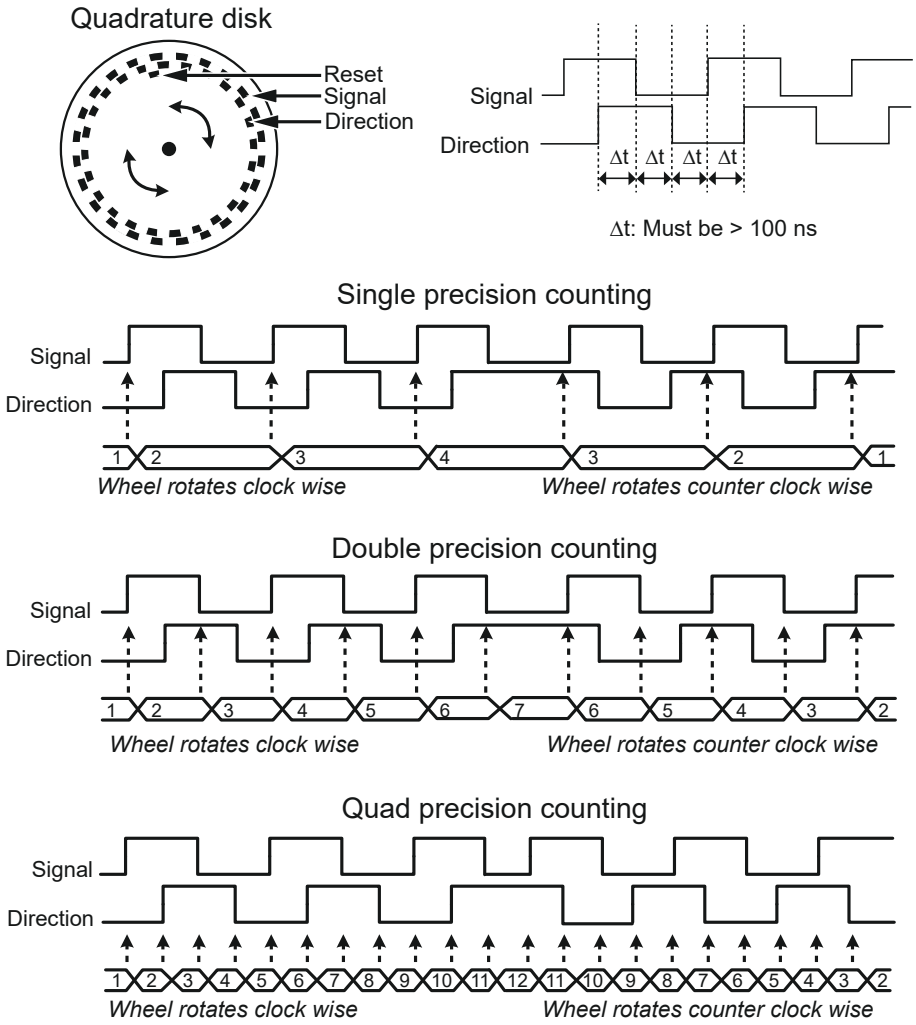


Figure A.129: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Count/Position	
Count/position mode is typically used for tracking movement of device under test. To reduce the sensitivity for count/position errors due to clock glitches use the minimum pulse width filter or enable the ABZ in stead of uni-/bi-polar input coupling .	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31}$ - 1; bi-directional count

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period (identical for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (10 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (9.76 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516 (504) µs for decimal (binary) time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators

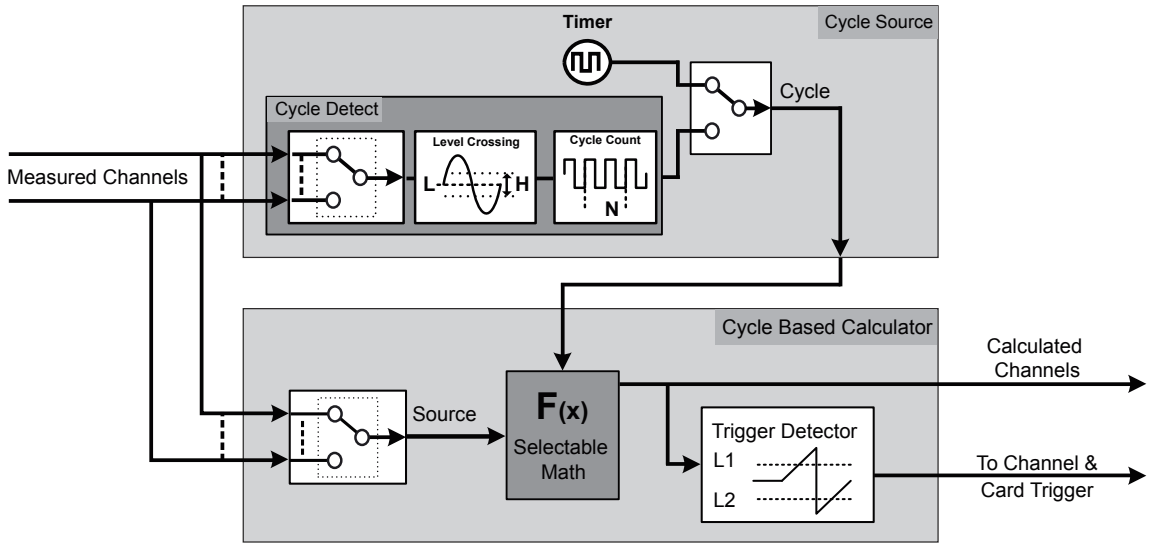


Figure A.130: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased
Cycle based calculator	
Number of calculators	32; at sample rates 200 kS/s or lower. At higher sample rates, the number of calculators is reduced to match the available DSP power
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and Crest Factor
Timer/Counter channel calculations	Frequency (to enable triggering), RPM of Angle
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)

The real-time formula database (RT-FDB) option offers an extensive set of math routines to enable almost any real-time mathematical challenge. The database structure enables the user to define a list of mathematical equations similar to the Perception review formula database.
The maximum supported sample rate is 2 MS/s.
The real-time formula database feature set is extended with higher Perception Versions. Different versions of Perception therefore can enable more or less features as described in this table.

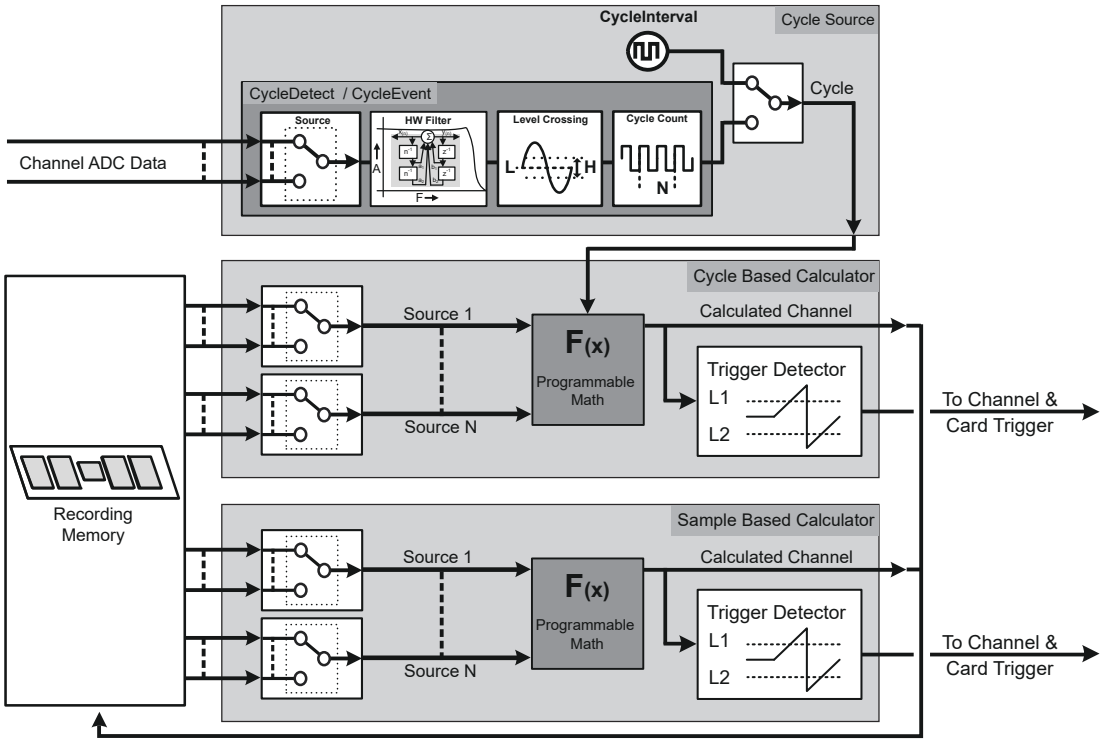


Figure A.131: Real-time formula database (RT-FDB) calculators

The real-time formula database supports the following list of calculations (Details of each calculation are described in the manual).

Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Basic calculations				
`+ (add)`	✓	✓	✓	✓(1)
`- (subtract)`	✓	✓	✓	✓(1)
`* (multiply)`	✓	✓	✓	✓(1)
`/ (divide)`	✓	✓	✓	✓(1)
Enhanced calculations				
`Abs`	✓	✓	✓	✓(1)
`Atan`	✓	✓	✓	✓(1)
`Atan2`	✓	✓	✓	✓(1)
`Cosine`	✓	✓	✓	✓(1)
`DegreesToRadians`	✓	✓	✓	✓(1)
`Min`	✓	✓	✓	✓(1)
`Max`	✓	✓	✓	✓(1)
`Modulo`	✓	✓	✓	✓(1)
`RadiansToDegrees`	✓	✓	✓	✓(1)
`Sine`	✓	✓	✓	✓(1)
`Sqrt`	✓	✓	✓	✓(1)
`Tan`	✓	✓	✓	✓(1)

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Boolean calculations				
`Equal`	✓	✓	✓	✓
`GreaterEqualThan`	✓	✓	✓	✓
`GreaterThan`	✓	✓	✓	✓
`LessEqualThan`	✓	✓	✓	✓
`LessThan`	✓	✓	✓	✓
`NotEqual`	✓	✓	✓	✓
`InsideBand`	✓	✓	✓	
`OutsideBand`	✓	✓	✓	
`And`	✓	✓	✓	✓
`Or`	✓	✓	✓	✓
`Xor`	✓	✓	✓	✓
`Not`	✓	✓	✓	✓
Cycle based calculations				
`CycleArea`		✓	✓	✓
`CycleBusDelay`		✓	✓	✓
`CycleCount`		✓	✓	✓
`CycleCrestFactor`		✓	✓	✓
`CycleEnergy`		✓	✓	✓
`CycleFundamentalPhase`		✓	✓	✓(2)
`CycleFundamentalRMS`		✓	✓	✓
`CycleFrequency`		✓	✓	✓
`CycleMax`		✓	✓	✓
`CycleMean`		✓	✓	✓
`CycleMin`		✓	✓	✓
`CyclePeak2Peak`		✓	✓	✓
`CyclePhase`		✓	✓	✓
`CycleRMS`		✓	✓	✓
`CycleRPM`		✓	✓	✓
`CycleSampleCount`		✓	✓	✓
`CycleTHD`(2)		✓	✓	✓(2)
Cycle source				
`CycleDetect`(4)		✓	✓	
`CycleEvent`		✓	✓	
`CycleInterval`		✓	✓	

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Hardware based signal filtering				
`HWFilter`(4)	✓		✓	
Software based signal filtering				
`FilterBesselBP`	✓		✓	
`FilterBesselHP`	✓		✓	
`FilterBesselLP`	✓		✓	
`FilterButterworthBP`	✓		✓	
`FilterButterworthHP`	✓		✓	
`FilterButterworthLP`	✓		✓	
`FilterChebyshevBP`	✓		✓	
`FilterChebyshevHP`	✓		✓	
`FilterChebyshevLP`	✓		✓	
Special category calculation				
`HarmonicsIEC61000`	✓		✓	
`Integrate`	✓		✓	
Signal transformation				
`DQZeroTransformation (Park)`(3)	✓		✓	✓(1)
`SpaceVectorTransformation`(3)	✓		✓	
`SpaceVectorInverse Transformation`(3)	✓		✓	
Signal generation				
`SineWave`	✓		✓	
`Ramp`	✓		✓	
Trigger functions				
`TriggerOnBooleanChange`			Trigger mark	
`TriggerOnLevel`			Trigger mark	

(1) Only cycle based results can be used for real-time output. Use the CycleMean calculation on recorded channel data or sample based results to enable the real-time output of this data.

(2) The time required to calculate the output depends on maximum cycle length and sample rate. Depending on the selected settings the output latency will increase. HBM refers to these calculations as not deterministic. All real-time output published values (deterministic and/or not deterministic) will always have the same latency.

(3) This formula is only available if the eDrive license is added to Perception.

(4) The output of HWFilter is used for CycleDetect.

Acquisition Modes

Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Acquisition Mode Details

	Single Sweep Multiple Sweeps				**Continuous**				**Dual Rate**			
	Enabled Channels				Enabled Channels				Enabled Channels			
16 Bit storage	1 Ch	8 Ch	16 Ch	16 Ch + Event Ch(s)	1 Ch	8 Ch	16 Ch	16 Ch + Event Ch(s)	1 Ch	8 Ch	16 Ch	16 Ch + Event Ch(s)
Max. sweep memory	960 MS	120 MS	60 MS	56 MS	not used				768 MS	96 MS	48 MS	44 MS
Max. sweep sample rate	500 kS/s				not used				500 kS/s			
Max. continuous FIFO	not used				960 MS	120 MS	60 MS	56 MS	192 MS	24 MS	12 MS	11 MS
Max. continuous sample rate	not used				500 kS/s				Sweep Sample Rate / 2			
Max. continuous streaming rate	not used				0.5 MS/s 1 MB/s	4 MS/s 8 MS/s	8 MS/s 16 MB/s	8.5 MS/s 17 MB/s	0.3 MS/s 0.5 MB/s	2 MS/s 4 MB/s	4 MS/s 8 MB/s	4.5 MS/s 9 MB/s
	Enabled Channels				Enabled Channels				Enabled Channels			
24 Bit storage	1 Ch	8 Ch	16 Ch	16 Ch + Event Ch(s) + T/C	1 Ch	8 Ch	16 Ch	16 Ch + Event Ch(s) + T/C	1 Ch	8 Ch	16 Ch	16 Ch + Event Ch(s) + T/C
Max. sweep memory	480 MS	60 MS	30 MS	25 MS	not used				384 MS	48 MS	24 MS	20 MS
Max. sweep sample rate	500 kS/s				not used				500 kS/s			
Max. continuous FIFO	not used				480 MS	60 MS	30 MS	25 MS	96 MS	12 MS	6 MS	5 MS
Max. continuous sample rate	not used				500 kS/s				Sweep Sample Rate / 2			
Max. continuous streaming rate	not used				0.5 MS/s 2 MB/s	4 MS/s 16 MB/s	8 MS/s 32 MB/s	9.5 MS/s 38 MB/s	0.3 MS/s 1 MB/s	2 MS/s 8 MB/s	4 MS/s 16 MB/s	4.8 MS/s 19 MB/s

Single Sweep	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Flexible Wire Diagram

Using the KAB2124, DIN rail breakouts (G088, G089 and/or G090) allow flexible connections to the GN1640B or GN840B.

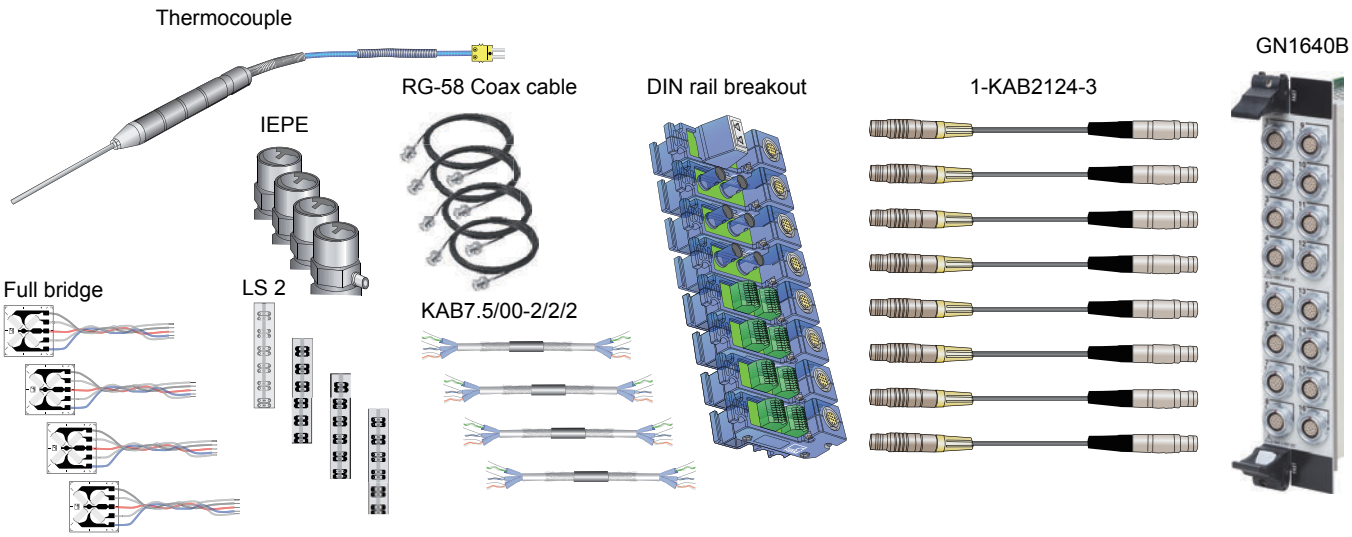


Figure A.132: Flexible wire diagram

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.7 B4770-1.1 en (GEN series GN1202B)

Capabilities Overview	
Receiver model	GN1202B
Transmitter models	GN110, GN111, GN112 and GN113
Maximum sample rate per channel	100 MS/s When either GN111 or GN113 is connected, the maximum sample rate for all channels will be limited to 25 MS/s
Memory per receiver	8 GB (4 GS)
Analog channels	1 input per transmitter (GN110, GN111, GN112 or GN113)
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	14 bit GN111 and GN113: 15 bit using four time over sampling
Isolation	Transmitter to receiver and transmitter to earth
Input type	Isolated, unbalanced differential inputs
Passive voltage/current probes	Passive, single-ended voltage probes
Sensors	Not supported
TEDS	Not supported
	Not supported at release of this card
Real-time formula database calculators (option)	Not supported at release of this card
Real-time calculated results output	Not supported at release of this card
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels. Due to technical implementation limits, some sample rates do not support Digital Event/ Timer/Counters (Supported from Perception 7.20 onwards)
Standard data streaming (CPCI up to 200 MB/s)	Not supported
Fast data streaming (PCIe up to 1 GB/s)	Supported
Slot width	1

Block Diagram

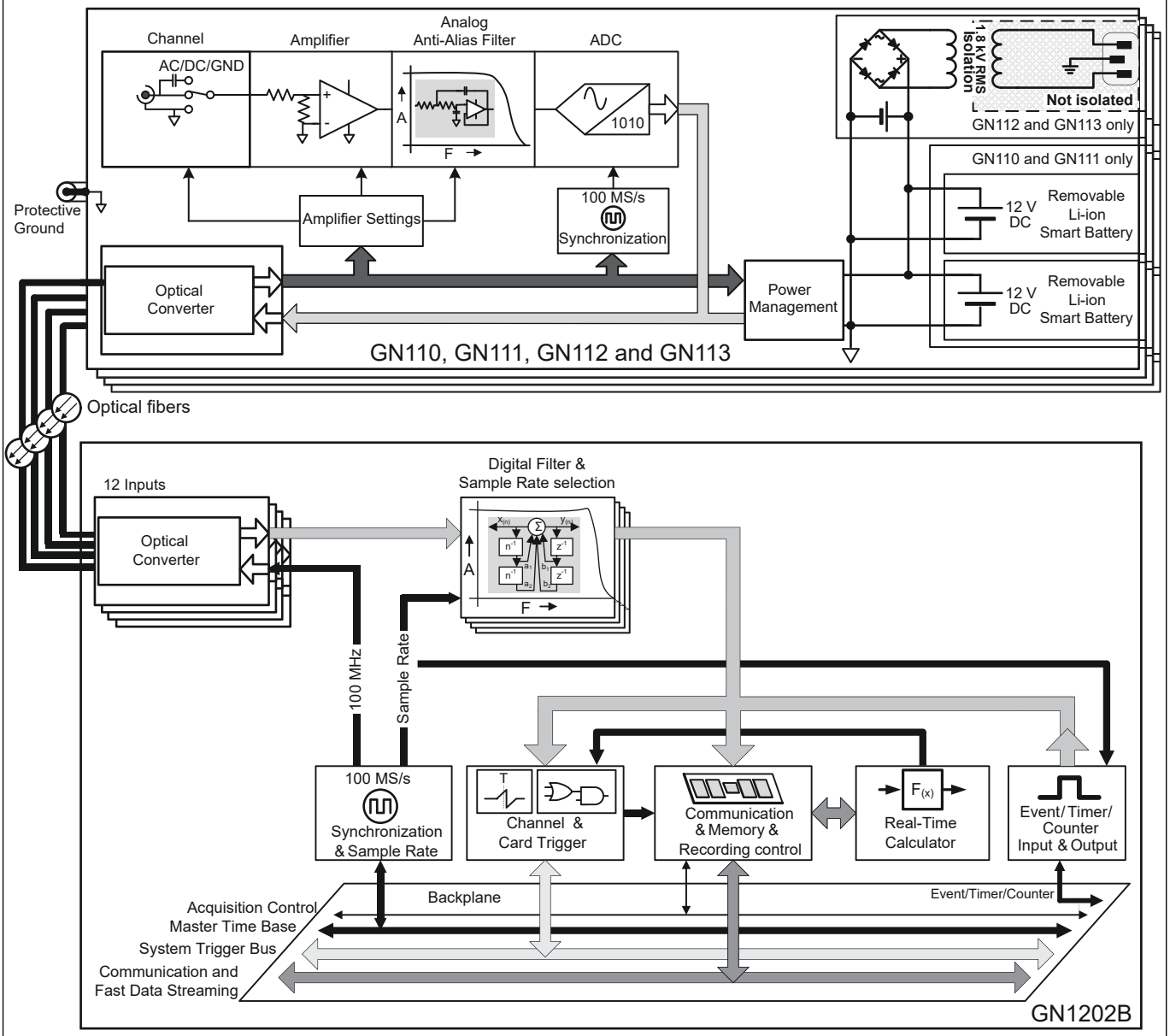


Figure A.133: Block Diagram

Typical and guaranteed specifications
The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification
In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards
The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input GN110, GN111, GN112 and GN113 (Transmitter)	
Channels	1
Connector	1; metal BNC
Input type	Isolated, unbalanced differential inputs (BNC connected to isolated common)
Input Coupling	
Coupling modes	AC / DC / GND
AC coupling frequency	1.6 Hz (±10%); - 3 dB

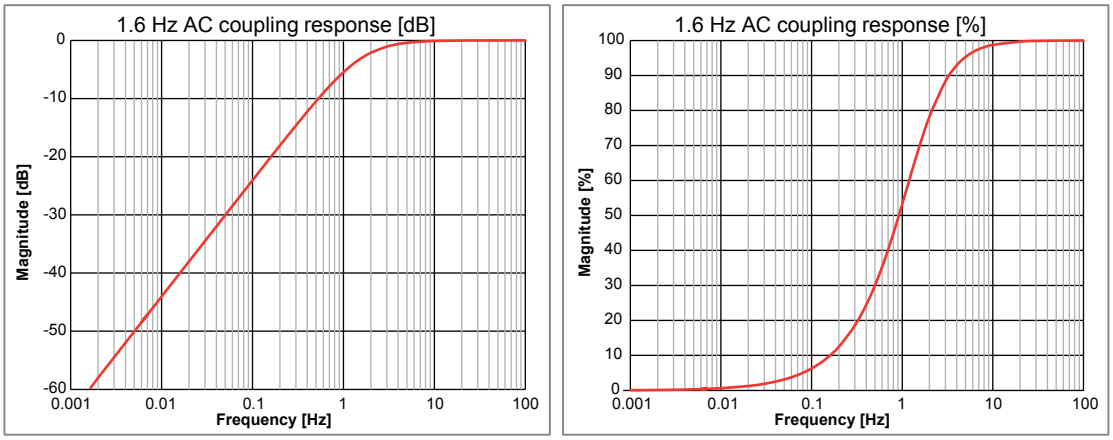


Figure A.134: Representative AC coupling response

Impedance	1 MΩ (± 2%) // 38 pF (± 5%)
Ranges	± 20 mV, ± 50 mV, ± 100 mV, ± 200 mV, ± 500 mV, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V, ± 50V and ± 100 V
Offset	± 50% in 1000 steps (0.1%) ± 100 V range has fixed 0% offset
DC Offset error	
Wideband	0.1% of Full Scale ± 50 µV
Bessel filter	0.1% of Full Scale ± 50 µV
Offset error drift	GN110 and GN111: ±(60 ppm + 10 µV)/°C (±(36 ppm + 6 µV)/°F) GN112 and GN113: ±(100 ppm + 10 µV)/°C (±(60 ppm + 6 µV)/°F)
DC Gain error	
Wideband	0.1% of Full Scale ± 50 µV
Bessel filter	0.1% of Full Scale ± 50 µV
Gain error drift	GN110 and GN111: ±100 ppm/°C (± 60ppm/°F) GN112 and GN113: ±(100 ppm + 10 µV)/°C (±(60 ppm + 6 µV)/°F)
Maximum static error (MSE)	
Wideband	0.1% of Full Scale ± 50 µV
Bessel filter	0.1% of Full Scale ± 50 µV
RMS Noise (50 Ω terminated)	
Wideband	0.05% of Full Scale ± 100 µV
Bessel filter	0.05% of Full Scale ± 100 µV
Common mode (referred to ground while protective ground is not connected) Requires a protected LAB environment and EN50191:2000 compliant work procedures	
Rejection (CMR)	> 72 dB @ 80 Hz (GN110 and GN111: > 100 dB typical)
Maximum common mode voltage	1.8 KV RMS (GN112 and GN113) >1.8 kV RMS (GN110 and GN111); Limits set by fiber cable and transmitter air gap isolation
Input bias current	< 2 nA
Rise time	14 ns

Analog Input GN110, GN111, GN112 and GN113 (Transmitter)	
Input overload protection	
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage remains less than 200% of the selected input range or 250 V, whichever value is the smallest.
Maximum nondestructive voltage	± 125 V DC; Ranges < ± 2 V ± 250 V DC; Ranges ≥ ± 2 V
Overload recovery time	Restored to 0.1% accuracy in less than 50 ns after 200% overload Restored to 10% accuracy in less than 10 ns after 200% overload

Analog to Digital Conversion	
Sample rate per channel	1 S/s to 100 MS/s
ADC resolution; one ADC per channel	14 bit
ADC type	CMOS pipelined multi step flash converter, LTC2254
Time base accuracy	Defined by mainframe: ± 3.5 ppm; aging after 10 years ± 10 ppm
Binary sample rate	Not supported
Maximum binary sample rate	N/A
External time base sample rate	0 S/s to 10 MS/s (See GEN series Isolated Digitizer manual for calculation details)
External time base level	TTL
External time base minimum pulse width	100 ns

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

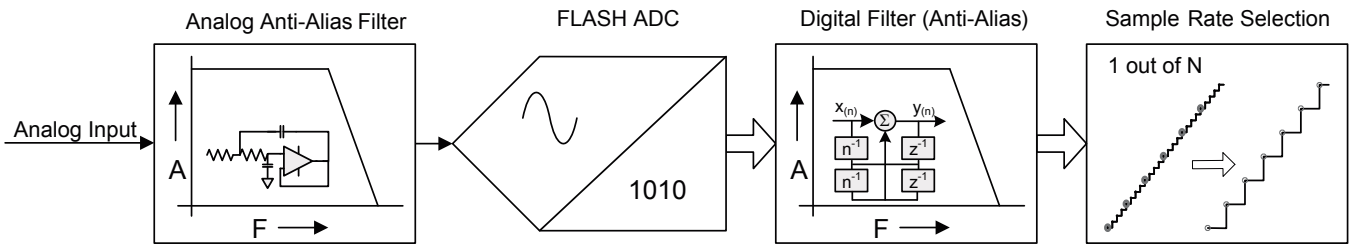


Figure A.135: Combined analog and digital anti-alias filter block diagram

Aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Wideband should not be used if working in a frequency domain with recorded data. Using wideband, enhanced resolution is not supported at lower sample rates.
Bessel (Fc @ -3 dB)	This analog Bessel filter can be used to reduce the higher bandwidth signals. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses. Using the Bessel filter, enhanced resolution is not supported at lower sample rates.
Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses. Enhanced resolution is supported by using oversampling combined with a digital filter at the following sample rates: 15 bit resolution at 25 MS/s and lower, 16 bit resolution at 10 MS/s and lower.
Butterworth IIR (Fc @ -3 dB)	When Butterworth IIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves. Enhanced resolution is supported by using oversampling combined with a digital filter at the following sample rates: 15 bit resolution at 25 MS/s and lower, 16 bit resolution at 10 MS/s and lower.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	Between 27 MHz and 36 MHz (-3 dB)
0.1 dB passband flatness (1)	DC to 3 MHz

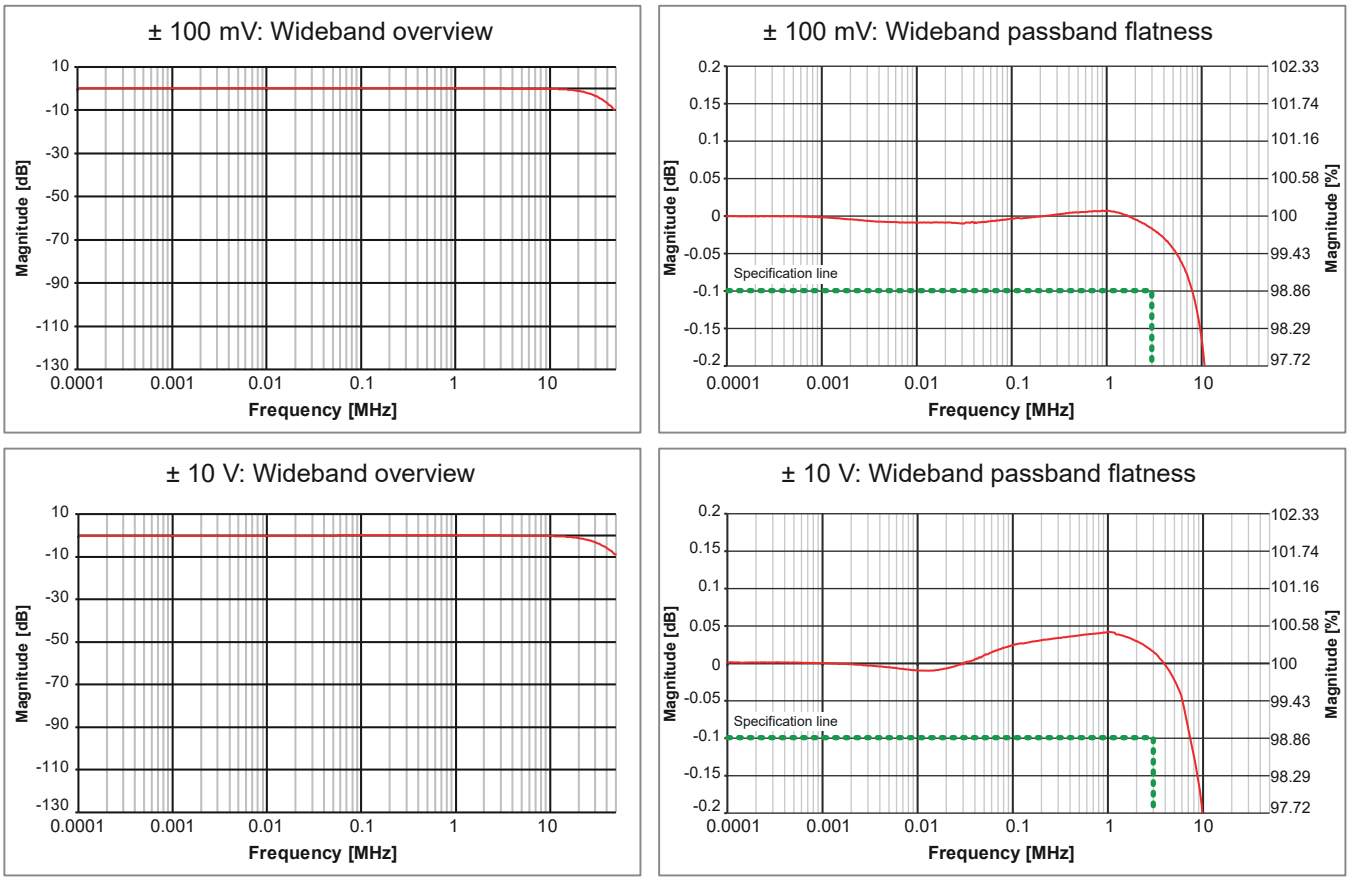
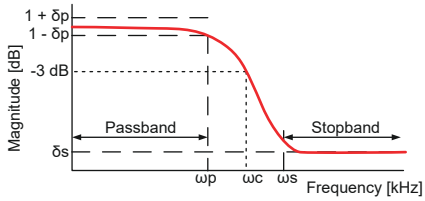


Figure A.136: Representative Wideband examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Bessel Filter (Analog Anti-Alias)

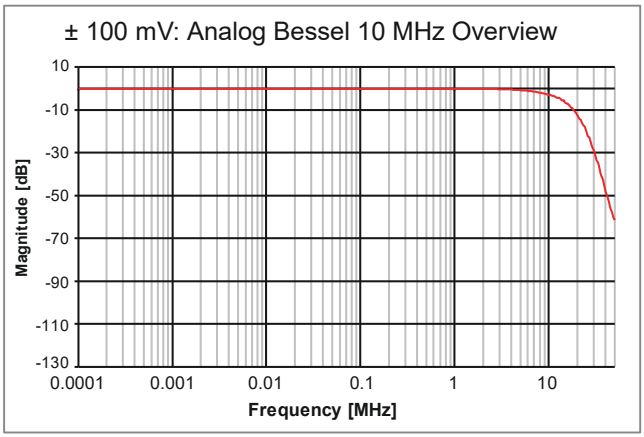


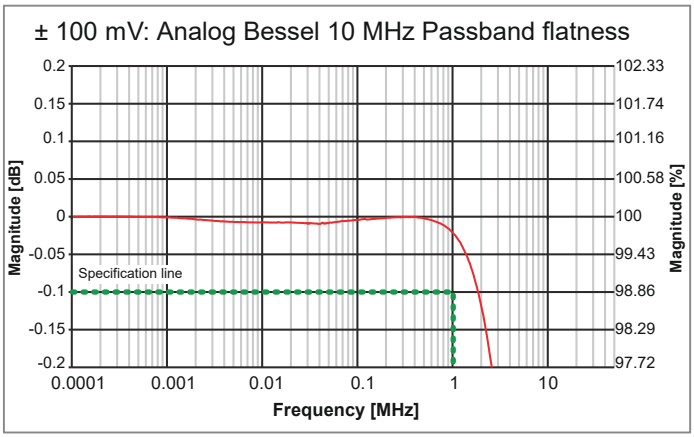
δp: Passband ripple
δs: Stopband attenuation

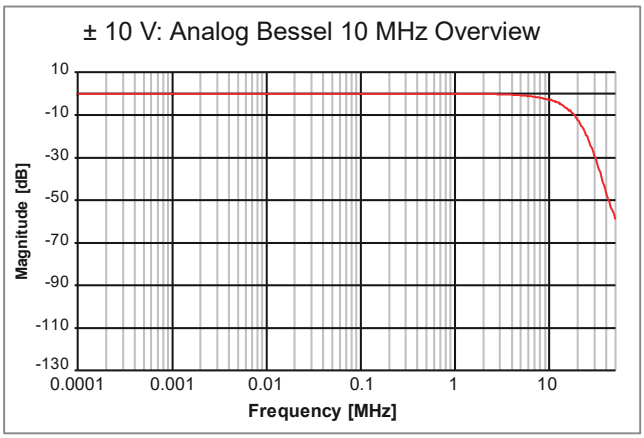
ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.137: Analog Bessel Filter

Analog Bessel filter	
Bandwidth	10 MHz ± 1 MHz (-3 dB)
Characteristic	6-pole Bessel, optimal step response
0.1 dB passband flatness (ωp)(1)	DC to 1 MHz
Stopband (δs)	-50 dB at ωs = 60 MHz
Analog Bessel filter roll-off:	-30 dB/Octave







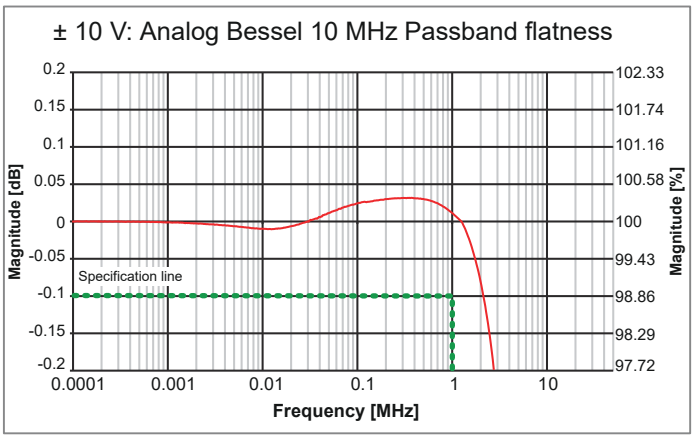
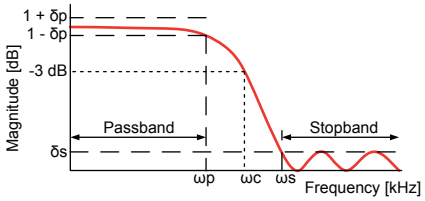


Figure A.138: Representative analog Bessel examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.139: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of the analog Bessel anti-alias filter and a digital Bessel IIR filter.	
Analog anti-alias filter	Bessel
Bessel IIR filter	
Characteristic	8-pole Bessel style IIR
User selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bandwidth (ωc)	User selectable from 50 Hz to 5 MHz
0.1 dB passband (ωp)(1)	DC to 0.16 * ωc
Stopband (δs)	-60 dB
Roll-off	-48 dB/Octave

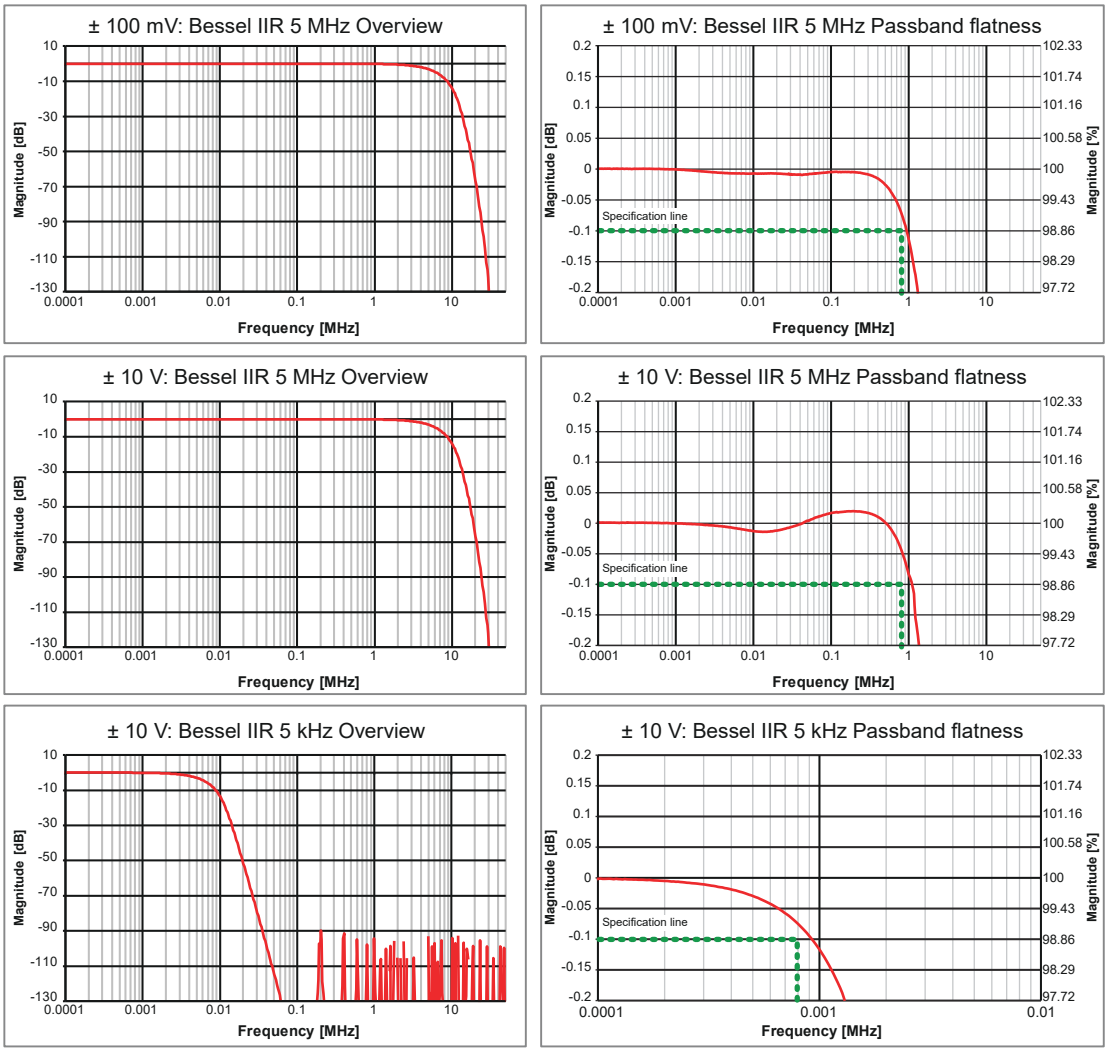
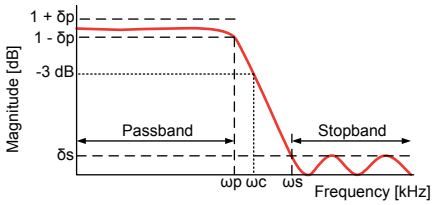


Figure A.140: Representative Bessel IIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)

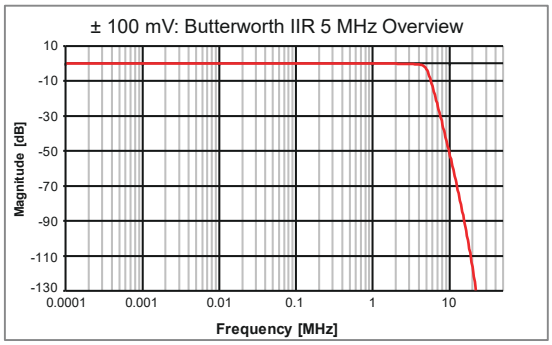


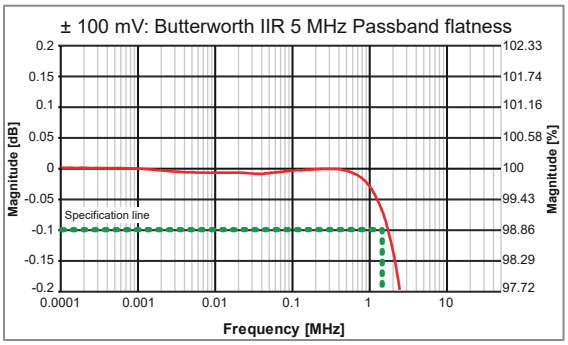
δp: Passband ripple
δs: Stopband attenuation

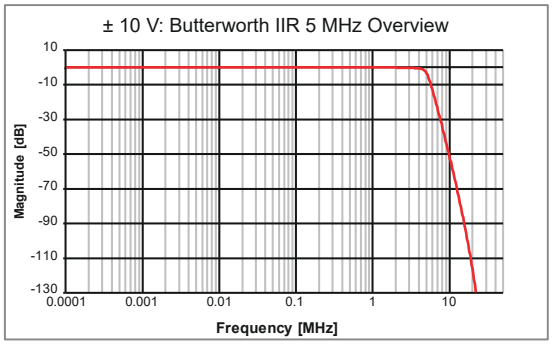
ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

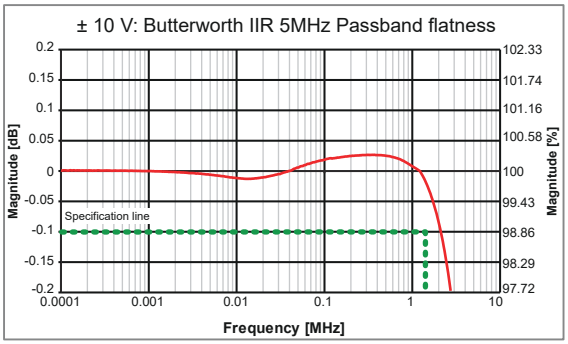
Figure A.141: Digital Butterworth IIR Filter

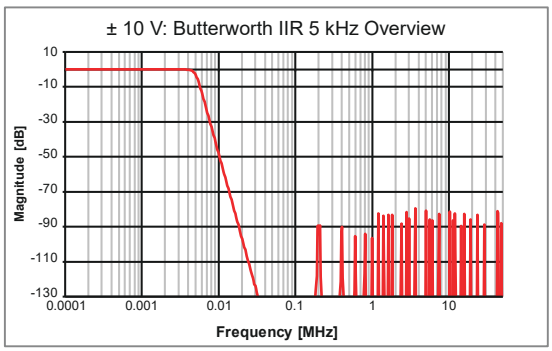
When Butterworth IIR filter is selected, this is always the combination of the analog Bessel anti-alias filter and a digital Butterworth IIR filter.	
Analog anti-alias filter	Bessel
Butterworth IIR filter	
Characteristic	8-pole Butterworth style IIR
User selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed
Bandwidth (ωc)	User selectable from 125 Hz to 5 MHz
0.1 dB passband (ωp)(1)	DC to 0.7 * ωc (for ωc > 1 MHz, DC to 0.3 * ωc, due to analog anti-alias filter bandwidth)
Stopband (δs)	-60 dB
Roll-off	-48 dB/octave











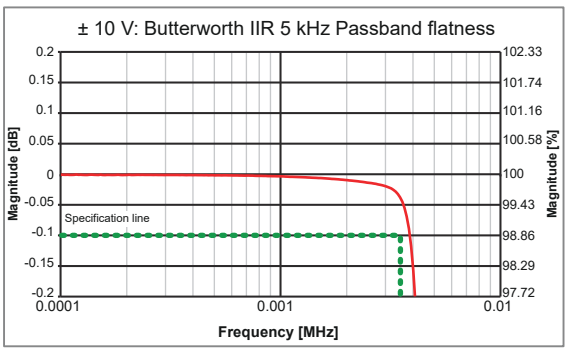


Figure A.142: Representative Butterworth IIR examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel/Bessel IIR/Butterworth IIR) or different filter bandwidths results in phase mismatches between channels.	
Channel to channel phase difference	Typical ± 10 ns with the same filter selections applied (≥ 100Hz)
Fiber cable length compensation	Yes, automatic when optical communication is established Optical cable delay is compensated to phase match standard GEN DAQ channels.
Typical fiber cable delay mismatch	± 20 ns
Fiber cable delay	5 ns/m; delay compensated by cable length compensation

On-Board Memory	
Per card	8 GB (4 GS)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size analog and digital event channels	16 bits, 2 bytes/sample
Storage sample size Timer/Counter channels	32 bits, 4 bytes/sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

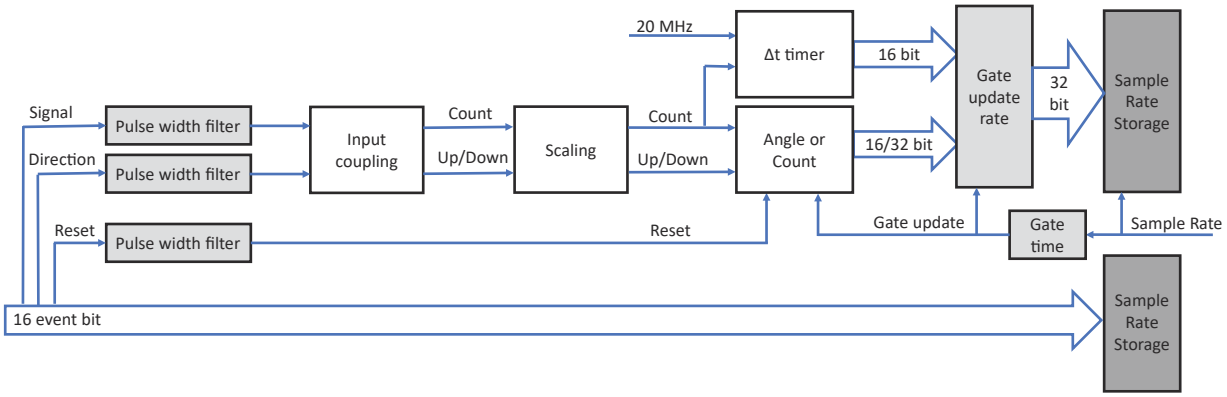


Figure A.143: Timer/Counter block diagram

Card Sample rate	Digital Event/Timer/Counter sample rate
≤10 MS/s	Sample rate
12.5 MS/s	Not supported
20 MS/s	Sample rate
25 MS/s	Not supported
40 MS/s	Not supported
50 MS/s	Not supported
100 MS/s	20 MS/s
Digital input events	16 per card
Levels	TTL input level, user programmable invert level
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs
Digital output events	2 per card
Output event 1	User selectable: Trigger, Alarm, set High or Low
Output event 2	User selectable: Recording active, set High or Low
Digital output event user selections	
Trigger	1 high pulse per trigger (on any channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay
Alarm	High when alarm condition is activated, low when not activated (alarm conditions of this card only) 200 µs ± 1 µs ± 1 sample period alarm event delay
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation
Timer/Counter	2 per card
Levels	TTL input levels
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)
Measurement modes	Count, Angle, Frequency and RPM (freq = count / Δt)

Input Coupling Uni- and Bi-directional Signal

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

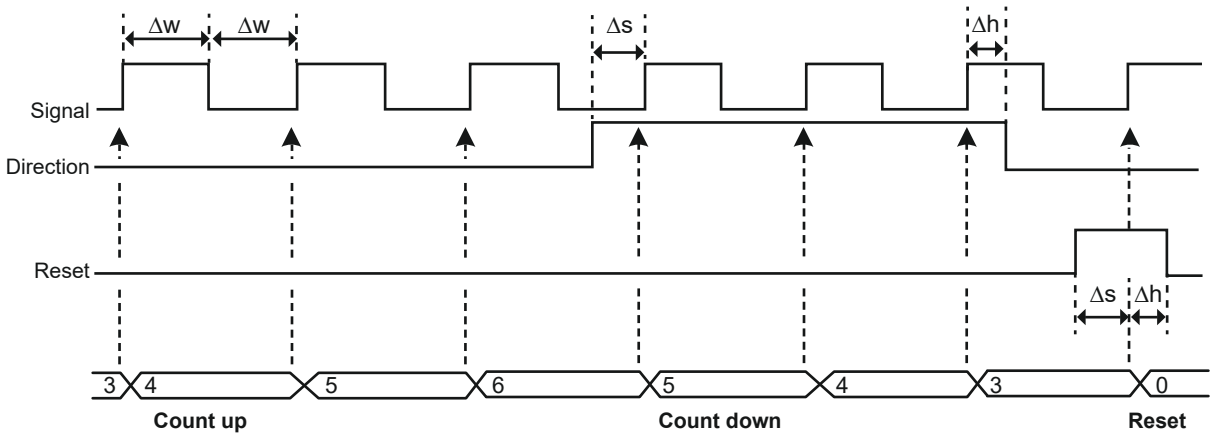


Figure A.144: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	4 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

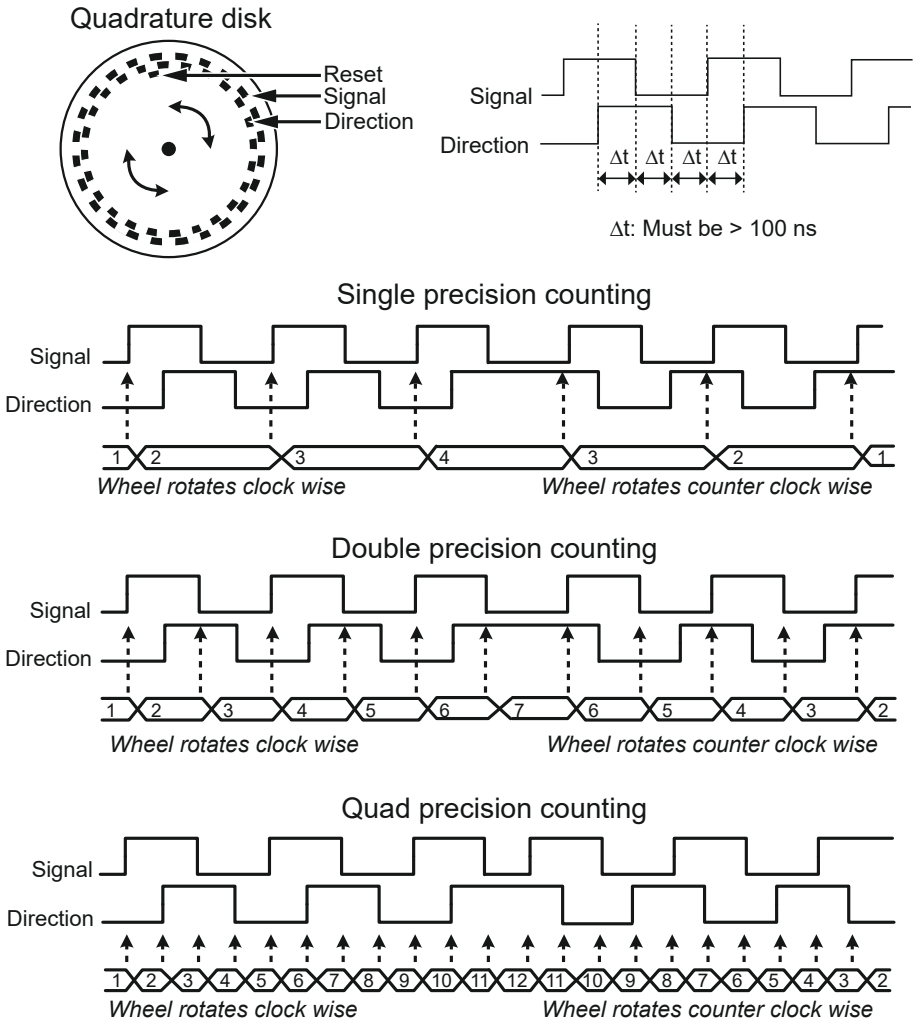


Figure A.145: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Count/Position	
Count/position mode is typically used for tracking movement of device under test. To reduce the sensitivity for count/position errors due to clock glitches use the minimum pulse width filter or enable the ABZ in stead of uni-/bi-polar input coupling .	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31} - 1$; bi-directional count

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to 1 GS
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1 GS after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per mainframe	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per mainframe	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (83 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Default 516 µs for decimal time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Off, Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	Selectable (83 µs to 516 µs) - 1 µs +/-1 µs + max 1 sample period

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)

The real-time formula database (RT-FDB) option offers an extensive set of math routines to enable almost any real-time mathematical challenge. The database structure enables the user to define a list of mathematical equations similar to the Perception review formula database.
The maximum supported sample rate is 2 MS/s.
The real-time formula database feature set is extended with higher Perception Versions. Different versions of Perception therefore can enable more or less features as described in this table.

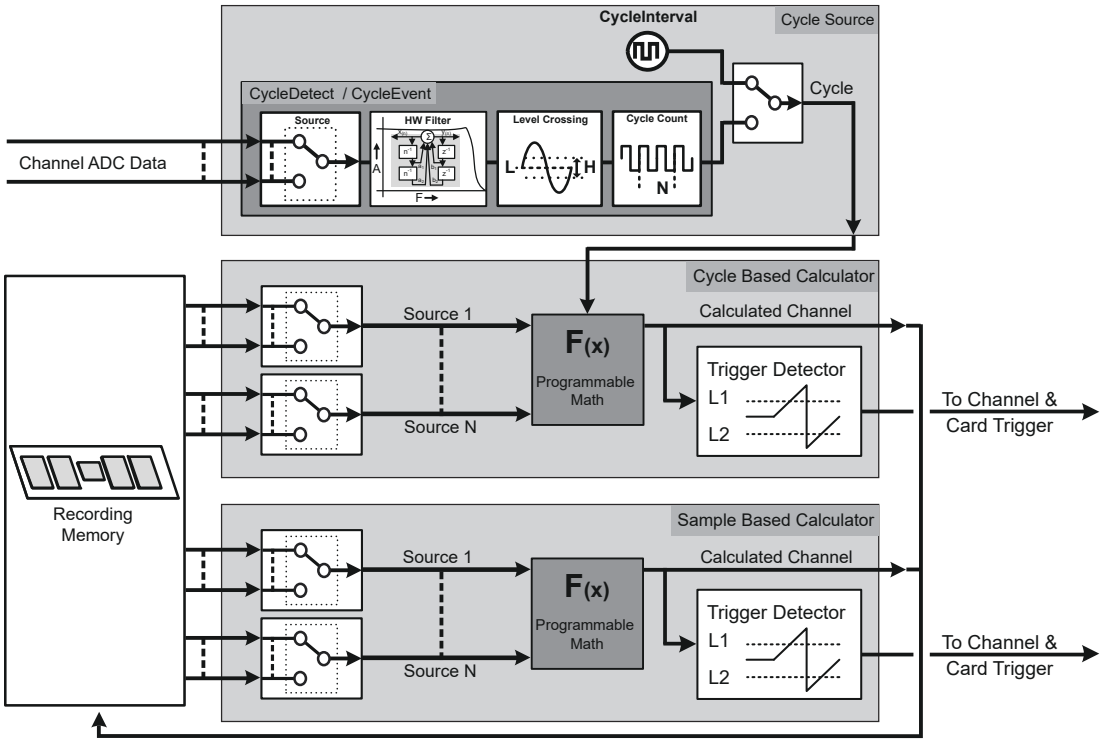


Figure A.146: Real-time formula database (RT-FDB) calculators

The real-time formula database supports the following list of calculations (Details of each calculation are described in the manual).

Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Basic calculations				
`+ (add)`	✓	✓	✓	✓(1)
`- (subtract)`	✓	✓	✓	✓(1)
`* (multiply)`	✓	✓	✓	✓(1)
`/ (divide)`	✓	✓	✓	✓(1)
Enhanced calculations				
`Abs`	✓	✓	✓	✓(1)
`Atan`	✓	✓	✓	✓(1)
`Atan2`	✓	✓	✓	✓(1)
`Cosine`	✓	✓	✓	✓(1)
`DegreesToRadians`	✓	✓	✓	✓(1)
`Min`	✓	✓	✓	✓(1)
`Max`	✓	✓	✓	✓(1)
`Modulo`	✓	✓	✓	✓(1)
`RadiansToDegrees`	✓	✓	✓	✓(1)
`Sine`	✓	✓	✓	✓(1)
`Sqrt`	✓	✓	✓	✓(1)
`Tan`	✓	✓	✓	✓(1)

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Boolean calculations				
`Equal`	✓	✓	✓	✓
`GreaterEqualThan`	✓	✓	✓	✓
`GreaterThan`	✓	✓	✓	✓
`LessEqualThan`	✓	✓	✓	✓
`LessThan`	✓	✓	✓	✓
`NotEqual`	✓	✓	✓	✓
`InsideBand`	✓	✓	✓	
`OutsideBand`	✓	✓	✓	
`And`	✓	✓	✓	✓
`Or`	✓	✓	✓	✓
`Xor`	✓	✓	✓	✓
`Not`	✓	✓	✓	✓
Cycle based calculations				
`CycleArea`		✓	✓	✓
`CycleBusDelay`		✓	✓	✓
`CycleCount`		✓	✓	✓
`CycleCrestFactor`		✓	✓	✓
`CycleEnergy`		✓	✓	✓
`CycleFundamentalPhase`		✓	✓	✓(2)
`CycleFundamentalRMS`		✓	✓	✓
`CycleFrequency`		✓	✓	✓
`CycleMax`		✓	✓	✓
`CycleMean`		✓	✓	✓
`CycleMin`		✓	✓	✓
`CyclePeak2Peak`		✓	✓	✓
`CyclePhase`		✓	✓	✓
`CycleRMS`		✓	✓	✓
`CycleRPM`		✓	✓	✓
`CycleSampleCount`		✓	✓	✓
`CycleTHD`(2)		✓	✓	✓(2)
Cycle source				
`CycleDetect`(4)		✓	✓	
`CycleEvent`		✓	✓	
`CycleInterval`		✓	✓	

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Hardware based signal filtering				
`HWFilter`(4)	✓		✓	
Software based signal filtering				
`FilterBesselBP`	✓		✓	
`FilterBesselHP`	✓		✓	
`FilterBesselLP`	✓		✓	
`FilterButterworthBP`	✓		✓	
`FilterButterworthHP`	✓		✓	
`FilterButterworthLP`	✓		✓	
`FilterChebyshevBP`	✓		✓	
`FilterChebyshevHP`	✓		✓	
`FilterChebyshevLP`	✓		✓	
Special category calculation				
`HarmonicsIEC61000`	✓		✓	
`Integrate`	✓		✓	
Signal transformation				
`DQZeroTransformation (Park)` (3)	✓		✓	✓(1)
`SpaceVectorTransformation`(3)	✓		✓	
`SpaceVectorInverse Transformation`(3)	✓		✓	
Signal generation				
`SineWave`	✓		✓	
`Ramp`	✓		✓	
Trigger functions				
`TriggerOnBooleanChange`			Trigger mark	
`TriggerOnLevel`			Trigger mark	

(1) Only cycle based results can be used for real-time output. Use the CycleMean calculation on recorded channel data or sample based results to enable the real-time output of this data.

(2) The time required to calculate the output depends on maximum cycle length and sample rate. Depending on the selected settings the output latency will increase. HBM refers to these calculations as not deterministic. All real-time output published values (deterministic and/or not deterministic) will always have the same latency.

(3) This formula is only available if the eDrive license is added to Perception.

(4) The output of HWFilter is used for CycleDetect.

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1 GS after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Single sweep	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	9 channels	10 channels	11 channels	12 channels	12 channels 1 Timer/Counter	12 channels 2 Timer/Counters	12 channels 2 Timer/Counters Digital events
Maximum sweep memory	1000 MS	1000 MS	1000 MS	950 MS	750 MS	620 MS	525 MS	450 MS	395 MS	350 MS	310 MS	280 MS	235 MS	205 MS	190 MS
Maximum sample rate	100 MS/s														

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1 GS after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Multi sweep	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	9 channels	10 channels	11 channels	12 channels	12 channels 1 Timer/Counter	12 channels 2 Timer/Counters	12 channels 2 Timer/Counters Digital events
Maximum sweep memory	1000 MS	1000 MS	1000 MS	950 MS	750 MS	620 MS	525 MS	450 MS	395 MS	350 MS	310 MS	280 MS	235 MS	205 MS	190 MS
Maximum sample rate	100 MS/s														

Continuous

Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Continu-ous	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	9 channels	10 channels	11 channels	12 channels	12 channels 1 Timer/Counter	12 channels 2 Timer/Counters	12 channels 2 Timer/Counters Digital events
Maximum FIFO	3800 MS	1800 MS	1200 MS	900 MS	720 MS	600 MS	510 MS	450 MS	400 MS	360 MS	320 MS	280 MS	230 MS	210 MS	190 MS
Maximum sample rate	25 MS/s												20 MS/s (Timer/Counter limitation)		
Maximum aggregate streaming rate	25 MS/s	50 MS/s	75 MS/s	100 MS/s	125 MS/s	150 MS/s	175 MS/s	200 MS/s	225 MS/s	250 MS/s	275 MS/s	300 MS/s	280 MS/s	320 MS/s	340 MS/s

Dual

Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length. If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1 GS after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off. When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended posttrigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	9 channels	10 channels	11 channels	12 channels	12 channels 1 Timer/Counter	12 channels 2 Timer/Counters	12 channels 2 Timer/Counters Digital events
Maximum sweep memory	1000 MS	1000 MS	1000 MS	760 MS	595 MS	490 MS	410 MS	355 MS	310 MS	275 MS	245 MS	220 MS	185 MS	160 MS	148 MS
Maximum sweep sample rate	100 MS/s														
Maximum FIFO	800 MS	400 MS	260 MS	180 MS	144 MS	120 MS	103 MS	89 MS	75 MS	68 MS	61 MS	55 MS	46 MS	40 MS	37 MS
Maximum continous sample rate	25 MS/s												20 MS/s (Timer/Counter limitation)		
Maximum aggregate streaming rate	25 MS/s	50 MS/s	75 MS/s	100 MS/s	125 MS/s	150 MS/s	175 MS/s	200 MS/s	225 MS/s	250 MS/s	275 MS/s	300 MS/s	280 MS/s	320 MS/s	340 MS/s

G091: 2 Gbit Optical SFP Module Multi Mode 850 nm (Option to be ordered seperately)

Small Form-factor Pluggable (SFP) optical transceiver for GN1202B and GEN2tB (Master/Slave option)

WARNING
Use HBM approved transceivers only.

Data rate	2.125 Gbps
Wavelength	850 nm
Input connector	LC
Form factor	SFP
Laser class	1
Original manufacturer's part number	Finisar FTLF8519P3BNL
To fulfill the laser class requirements, the transceiver must be used under the following conditions:	
Storage temperature	-40 °C to +85 °C
Case operating temperature	-20 °C to +85 °C

Fiber Optic Link

Light source	Class 1 laser product
Transfer rate	2.125 Gbit/s
Wavelength	850 nm
Connector	LC duplex on GN1202B SCRJ/IP67 duplex on GN110, GN111, GN112 and GN113
Cable	
Isolation	10^{15} Ω/m
Type	Duplex Multi Mode, 50/125 µm, ISO/IEC 11801 type OM2, OM3 or OM4
Coupler	LC duplex or SCRJ/IP67 duplex
Maximum cable length For every extra coupler used subtract 200 m (656 ft). Refer to the GEN series Isolated Digitizer manual for details on maximum length calculations.	
ISO/IEC 11801 type OM2	500 m (1640 ft) no extra cable couplers used 300 m (984 ft) 1 additional cable coupler used
ISO/IEC 11801 type OM3	1000 m (3280 ft) no extra cable couplers used 800 m (2624 ft) 1 additional cable coupler used

Power Requirement GN110 and GN111 (Transmitter)

Battery powered	Maximum 2 removable batteries possible **Note** *Use HBM approved batteries only. See option G034 for approved battery details.*
Power consumption	6 VA typical, 8 VA maximum
Operation Time (using G034 batteries)	30 hours; 2 batteries installed (15 hours; 1 battery installed) Perception software can activate a low power sleep mode to extend the operation time

Power Requirement GN112 and GN113 (Transmitter)

Power supply	115/230 V AC @ 47 - 63 Hz (manual voltage selector)
Power consumption	12 VA maximum
Power supply isolation	
Protective ground connected	0 V, both sides grounded
Protective ground not connected	1.8 kV RMS (IEC 61010-1:2010) Requires a protected LAB environment and EN50191:2000 compliant work procedures
Fuse(s)	2 x 250 mA; Slow blow
Battery	12 V @ 300 mAh; Internal, rechargeable, NiMH
Battery back-up time	5 minutes (with new and fully charged battery)

Physical, Weight and Dimensions GN110 and GN111	
Weight	4.6 kg (10 lb) including two batteries
Dimensions including handles	175 mm (6.89") x 277 mm (10.91") x 119 mm (4.69") (W x D x H)
Battery carrier	2 (batteries need to be ordered separately)
Shielding and casing	Single metal shielding in plastic housing. Correct operation has been verified by placing the transmitter cabinet within 1 meter of an EMC field created by a 80 kA current
Cooling fans	0
Handle	One carrying handle
Protective ground	M6 screw terminal

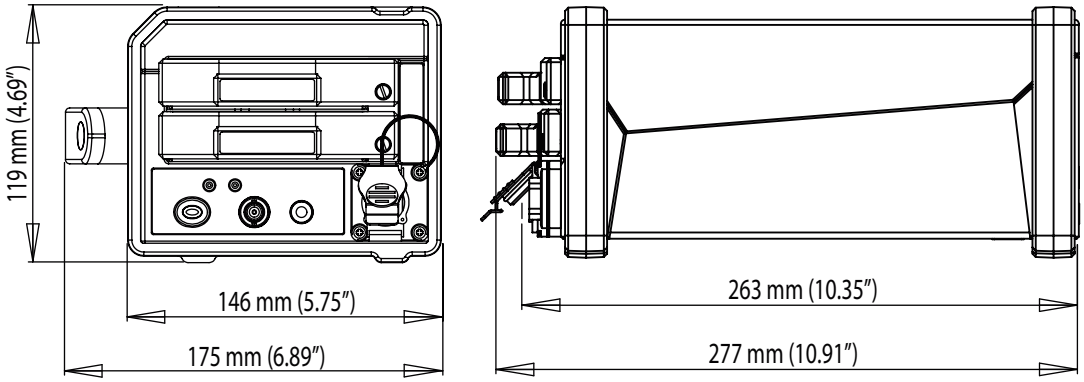


Figure A.147: Dimensions GN110 and GN111 transmitter

Physical, Weight and Dimensions GN112 and GN113	
Weight	3 kg (6.6 lb)
Dimensions including handles	175 mm (6.89”) x 267 mm (10.51”) x 119 mm (4.69”) (W x D x H)
Shielding and casing	Single metal shielding in plastic housing. Correct operation has been verified by placing the transmitter cabinet within 1 meter of an EMC field created by a 80 kA current
Cooling fans	1
Handle	One carrying handle
Protective ground	M6 screw terminal

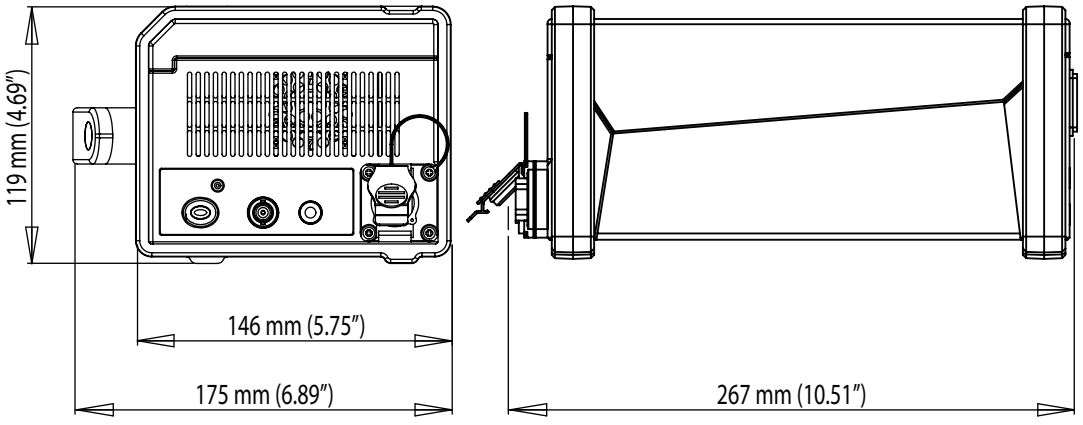


Figure A.148: Dimensions GN112 and GN113 transmitter

Environmental Specifications	
Temperature Range	
Operational	GN110 and GN111: -15 °C to +50 °C (+5 °F to +122 °F) GN112 and GN113: 0 °C to +40 °C (+32 °F to +104 °F) GN1202B: 0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives	
Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2011)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2011)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 10 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.8 B3240-3.1 en (GEN series GN3210)

Capabilities Overview	
Model	GN3210
Maximum sample rate per channel	250 kS/s
Memory per card	2 GB
Analog channels	32
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16/24 bit
Isolation	Not supported
Input type	Analog balanced differential
Passive voltage/current probes	Passive, single-ended voltage probes Passive, differential matched voltage probes
Sensors	IEPE and charge
TEDS	Class 1, IEPE sensors
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Not supported
Real-time calculated results output	Not supported
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels
Standard data streaming (CPCI up to 200 MB/s)	Yes, supported by all GEN series mainframes
Fast data streaming (PCIe up to 1 GB/s)	Not supported
Slot width	1

Block Diagram

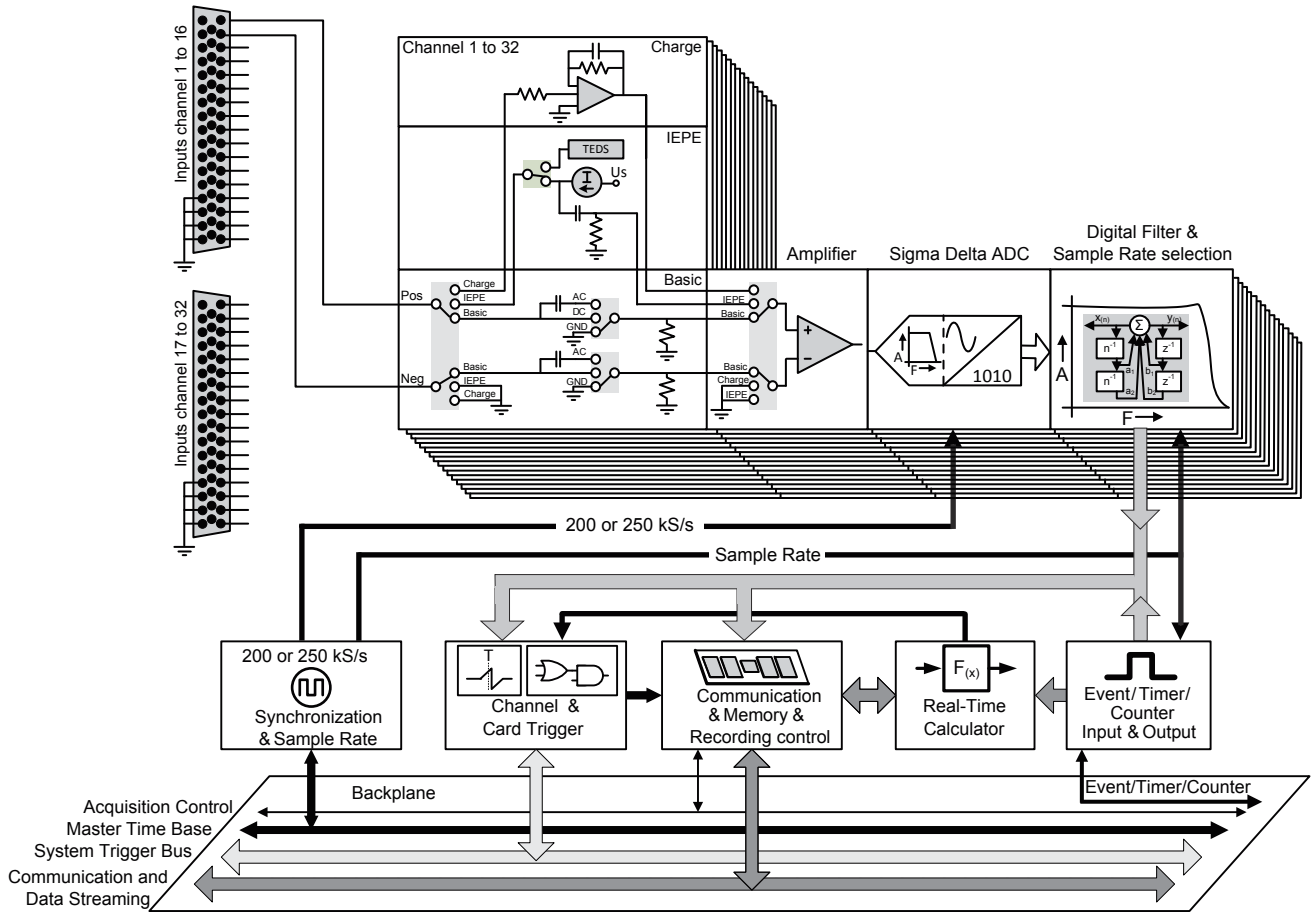


Figure A.149: Block diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input Section	
Channels	32
Connectors	D-Sub (DD-50) connector
Input type	Analog isolated balanced differential
Input coupling	Differential, single-ended (positive or negative)
Signal input coupling	
Coupling modes	AC, DC, GND
AC coupling frequency	1.6 Hz ± 10%; - 3 dB

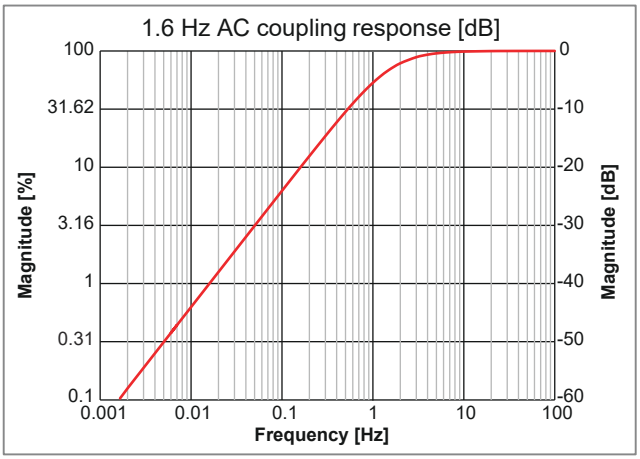


Figure A.150: Representative AC coupling response

Impedance	2 x 1 MΩ ± 0.5% // 75 pF ± 15%
Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Offset	± 50% in 1000 steps (0.1%); ± 20 V range has fixed 0% offset
DC Offset error	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV
Offset error drift	±(10 ppm + 2 µV)/°C (±(6 ppm + 1.5 µV)/°F)
DC Gain error	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
Gain error drift	± 10 ppm/°C (± 6 ppm/°F)
Maximum static error (MSE)	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
RMS Noise (50 Ω terminated)	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV

Analog Input Section

Common mode (referred to system ground)		
Ranges	Less than ± 2 V	Larger than or equal to ± 2 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	2 V RMS	33 V RMS

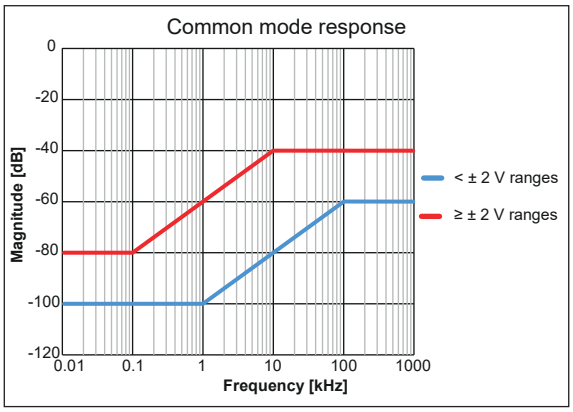


Figure A.151: Representative common mode response

Input overload protection	
Over voltage impedance change	The activation of the over voltage protection system will result in a reduced input impedance. The over voltage protection will not be active as long as the input voltage is less than 200% of the selected input range or 50 V DC whichever is the smallest value.
Maximum nondestructive voltage	± 50 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

Input Ranges When Using Passive Voltage Probes

Detailed probe specifications can be found at the end of this datasheet	
Single-ended	**Added voltage ranges**
G901 (10:1 divide factor)	± 50 V, ± 100 V, ± 200 V
G902 (10:1 divide factor)	± 50 V, ± 100 V, ± 200 V
G903 (100:1 divide factor)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV
G904 (100:1 divide factor)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV
G906 (1000:1 divide factor)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV, ± 5 kV, ± 10 kV (± 20 kV @ DC to 60 Hz)
Differential matched	**Added voltage ranges**
G907 (10:1 divide factor)	± 50 V, ± 100 V, ± 200 V

Input Ranges When Using Active Differential Voltage Probes

G909 (20:1 divide factor)	± 140 V RMS input and ± 1000 V RMS common mode
G909 (200:1 divide factor)	± 1000 V RMS input and ± 1000 V RMS common mode

Input Ranges When Using Current Clamps

Detailed probe specifications can be found at the end of this datasheet	
Clamp type	**Added current ranges**
G912 (AC/DC)	± 30 mA to ± 30 A DC ± 30 mA to ± 20 A RMS
G913 (AC)	± 100 mA to ± 1000 A RMS
G914 (AC)	± 50 mA to ± 20 A RMS

IEPE Sensor	
In IEPE mode the negative input of each channel is internally grounded. Best measurement results can be obtained if the negative input pin of each channel is used for the coaxial ground/shield. The return current then flows straight to the channel ground and not to the common card ground.	
Input ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Over voltage protection	- 1 V to 22 V DC
IEPE gain error	0.1% of Full Scale ± 300 µV
IEPE gain error drift	± 10 ppm/°C (± 6 ppm/°F)
IEPE compliance voltage	≥ 22 V
Excitation current	2, 4, 6, 8 mA, software selectable
Excitation current accuracy	± 5%
Coupling time constant	1.5 s
-3 dB high pass bandwidth	0.11 Hz
Maximum cable length	100 m (RG-58)
Wire diagnostics	Open and shorted IEPE wiring detected (Requires Perception V7.00 or higher)
TEDS support	Class 1, including software selectable auto detect the presence of an attached sensor

Charge Amplifier	
In charge mode the negative input of each channel is internally grounded. Best measurement results can be obtained if the negative input pin of each channel is used for the coaxial ground/shield. The return current then flows straight to the channel ground and not to the common card ground.	
Input ranges	± 10 pC, ± 20 pC, ± 50 pC, ± 100 pC, ± 200 pC, ± 0.5 nC, ± 1 nC, ± 2 nC
Over voltage protection	± 20 V DC
Charge gain error	± 2% of Full Scale
Charge gain error drift	± 30 ppm/°C (± 17 ppm/°F)
-3 dB high pass bandwidth limit	1 Hz
-3 dB low pass bandwidth limit	33 kHz ± 10% when a 650 pF source capacity is used 106 kHz ± 10% when a 250 pF source capacity is used
TEDS support	No

Channel Earthing

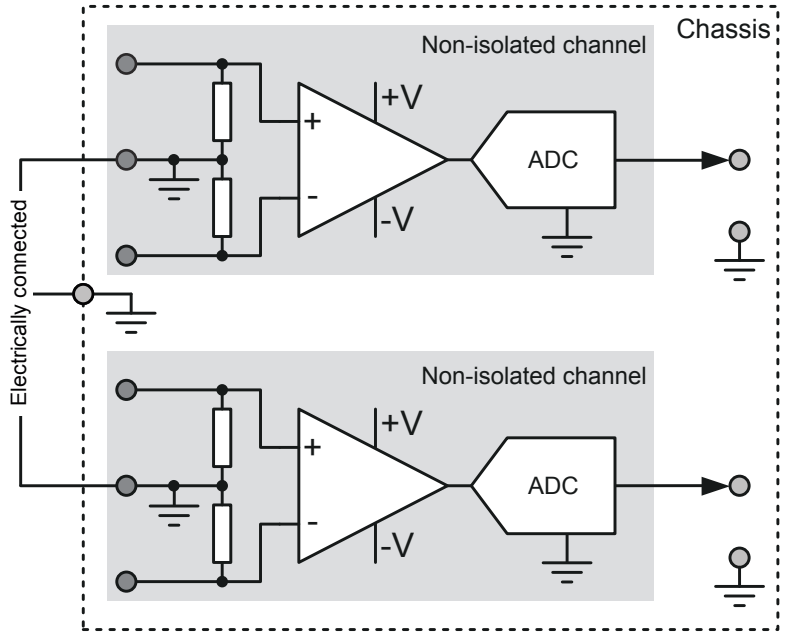


Figure A.152: Earthing schematic

Analog to Digital Conversion

Sample rate; per channel	1 S/s to 250 kS/s
ADC resolution; one ADC per channel	24 bit
ADC type	Sigma Delta (Σ-Δ) ADC; Analog Devices AD7764BRUZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; produces rounded BIN values when calculating FFT's
Maximum binary sample rate	256 kS/s
External time base frequency	0 S/s to 25 kS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ±30 ppm.

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

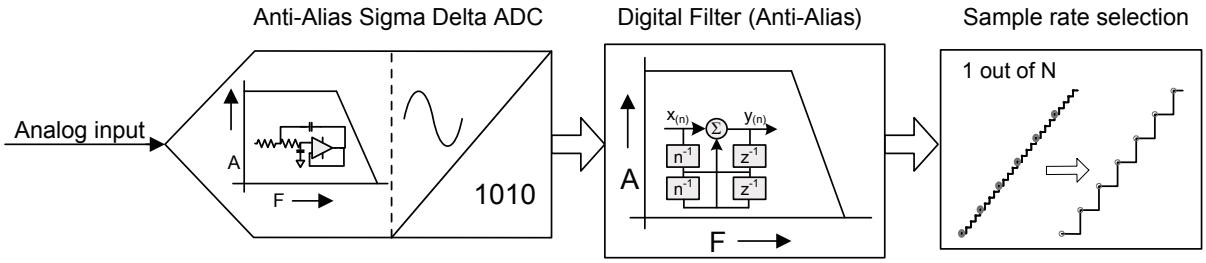


Figure A.153: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter integrated inside the Sigma Delta Analog to Digital Converter (ADC) always sampling at a fixed sample rate. This setup avoids the need for other analog anti-alias filters.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Sigma Delta Wideband	When Sigma Delta wideband is selected the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) is always in the signal path. Therefore, the anti-alias protection is always active when Sigma Delta wideband is selected.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Bessel IIR filter. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Butterworth IIR filter. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Elliptic IIR filter. This filter is best used when working in the frequency domain. When working in the time domain, this is best used for signals that are (close to) sine waves.
Elliptic Bandpass IIR	When Elliptic Bandpass IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Elliptic Bandpass IIR filter. Elliptic Bandpass filters are best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Sigma Delta Wideband (Analog Anti-Alias)

When Sigma Delta wideband is selected there is always the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) in the signal path. Therefore there is always anti-alias protection when wideband is selected. Care must be taken as this filter introduces slight overshoots on square wave or pulse response signals. Signals of sine wave type will not be effected.

Wideband

Characteristic	Sigma delta, optimal frequency response
-3 dB Bandwidth	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
0.1 dB passband flatness(1)	DC to 20 kHz

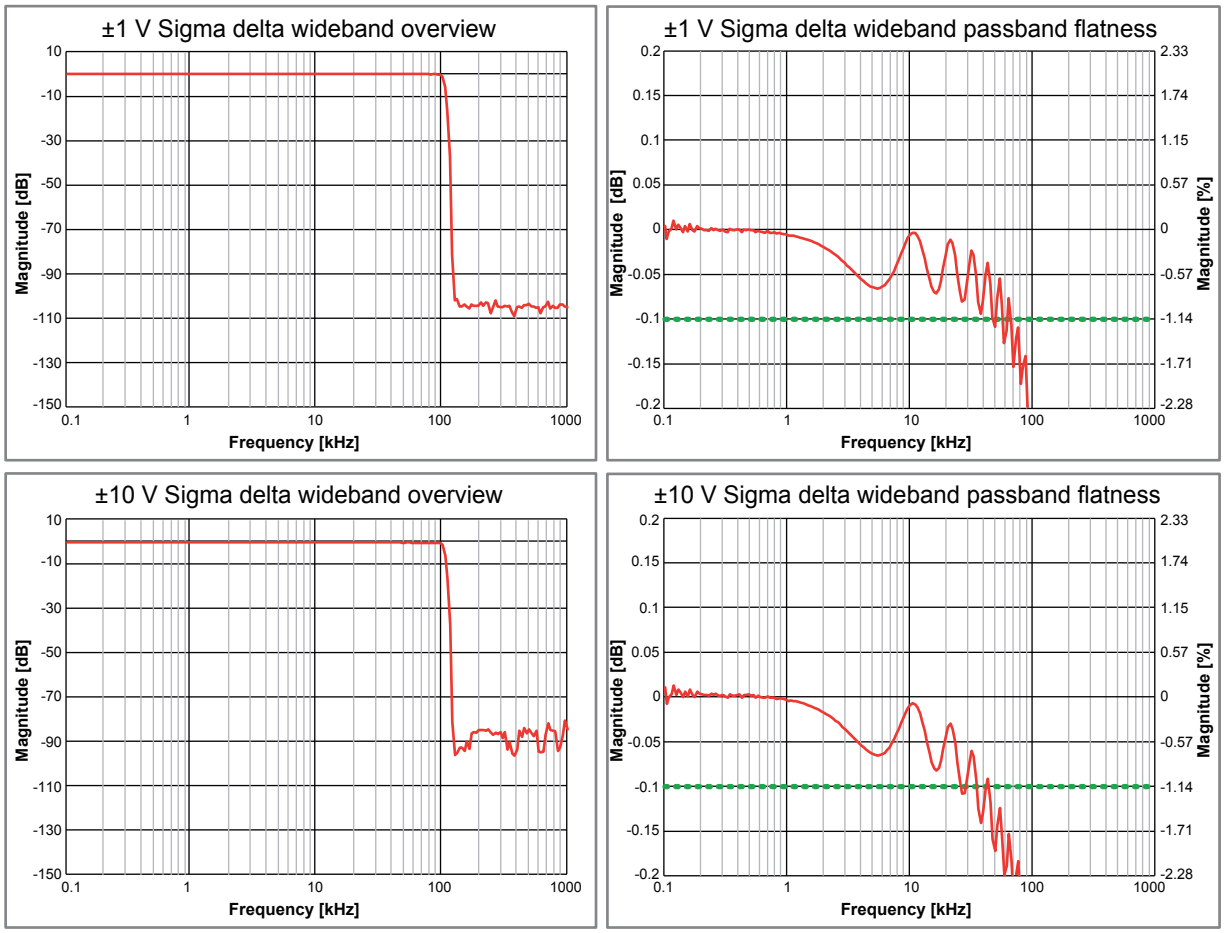
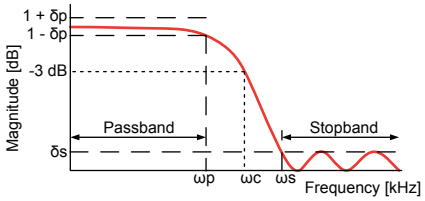


Figure A.154: Representative Sigma Delta Wideband examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.155: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Bessel IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Bessel IIR Filter	
Characteristic	12-pole Bessel style IIR 8-pole Bessel style IIR filter frequencies ωc = 25 kHz and ωc = 12.5 kHz
User selection	Auto tracking to sample rate divided by: 10, 20, 40, 100 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	User selectable from 40 Hz to 25 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/10
Stopband attenuation (δs)	80 dB
Roll-off	72 dB/octave for 12-pole filters; 48 dB/octave for 8-pole filters

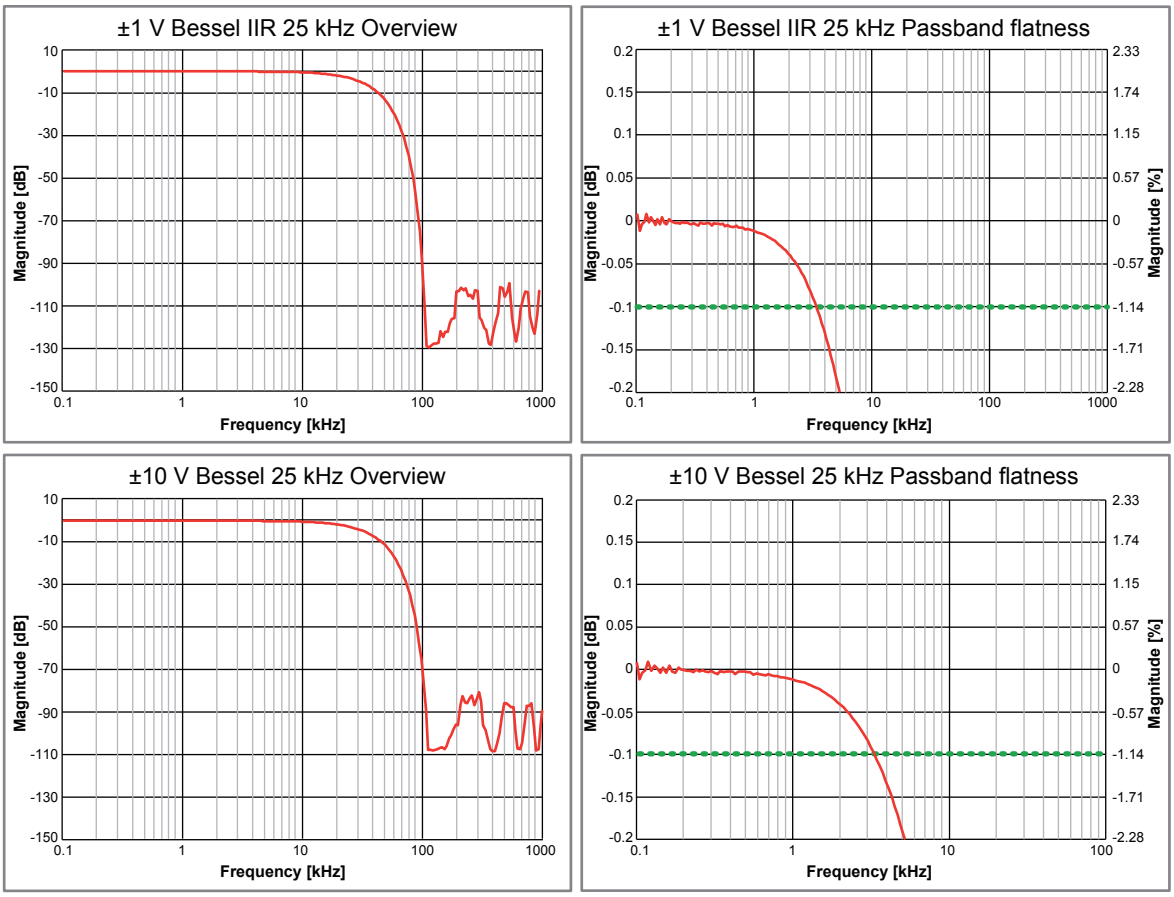
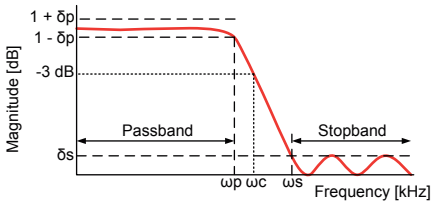


Figure A.156: Representative Bessel IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.157: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Butterworth IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Butterworth IIR Filter	
Characteristic	12-pole Butterworth style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed.
Bandwidth (ωc)	User selectable from 100 Hz to 62.5 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/2 or maximum 10 kHz
Stopband attenuation (δs)	80 dB
Filter roll-off	72 dB/octave

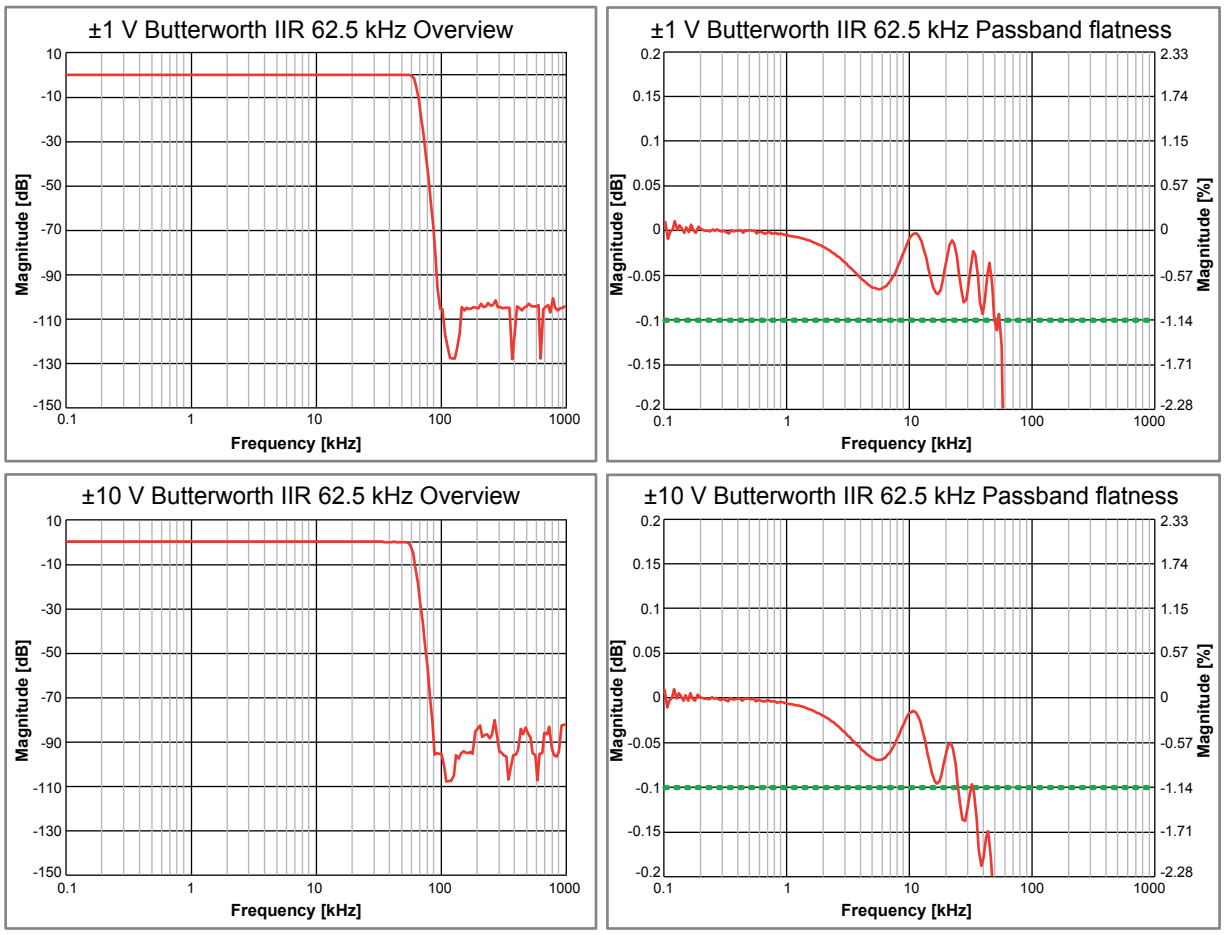
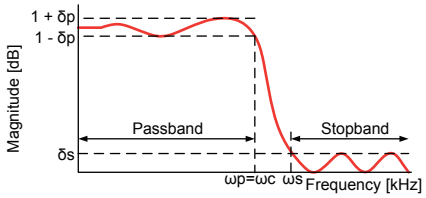


Figure A.158: Representative Butterworth IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.159: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Elliptic IIR Filter	
Characteristic	11th order Elliptic style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	100 Hz to 62.5 kHz
Stopband frequency (ωs)	Approximately 1.25 * ωc
0.1 dB passband flatness (ωp)(1)	DC to ωc/1.5 or maximum 10 kHz
Stopband attenuation (δs)	80 dB

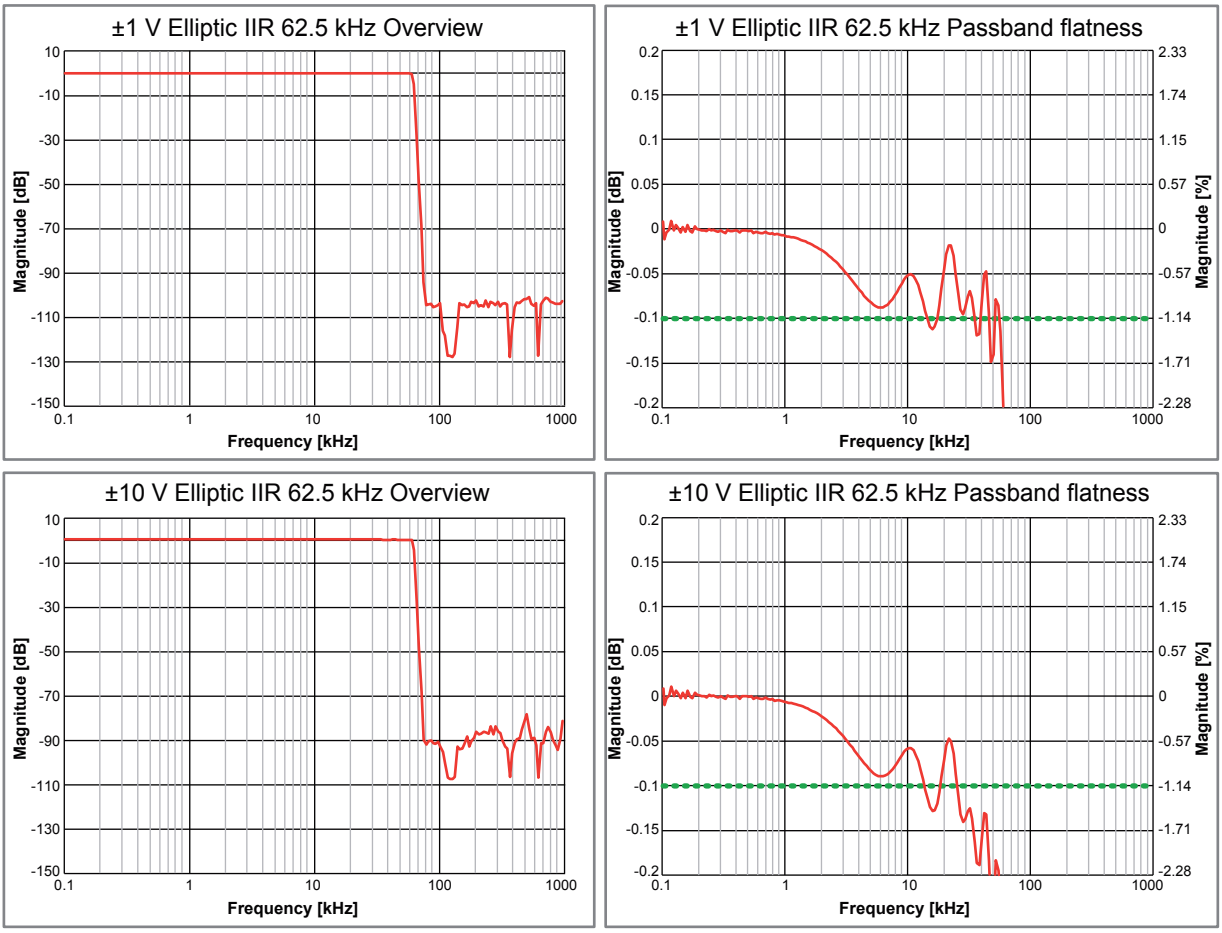
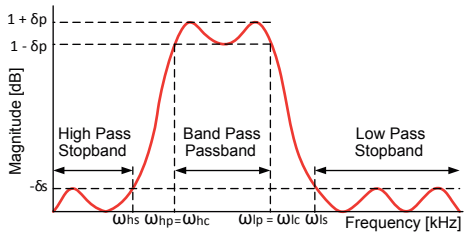


Figure A.160: Representative Elliptic IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Elliptic IIR Bandpass Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.161: Digital Elliptic IIR Bandpass Filter

When Elliptic IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Elliptic IIR bandpass filter	
Characteristic	14th order Elliptic style IIR
User selection	Two fixed high pass frequencies to be combined with four fixed low pass frequencies
High pass bandwidth (ωhc)	40 Hz and 100 Hz
High pass stopband frequency (ωhs)	Approximately ωhc / 2.5
Low pass bandwidth (ωlc)	2 kHz, 20 kHz, 40 kHz and 50 kHz
Low pass stopband frequency (ωs)	Approximately 1.5 to 2.5 * ωc
0.1 dB passband flatness (ωp)(1)	ωhc to ωlc or maximum 10 kHz
Stopband attenuation (δs)	80 dB

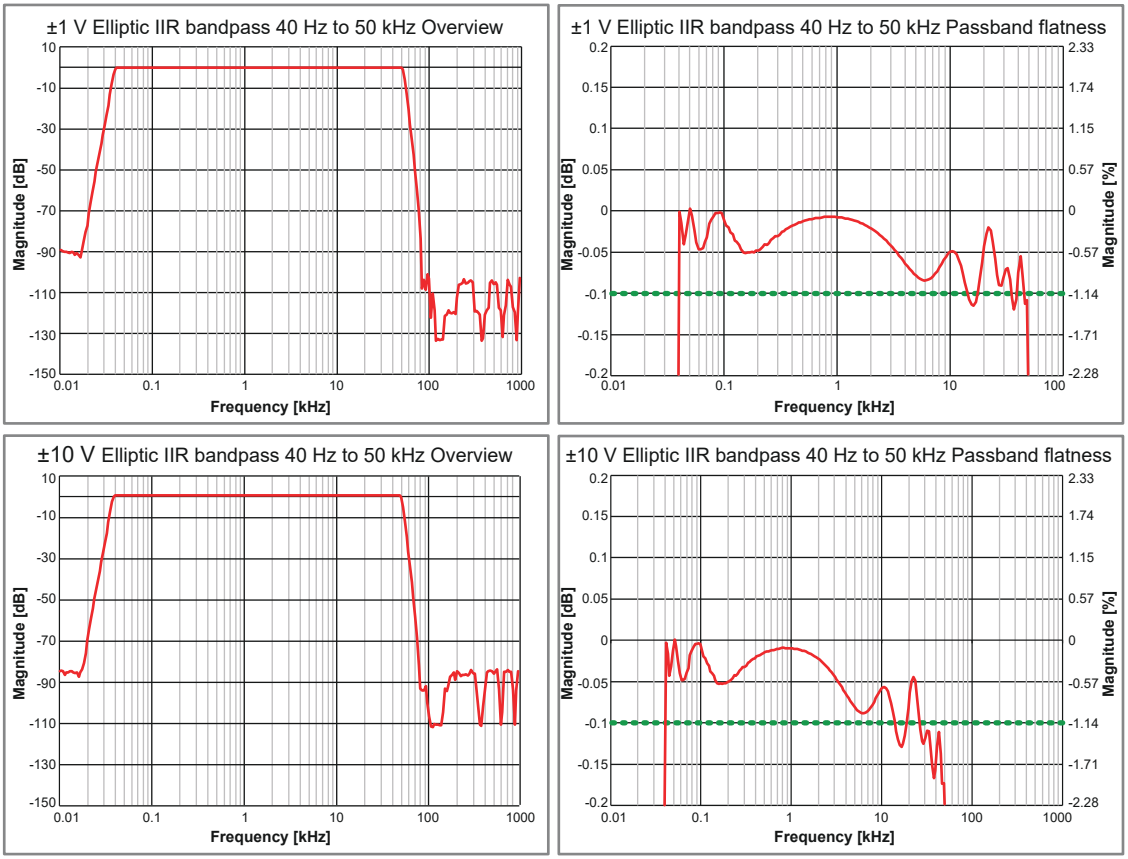


Figure A.162: Representative Elliptic IIR band pass examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths will lead to phase mismatches between channels.	
Wideband	10 kHz Sine wave
Channels on card	0.1 deg (30 ns)
GN3210 Channels within mainframe	0.1 deg (30 ns)
Bessel IIR, Filter frequency 25 kHz @ 250 kS/s	
Channels on card	0.1 deg (30 ns)
GN3210 Channels within mainframe	0.1 deg (30 ns)
Butterworth IIR, Filter frequency 62.5 kHz @ 250 kS/s	
Channels on card	0.1 deg (30 ns)
GN3210 Channels within mainframe	0.1 deg (30 ns)
Elliptic IIR, Filter frequency 62.5 kHz @ 250 kS/s	
Channels on card	0.1 deg (30 ns)
GN3210 Channels within mainframe	0.1 deg (30 ns)
GN3210 channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	2 GB (1 GSample @ 16 Bits Storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered and not recording
Storage sample size	16 bits, 2 bytes/sample 24 bits, 4 bytes/sample (required for Timer/Counter usage)

Digital Event/Timer/Counter(1)

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.

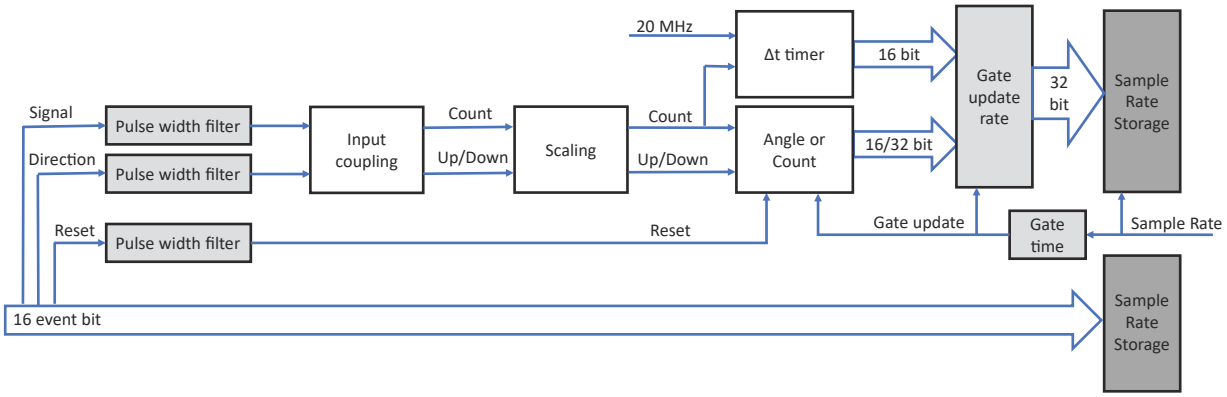


Figure A.163: Timer/Counter block diagram

Digital input events	16 per card
Levels	TTL input level, user programmable invert level
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs
Overvoltage protection	± 30 V DC continuously
Minimum pulse width	100 ns
Maximum frequency	5 MHz
Digital output events	2 per card
Levels	TTL output levels, short circuit protected
Output event 1	User selectable: Trigger, Alarm, set High or Low
Output event 2	User selectable: Recording active, set High or Low
Digital output event user selections	
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay
Alarm	High when alarm condition is activated, low when not activated (alarm conditions of this card only) 200 µs ± 1 µs ± 1 sample period alarm event delay
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation
Timer/Counter	2 per card; only available in 32 bit storage mode
Levels	TTL input levels
Inputs	All pins are shared with digital event inputs
Timer-Counter modes	Uni- and bi-directional count Bi-directional quadrature count Uni- and bi-directional frequency/RPM measurement

(1) Only if supported by mainframe

Timer/Counter Mode Uni- and Bi-directional Count

Counter mode is typically used for tracking movement of device under test. When possible use the quadrature modes as these are less sensitive to counting errors.

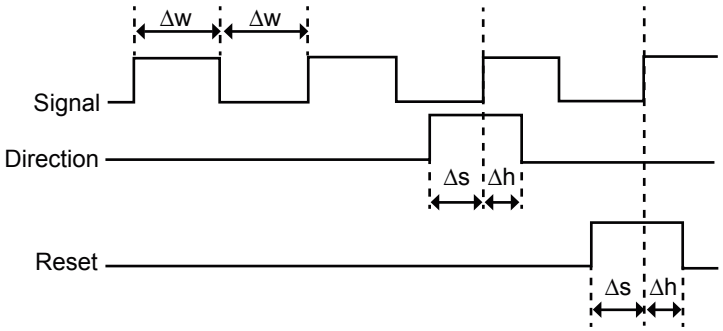


Figure A.164: Uni- and Bi-directional count timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Maximum input frequency	5 MHz
Minimum pulse width (Δw)	100 ns
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31} - 1$; bi-directional count
Gate measuring time	Sample period (1 / sample rate) to 50 s Can be selected by user to control update rate independent of sample rate
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional count Low: increment counter High: decrement counter
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Timer/Counter Mode Bi-directional Quadrature Count

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

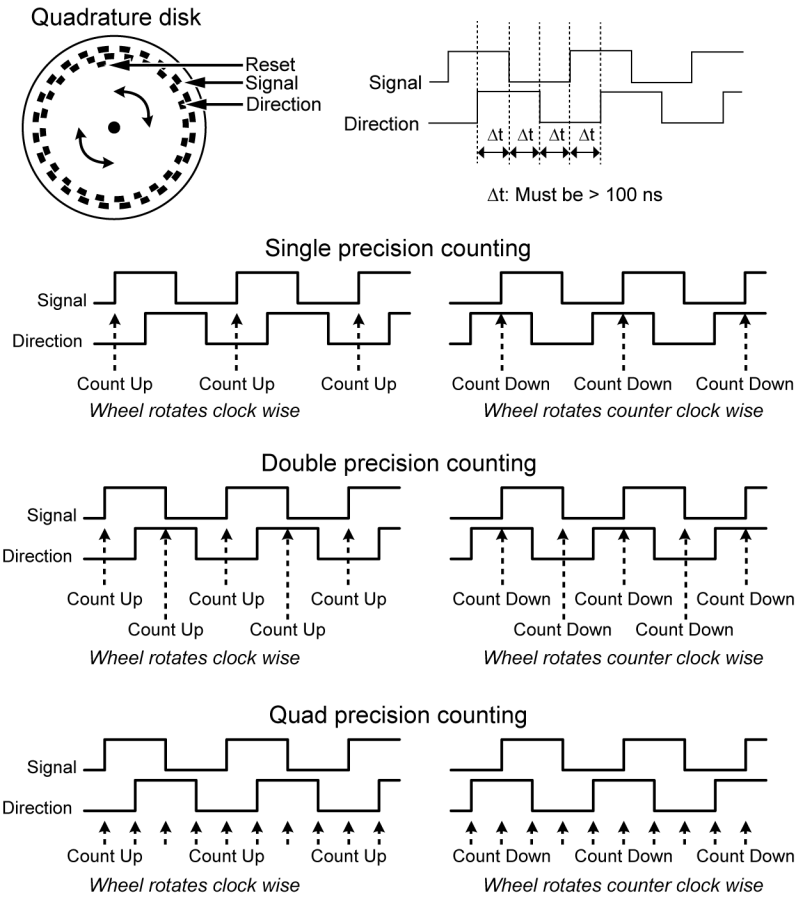


Figure A.165: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Maximum input frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single, dual or quad precision
Counter range	-2^{31} to $+2^{31} - 1$
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Timer/Counter Mode: Uni- and Bi-directional Frequency/RPM Measurement

Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.

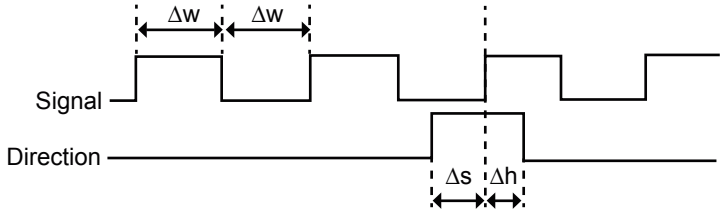


Figure A.166: Uni- and Bi-directional count timing

Inputs	2 pins: signal, direction
Maximum input frequency	5 MHz
Minimum pulse width (Δw)	100 ns
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s Can be selected by user to control update rate independent of sample rate
Direction input	
Level sensitivity	Only used when in bi-directional frequency/RPM mode Low: Positive frequency/RPM, e.g. left rotations High: Negative frequency/RPM, e.g. right rotations
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Triggering	
Channel trigger/qualifier	1 fully independent per channel either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger in edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger in delay	± 1 µs + maximum 1 sample period (Identical for decimal and binary time base)
Send to external trigger out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; see mainframe datasheet for details
Trigger out delay	Selectable (180 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (176 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516(504) µs for decimal (binary) time base, to be compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger (1)	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

(1) Only if supported by mainframe

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®	
Patent Number : 7,868,886 Real-time extraction of basic signal parameters. Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording. During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.	
Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators

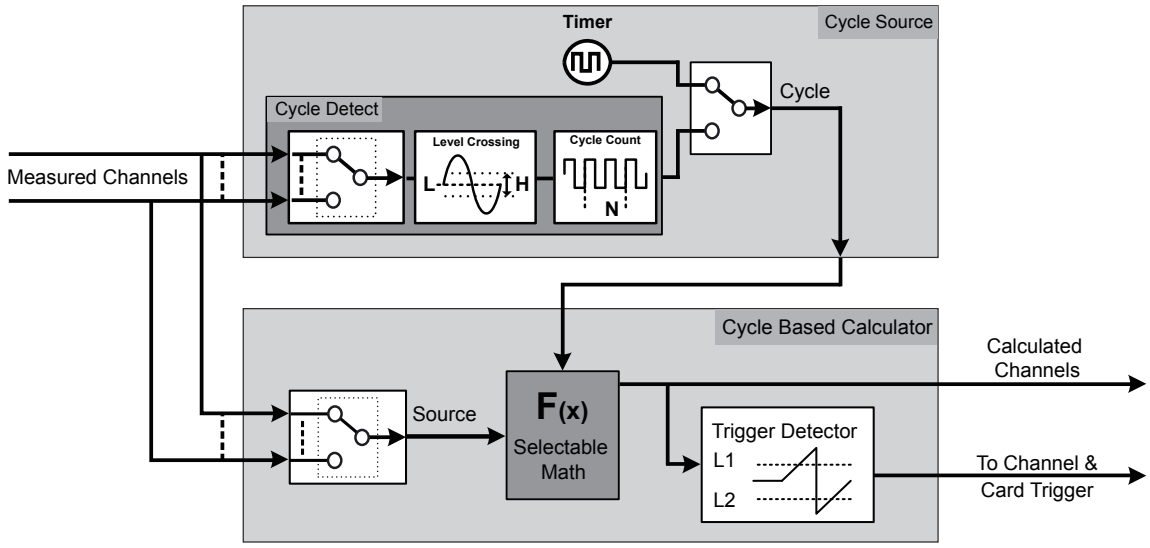


Figure A.167: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased.
Cycle based calculator	
Number of calculators	32; at sample rates 200 kS/s or lower. At higher sample rates, the number of calculators is reduced to match the available DSP power.
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software.
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and Crest Factor
Timer/Counter channel calculations	Frequency (to enable triggering). RPM of Angle.
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period.
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level.
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms.

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Acquisition Modes

Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Recording Mode Details

Recording Mode Details (16 Bit storage)

	Single Sweep Multiple Sweeps			**Continuous**			**Dual Rate**		
	Enabled Channels			Enabled Channels			Enabled Channels		
	1 Ch	16 Ch	32 Ch	1 Ch	16 Ch	32 Ch	1 Ch	16 Ch	32 Ch
Max. sweep memory	1000 MS	62 MS	31 MS	not used			800 MS	50 MS	25 MS
Max. sweep sample rate	250 kS/s			not used			250 kS/s		
Max. continuous FIFO	not used			1000 MS	62 MS	31 MS	200 MS	12.5 MS	6 MS
Max. continuous sample rate	not used			250 kS/s			Sweep Sample Rate / 2		
Max. aggregate continuous streaming rate	not used			0.25 MS/s 0.5 MB/s	4.0 MS/s 8.0 MB/s	8.0 MS/s 16.0 MB/s	0.25 MS/s 0.5 MB/s	4.0 MS/s 8.0 MB/s	8.0 MS/s 16.0 MB/s

Recording Mode Details (24 Bit storage)

	Single Sweep			**Continuous**			**Dual Rate**		
	Enabled Channels			Enabled Channels			Enabled Channels		
	1 Ch	16 Ch	32 Ch	1 Ch	16 Ch	32 Ch	1 Ch	16 Ch	32 Ch
Max. sweep memory	500 MS	31 MS	15.5 MS	not used			400 MS	25 MS	12.5 MS
Max. sweep sample rate	250 kS/s			not used			250 kS/s		
Max. continuous FIFO	not used			500 MS	31 MS	15.5 MS	100 MS	6 MS	3 MS
Max. continuous sample rate	not used			250 kS/s			Sweep Sample Rate / 2		
Max. aggregate continuous streaming rate	not used			0.25 MS/s 1.0 MB/s	4.0 MS/s 16.0 MB/s	8.0 MS/s 32.0 MB/s	0.25 MS/s 1.0 MB/s	4.0 MS/s 16.0 MB/s	8.0 MS/s 32.0 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Connector Pin Assignment	
Connector type	POSITRONIC HDC50F5R8N0X/AA
Mating connector type	Harting part number 9670505615 (Metal shell 61030010019, cable clamp 61030000145, blanking piece 61030000041)
Output voltage	5 V ± 20%
Output current	0.3 A maximum (all output pins internally connected)

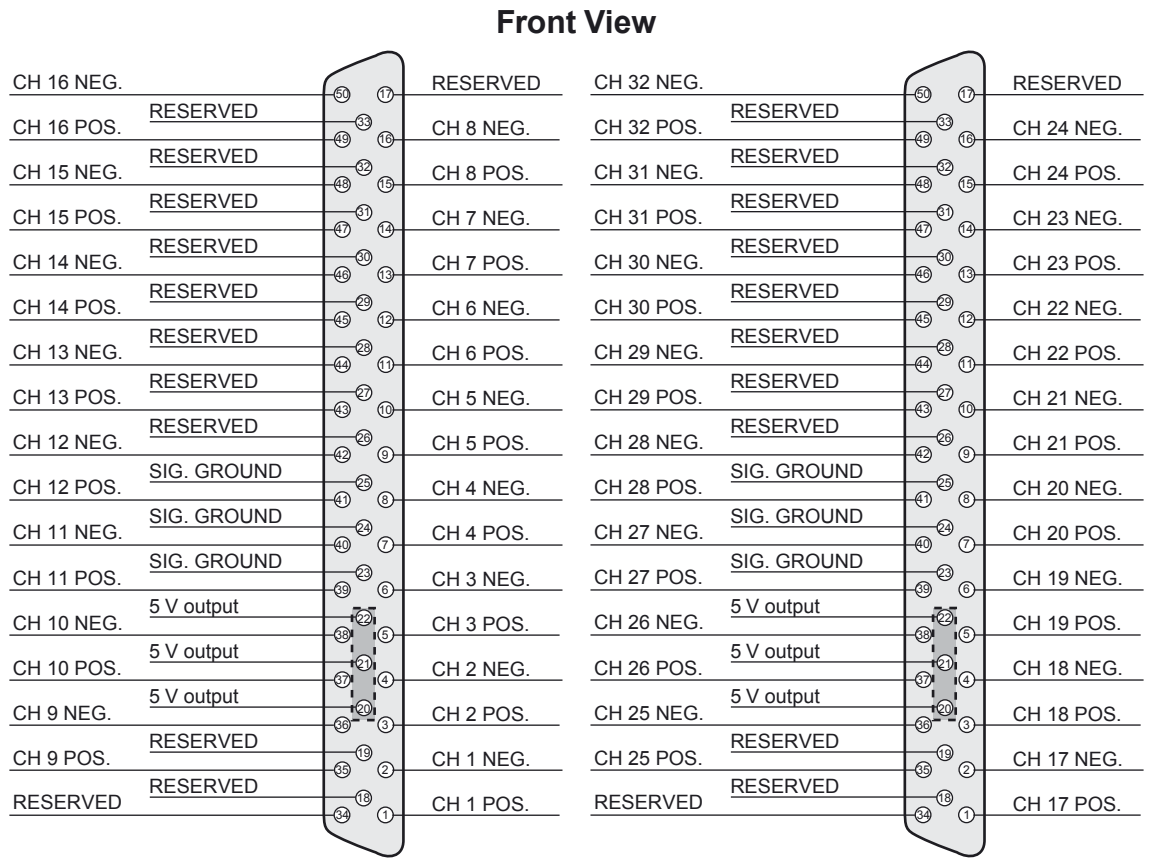


Figure A.168: Input connector pin diagram (Front view)

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.9 B3264-3.1 en (GEN series GN3211)

Capabilities Overview	
Model	GN3211
Maximum sample rate per channel	20 kS/s
Memory per card	200 MB
Analog channels	32
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16 bit
Isolation	Not supported
Input type	Analog balanced differential
Passive voltage/current probes	Passive, single-ended voltage probes Passive, differential matched voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Not supported
Real-time calculated results output	Not supported
Digital Event/Timer/Counter	16 digital events; no Timer/Counters
Standard data streaming (CPCI up to 200 MB/s)	Yes, supported by all GEN series mainframes
Fast data streaming (PCIe up to 1 GB/s)	Not supported
Slot width	1

Block Diagram

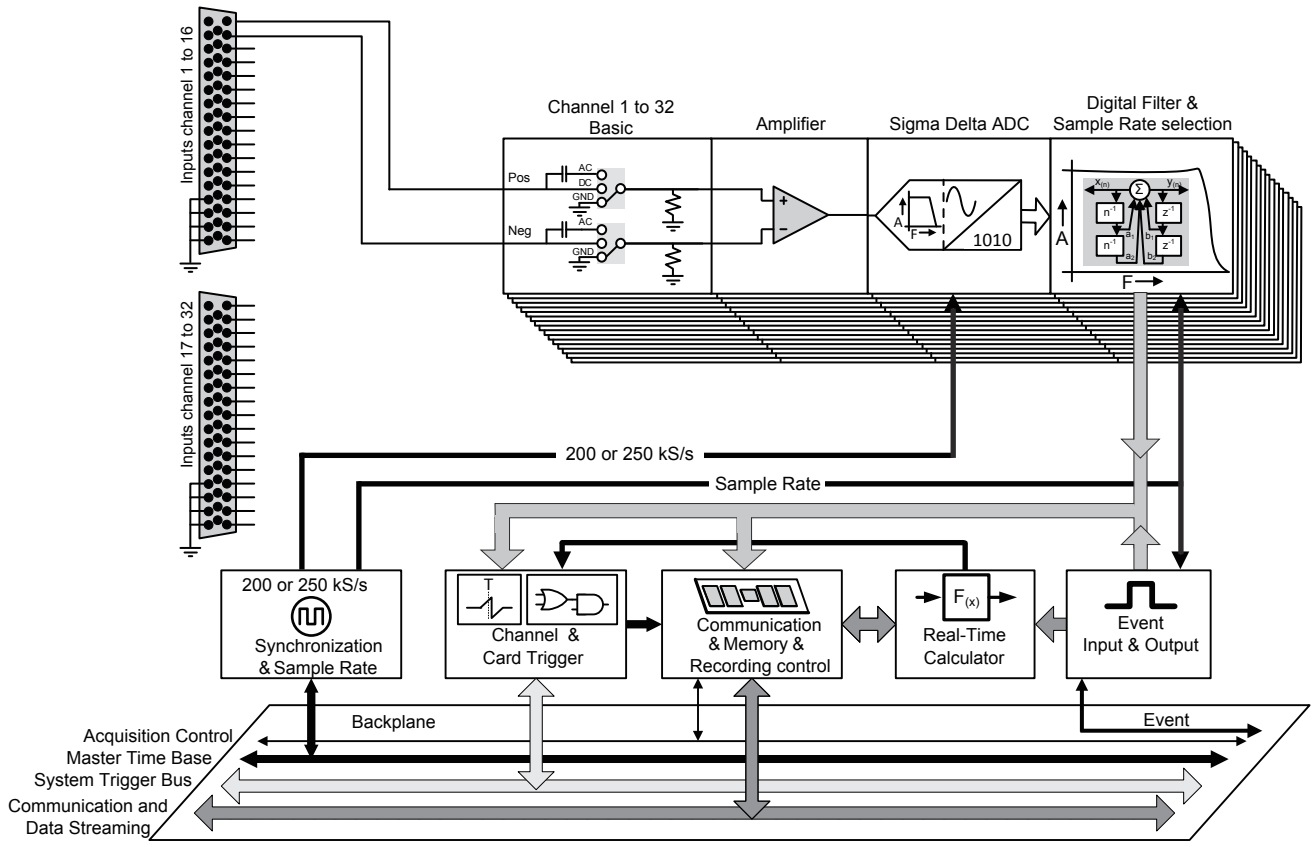


Figure A.169: Block diagram

Typical and guaranteed specifications

The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification

In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards

The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input Section	
Channels	32
Connectors	D-Sub (DD-50) connector
Input type	Analog isolated balanced differential
Input coupling	Differential, single-ended (positive or negative)
Signal input coupling	
Coupling modes	AC, DC, GND
AC coupling frequency	1.6 Hz ± 10%; - 3 dB

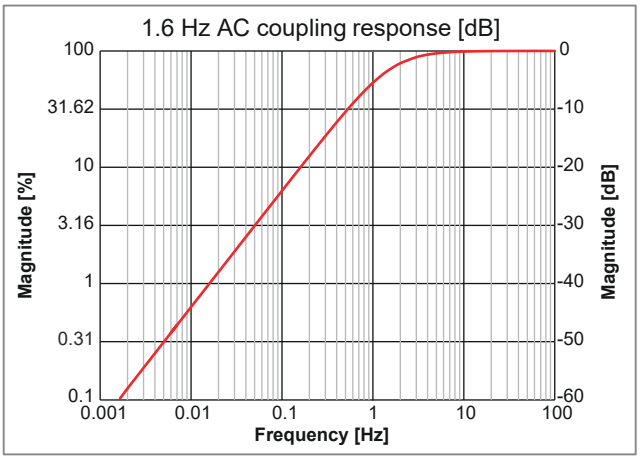


Figure A.170: Representative AC coupling response

Impedance	2 x 1 MΩ ± 0.5% // 75 pF ± 15%
Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Offset	± 50% in 1000 steps (0.1%); ± 20 V range has fixed 0% offset
DC Offset error	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV
Offset error drift	±(10 ppm + 2 µV)/°C (±(6 ppm + 1.5 µV)/°F)
DC Gain error	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
Gain error drift	± 10 ppm/°C (± 6 ppm/°F)
Maximum static error (MSE)	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
RMS Noise (50 Ω terminated)	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV

Analog Input Section		
Common mode (referred to system ground)		
Ranges	Less than ± 2 V	Larger than or equal to ± 2 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	2 V RMS	33 V RMS

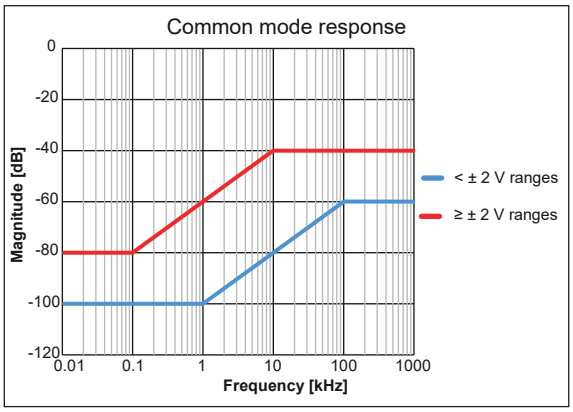


Figure A.171: Representative common mode response

Input overload protection	
Over voltage impedance change	The activation of the over voltage protection system will result in a reduced input impedance. The over voltage protection will not be active as long as the input voltage is less than 200% of the selected input range or 50 V DC whichever is the smallest value.
Maximum nondestructive voltage	± 50 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

Input Ranges When Using Passive Voltage Probes	
Detailed probe specifications can be found at the end of this datasheet	
Single-ended	**Added voltage ranges**
G901 (10:1 divide factor)	± 50 V, ± 100 V, ± 200 V
G902 (10:1 divide factor)	± 50 V, ± 100 V, ± 200 V
G903 (100:1 divide factor)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV
G904 (100:1 divide factor)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV
G906 (1000:1 divide factor)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV, ± 5 kV, ± 10 kV (± 20 kV @ DC to 60 Hz)
Differential matched	**Added voltage ranges**
G907 (10:1 divide factor)	± 50 V, ± 100 V, ± 200 V

Input Ranges When Using Active Differential Voltage Probes	
G909 (20:1 divide factor)	± 140 V RMS input and ± 1000 V RMS common mode
G909 (200:1 divide factor)	± 1000 V RMS input and ± 1000 V RMS common mode

Input Ranges When Using Current Clamps	
Detailed probe specifications can be found at the end of this datasheet	
Clamp type	**Added current ranges**
G912 (AC/DC)	± 30 mA to ± 30 A DC ± 30 mA to ± 20 A RMS
G913 (AC)	± 100 mA to ± 1000 A RMS
G914 (AC)	± 50 mA to ± 20 A RMS

Channel Earthing

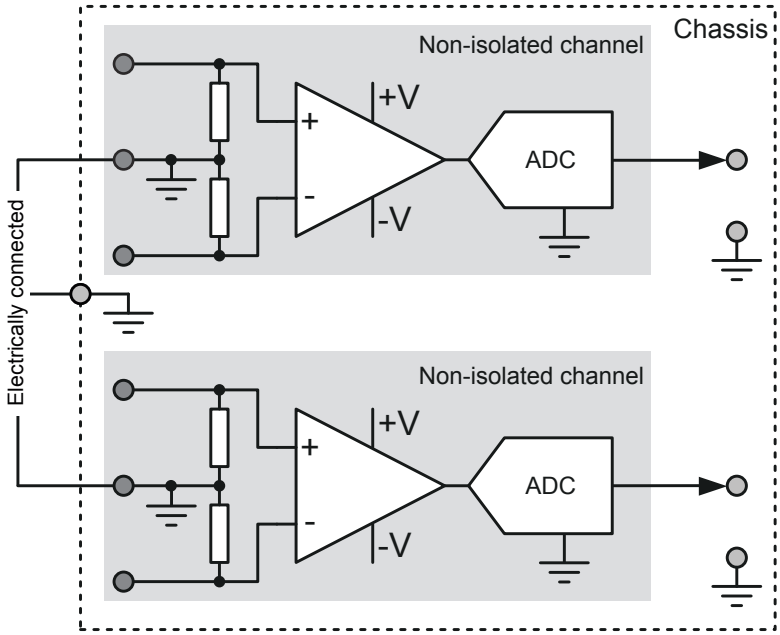


Figure A.172: Earthing schematic

Analog to Digital Conversion

Sample rate; per channel	1 S/s to 20 kS/s
ADC resolution; one ADC per channel	24 bit, only 16 bit recorded
ADC type	Sigma Delta (Σ-Δ) ADC; Analog Devices AD7764BRUZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; produces rounded BIN values when calculating FFT's
Maximum binary sample rate	20.48 kS/s
External time base frequency	0 S/s to 20 kS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ±30 ppm.

Anti-Alias Filters

Note on phase matching channels. Every filter characteristic and/or filter bandwidth selection comes with it's own specific phase response. Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

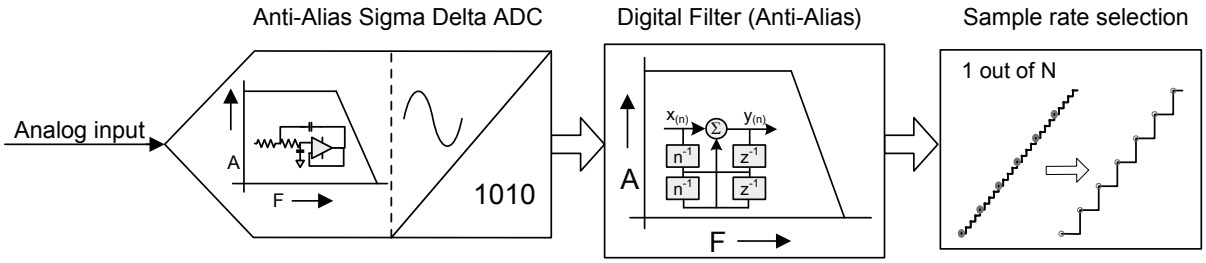


Figure A.173: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter integrated inside the Sigma Delta Analog to Digital Converter (ADC) always sampling at a fixed sample rate. This setup avoids the need for other analog anti-alias filters.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Sigma Delta Wideband	When Sigma Delta wideband is selected the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) is always in the signal path. Therefore, the anti-alias protection is always active when Sigma Delta wideband is selected.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Bessel IIR filter. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Butterworth IIR filter. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Sigma Delta Wideband (Analog Anti-Alias)

When Sigma Delta wideband is selected there is always the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) in the signal path. Therefore there is always anti-alias protection when wideband is selected. Care must be taken as this filter introduces slight overshoots on square wave or pulse response signals. Signals of sine wave type will not be effected.

Wideband

Characteristic	Sigma delta, optimal frequency response
-3 dB Bandwidth	80 kHz ± 5 kHz
0.1 dB passband flatness(1)	DC to 20 kHz

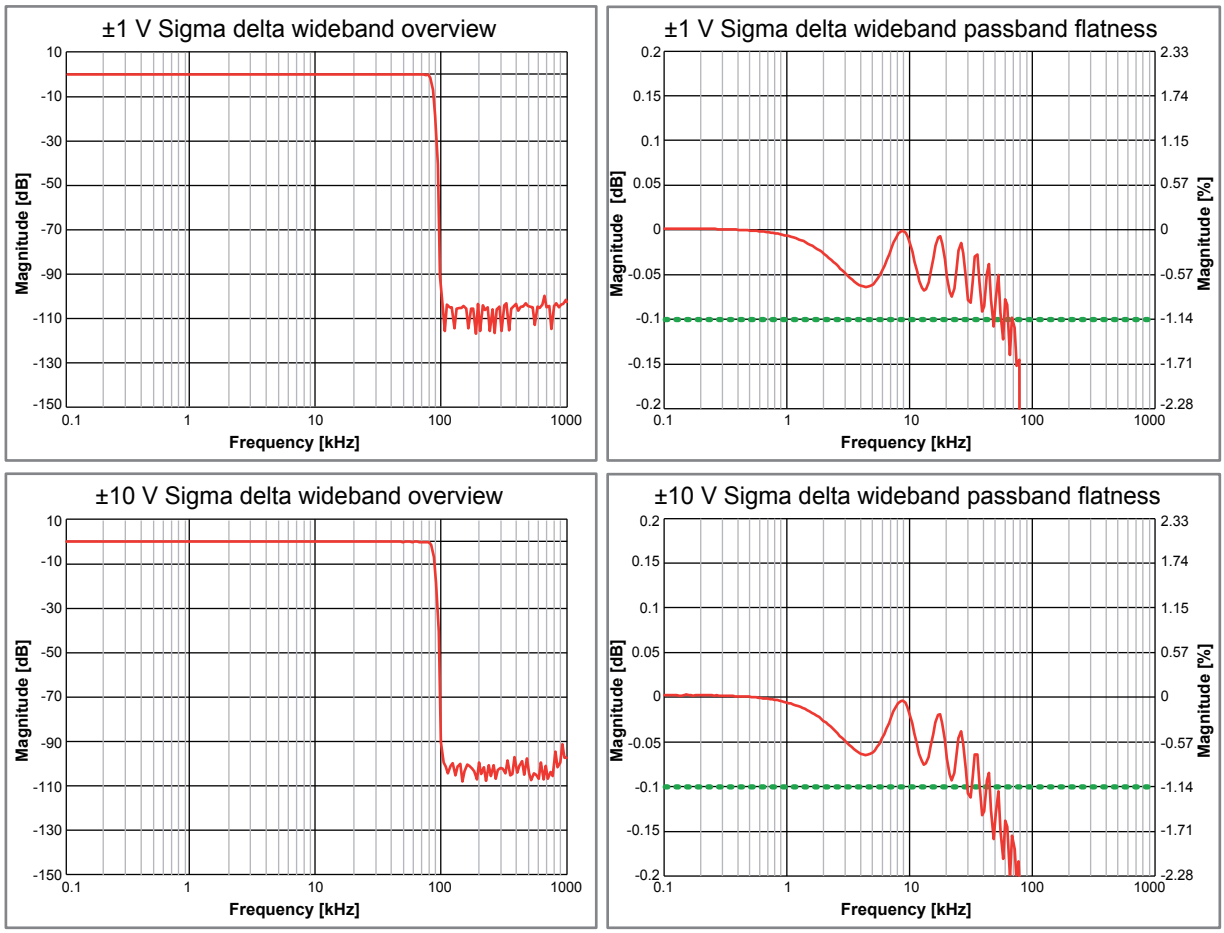
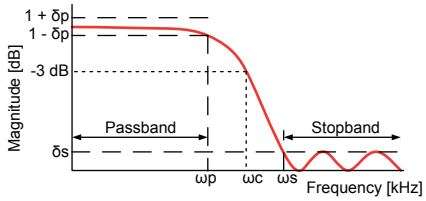


Figure A.174: Representative Sigma Delta Wideband examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.175: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Bessel IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
Low pass -3 dB bandwidth	80 kHz ± 5 kHz
Bessel IIR Filter	
Characteristic	12-pole Bessel style IIR
User selection	Auto tracking to sample rate divided by: 10, 20, 40, 100 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	User selectable from 40 Hz to 2 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/10
Stopband attenuation (δs)	80 dB
Roll-off	72 dB/octave for 12-pole filters

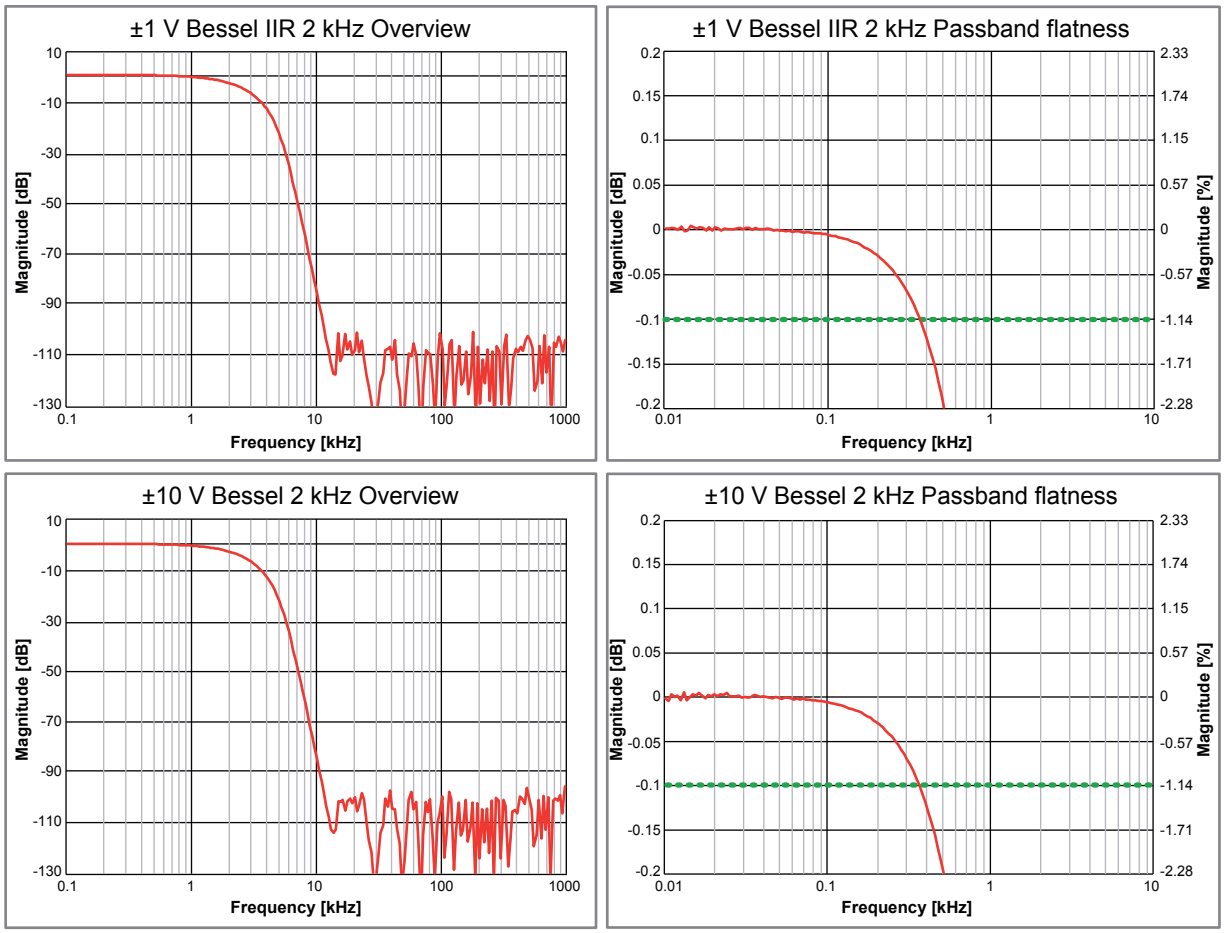
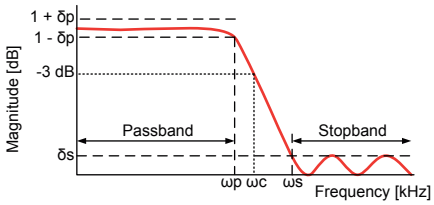


Figure A.176: Representative Bessel IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.177: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Butterworth IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
Low pass bandwidth	80 kHz ± 5 kHz (-3 dB)
Butterworth IIR Filter	
Characteristic	12-pole Butterworth style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed.
Bandwidth (ωc)	User selectable from 100 Hz to 5 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/2
Stopband attenuation (δs)	80 dB
Filter roll-off	72 dB/octave

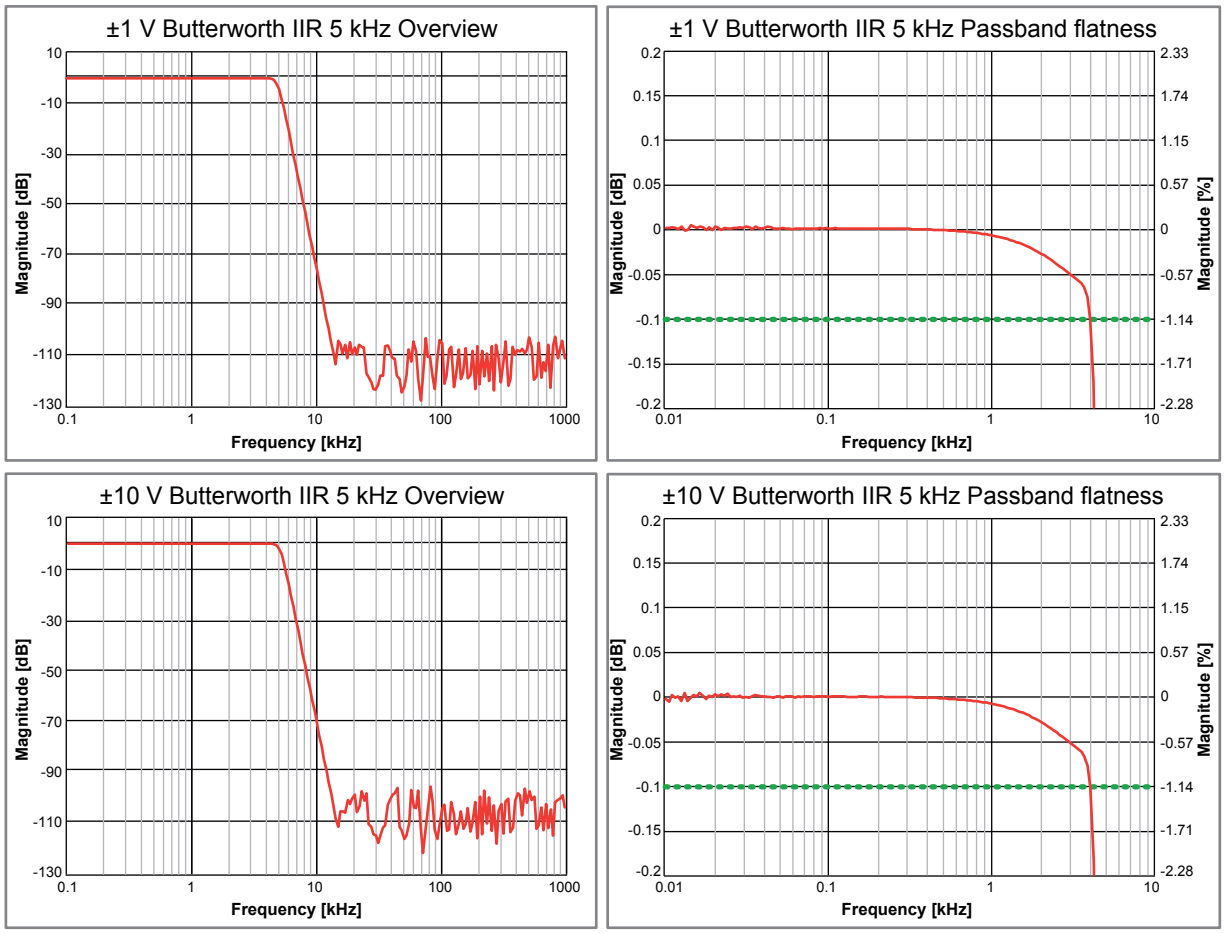


Figure A.178: Representative Butterworth IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths will lead to phase mismatches between channels.	
Wideband	1 kHz Sine wave
Channels on card	0.01 deg (30 ns)
GN3211 Channels within mainframe	0.01 deg (30 ns)
Bessel IIR, Filter frequency 2 kHz @ 20 kS/s	
Channels on card	0.01 deg (30 ns)
GN3211 Channels within mainframe	0.01 deg (30 ns)
Butterworth IIR, Filter frequency 5 kHz @ 20 kS/s	
Channels on card	0.01 deg (30 ns)
GN3211 Channels within mainframe	0.01 deg (30 ns)
GN3211 channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	200 MByte (100 MSample @ 16 Bits Storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered and not recording
Storage sample size	16 bits, 2 bytes/sample

Digital Event(1)

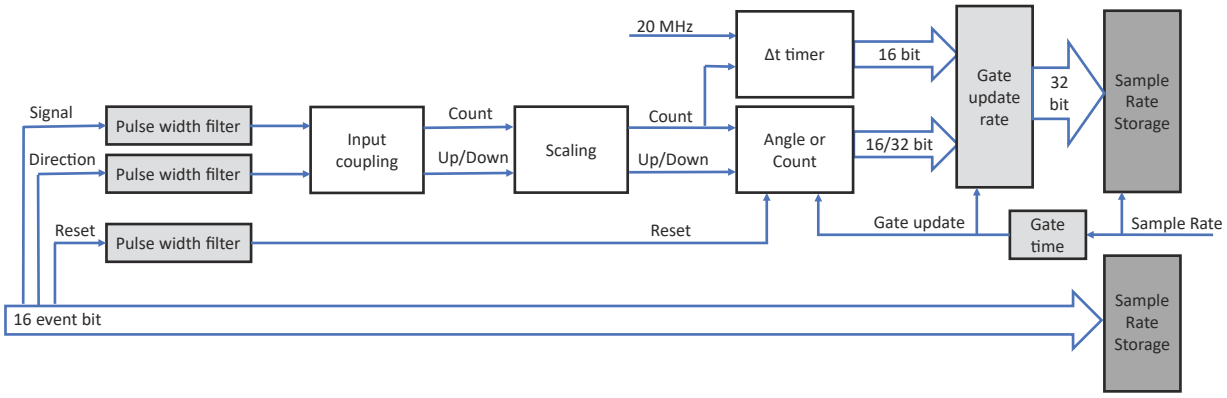


Figure A.179: Timer/Counter block diagram

Digital input events	16 per card
Levels	TTL input level, user programmable invert level
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs
Overvoltage protection	± 30 V DC continuously
Minimum pulse width	100 ns
Maximum frequency	5 MHz
Digital output events	2 per card
Levels	TTL output levels, short circuit protected
Output event 1	User selectable: Trigger, Alarm, set High or Low
Output event 2	User selectable: Recording active, set High or Low
Digital output event user selections	
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay
Alarm	High when alarm condition is activated, low when not activated (alarm conditions of this card only) 200 µs ± 1 µs ± 1 sample period alarm event delay
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation
External start	Rising/Falling edge selected by user starts a new recording
External stop	Rising/Falling edge selected by the user stops the recording

(1) Only if supported by mainframe

Triggering	
Channel trigger/qualifier	1 fully independent per channel either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger in edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger in delay	± 1 µs + maximum 1 sample period (Identical for decimal and binary time base)
Send to external trigger out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; see mainframe datasheet for details
Trigger out delay	Selectable (180 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (176 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516(504) µs for decimal (binary) time base, to be compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger (1)	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

(1) Only if supported by mainframe

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®	
Patent Number : 7,868,886 Real-time extraction of basic signal parameters. Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording. During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.	
Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators (Perception V6.72 and higher)

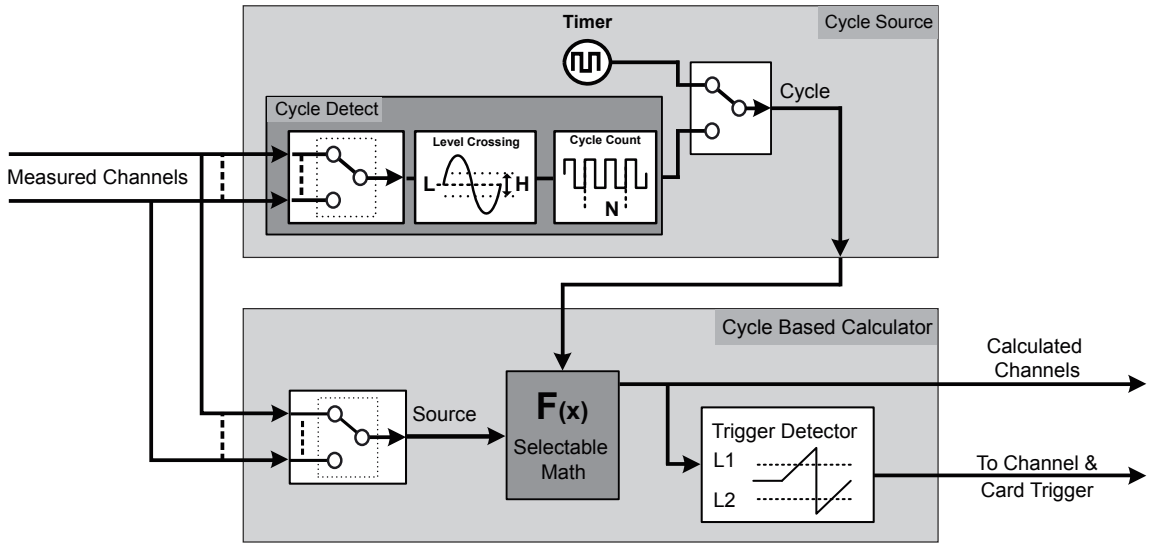


Figure A.180: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased.
Cycle based calculator	
Number of calculators	32
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software.
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and MeanOfMultiplication
Timer/Counter channel calculations	Frequency (to enable triggering). RPM of Angle.
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period.
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level.
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms.

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Recording Mode Details

Recording Mode Details (16 Bit storage)

	Single Sweep Multiple Sweeps			**Continuous**			**Dual Rate**		
	Enabled Channels			Enabled Channels			Enabled Channels		
	1 Ch	16 Ch	32 Ch	1 Ch	16 Ch	32 Ch	1 Ch	16 Ch	32 Ch
Max. sweep memory	100 MS	5.7 MS	2.7 MS	not used			80 MS	4.5 MS	2.1 MS
Max. sweep sample rate	20 kS/s			not used			250 kS/s		
Max. continuous FIFO	not used			100 MS	5.7 MS	2.7 MS	20 MS	0.9 MS	0.6 MS
Max. continuous sample rate	not used			20 kS/s			Sweep Sample Rate / 2		
Max. aggregate continuous streaming rate	not used			0.02 MS/s 0.04 MB/s	0.32 MS/s 0.64 MB/s	0.64 MS/s 1.28 MB/s	0.02 MS/s 0.04 MB/s	0.32 MS/s 0.64 MB/s	0.64 MS/s 1.28 MB/s

Single Sweep	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Connector Pin Assignment	
Connector type	POSITRONIC HDC50F5R8N0X/AA
Mating connector type	Harting part number 9670505615 (Metal shell 61030010019, cable clamp 61030000145, blanking piece 61030000041)
Output voltage	5 V ± 20%
Output current	0.3 A maximum (all output pins internally connected)

Front View

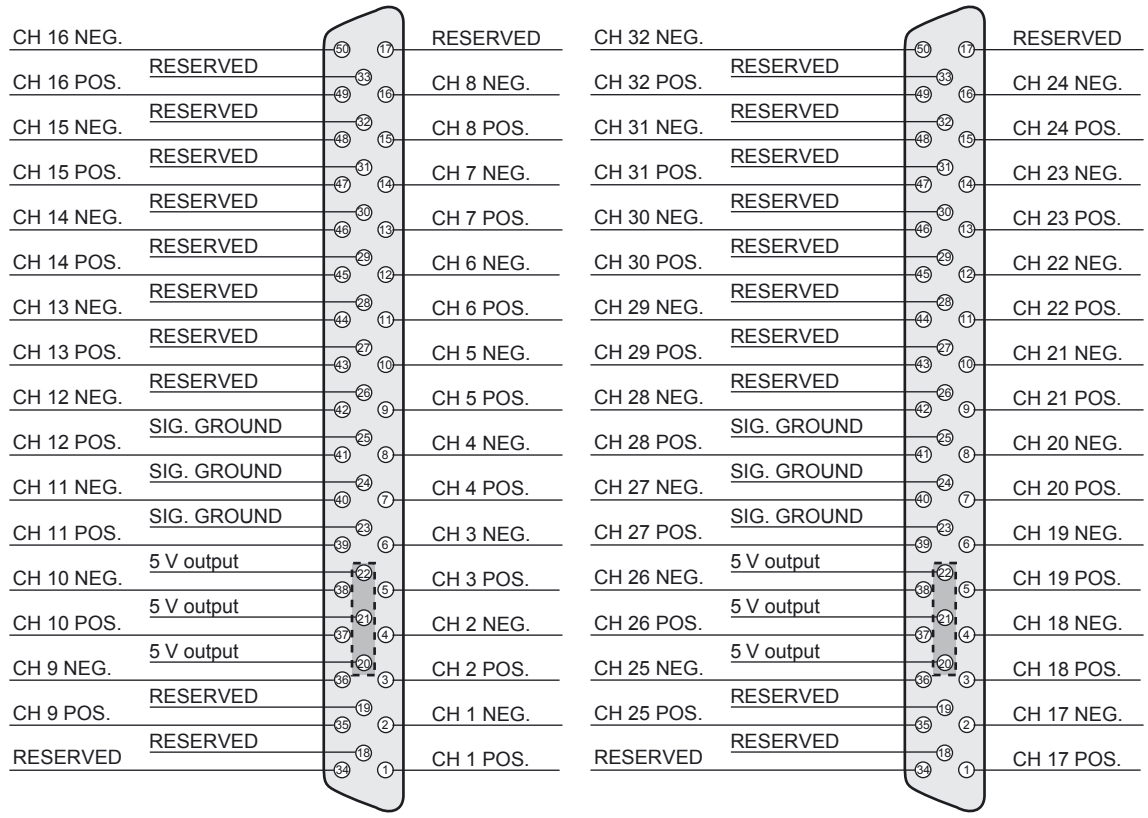


Figure A.181: Input connector pin diagram (Front view)

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

A.10 B04596_01_E00_01 (GEN series GN810xB)

Capabilities Overview			
Model	GN8101B	GN8102B	GN8103B
Maximum sample rate per channel	250 MS/s	100 MS/s	25 MS/s
Memory per card	8 GB		
Analog channels	8		
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter		
ADC resolution	14 bit		
Isolation	Not supported		
Input type	Single-ended Differential using the differential probe		
Passive voltage/current probes	Passive, singled-ended voltage probes		
TEDS	Not supported		
Real-time cycle based calculators	Not supported		
Real-time formula database calculators (option)	Extensive set of user programmable math routines		
Real-time calculated results output	Ethernet software API	EtherCAT®	CAN/CAN FD
Result blocks per second	2000	1000	500
Latency	Ethernet dependent	1 ms	CAN bus speed
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels		
Standard data streaming (CPCI up to 200 MB/s)	Not supported(1)		
Fast data streaming (PCIe up to 1 GB/s)	Supported		
Slot width	1		

(1) GEN2i, GEN5i, GEN7t and GEN16t do not support GN8101B, GN8102B or GN8103B.

Block Diagram

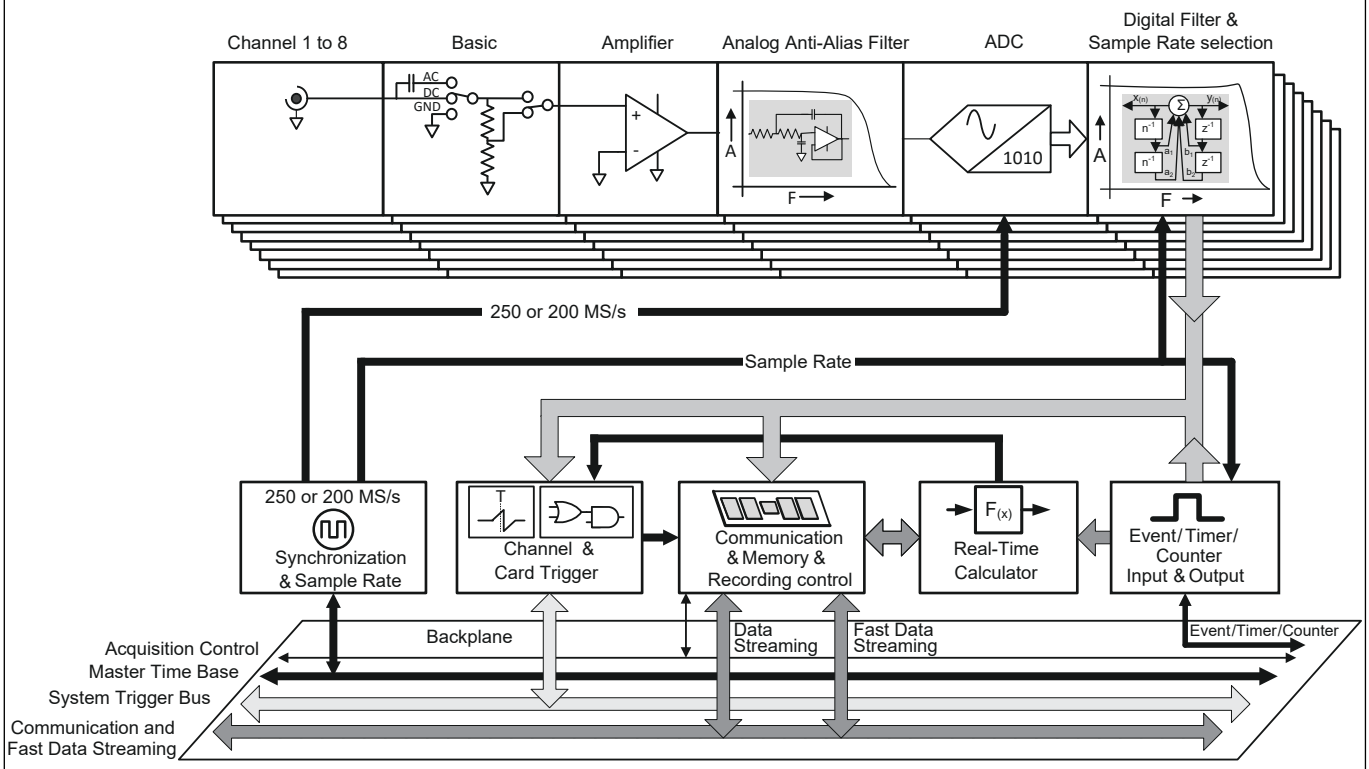


Figure A.182: Block Diagram

Typical and guaranteed specifications
The typical and guaranteed specification given in this data sheet are derived from the 1 σ (68.27%) and 5 σ (99.9999%) statistical calibration result analysis. Rounding and optimizations have been applied before defining both specifications.

Guaranteed specification
In the rare case a card might not meet the guaranteed specifications during final testing in production, this card is not released for sale.

Adding/removing or swapping cards
The specifications listed are valid for cards that have been calibrated and are used in the same mainframe, mainframe configuration and slots as they were at the time of calibration.
If cards are added, removed or relocated the thermal conditions of the card will change, resulting in additional thermal drift errors. The maximum expected error will be up to two times the specified Offset and Gain error as well as 10 dB reduced common mode rejection.
Recalibration after configuration changes is therefore highly recommended.

Analog Input Section	
Channels	8
Connectors	Metal BNC
Input type	Analog, single-ended
Input impedance	
1 MΩ impedance	≤ ± 1V ranges: 1 MΩ ± 1% // 27.5 pF ± 5% > ± 1V ranges: 1 MΩ ± 1% // 18.5 pF ± 5%
50 Ω impedance	50 Ω ± 2%
Input coupling	
Coupling modes	AC, DC, GND
AC coupling frequency (1 MΩ impedance)	1.6 Hz ± 10%; - 3 dB
AC coupling frequency (50 Ω impedance)	32 kHz ± 10%; - 3 dB

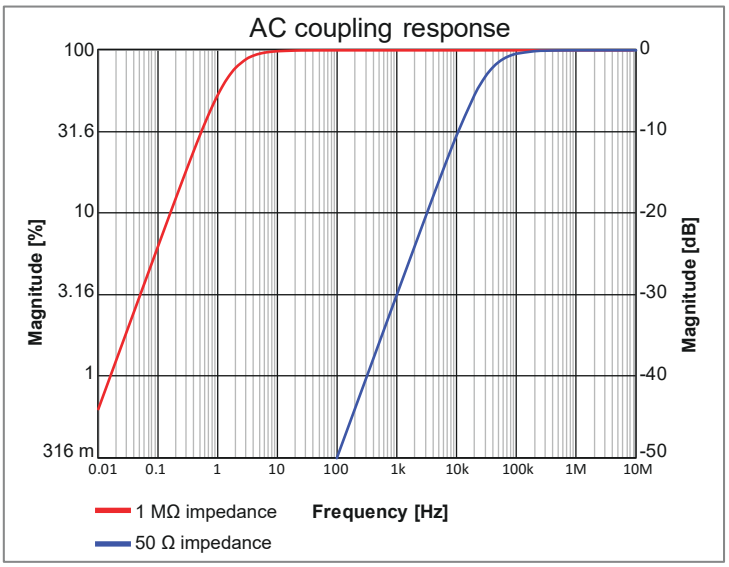
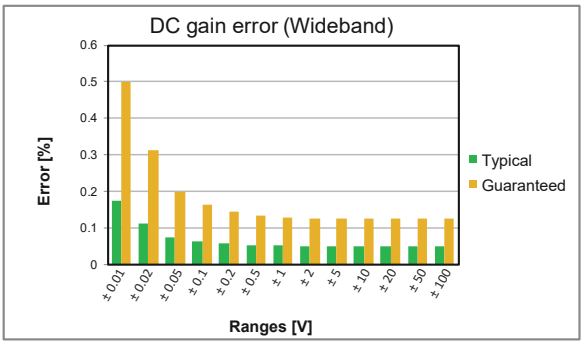


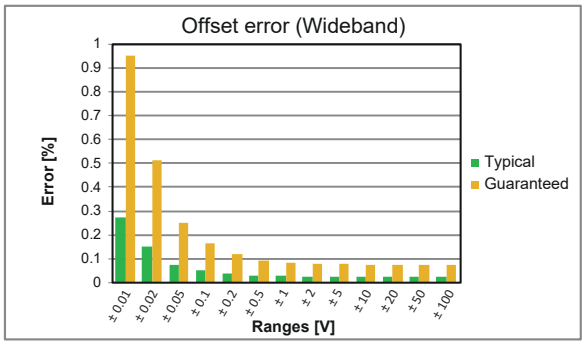
Figure A.183: Representative AC coupling response

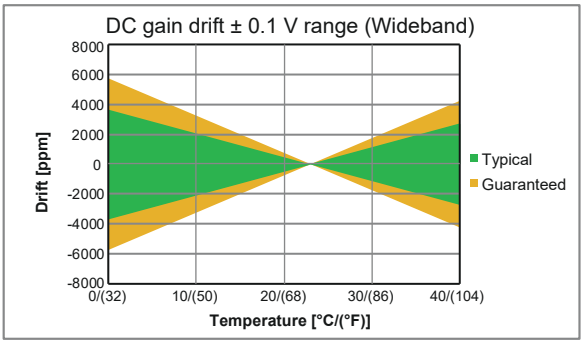
Ranges	
1 MΩ impedance	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V, ± 50 V, ± 100 V
50 Ω impedance	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V
Offset	± 50% in 1000 steps (0.1%); When 1 MΩ input is selected, the ± 100 V range has fixed 0% offset. When 50 Ω input is selected, the ± 5 V range has fixed 0% offset.
Overvoltage impedance change	The activation of the overvoltage protection system results in a reduced input impedance. The overvoltage protection is not active for as long as the input voltage remains less than 200% of the selected input range or 125 V, whichever value is the smallest.
Maximum nondestructive voltage	
1 MΩ impedance	± 125 V DC
50 Ω impedance	± 7 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 40 ns after 200% overload

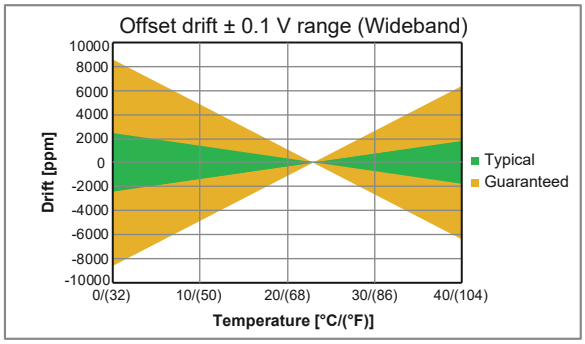
Voltage Specifications (Wideband)

	Typical	Guaranteed
DC gain error	0.05% of Full Scale ± 25 µV	0.125% of Full Scale ± 75 µV
DC offset error	0.025% of Full Scale ± 50 µV	0.075% of Full Scale ± 175 µV
DC gain error drift	160 ppm of reading / °C (89 ppm of reading / °F)	250 ppm of reading / °C (139 ppm of reading / °F)
DC offset drift	± (55 ppm of Full Scale + 10 µV) / °C (± (31 ppm of Full Scale + 6µV) / °F)	± (175 ppm of Full Scale + 40 µV) / °C (± (98 ppm of Full Scale + 23 µV) / °F)
RMS Noise (50 Ω terminated)	0.05% of Full Scale ± 100 µV	0.075% of Full Scale ± 125 µV









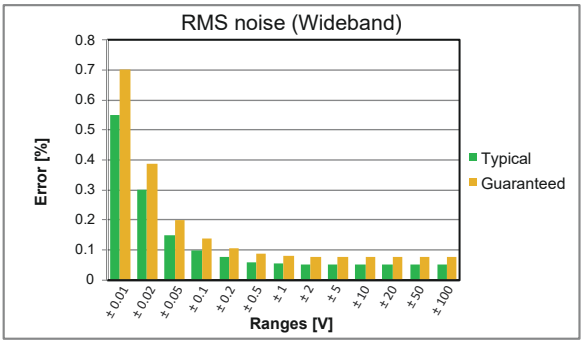
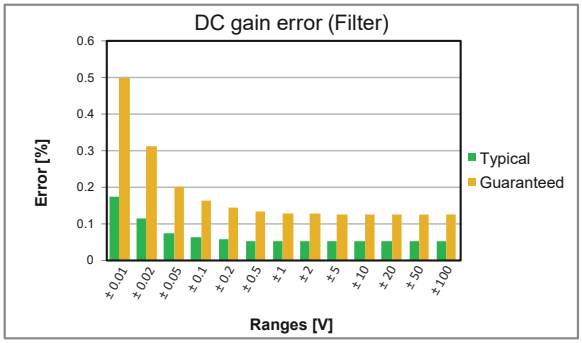
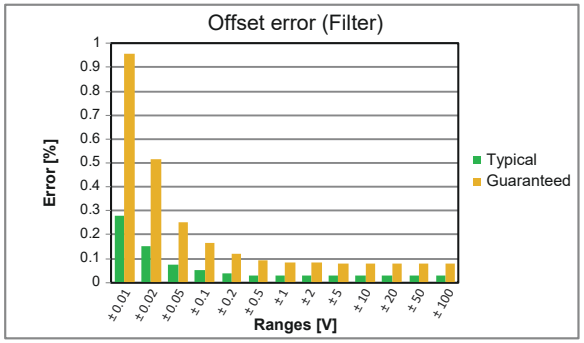


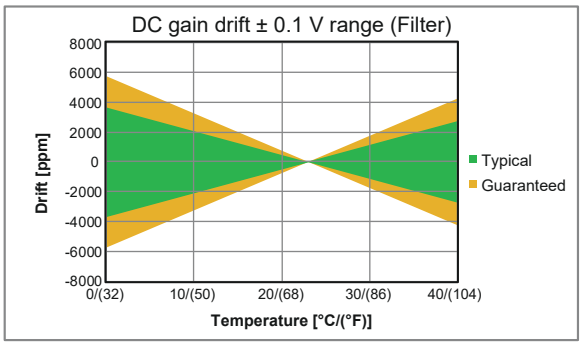
Figure A.184: Wideband voltage specification

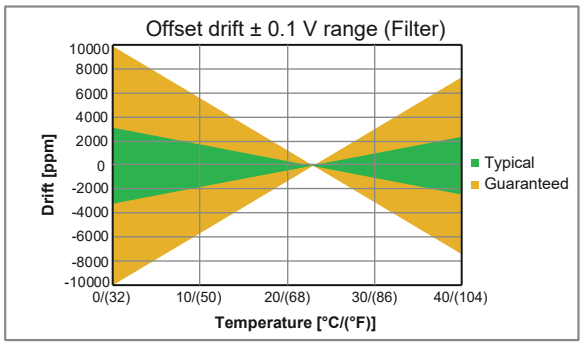
Voltage Specifications (Analog Filter Used)

	Typical	Guaranteed
DC gain error	0.05% of reading ± 25 µV	0.125% of reading ± 75 µV
DC offset error	0.025% of Full Scale ± 50 µV	0.075% of Full Scale ± 175 µV
DC gain error drift	160 ppm of reading / °C (89 ppm of reading / °F)	250 ppm of reading / °C (139 ppm of reading / °F)
DC offset drift	± (85 ppm of Full Scale + 10 µV) / °C (± (48 ppm of Full Scale + 6 µV) / °F)	± (225 ppm of Full Scale + 40 µV) / °C (± (125 ppm of Full Scale + 23 µV) / °F)
RMS Noise (50 Ω terminated)	0.05% of Full Scale ± 75 µV	0.075% of Full Scale ± 100 µV









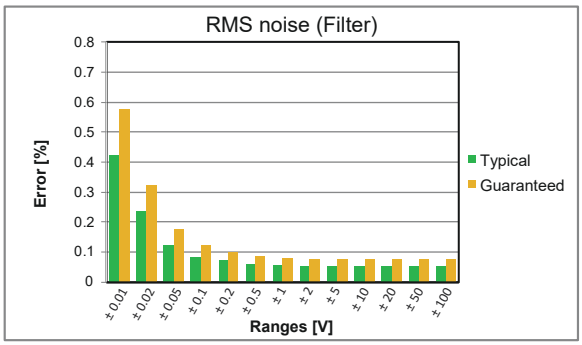


Figure A.185: Filter used voltage specification

Channel Earthing

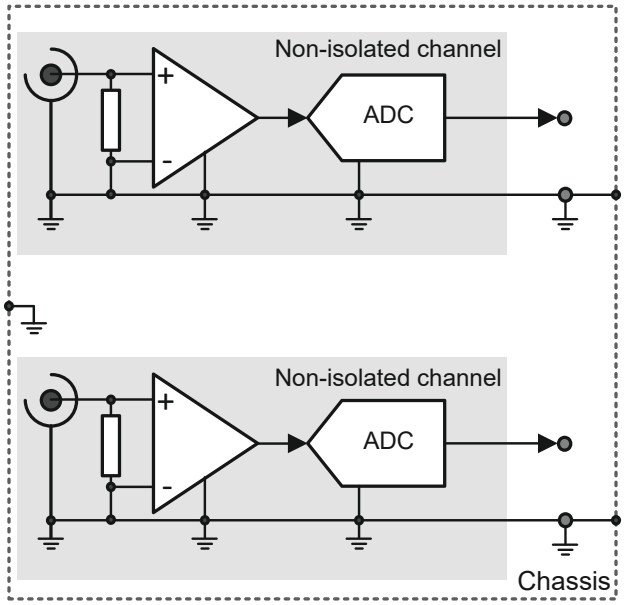


Figure A.186: Earthing schematic

Analog to Digital Conversion

Sample rate; per channel	10 S/s to 250 MS/s (GN8101B), 100 MS/s (GN8102B) or 25 MS/s (GN8103B)
ADC resolution; one ADC per channel	14 bit
ADC type	Pipelined multistep converter, Analog Devices AD9250
Time base accuracy	Defined by mainframe: ± 3.5 ppm; aging after 10 years ± 10 ppm
Binary sample rate	Supported; calculating FFTs results in rounded BIN values
Maximum binary sample rate	204.8 MS/s (GN8101B), 102.4 MS/s (GN8102B) or 25.6 MS/s (GN8103B)
External time base	Not supported

Anti-Alias Filters

Using different filter selections (Wideband/Bessel/Bessel IIR) or different filter bandwidths can result in phase mismatches between channels.

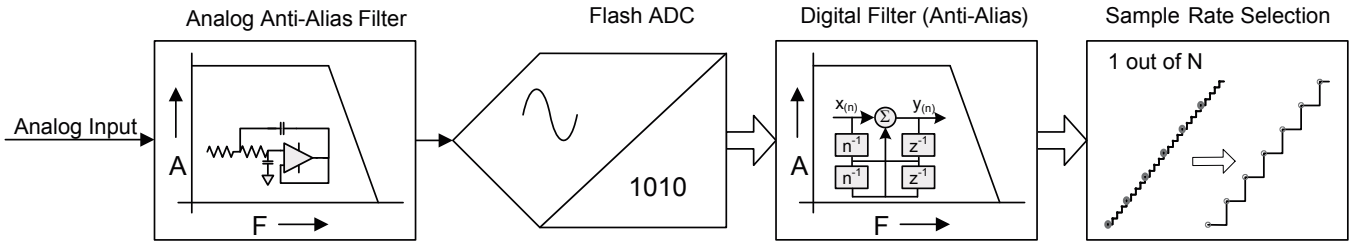


Figure A.187: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter supports a range of fixed bandwidth anti-alias filters. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Wideband should not be used if working in a frequency domain with recorded data. Using wideband, enhanced resolution is not supported at lower sample rates.
Bessel (Fc @ -3 dB)	This analog Bessel filter can be used to reduce the higher bandwidth signals, but is also used to minimize aliasing at sample rates above 100 MS/s. For lower sample rates, the digital IIR filter must be used to prevent aliasing. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses. Using the Bessel filter, enhanced resolution is not supported at lower sample rates.
Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. This can only be used for sample rates up to 100 MS/s. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses. Enhanced resolution is supported by using over sampling combined with a digital filter at the following sample rates: 15 bit resolution at 50 MS/s and lower, 16 bit resolution at 12.5 MS/s and lower.
Butterworth IIR (Fc @ -3 dB)	When Butterworth IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Butterworth IIR filter to prevent aliasing at lower sample rates. This can only be used for sample rates up to 100 MS/s. Butterworth filters are typically used when looking at signals in the frequency domain. They are best used for measuring continuous varying signals without sharp edge signals like square waves or step responses. Enhanced resolution is supported by using over sampling combined with a digital filter at the following sample rates: 15 bit resolution at 50 MS/s and lower, 16 bit resolution at 12.5 MS/s and lower.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	≥ ± 50 mV ranges: between 100 MHz and 160 MHz (-3 dB); ≤ ± 20 mV ranges: between 75 MHz and 100 MHz (-3 dB)
0.1 dB passband flatness(1)	DC to 5 MHz

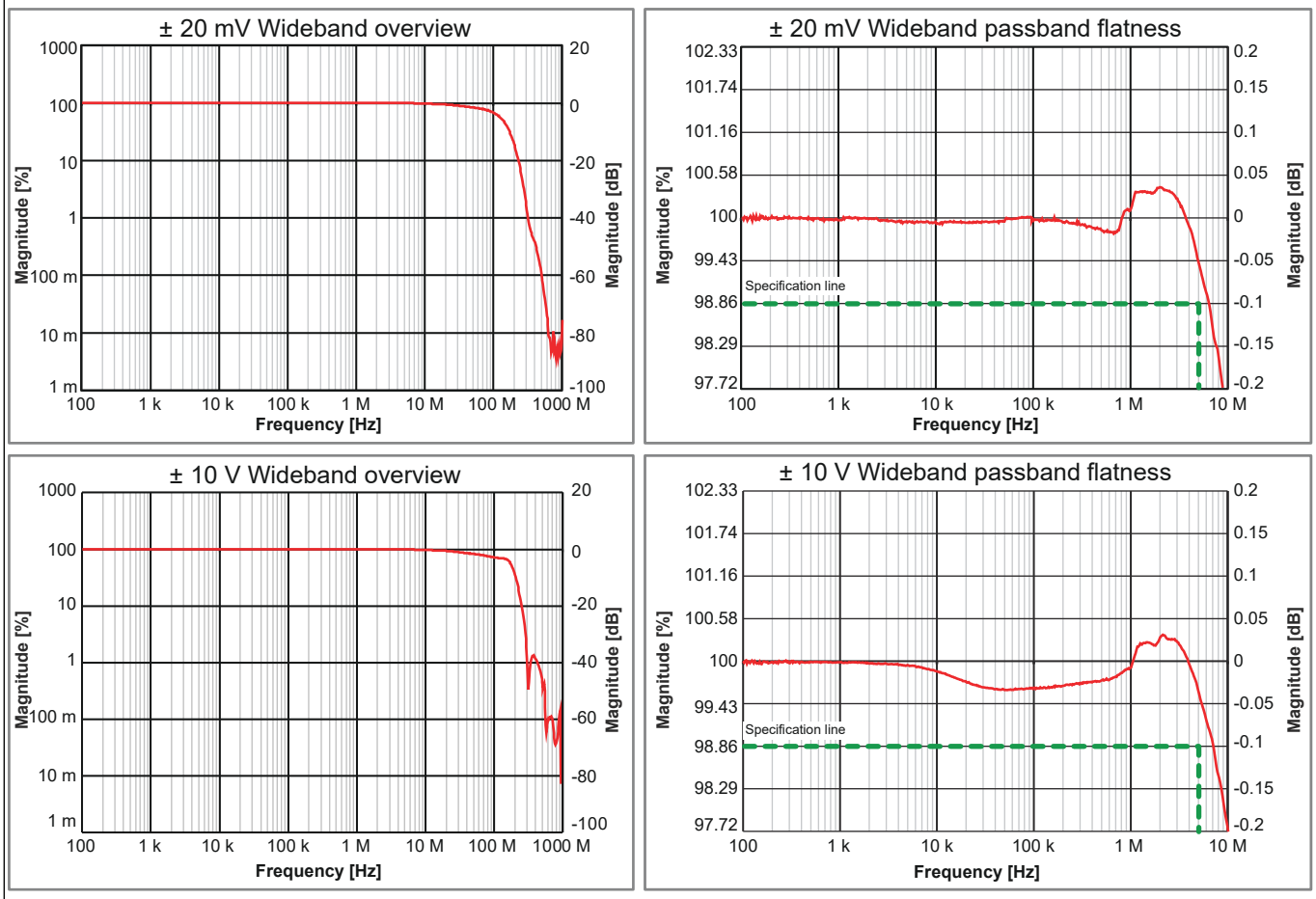
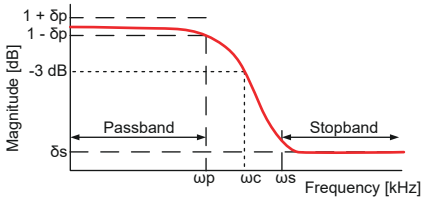


Figure A.188: Representative Wideband examples

(1) Measured using Fluke 5730A calibrator, DC normalized and a Fluke 9500B calibrator for the card, when 1 MΩ input is selected.

Bessel Filter (Analog Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.189: Bessel Filter

When Bessel filter is selected, this is only the analog Bessel anti-alias filter and not a digital filter.

Bessel filter bandwidth	32 MHz ± 3 MHz (-3 dB)
Bessel filter characteristic	6-pole Bessel, optimal step response
Bessel filter 0.1 dB passband flatness(1)	DC to 4 MHz
Stopband magnitude (δs) at frequency (ωs)	≥ ± 50 mV ranges: -50 dB at ωs = 700 MHz; ≤ ± 20 mV ranges: -70 dB at ωs = 700 MHz
Bessel filter roll-off	36 dB/Octave

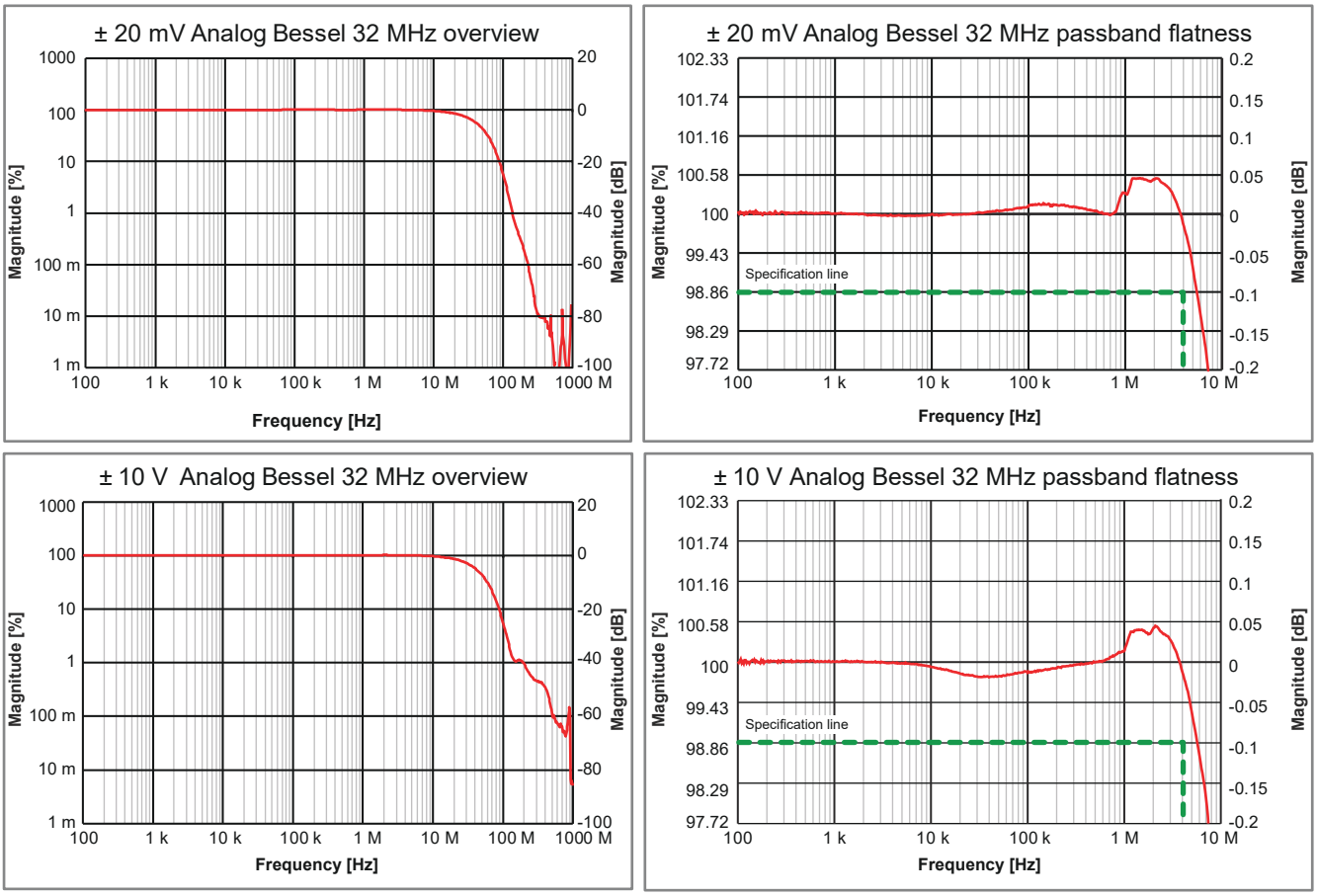
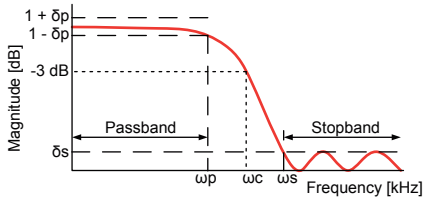


Figure A.190: Representative Bessel examples

(1) Measured using Fluke 5730A calibrator, DC normalized and a Fluke 9500B calibrator for the card, when 1 MΩ input is selected.

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.191: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-alias filter bandwidth	32 MHz ± 3 MHz (-3 dB)
Analog anti-alias filter characteristic	6-pole Bessel, optimal step response
Bessel IIR filter characteristic	8-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed. Maximum sample rate: 100 MS/s (GN8101B/ GN8102B), 25 MS/s (GN8103B), minimum filter selection: 40 Hz.
Bessel IIR filter bandwidth (ωc)	User selectable from 40 Hz to 10 MHz
Bessel IIR 0.1 dB passband (ωp)(1)	DC to 0.1 * ωc or 2 MHz, whichever is lower
Stopband magnitude (δs) at frequency (ωs)	-80 dB at 8 * ωc With the Bessel IIR filter bandwidth selection at high corner frequencies, the magnitude can be more due to the analog anti-alias filter characteristic. At high bandwidth selections, the analog filter can increase this peak to -30 dB, see Figure A.192.
Bessel IIR filter roll-off	48 dB/octave

Bessel IIR Filter (Digital Anti-Alias)

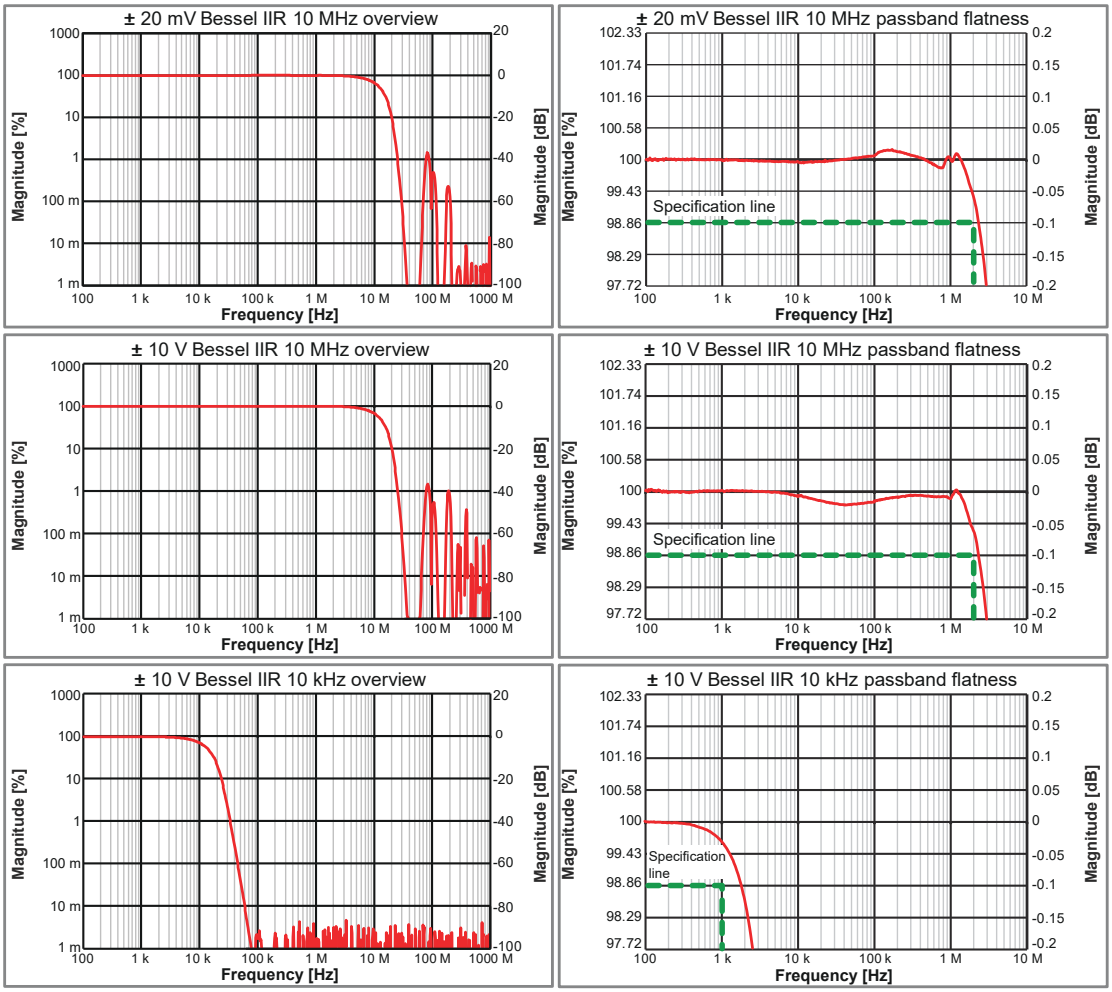
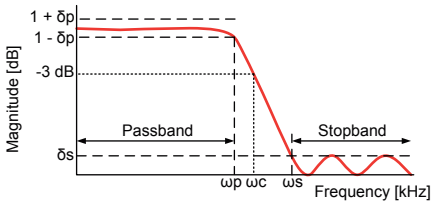


Figure A.192: Representative Bessel IIR examples

(1) Measured using Fluke 5730A calibrator, DC normalized and a Fluke 9500B calibrator for the card, when 1 MΩ input is selected.

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure A.193: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Butterworth IIR filter.

Analog anti-alias filter bandwidth	32 MHz ± 3 MHz (-3 dB)
Analog anti-alias filter characteristic	6-pole Bessel, extended passband response
Butterworth IIR filter characteristic	8-pole Butterworth style IIR
Butterworth IIR filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed. Maximum sample rate: 100 MS/s (GN8101B/ GN8102B), 25 MS/s (GN8103B), minimum filter selection: 50 Hz.
Butterworth IIR filter bandwidth (ωc)	User selectable from 50 Hz to 25 MHz
Butterworth IIR 0.1 dB passband (ωp)(1)	DC to 0.7 * ωc or 4 MHz, whichever is lower
Stopband magnitude (δs) at frequency (ωs)	-80 dB at 4 * ωc With the Butterworth IIR filter bandwidth selection at high corner frequencies, the magnitude can be more due to the analog anti-alias filter characteristic. At high bandwidth selections, the analog filter can increase this peak to -20 dB, see Figure A.194.
Butterworth IIR filter roll-off	48 dB/octave

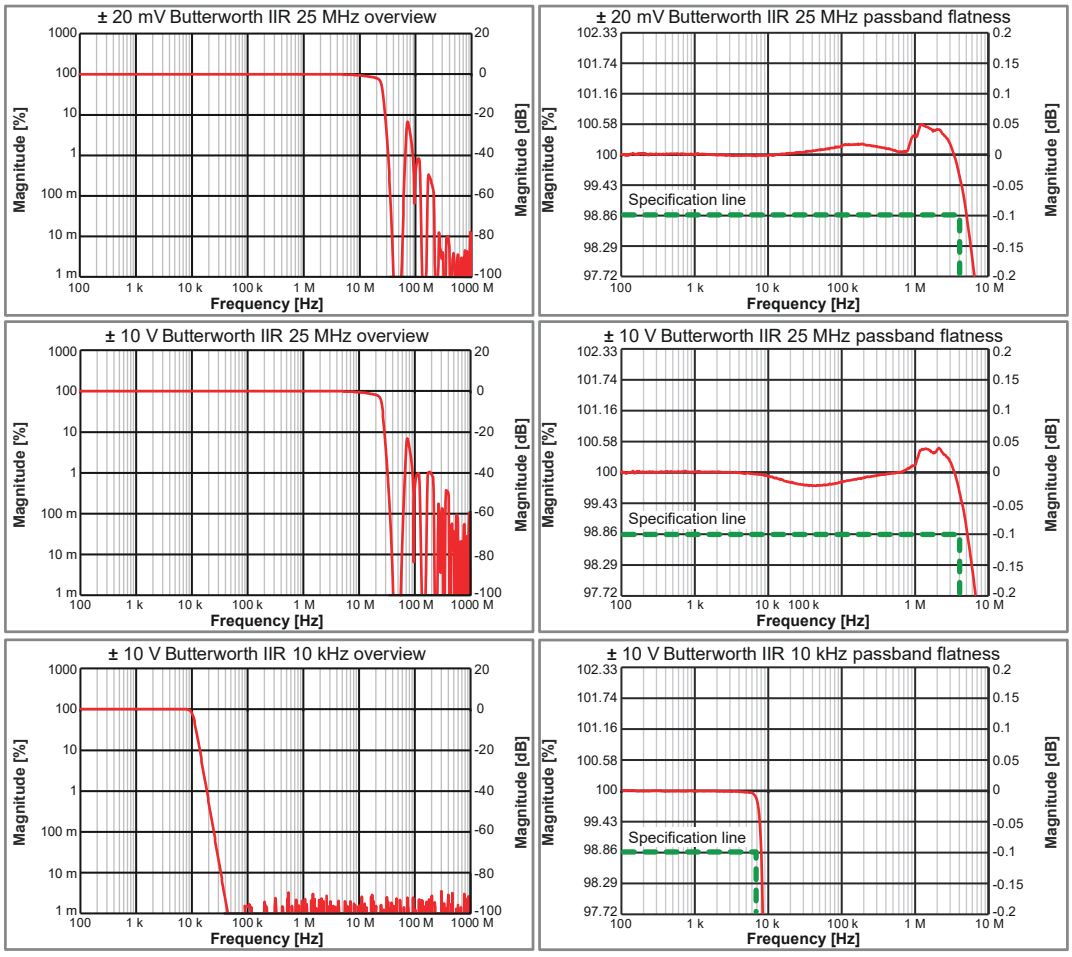


Figure A.194: Representative Butterworth IIR examples

(1) Measured using Fluke 5730A calibrator, DC normalized and a Fluke 9500B calibrator for the card, when 1 MΩ input is selected.

Channel to Channel Phase Match

Using different filter selections (Wideband/analog Bessel/Bessel IIR/Butterworth IIR) or different filter bandwidths will lead to phase mismatches between channels. Under a condition of a sample rate of 250 MS/s and a frequency from 100 kHz to 50 MHz or filter frequency, whichever has a smaller bandwidth.

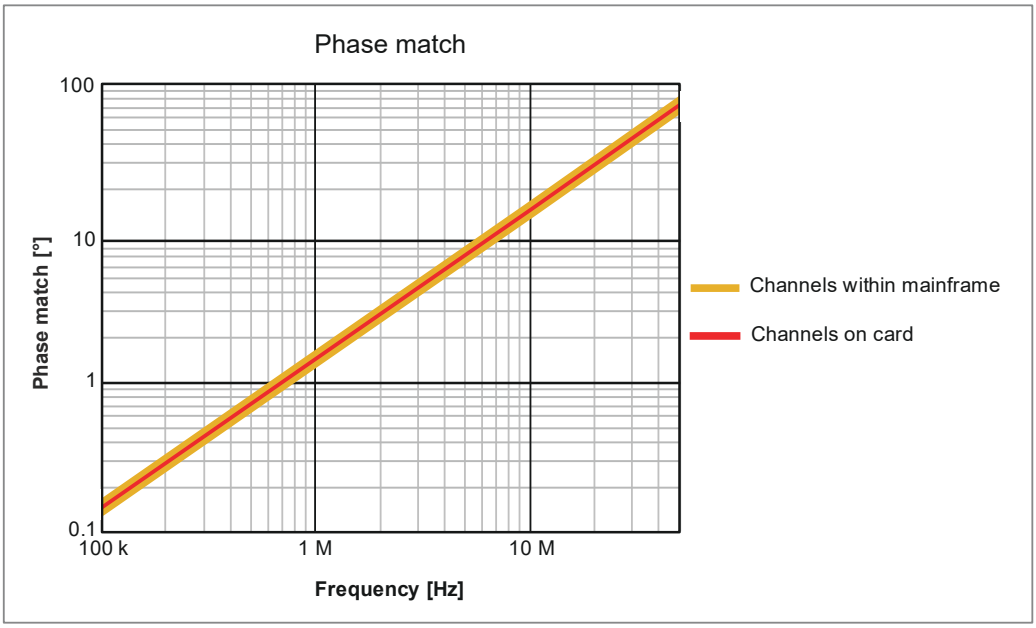


Figure A.195: Representative channel to channel phase match

	All ranges
Wideband	
Channels on card	4 ns
Channels within mainframe	4 ns
Analog Bessel	
Channels on card	4 ns
Channels within mainframe	4 ns
Bessel IIR	
Channels on card	4 ns
Channels within mainframe	4 ns
Butterworth IIR	
Channels on card	4 ns
Channels within mainframe	4 ns
GN8101B/GN8102B/GN8103B channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave)

Channel to Channel Crosstalk

Channel to channel crosstalk is measured with a 50 Ω termination resistor on the input and uses sine wave signals on the channel above and below the channel being tested. To test Channel 2, Channel 2 is terminated with 50 Ω, while Channels 1 and 3 are connected to the sine wave generator.

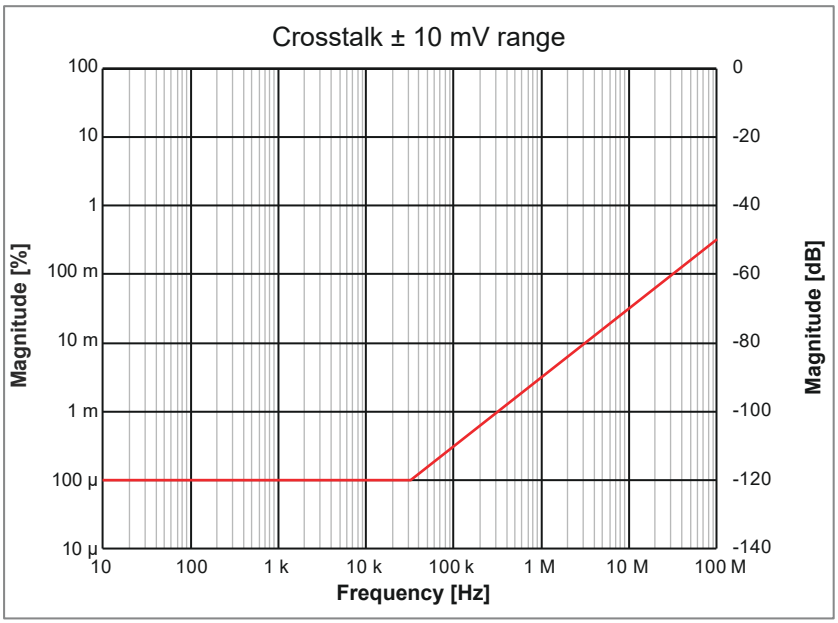


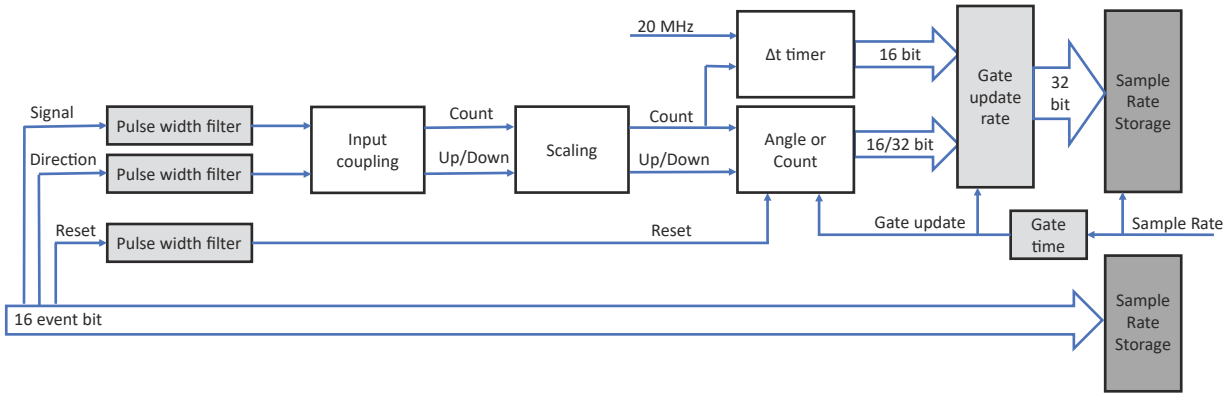
Figure A.196: Representative crosstalk overview

On-board Memory

Per card	8 GB (4 GS)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size analog and digital event channels	16 bits, 2 bytes/sample
Storage sample size Timer/Counter channels	32 bits, 4 bytes/sample

Digital Event/Timer/Counter

The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.



Card sample rate	Digital Event/Timer/Counter sample rate
≤10 MS/s	Sample rate
12.5 MS/s	Not supported
20 MS/s	Sample rate
25 MS/s	Not supported
40 MS/s	20 MS/s (GN8101B and GN8102B only)
50 MS/s	Not supported
100 MS/s	20 MS/s (GN8101B and GN8102B only)
125 MS/s	Not supported
200 MS/s	20 MS/s (GN8101B only)
250 MS/s	Not supported
Digital input events	16 per card
Levels	TTL input level, user programmable invert level
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs
Overvoltage protection	± 30 V DC continuously
Minimum pulse width	100 ns
Maximum frequency	5 MHz
Digital output events	2 per card
Levels	TTL output levels, short circuit protected
Output event 1	User selectable: Trigger, Alarm, set High or Low
Output event 2	User selectable: Recording active, set High or Low
Digital output event user selections	
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay
Alarm	High when alarm condition is activated, low when not activated (alarm conditions of this card only) 200 µs ± 1 µs ± 1 sample period alarm event delay
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation
Timer/Counter	2 per card
Levels	TTL input levels
Inputs	3 pins: signal, reset and direction All pins are shared with digital event inputs
Input coupling	Uni-directional, Bi-directional and ABZ incremental encoder (Quadrature)
Measurement modes	Count, Angle, Frequency and RPM (freq = count / Δt)

Input Coupling Uni- and Bi-directional Signal

Uni- and bi-directional input coupling is used when the direction signal is a stable signal.

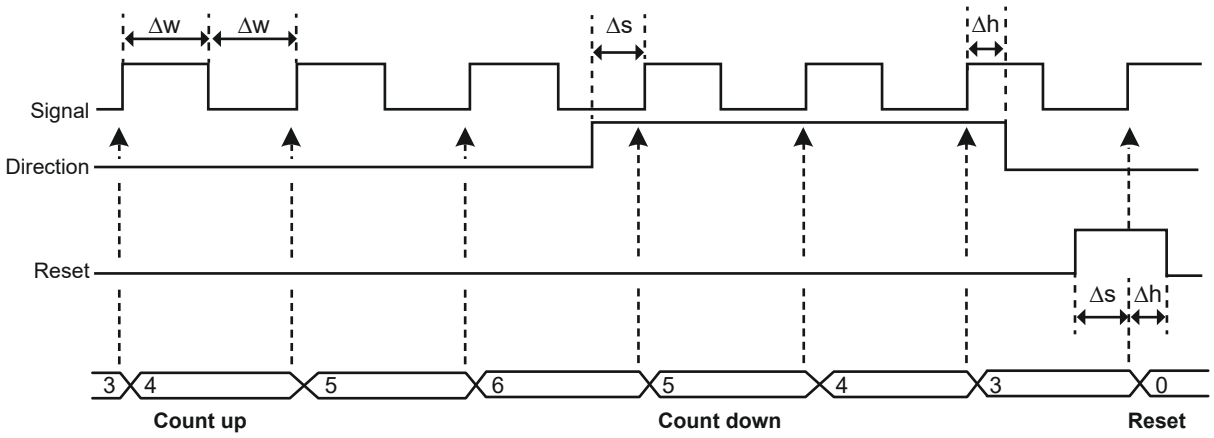


Figure A.197: Uni- and Bi-directional timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	4 MHz
Minimum pulse width (Δw)	100 ns
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional mode Low: increment counter/positive frequency High: decrement counter/negative frequency
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Input Coupling ABZ Incremental Encoder (Quadrature)

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

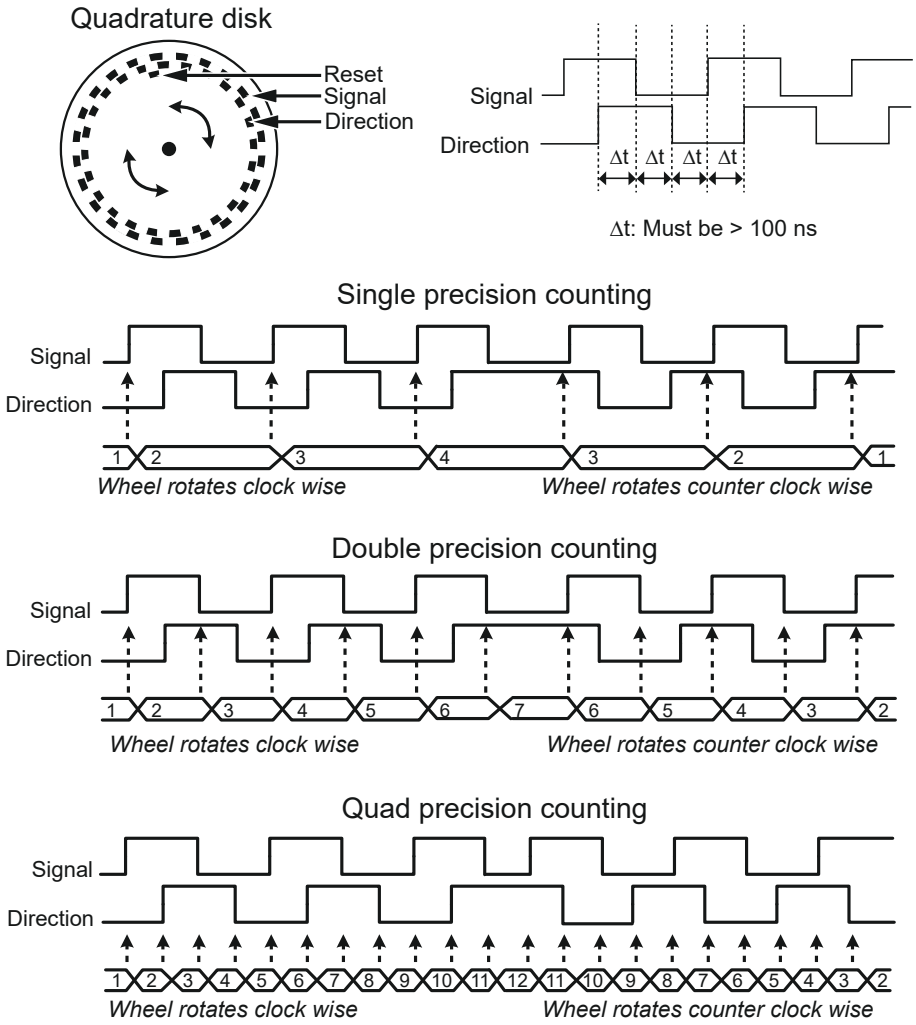


Figure A.198: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Minimum pulse width filter	100 ns, 200 ns, 500 ns, 1 µs, 2 µs, 5 µs
Maximum input signal frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single (X1), dual (X2) or quad (X4) precision
Input coupling	ABZ incremental encoder (Quadrature)
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Measurement Mode Angle	
In angle measurement mode the counter will use a user defined maximum angle and revert back to zero when this count value is reached. Using the reset input the measured angle can be synchronized to the mechanical angle. The real-time calculators can extract the RPM from the measured angle independent from the mechanical synchronization.	
Angle options	
Reference	User selectable. Enables the use of the reset pin to reference the mechanical angle to the measured angle
Angle at reference point	User defined to specify mechanical reference point
Reset pulse	Angle value is reset to user defined "angle at reference point" value
Pulses per rotation	User defined to specify the encoder/count resolution
Maximum pulses per rotation	32767
Maximum RPM	30 * sample rate (Example: Sample rate 10 kS/s means maximum 300 k RPM)

Measurement Mode Frequency/RPM	
Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.	
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s. Minimum gate measuring time is 50 ns. Can be selected by user to control update rate independent of sample rate

Measurement Mode Count/Position	
Count/position mode is typically used for tracking movement of device under test. To reduce the sensitivity for count/position errors due to clock glitches use the minimum pulse width filter or enable the ABZ in stead of uni-/bi-polar input coupling .	
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31}$ - 1; bi-directional count

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	Selectable: (10 µs to 516 µs) - 1 µs ± 1 µs + maximum 1 sample period using decimal time base (9.76 µs to 504 µs) - 1 µs ± 1 µs + maximum 1 sample period using binary time base

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to 1 GS
Maximum trigger rate	400 triggers per second
Maximum delayed trigger	1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger In edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger In delay	± 1 µs + maximum 1 sample period (identical for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger Out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger Out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; For details, please refer to the mainframe datasheet
Trigger Out delay	Selectable (10 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (9.76 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516 (504) µs for decimal (binary) time base, compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from external RTC channels Logical AND of qualifiers from external RTC channels
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge, falling edge or both edges
Qualifiers	Active High or Active Low for every event channel

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Maximum, Minimum and Peak to Peak values

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)

The real-time formula database (RT-FDB) option offers an extensive set of math routines to enable almost any real-time mathematical challenge. The database structure enables the user to define a list of mathematical equations similar to the Perception review formula database.
The maximum supported sample rate is 2 MS/s.
The real-time formula database feature set is extended with higher Perception Versions. Different versions of Perception therefore can enable more or less features as described in this table.

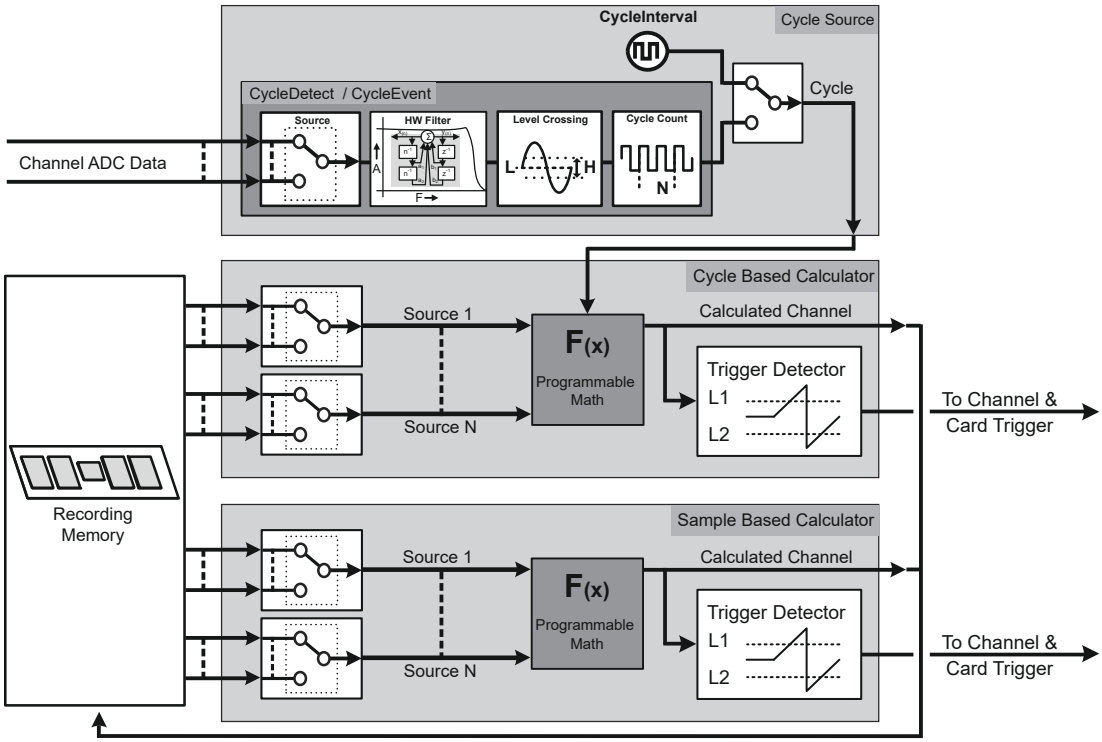


Figure A.199: Real-time formula database (RT-FDB) calculators

The real-time formula database supports the following list of calculations (Details of each calculation are described in the manual).

Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Basic calculations				
`+ (add)`	✓	✓	✓	✓(1)
`- (subtract)`	✓	✓	✓	✓(1)
`* (multiply)`	✓	✓	✓	✓(1)
`/ (divide)`	✓	✓	✓	✓(1)
Enhanced calculations				
`Abs`	✓	✓	✓	✓(1)
`Atan`	✓	✓	✓	✓(1)
`Atan2`	✓	✓	✓	✓(1)
`Cosine`	✓	✓	✓	✓(1)
`DegreesToRadians`	✓	✓	✓	✓(1)
`Min`	✓	✓	✓	✓(1)
`Max`	✓	✓	✓	✓(1)
`Modulo`	✓	✓	✓	✓(1)
`RadiansToDegrees`	✓	✓	✓	✓(1)
`Sine`	✓	✓	✓	✓(1)
`Sqrt`	✓	✓	✓	✓(1)
`Tan`	✓	✓	✓	✓(1)

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Boolean calculations				
`Equal`	✓	✓	✓	✓
`GreaterEqualThan`	✓	✓	✓	✓
`GreaterThan`	✓	✓	✓	✓
`LessEqualThan`	✓	✓	✓	✓
`LessThan`	✓	✓	✓	✓
`NotEqual`	✓	✓	✓	✓
`InsideBand`	✓	✓	✓	
`OutsideBand`	✓	✓	✓	
`And`	✓	✓	✓	✓
`Or`	✓	✓	✓	✓
`Xor`	✓	✓	✓	✓
`Not`	✓	✓	✓	✓
Cycle based calculations				
`CycleArea`		✓	✓	✓
`CycleBusDelay`		✓	✓	✓
`CycleCount`		✓	✓	✓
`CycleCrestFactor`		✓	✓	✓
`CycleEnergy`		✓	✓	✓
`CycleFundamentalPhase`		✓	✓	✓(2)
`CycleFundamentalRMS`		✓	✓	✓
`CycleFrequency`		✓	✓	✓
`CycleMax`		✓	✓	✓
`CycleMean`		✓	✓	✓
`CycleMin`		✓	✓	✓
`CyclePeak2Peak`		✓	✓	✓
`CyclePhase`		✓	✓	✓
`CycleRMS`		✓	✓	✓
`CycleRPM`		✓	✓	✓
`CycleSampleCount`		✓	✓	✓
`CycleTHD`(2)		✓	✓	✓(2)
Cycle source				
`CycleDetect`(4)		✓	✓	
`CycleEvent`		✓	✓	
`CycleInterval`		✓	✓	

Real-time Formula Database Calculators V7.30 (Option to be ordered separately)				
Operation	Sample based results synchronous	Cycle based results asynchronous	Storage in PNRF recording	Real-time output
Hardware based signal filtering				
`HWFilter`(4)	✓		✓	
Software based signal filtering				
`FilterBesselBP`	✓		✓	
`FilterBesselHP`	✓		✓	
`FilterBesselLP`	✓		✓	
`FilterButterworthBP`	✓		✓	
`FilterButterworthHP`	✓		✓	
`FilterButterworthLP`	✓		✓	
`FilterChebyshevBP`	✓		✓	
`FilterChebyshevHP`	✓		✓	
`FilterChebyshevLP`	✓		✓	
Special category calculation				
`HarmonicsIEC61000`	✓		✓	
`Integrate`	✓		✓	
Signal transformation				
`DQZeroTransformation (Park)` (3)	✓		✓	✓(1)
`SpaceVectorTransformation`(3)	✓		✓	
`SpaceVectorInverse Transformation`(3)	✓		✓	
Signal generation				
`SineWave`	✓		✓	
`Ramp`	✓		✓	
Trigger functions				
`TriggerOnBooleanChange`			Trigger mark	
`TriggerOnLevel`			Trigger mark	

(1) Only cycle based results can be used for real-time output. Use the CycleMean calculation on recorded channel data or sample based results to enable the real-time output of this data.

(2) The time required to calculate the output depends on maximum cycle length and sample rate. Depending on the selected settings the output latency will increase. HBM refers to these calculations as not deterministic. All real-time output published values (deterministic and/or not deterministic) will always have the same latency.

(3) This formula is only available if the eDrive license is added to Perception.

(4) The output of HWFilter is used for CycleDetect.

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used. In Dual mode the RT-FDB calculators sample based results are only calculated for the sweep sections of the recorded data. Due to the asynchronous nature of cycle based results, all cycle based results are continuously stored and used in both the sweep as well as the continuous sections of the recording.

Single Sweep	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1 GS after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Single sweep	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	8 channels 1 Timer/Counter	8 channels 2 Timer/Counters	8 channels 2 Timer/Counters Digital events
Maximum sweep memory	1000 MS	1000 MS	1000 MS	940 MS	740 MS	605 MS	510 MS	435 MS	340 MS	280 MS	250 MS
Maximum sweep sample rate	250 MS/s (GN8101B) 100 MS/s (GN8102B) 25 MS/s (GN8103B)								200 MS/s (GN8101B) 100 MS/s (GN8102B) 20 MS/s (GN8103B)		

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1 GS after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording and maximum 2000 sweeps waiting for storage
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Multi sweep	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	8 channels 1 Timer/Counter	8 channels 2 Timer/Counters	8 channels 2 Timer/Counters Digital events
Maximum sweep memory	1000 MS	1000 MS	1000 MS	940 MS	740 MS	605 MS	510 MS	435 MS	340 MS	280 MS	250 MS
Maximum sweep sample rate	250 MS/s (GN8101B) 100 MS/s (GN8102B) 25 MS/s (GN8103B)								200 MS/s (GN8101B) 100 MS/s (GN8102B) 20 MS/s (GN8103B)		

Continuous

Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Continuous	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	8 channels 1 Timer/Counter	8 channels 2 Timer/Counters	8 channels 2 Timer/Counters Digital events
Maximum FIFO	3800 MS	1800 MS	1200 MS	900 MS	720 MS	600 MS	510 MS	450 MS	360 MS	280 MS	250 MS
Maximum sample rate	25 MS/s								20 MS/s		
Maximum aggregate streaming rate	25 MS/s	50 MS/s	75 MS/s	100 MS/s	125 MS/s	150 MS/s	175 MS/s	200 MS/s	200 MS/s	240 MS/s	260 MS/s

Dual

Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length. If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1 GS after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off. When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended posttrigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	1 channel	2 channels	3 channels	4 channels	5 channels	6 channels	7 channels	8 channels	8 channels 1 Timer/Counter	8 channels 2 Timer/Counters	8 channels 2 Timer/Counters Digital events
Max. sweep memory	1000 MS	1000 MS	1000 MS	745 MS	585 MS	477 MS	399 MS	342 MS	267 MS	217 MS	195 MS
Max. sweep sample rate	250 MS/s (GN8101B) 100 MS/s (GN8102B) 25 MS/s (GN8103B)								200 MS/s (GN8101B) 100 MS/s (GN8102B) 20 MS/s (GN8103B)		
Max. FIFO	800 MS	400 MS	260 MS	180 MS	144 MS	120 MS	103 MS	89 MS	68 MS	55 MS	50 MS
Max. continuous	Sweep Sample Rate / 2 with a max. of 25 MS/s								Sweep Sample Rate / 2 with a max. of 20 MS/s		
Max. aggregate streaming rate	25 MS/s	50 MS/s	75 MS/s	100 MS/s	125 MS/s	150 MS/s	175 MS/s	200 MS/s	200 MS/s	240 MS/s	260 MS/s

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 10 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

B Options, to be ordered separately

B.1 Batteries and battery chargers

B.1.1 Rechargeable Li-ion SM202 battery

G034, G301: Rechargeable Li-ion SM202 Battery (Option, to be ordered separately)	
Option G034 is battery only. Option G301 is a combination of the battery (G034) and the battery carrier (see Figure B.1) **Note** *Shipment regulations don't allow HBM to import batteries to all countries. These regulations change almost yearly and are increasingly becoming more strict. Check with the local HBM office before ordering the battery from HBM.* *Use only HBM approved batteries to avoid unexpected failures and/or specification deviations.* Standard G034 batteries have almost all world-wide approvals and are available for purchase locally in most countries. For more information, please refer to the following website: www.rrc-ps.com	
Chemical system	Lithium Ion (Li-Ion)
Battery voltage	11.25 V
Typical weight	490 g (1.1 lb)
Nominal capacity	8850 mAh
Mechanical form factor	SM202
Dimensions	149 mm (5.86”) x 89 mm (3.50”) x 19.7 mm (0.77”) (D x W x H)
Smart battery	SMbus & SBDS revision 1.1 Compliant
Maximum charge voltage	13.0 V
Recommended charge current	4.0 A
Typical charging time	3 hours @ a charging current of 4 A
Discharge temperature	-20 °C to +55 °C (-4 °F to +131 °F)
Charge temperature	+0 °C to +40 °C (+32 °F to +104 °F)
Storage temperature	-20 °C to +50 °C (-4 °F to +122 °F). Recommended -20 °C to +25 °C (-4 °F to +77 °F)
Original manufacturer's part number	RRC power solutions RRC2020
Compliance information	CE / UL 2054 / UL1642 / FCC / IEC 62133 / EN 60950 / RoHS / UN 38.3 / PSE / RCM / CQC / BIS IS160346
Availability	Available in most countries worldwide
Recycling	Registered with most recycling systems worldwide

Figure B.1: G034 battery (left) and G301 battery with carrier (right)

B.1.2 Li-ion battery charger

G109: Li-ion Battery Charger (Option, to be ordered separately)	
Li-ion two-bay battery charger	
Smart battery support	SmBus Level 3
Maximum charge current	3 A, or limited by smart battery
Battery recalibration	SmBus 1.2 A @ 12 V
Charge strategy	Simultaneous for two batteries.

Figure B.2: Two-bay Li-ion battery charger

B.2 BNC to banana adapter

B.2.1 BNC to banana adapter

1-G067: BNC to Banana Adapter (Option, to be ordered separately)

Set of six pieces, safety isolated female BNC to dual 4 mm protected banana adapter.
1000 V RMS CAT II, 600 V RMS CAT III and 1 A current safety ratings. Can be used with GN610B/GN611B input cards.

Figure B.3: BNC to banana adapter

B.3 Breakout cables and panels

B.3.1 Breakout cables

KAB171, KAB172: Breakout Cables (Option, to be ordered separately)	
	
Figure B.4: KAB171/KAB172 breakout cable	
Cable length	1.5 m
Cable type	Multiple coax cables bundled in a sleeve to minimize crosstalk between cables
Coax cable	Axon RG178 B/U (RoHS compliant)
Cable impedance	50 Ω, 105 pF/m
Cable shield	All shields are connected to one another and connected to DSUB ground pins
BNC label	Each BNC is labeled using color and text. Label indicates the channel number and the input type (positive or negative).
Cable variants	
KAB171	SUBD connector to 16 male BNCs, 1 BNC/channel (single-ended) 16 coax cables (1 coax cable/channel), 5 V output not connected in cable
KAB172	SUBD connector to 32 male BNCs, 2 BNCs/channel (differential) 32 coax cables (2 coax cables/channel), 5 V output not connected in cable

KAB183: Push-Pull Sensor Cable	
Sensor line for connection of sensors to card. 14 wires with open ends, lengths 1 m (3.3 ft) or 10 m (33 ft) using ODU 14 pin push-pull plug	

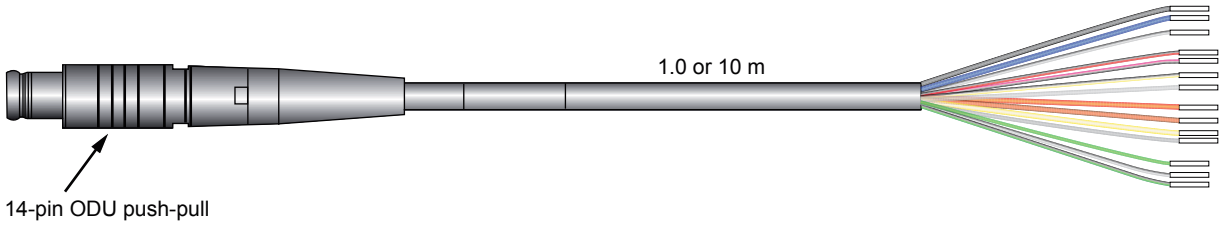
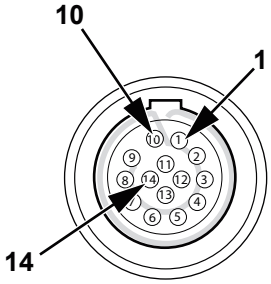



Figure B.5: Push-pull sensor cable	
Cable length	1 m (3.3 ft) or 10 m (33 ft)
Cable type	14 wires, 7 * 2 pair twisted, with cable shield
Cable impedance	tbd Ω, tbd pF/m

KAB183: Push-Pull Sensor Cable



1	Black	6	Yellow/Black	11	Grey
2	Blue	7	White	12	Green
3	White/Black	8	Red	13	Grey/Black
4	Red/Black	9	Brown	14	Green/Black
5	Pink/Black	10	Yellow		

Figure B.6: Pin number and wire colors

KABXXX: Breakout Cable (Option, to be ordered separately)

Figure B.7: Eight channel breakout cable

Cable length	3.0 m (9.9 ft)
Cable type	16 coax cables to minimize crosstalk between cables, bundled in a sleeve for ease of use
Coax cable	Axon RG178 B/U (RoHS compliant)
Cable impedance	50 Ω, 105 pF/m
Cable shield	Per channel the coax cable shield of the positive and negative input are connected to the channel signal ground.
BNC label	Each BNC is labeled using color and text. Label indicates the channel number and the input type (positive or negative).

B.3.2 Breakout panels

G056, G058: Breakout Panels (Option, to be ordered separately)

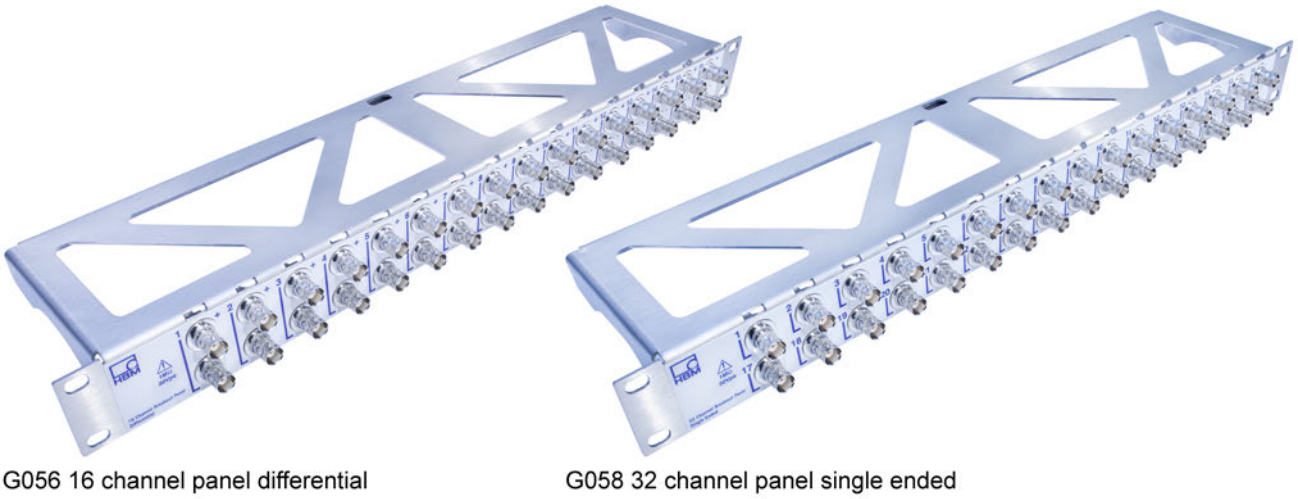


Figure B.8: G056/G058 Breakout panel

Rackmount	19-inch, 1U height
Panel connector	Metal BNC, female in to female out, not isolated from panel
Panel variants	
G056	16 channel, differential (2 BNCs / channel) To be used with: GN3210/GN3211 using KAB172 GN840B/GN1640B using KAB433
G058	32 channel, single-ended (1 BNC / channel) To be used with: GN3210/GN3211 using KAB172 GN840B/GN1640B using KAB433

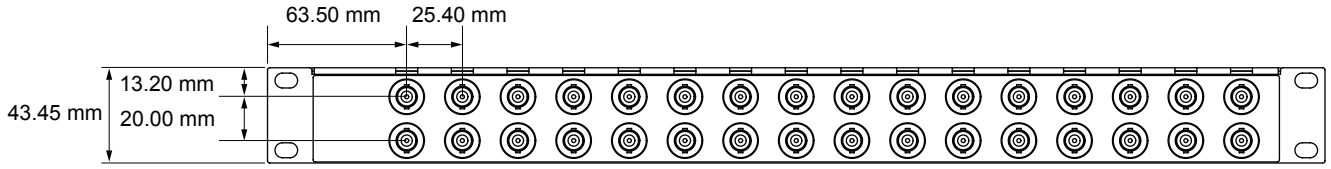


Figure B.9: Breakout panel dimensions

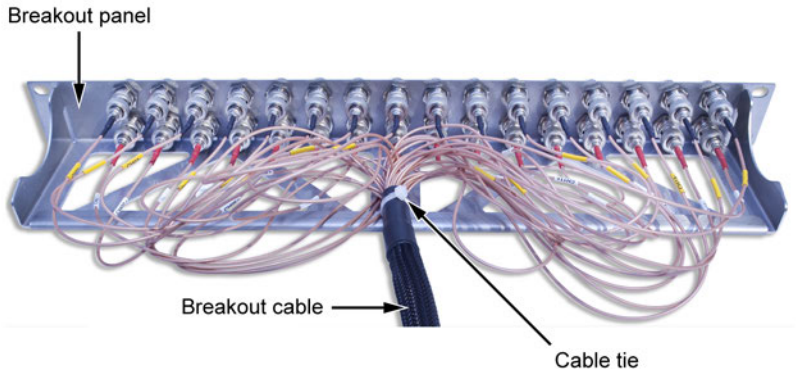


Figure B.10: Breakout cable connected to breakout panel

B.3.3 DIN rail breakouts

1-G088: Generic breakout

DIN rail breakout block push-in connector
DIN rail mountable breakout block. Converts ODU input connector to 12 pin spring/push-in connector.

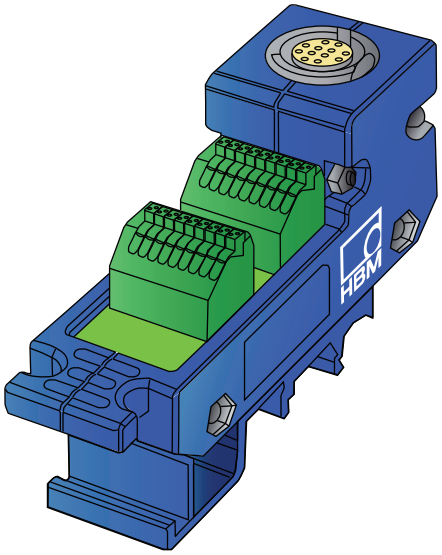


Figure B.11: DIN rail mountable breakout block (1-G088)

1-G089: Thermocouple breakout

DIN rail thermocouple with cold juntion and TEDS
DIN rail mountable breakout block. Converts ODU input connector to universal mini thermocouple connector. Includes digital cold junction temperature measurement and TEDS ID (class 2).

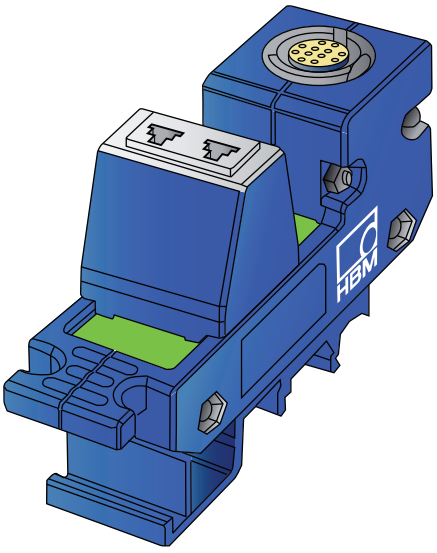


Figure B.12: DIN rail mountable breakout block (1-G089)

1-G090: Basic/IEPE/piezoelectric breakout terminal

DIN rail BNC breakout
DIN rail mountable breakout block. Converts ODU input connector to dual BNC differential output.

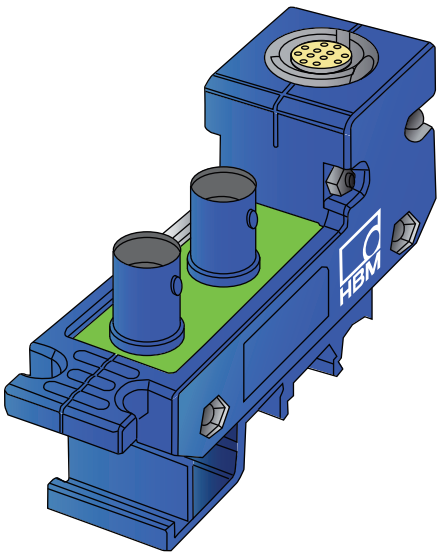


Figure B.13: DIN rail mountable breakout block (1-G090)

G088, G089 and G090 card breakouts assembled on a 19" DIN rail

For the GN840B and GN1640B card breakouts are created that can be assembled on a 19" DIN rail. These DIN rail breakouts mounted on a rail create a breakout panel.

Figure B.14: 1-G088, 1-G089, 1-G090 assembled on a 19" DIN rail

B.4 Burden resistor

B.4.1 High precision burden resistor

High Precision Burden Resistor (Option, to be ordered separately)

Low ohmic, 1 W, 0.02% high precision, low thermal drift burden resistor. Uses 4 wire connection to reduce inaccuracy caused by the currents running to the burden resistor. Using banana input connectors and banana output pins. Directly compatible with GN610B and GN611B acquisition cards.

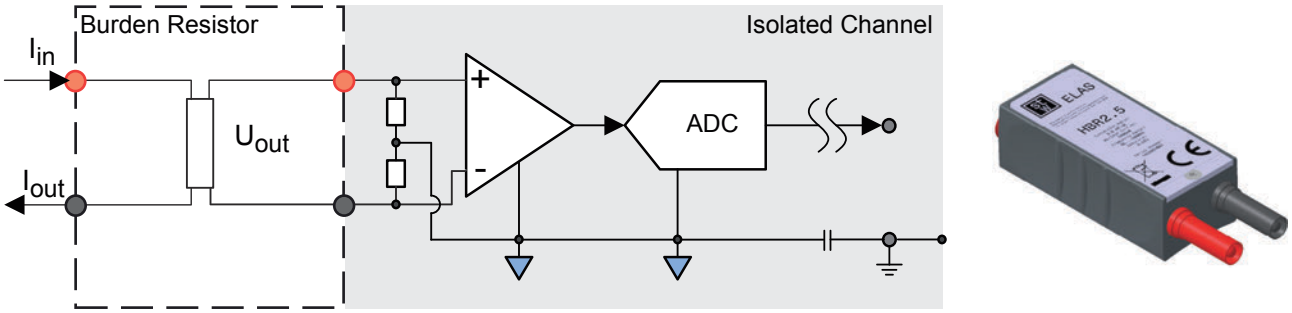


Figure B.15: Block diagram and image

Inaccuracy	± 0.02%		
Temperature coefficient	± 5 ppm / °C (± 9 ppm / °F)		
Bandwidth	-0.5 dB @ 300 kHz		
Input pins	4 mm safety banana, 13 mm (0.51") spacing		
Output pins	4 mm safety banana, 19 mm (0.75") spacing		
Isolation (terminals – earth)	50 V RMS		
Resistor technology	Metal foil		
Maximum power dissipation	1 W		
Original manufacturers part number	HBR1.0	HBR2.5	HBR10
Impedance	1 Ω	2.5 Ω	10 Ω
Maximum input current	1 A	0.63 A	0.31 A
Weight	60 g (2.12 oz)		
Operating temperature range	0 °C to +40 °C (32 °F to 104 °F)		

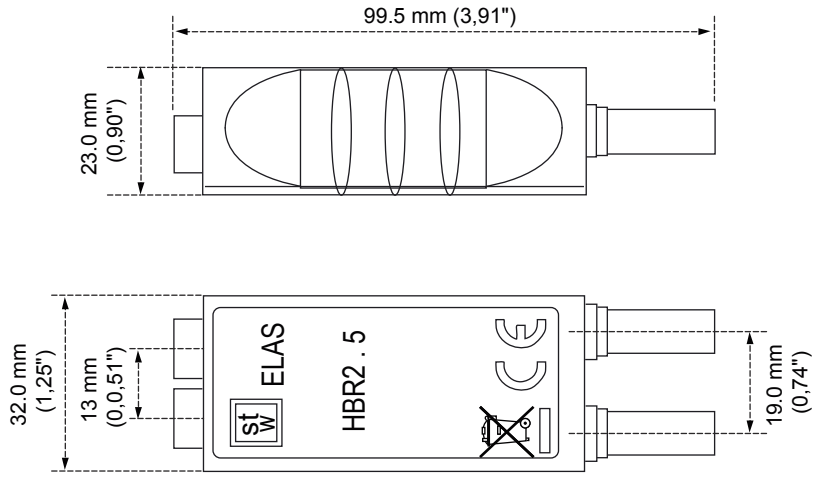


Figure B.16: Dimensions

B.5 Card adapters

B.5.1 Artificial star adapter

G068: Artificial Star Adapter (Option, to be ordered separately)	
The artificial star adapter creates an artificial star point to measure 3 phase signals	
Maximum input voltage	1000 V DC (707 V RMS) between each of the phases
Inputs	3; 4 mm safety banana plugs
Outputs	6; 4 mm safety banana pins; plugs straight into GN610B/GN611B cards
Artificial star N	Reference plug only. Not to be used as input
Safety	Compliant with IEC61010-1 600 V RMS CAT II
Application use	The 3 phase signals L1, L2 and L3 can be connected with inputs L1, L2, L3 of the artificial star adapter. The connection N* is the voltage present on the artificial “star point”.

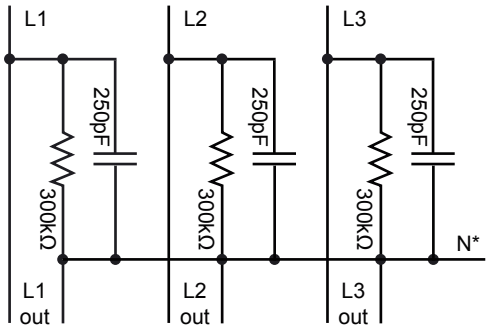


Figure B.17: Electrical schematic

Weight	170 g (6 oz)
Material housing	Polyurethane, vacuum resin casting
Setup	Two boxes can be plugged into a single GN610B/GN611B card Two or more GN610B/GN611B cards with Artificial star adapters fit next to each other
Temperature range	
Operational temperature	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (storage)	-25 °C to +70 °C (-13 °F to +158 °F)

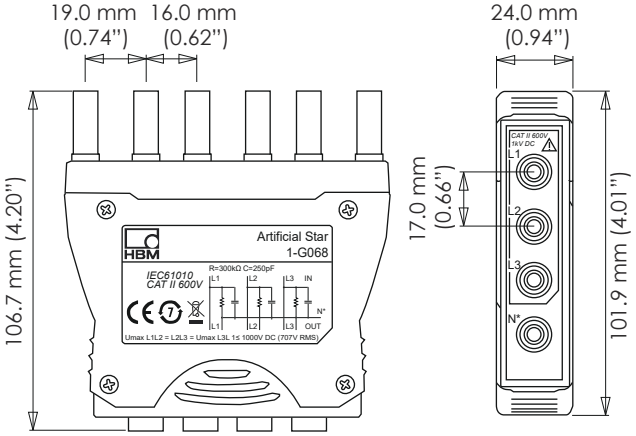


Figure B.18: Artificial star adapter

B.5.2 Artifical star adapter wiring diagram

Artifical Star Adapter Wiring Diagram

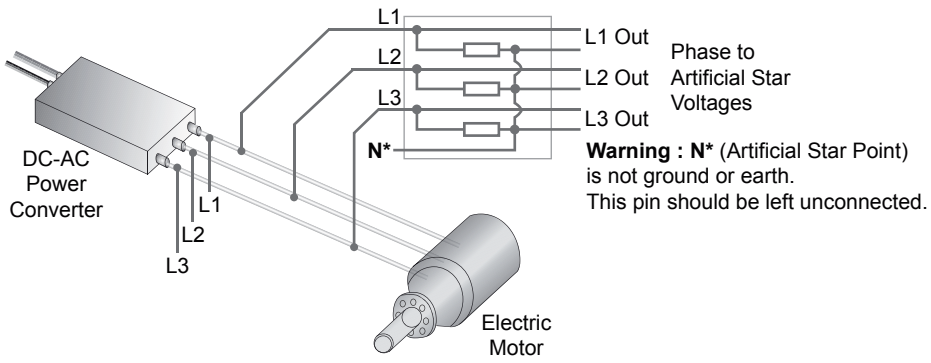


Figure B.19: Three phase representative use of artificial star adapter

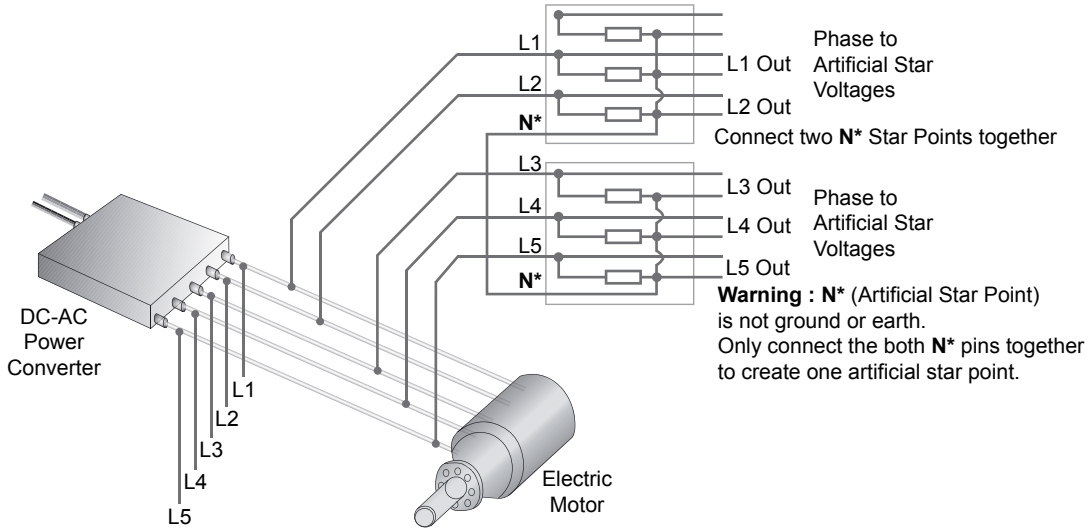


Figure B.20: Five or more phase representative use of dual star adapter

B.6 Option carrier card extensions

B.6.1 Master output card

G083: Master Output Card (Option, to be ordered separately)

Supports up to four Slave mainframes, multiple Master output cards supported (G081 option carrier card required)

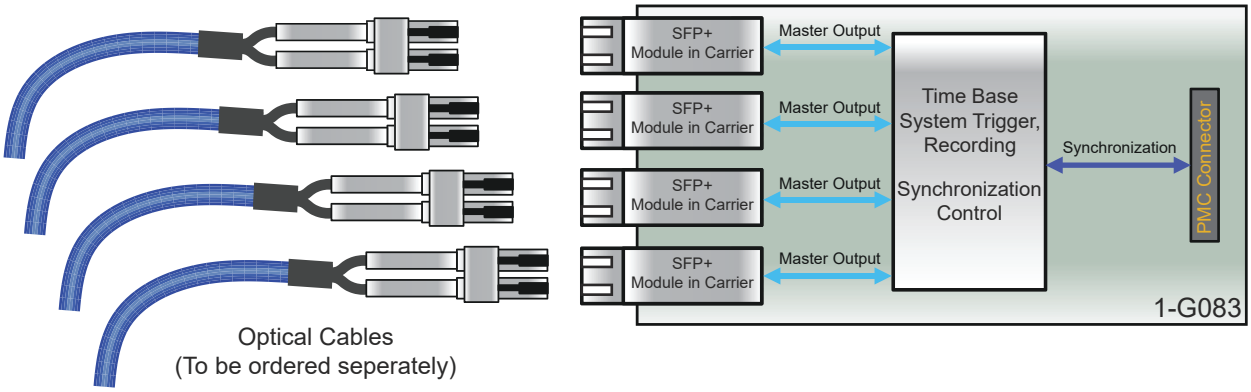


Figure B.21: Block diagram Master output card (G081 required)

Master outputs	Four per Master output card. Up to two Master output cards per option carrier card. All but the first mainframe slots can be filled with option carrier cards.
Mainframe to mainframe phase shift	± 150 ns RMS; measured on analog signals using identical acquisition modules, identical sample rates and filter settings in each mainframe
LED signaling	Optical link synchronized, not connected, function disabled
Master mode	Basic and extended synchronization supported; four Slaves per Master output card Two Master output cards per option carrier card, multiple option carrier cards per mainframe
Slave mode	Not supported. Use Master/Slave synchronization connector of mainframe for Slave mode.
Maximum mainframes	GEN2tB: 9 Slave mainframes, 10 including Master mainframe GEN3i and GEN3t : 17 Slave mainframes, 18 including Master mainframe GEN7i and GEN7tA : 49 Slave mainframes, 50 including Master mainframe GEN17tA : 129 Slave mainframes, 130 including Master mainframe
Time required to full synchronization after Master/Slave signal detected	
No recording active	1 minute typical
Recording or pause active	1 minute plus 25 s per ms recording time deviation from Master time
User notifications while recording	Time marks on Master/Slave signal lost/restored and Master/Slave time synchronized
Basic synchronization (backward compatible with the legacy GEN series Master/Slave card option)	
Cable length propagation delay	±5 ns/m; Automatic cable length detection and propagation delay compensation
First sample	Synchronizes the first sample in a continuous recording for each mainframe. First samples are not recorded in the Slave mainframes defined by the cable length propagation delays. Signal phase shifts are not introduced by this propagation delay.
Synchronized time base	Prevents frequency drift of the sample rates within each mainframe
Measured channel trigger exchange	Synchronously exchanges measured channel triggers connected to the Master/Slave trigger bus between mainframes. Typically used for the sweep recording modes.
Extended synchronization (Not supported by the legacy GEN series Master/Slave card option)	
Calculated channel trigger exchange	Synchronously exchanges real-time calculated (RTC) channel triggers between mainframes. Separate exchange required due to the longer internal delays of RTC channel triggers that were caused by the mathematics prior to establishing a trigger.
Synchronous manual trigger	User action within Perception to trigger all mainframes synchronously
Synchronous recording actions	Start/Stop and Pause a recording across multiple mainframes, each controlled by a separate instance of Perception. Stop recording is a non-synchronous action. Synchronously records distributed data with a mix of GEN7i/GEN3i mainframes in Master/Slave setup while running Perception on each of the mainframes. A more typical Master/Slave setup would be to control both systems from one Perception application.

G083: Master Output Card (Option, to be ordered separately)	
Connection	
Optical wavelength	850 nm
Optical cable type	Multi Mode 50/125 µm (KAB280)
Optical data rate	2 Gbit/s SFP (not compatible with 1 Gbit optical network SFP 1-G062)
Maximum cable length	500 m; Propagation delay caused by cable length automatically compensated for
Connector type	Duplex LC

B.6.2 Option carrier card

G081: Option Carrier Card (Option, to be ordered separately)

Used to enable optional synchronization and other interface cards. (See option card specifications for more details)

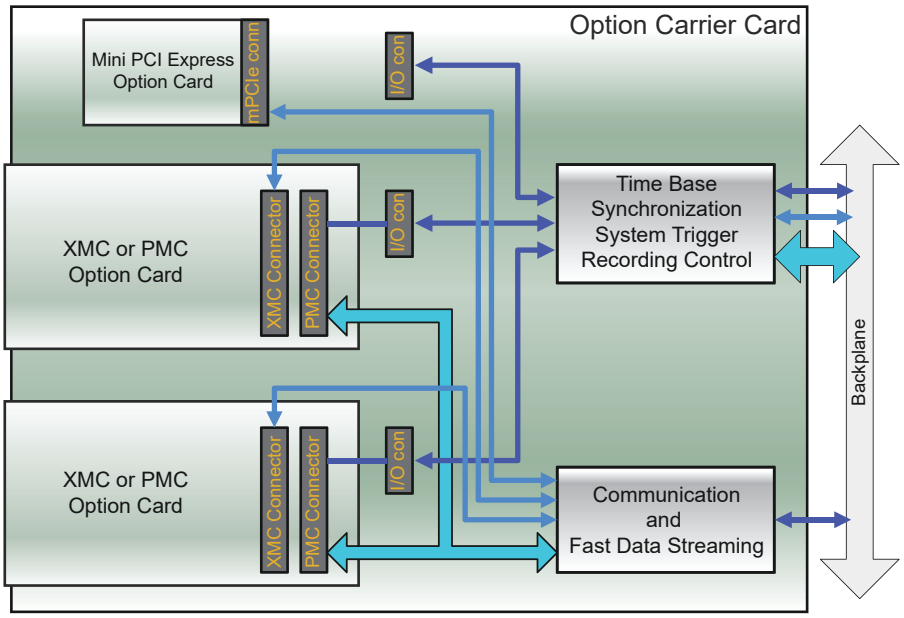


Figure B.22: Block diagram option carrier card

Maximum option carrier cards	Limited by size of mainframe (number of slots -1) All mainframe slots can be used with an option carrier card. Each mainframe needs at least one acquisition card.
Supported mainframes	GEN2tB, GEN3i, GEN3t, GEN7i, GEN7tA and GEN17tA Requires a fast data streaming bus (1)
Option card types	
PMC/XMC cards	Two per option carrier card
Mini PCI express cards	One per option carrier card
Supported PMC/XMC option cards	
Master output card	1-G083 Master output card to support four Slave mainframes per Master output card Two Master output cards per option carrier card, multiple option carrier cards per mainframe
10 Gbit Ethernet card, optical	1-G064 10 Gbit Ethernet card with SFP modules to support 850 nm and 1330 nm optical networks One Ethernet option card per mainframe, cannot be combined with 1-G084
10 Gbit Ethernet card, electrical	1-G084 10 Gbit Ethernet card with RJ45 copper cable support One Ethernet option card per mainframe, cannot be combined with 1-G064
EtherCAT® card	1-G082 EtherCAT® card with configurable slave SDO and PDO data output (no setup) One EtherCAT® option card per mainframe EtherCAT® card not supported in GEN3i and GEN7i
At the time of this specification's release, no Mini PCI express option cards are supported	

(1) Legacy mainframes have different means of supporting similar options

B.6.3 10Gbit Ethernet card, optical

G064: 10Gbit Ethernet Card, Optical (Option, to be ordered separately)

Supports up to two 10Gbit Ethernet connections using SFP+ modules with optical LC connectors (G081 option carrier card required)

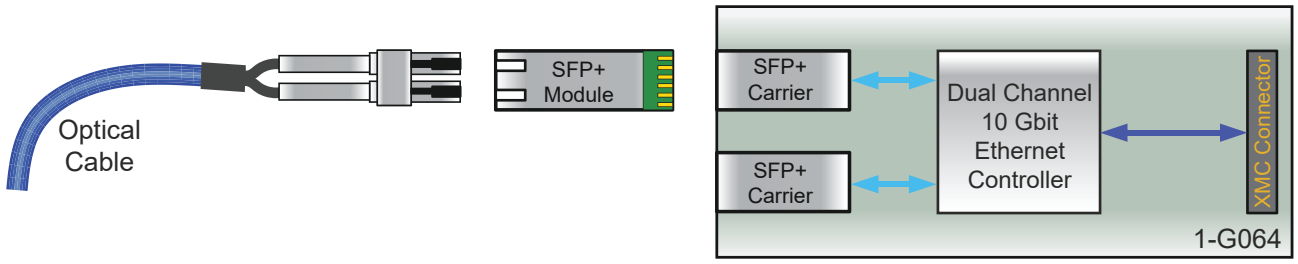


Figure B.23: Block diagram 10Gbit Ethernet card, optical (G081 required)

Maximum number of Ethernet option cards	One Ethernet option card per mainframe, cannot be combined with 1-G084
Network interface	Up to two interfaces each 10 Gbit/s optical using SFP+ modules with LC connectors
Supported SFP+ modules	Multi Mode (10GBASE-SR), to be ordered separately Single Mode (10GBASE-LR), to be ordered separately
Multi Mode SFP+ module (10GBASE-SR)	
Ordering part number	1-G065
Ethernet Speed	1 or 10 Gbit (auto detection)
Optical wave length	850 nm
Maximum cable length	82 m (269 ft) using OM3 specified optical cable (KAB280)
Single Mode SFP+ module (10GBASE-LR)	
Ordering part number	1-G066
Ethernet Speed	1 or 10 Gbit (auto detection)
Optical wave length	1310 nm
Maximum cable length	10 km (6.2 mi) using OS2 specified optical cable (KAB288 or KAB289)
TCP/IP IPv4	
Address setup	DHCP/Auto IP or fixed IP
DHCP setup	When DHCP fails, the APIPA (Automatic Private IP Addressing) setup is used similarly to Windows® PCs
Gateway setup	Gateway setup supported for control through VPN and/or Internet
TCP/IP IPv6	Not supported
PTP V2 (IEEE1588:2008) synchronization	Not supported on Ethernet option cards
Wake On LAN	Not supported on Ethernet option cards
Multiple Ethernet use cases	iSCSI data storage can be used on a separate (dedicated) Ethernet interface PTP V2 (IEEE1588:2008) can be used on a separate (dedicated) Ethernet interface A combination of 10 Gbit and 1 Gbit Ethernet interfaces is supported
Maximum transfer speed	
Continuous recording to remote PC	400 MB/s(1)
Continuous recording to iSCSI NAS	150 MB/s(2)

(1) Tested using circular recording for 48 hours. Test setup uses a Windows® 7 PC with Intel i7 CPU and SSD with sustained write speeds exceeding 700 MB/s and a 10 Gbit Ethernet link.

(2) Tested using circular recording for 48 hours. Test setup uses a Synology® RS3412 configured with a eight disk RAID 0 block level iSCSI partition and a 10 Gbit Ethernet link.

B.6.4 10Gbit Ethernet card, electrical

G084: 10Gbit Ethernet Card, Electrical (Option, to be ordered separately)	
Supports up to two 10Gbit Ethernet connections using RJ45 connectors (G081 option carrier card required)	

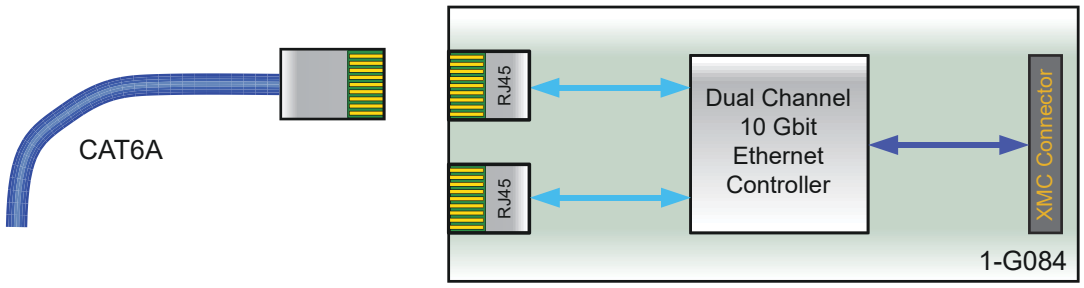


Figure B.24: Block diagram 10Gbit Ethernet card, electrical (G081 required)

Maximum number of Ethernet option cards	One Ethernet option card per mainframe, cannot be combined with 1-G064
Network interface	Up to two interfaces for each 1 Gbit or 10 Gbit/s (auto detection)
Network interface connector	RJ45 (10GBASE-T) using CAT6A or higher cable rating
Maximum cable length (10GBASE-T)	
CAT6A or higher	100 m (330 ft) at 10 Gbit/s
CAT6	55 m (180 ft) at 10 Gbit/s 100 m (330 ft) at 1 Gbit/s
CAT5e	100 m (330 ft) at 1 Gbit/s (not supported at 10 Gbit/s)
TCP/IP IPv4	
Address setup	DHCP/Auto IP or fixed IP
DHCP setup	When DHCP fails, the APIPA (Automatic Private IP Addressing) is used similarly to Windows® PCs
Gateway setup	Gateway setup supported for control through VPN and/or Internet
TCP/IP IPv6	Not supported
PTP V2 (IEEE1588:2008) synchronization	Not supported on Ethernet option cards
Wake On LAN	Not supported on Ethernet option cards
Multiple Ethernet use cases	iSCSI data storage can be used on a separate (dedicated) Ethernet interface PTP V2 (IEEE1588:2008) can be used on a separate (dedicated) Ethernet interface A combination of 10 Gbit and 1 Gbit Ethernet interfaces is supported
Maximum transfer speed	
Continuous recording to remote PC	400 MB/s(1)
Continuous recording to iSCSI NAS	150 MB/s(2)

(1) Tested using circular recording for 48 hours. Test setup uses a Windows® 7 PC with Intel i7 CPU and SSD with sustained write speeds exceeding 700 MB/s and a 10 Gbit Ethernet link.

(2) Tested using circular recording for 48 hours. Test setup uses a Synology® RS3412 configured with a eight disk RAID 0 block level iSCSI partition and a 10 Gbit Ethernet link.

B.7 Current clamps

B.7.1 AC/DC Current Clamp i30s

G912: AC/DC Current Clamp i30s (Option, to be ordered separately)	
To be used with single-ended isolated or non-isolated amplifiers or with differential isolated or non-isolated amplifiers in single-ended mode	

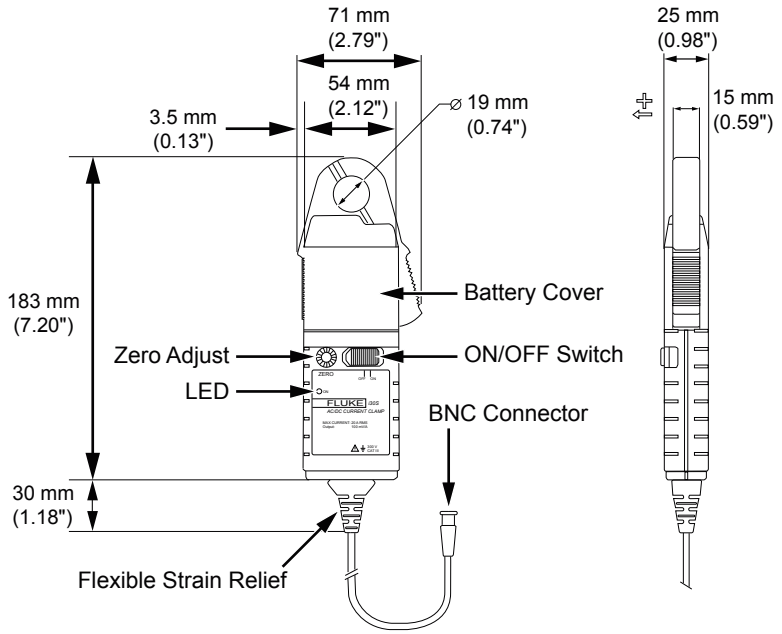


Figure B.25: Dimensions

The i30s current clamp is based on Hall effect technology to measure both DC and AC current. The i30s current clamp may be used with recording instruments to measure the current accurately and non-intrusively.

Electrical specifications	
Current range	30 mA to 30 A DC, 30 mA to 20 A RMS
Inaccuracy	± 1% of reading ± 2 mA (at +25 °C, 77 °F)
Phase shift	< 2 degrees when using frequencies below 1 kHz
Crest factor	1.4
Conductor position sensitivity	± 1% relative to center reading
Output sensitivity	100 mV/A
Bandwidth	DC to -0.5 dB @ 100 kHz
Load impedance	> 100 kΩ
Temperature drift	± 0.01% of reading/°C
Isolation/Working voltage	300 V RMS CAT III, pollution degree 2, frequencies below 1 kHz
General specifications	
Power supply	9 V Alkaline, MN1604/PP3, 30 hours, low battery indicator
Maximum conductor diameter	19 mm (0.75”)
Output connection	Safety BNC connector
Probe cable length	2 m (6.5 ft)
Probe dimensions (HxWxD)	183 x 71 x 25 mm (7.20” x 2.80” x 0.99”)
Probe weight	Typically 250 g (8.8 oz)
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturer's part number	Fluke i30s AC/DC Current Clamp

G912: AC/DC Current Clamp i30s (Option, to be ordered separately)

Figure B.26: AC/DC Current Clamp i30s

B.7.2 AC Current Clamp SR661

G913: AC Current Clamp SR661 (Option, to be ordered separately)

To be used with single-ended isolated or non-isolated amplifiers or with differential isolated or non-isolated amplifiers in single-ended mode

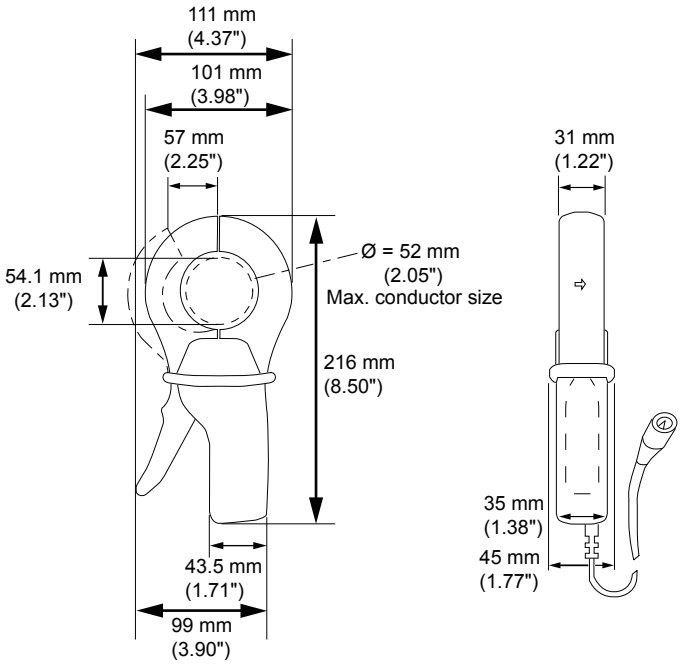


Figure B.27: Dimensions

Built to the highest safety standards, including CE compliance and UL approval in the USA and Canada. Has excellent transformation, low phase shifts and a broad frequency response. Permits the current to be measured accurately for power and power quality applications.

Electrical specifications			
Current range	0.1 A to 1200 A RMS, can be manually selected in 3 steps: 10 A, 100 A, 1000 A		
Selected current range	**10 A**	**100 A**	**1000 A**
Measurement range	0.1 to 12 A	0.1 to 120 A	1 to 1200 A
Output sensitivity	100 mV/A	10 mV/A	1 mV/A
Inaccuracy	± 3% ± 10 mV	± 2% ± 5 mV	± 1% ± 1 mV
Phase shift	≤ 15 degrees	≤ 15 degrees	≤ 3 degrees
Maximum overload	12 A, continuous	120 A, continuous	1200 A, for 20 minutes
Bandwidth	1 Hz to -3 dB @ 100 kHz		
Load impedance	1 MΩ @ 47 pF		
Isolation/Working voltage	600 V RMS CAT III, pollution degree 2		
General specifications			
Maximum conductor diameter	52 mm (2.25”)		
Output connection	Safety BNC connector		
Probe cable length	2 m (6.5 ft)		
Probe dimensions (HxWxD)	216 x 111 x 45 mm (8.50” x 4.37” x 1.77”)		
Probe weight	Typically 550 g (1.21 lb)		
Probe operating temperature range	-10 °C to +50 °C (14 °F to 122 °F)		
Original manufacturer's part number	AEMC SR661 AC Current Clamp		

G913: AC Current Clamp SR661 (Option, to be ordered separately)

Figure B.28: SR661 AC Current Clamp

B.7.3 AC Current Clamp M1V-20-2

G914: AC Current Clamp M1V-20-2 (Option, to be ordered separately)

To be used with single-ended isolated or non-isolated amplifiers or with differential isolated or non-isolated amplifiers in single-ended mode

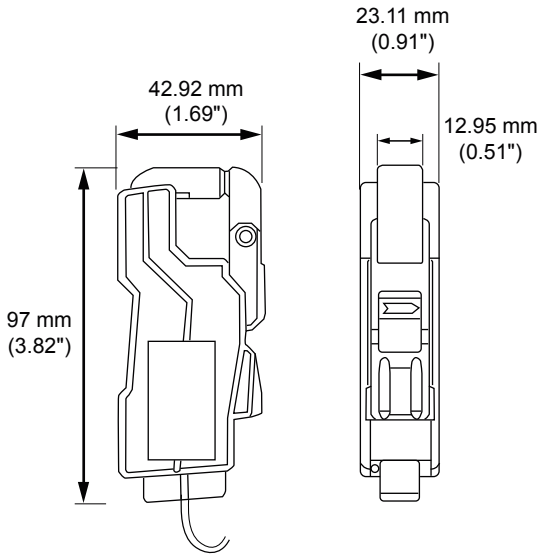


Figure B.29: Dimensions

AC current micro clamp, compliant with IEC standard 348 CLASS II 600 V	
Electrical specifications	
Current range	50 mA to 20 A RMS
Inaccuracy	± 1%
Output sensitivity	100 mV/A
Bandwidth	-3 dB @ 30 Hz to 100 kHz, 3% @ 40 Hz to 2 kHz
Load impedance	> 30 kΩ
Isolation/Working voltage	640 V RMS
General specifications	
Maximum conductor diameter	15 mm (0.59”)
Output connection	Metal BNC
Probe cable length	2 m (6.5 ft)
Probe dimensions (HxWxD)	97 x 43 x 23 mm (3.82” x 1.69” x 0.91”)
Probe weight	Typically 114 g (0.25 lb)
Probe operating temperature range	-10 °C to +50 °C (14 °F to 122 °F)
Original manufacturer's part number	AYA instruments M1V-20-2

Figure B.30: M1V-20-2

B.8 Current transducers and accessories

B.8.1 Current transducers

Current Transducers (Option, to be ordered separately)

Current loop (compensated) current transducers (CT) using an extremely accurate zero flux detector with excellent linearity and low temperature drift. Electrostatic shield between primary and secondary circuit, with low insertion loss and high immunity to electrostatic and magnetic fields. To be used with CT power supply and burden resistor to measure high frequency currents.

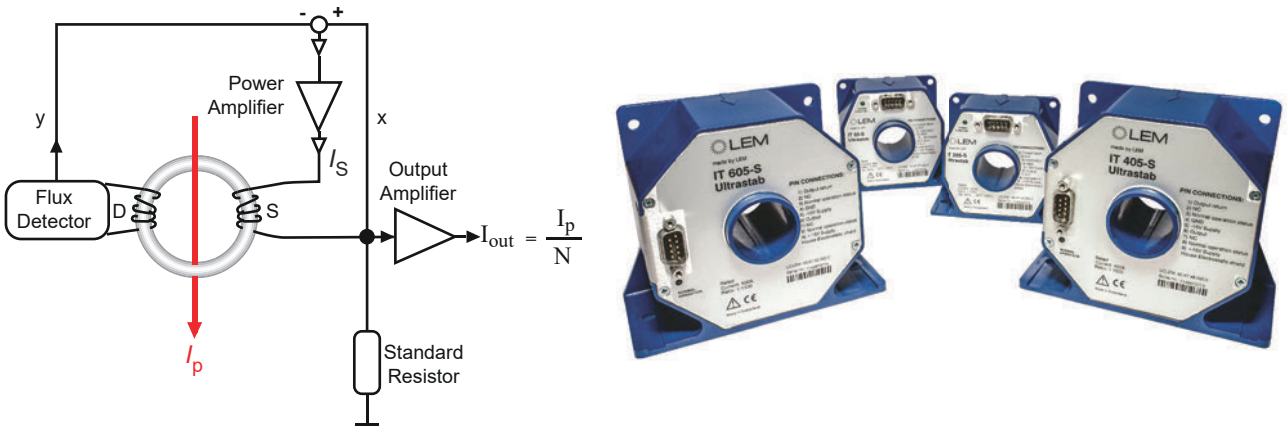


Figure B.31: Simplified block diagram and image

Isolation	150 V RMS reinforced isolation 300 V RMS single isolation				
Linearity	≤ 3 ppm				
Temperature coefficient of I_{oe}	≤ 0.5 ppm/°C (± 0.9 ppm / °F)				
Supply voltages	+ 15 V (± 5%) and - 15 V (± 5%), ≤ 80 mA + I_s				
Original manufacturers part number	LEM ULTRASTAB series				
Operating temperature range	10 °C to +50 °C (50 °F to 122 °F)				
Device	IT 1000-S/SP1	IT 605-S	IT405-S	IT 205-S	IT 65-S
Primary nominal current DC	1000 A DC	600 A DC	400 A DC	200 A DC	60 A DC
Primary nominal current AC	707 A RMS	600 A RMS	400 A RMS	200 A RMS	60 A RMS
Secondary nominal current DC	1000 mA DC	266 mA RMS	200 mA RMS	200 mA RMS	100 mA DC
Conversion ratio (N)	1000:1	1500:1	1500:1	1000:1	600:1
Burden recommendation	HBR1.0	HBR2.5	HBR2.5	HBR2.5	HBR10.0
Small signal bandwidth (-3 dB)	500 kHz	300 kHz	300 kHz	1000 kHz	800 kHz
Weight (typical)	1.0 kg (35.3 oz)	1.08 kg (38.0 oz)	1.08 kg (38.0 oz)	0.35 kg (12.34 oz)	0.33 kg (11.64 oz)
Dimensions					
Cable diameter	30 mm (1.18")	30 mm (1.18")	30 mm (1.18")	26 mm (1.02")	26 mm (1.02")
Width	128 mm (5,03”)	128 mm (5,03”)	128 mm (5,03”)	93 mm (3,66”)	93 mm (3,66”)
Height	106 mm (4,17”)	106 mm (4,17”)	106 mm (4.17”)	77.7 mm (3,05”)	77.7 mm (3,05”)
Depth	85 mm (3,34”)	67 mm (2,63”)	67 mm (2,63”)	47 mm (1.85”)	47 mm (1.85”)

Current Transducers (Option, to be ordered separately)

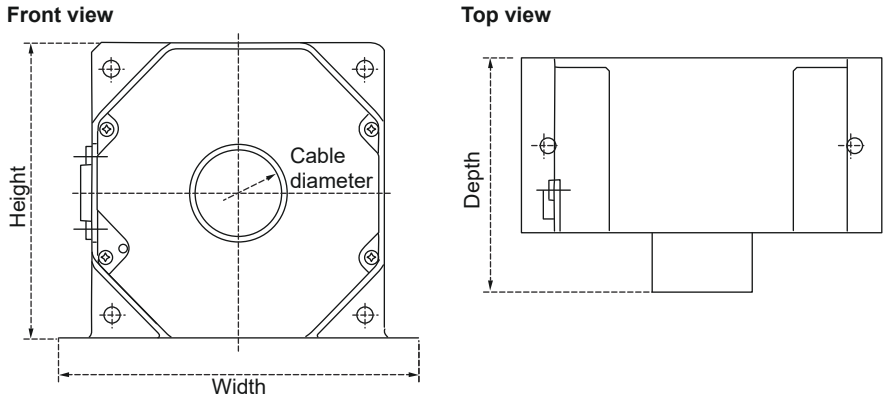


Figure B.32: Dimensions

B.8.2 Connection cable LEM CT to MCTS

Connection cable LEM CT to MCTS (Option, to be ordered separately)

Connection cable between LEM current transducer and MCTS power supply. Available in lengths of 2.5 m (8.20 ft), 5 m (16.40 ft) and 10 m (32.81 ft).

Figure B.33: Connection cable LEM CT to MCTS

B.8.3 Power supply for current transducer

Power Supply for Current Transducer (Option, to be ordered separately)

Empty modular 19” rack with 1 to maximum 6 channel CT support. Housing for the modular power supply and control for LEM current transducers.

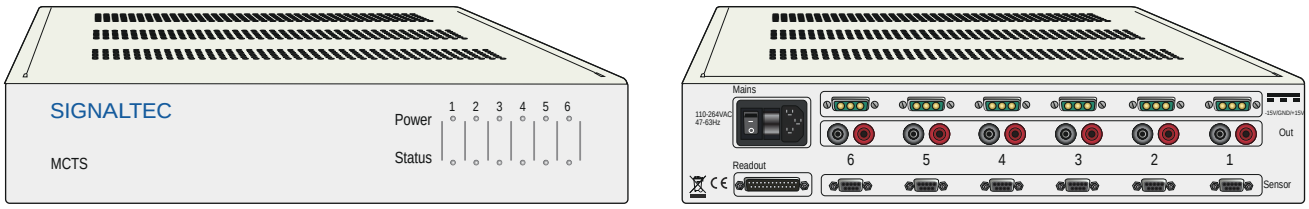


Figure B.34: Front side (left) and rear side (right)

Maximum number of CTs	6
Input connectors	9 pin SUBD
Output connectors	4 mm banana plugs
Signal LEDS	CT Power, CT Status
Power supply	100 to 240 V AC, 47 to 63 Hz @ 650 mA
Weight	Typical 6.5 kg (14.33 lb) configured with 6 channels
Original manufacturers part number	MCTS
Operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Dimensions	
Height	87.2 mm (3,43”)
Width / Width including mounting ears	442 mm (17,40”) / 466 mm (18,34”)
Depth including handles	415 mm (16,33”)

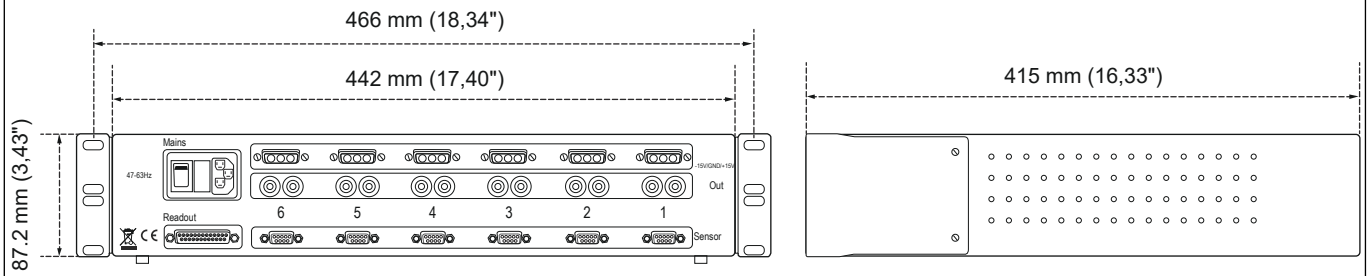


Figure B.35: Dimensions

B.8.4 Current transducer (CT) wire diagram

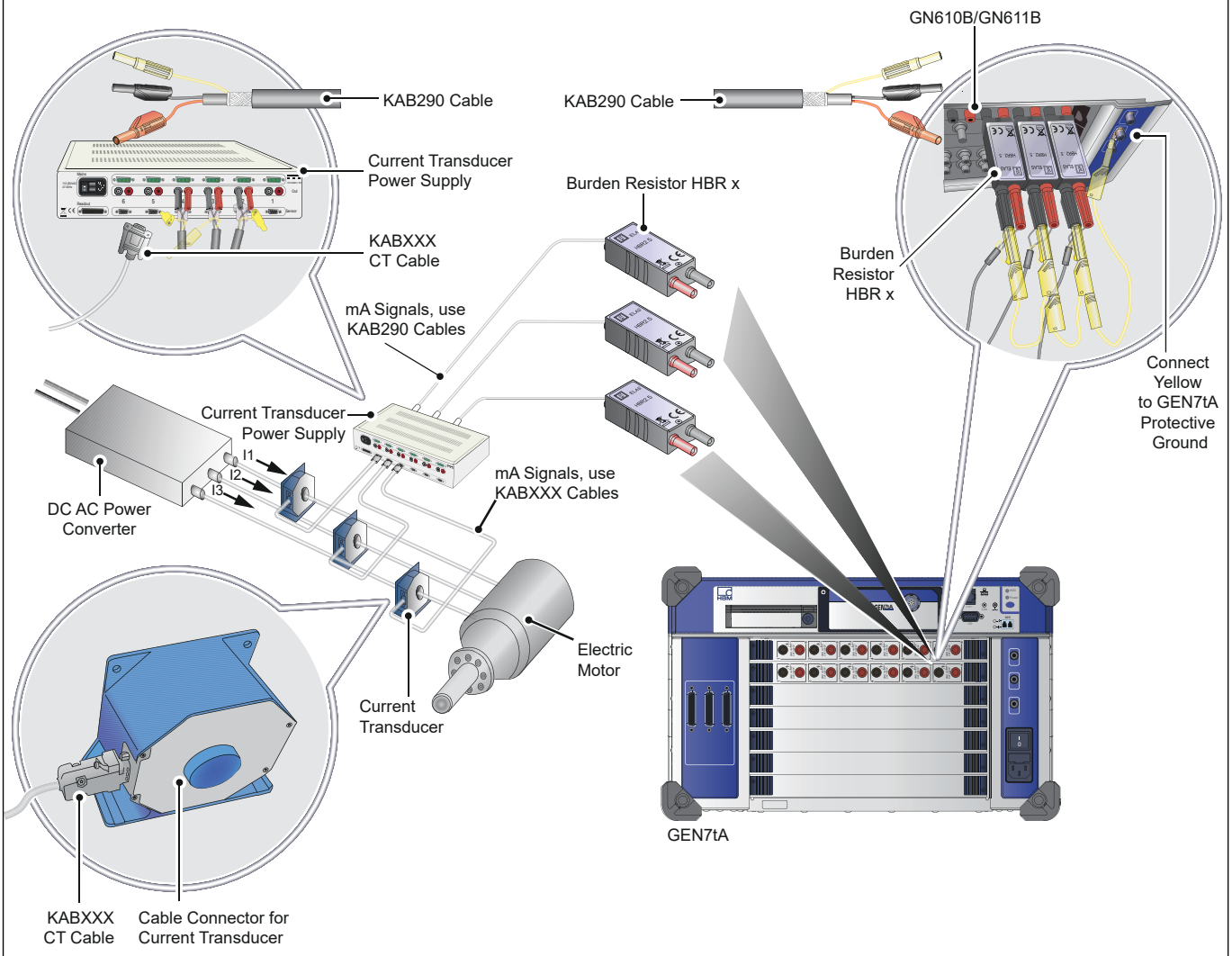


Figure B.36: Current transducer connection diagram

Note *For more information, please refer to "A4775-1.0 en GN610_GN611B to Current Transducer cabling" Installation Guide.*

B.9 Fiber optic cables and SFPs

B.9.1 Standard fiber optic duplex cable

KAB277: Fiber Cables (Option, to be ordered separately)	
Standard fiber optic duplex cable (1-KAB277-xxx)	

Figure B.37: Block diagram and image

Connector type	LC - SCRJ
Glass rating	OM2; Multi Mode
Core/Cladding diameter	50/125 µm
Jacket size	2 mm (0.08")
Jacket rating	Low-smoke zero-halogen
Attenuation	≤ 2.7 dB/km @ 850 nm
Available lengths	10, 20, 50 and 100 m (33, 66, 164 and 328 ft)
Operating temperature	-40 °C to +80 °C

B.9.2 Heavy duty fiber optic duplex cable

KAB278: Fiber Cables (Option, to be ordered separately)	
Heavy duty fiber optic duplex cable (1-KAB278-xxx)	

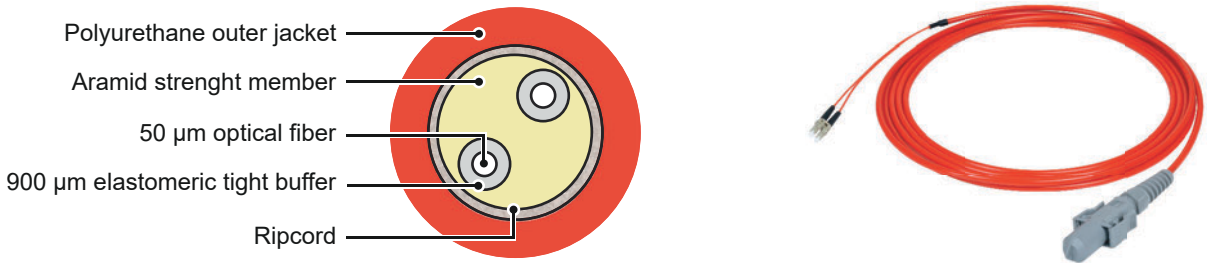


Figure B.38: Block diagram and image

Connector type	LC - SCRJ/IP67
Glass rating	OM2; Multi Mode
Core/Cladding diameter	50/125 µm
Jacket size	6 mm (0.24")
Jacket rating	Polyurethane, halogen free, non-corrosive
Jacket coating	High chemical resistance against acids/alkalis
Attenuation	≤ 2.7 dB/km @ 850 nm
Available lengths	10, 20, 50, 100, 150 and 300 m (33, 66, 164, 328, 492 and 984 ft)
Operating temperature	-40 °C to +80 °C

KAB278: Fiber Cables (Option, to be ordered separately)

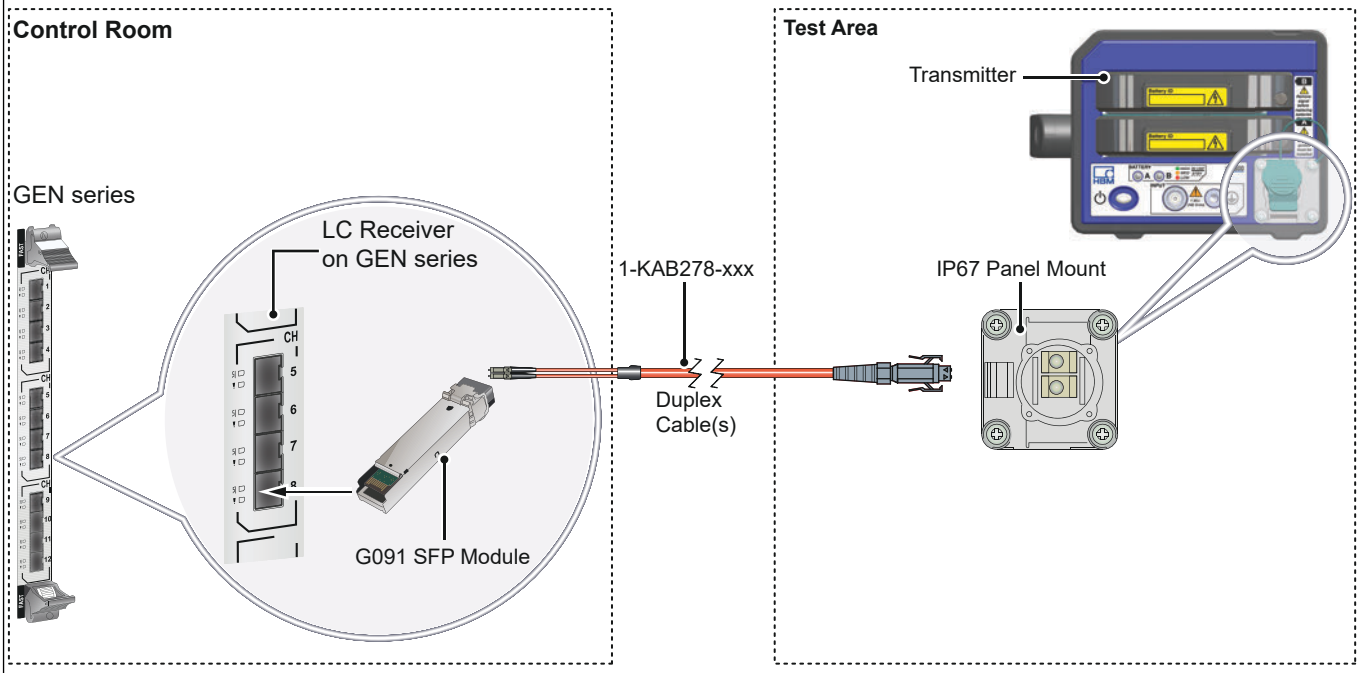


Figure B.39: Application area of a fiber optic duplex cable (Example 1)

B.9.3 Heavy duty fiber optic duplex patch cable

KAB279: Fiber Cables (Option, to be ordered separately)

Heavy duty fiber optic duplex patch cable (1-KAB279-xxx)

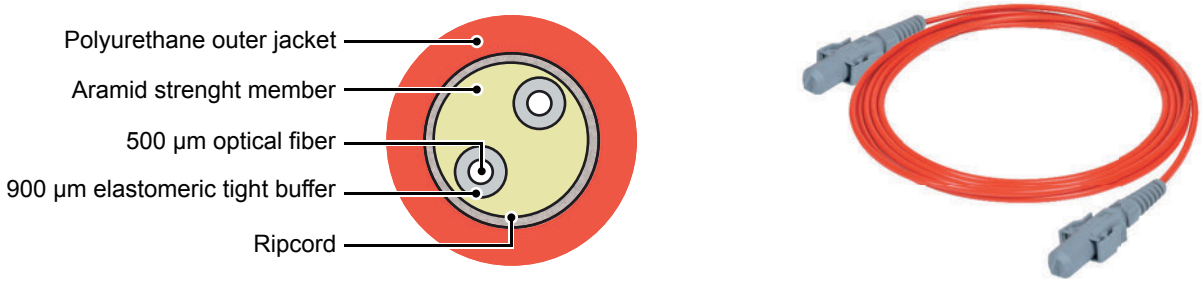


Figure B.40: Block diagram and image

Connector type	SCRJ/IP67 - SCRJ/IP67
Glass rating	OM2; Multi Mode
Core/Cladding diameter	50/125 µm
Jacket size	6 mm (0.24")
Jacket rating	Polyurethane, halogen free, non-corrosive
Jacket coating	High chemical resistance against acids/alkalis
Attenuation	≤ 2.7 dB/km @ 850 nm
Available lengths	20 and 50 m (66 and 164 ft)
Operating temperature	-40 °C to +80 °C

B.9.4 Standard zipcord fiber optic duplex Multi Mode patch cable

KAB280: Fiber Optic Cable MM 50/125um LC-LC (Option, to be ordered separately)

Standard zipcord fiber optic duplex Multi Mode patch cable
Used with 850 nm optical 1 Gbit or 10 Gbit Ethernet (1-G062 and 1-G065), Master/ Slave synchronization and GN1202B cards. Typically used for fixed cable routing or LAB environments.

Figure B.41: Block diagram and image

Connector type	LC - LC
Cable rating	OM3; Multi Mode, 850 nm
Core/Cladding diameter	50/125 µm
Jacket size/diameter	Typically 2 mm (0.08") single core
Jacket rating	Low-smoke zero-halogen
Attenuation	≤ 2.7 dB/km @ 850 nm
Available lengths	3, 10, 20 and 50 m (10, 33, 66 and 164 ft). For other lengths contact custom systems(1).
Bend radius	30 mm (1.2")
Weight	Typically 14 kg/km (9 lb/1000 ft)
Operating temperature	-40 °C to +80 °C (-40 °F to 176 °F)

(1) Contact custom systems at: customsystems@hbm.com

B.9.5 Standard zipcord fiber optic duplex Single Mode patch cable

KAB288: Fiber Optic Cable SM 9/125um LC-LC (Option, to be ordered separately)	
Standard zipcord fiber optic duplex Single Mode patch cable Used with 1310 nm optical 1 Gbit or 10 Gbit Ethernet (1-G063 and 1-G066). Typically used for fixed cable routing or LAB environments.	
	
Figure B.42: Block diagram and image	
Connector type	LC - LC
Cable rating	OS2; Single Mode, 1310 nm
Core/Cladding diameter	9/125 µm
Jacket size/diameter	Typically 2 mm (0.08") single core
Jacket rating	Low-smoke zero-halogen
Attenuation	≤ 0.5 dB/km @ 1310 nm
Available lengths	2, 10, 20, 50 and 100 m (6.6, 33, 66, 164 and 330 ft). For other lengths contact custom systems(1).
Bend radius	30 mm (1.2")
Weight	Typically 14 kg/km (9 lb/1000 ft)
Operating temperature	-40 °C to +70 °C (-40 °F to 158 °F)

(1) Contact custom systems at: customsystems@hbm.com

B.9.6 Heavy duty fiber optic duplex Single Mode cable

KAB289: Robust Fiber Optic Cable SM 9/125um LC-LC (Option, to be ordered separately)

Heavy duty fiber optic duplex Single Mode cable
Used with 1310 nm optical 1 Gbit or 10 Gbit Ethernet (1-G063 and 1-G066). Typically used for test cell environments.

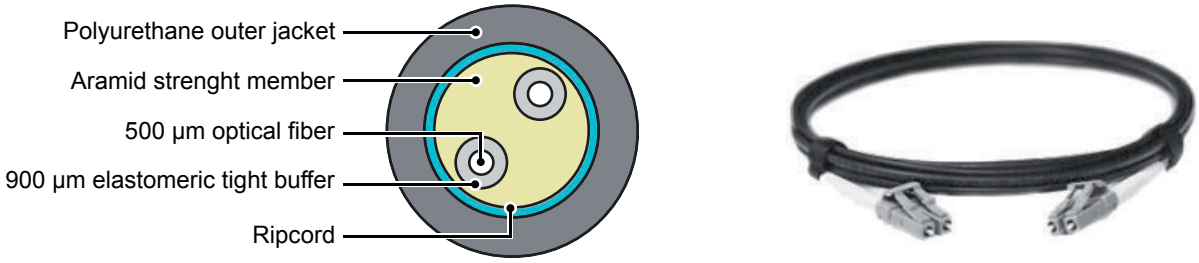


Figure B.43: Block diagram and image

Connector type	LC - LC
Cable rating	OS2; Single Mode, 1310 nm
Core/Cladding diameter	9/125 µm
Jacket size/diameter	5.8 mm (0.23")
Jacket rating	Polyurethane, halogen free
Attenuation	≤ 0.5 dB/km @ 1310 nm
Available lengths	10, 20, 50, 100, 150 and 300 m (33, 66, 164, 328, 492 and 984 ft). For other lengths contact custom systems(1).
Bend radius	58 mm (2.3")
Crush resistance	2000 N/cm
Weight	Typcially 32 kg/km (21.5 lb/1000 ft)
Operating temperature	-46 °C to +85 °C (-50.8 °F to 185 °F)

(1) Contact custom systems at: customsystems@hbm.com

B.9.7 1 Gbit Optical Network SFP module 850 nm

G062: 1 Gbit Optical Network SFP module 850 nm (Option, to be ordered separately)
GEN DAQ 1 Gbit Ethernet SFP, 850 nm Multi Mode, up to 500 m optical cable length supported, LC connector support. 1 Gbit SFP modules are not compatible with the 10 Gbit SFP+ modules.

Figure B.44: 1 Gbit Optical Network SFP module 850 nm

B.9.8 1 Gbit Optical Network SFP module 1310 nm

G063: 1 Gbit Optical Network SFP module 1310 nm (Option, to be ordered separately)
GEN DAQ 1 Gbit Ethernet SFP, 1310 nm Single Mode, up to 10 km optical cable length supported, LC connector support. 1 Gbit SFP modules are not compatible with the 10 Gbit SFP+ modules.

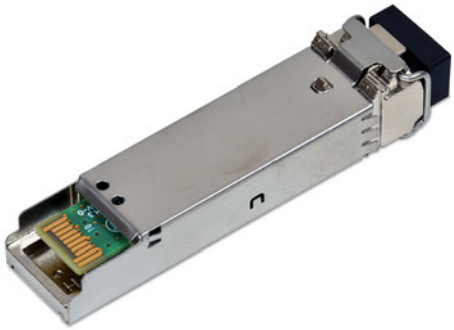


Figure B.45: 1 Gbit Optical Network SFP module 1310 nm

B.9.9 10 Gbit Optical Network SFP module 850 nm

1-G065: 10 Gbit Optical Network SFP module 850 nm (Option, to be ordered separately)
GEN DAQ 10 Gbit Ethernet SFP+, 850 nm Multi Mode, up to 82 m optical cable length supported, LC connector support. 10 Gbit SFP+ modules are not compatible with the 1 Gbit SFP modules.

Figure B.46: 1 Gbit Optical Network SFP module 850 nm

B.9.10 10 Gbit Optical Network SFP module 1310 nm

1-G066: 10 Gbit Optical Network SFP module 1310 nm (Option, to be ordered separately)
GEN DAQ 10 Gbit Ethernet SFP+, 1310 nm Single Mode, up to 10 km optical cable length supported, LC connector support. 10 Gbit SFP+ modules are not compatible with the 1 Gbit SFP modules.

Figure B.47: 1 Gbit Optical Network SFP module 1310 nm

B.10 Mainframe adapters

B.10.1 G070A Torque/RPM adapter

- **Connect up to two torque transducers**
- **Connect to T12/T40B using standard cables**
- **RS422 differential input signals for highest immunity**
- **Connect to GEN DAQ mainframe using standard cable**
- **Dual signal output for dual use with test cell control system**
- **Low latency outputs**
- **Power T12/T40B from adapter (Power supply not included)**
- **Connect to binary, frequency or a,b,z based sensors using RS422 signals**

The Torque/RPM adapter enables the connection of HBM's T12, T40B or similar torque transducers to GEN DAQ mainframes. The use of differential signals improves the immunity to external disturbance especially when using long cables in electrically noisy environments. For easy connectivity of transducers the adapter can optionally route power over the transducer cables, this avoids the need of separate power cables. This power input is separately connected to the adapter per transducer.
Whenever a test cell control system requires parallel access to the torque and/or speed signals, the adapter reconditions the incoming signals and outputs all input signals as RS422 differential signals.
All outputs come with low latency to support real-time safety monitoring applications.
Each of the torque and speed inputs are directly connected to the GEN DAQ high resolution Timer/Counter channels. The speed input supports direction and reference pulse to enable rotational angle measurement. The torque input supports shunt to optimize accuracy.
In addition to HBM torque sensors, the adapter allows use with any binary, frequency or a, b, z based sensor. E.g. for more accurate/higher resolution rotational speed and angle measurement, standard industrial incremental encoders with RS422 signals can be used simultaneously with the HBM torque transducer.
All event inputs provided by the GEN DAQ mainframe that are not used to connect to the torque and speed signals are rewired to a pin compatible event I/O connector.

Torque/RPM Adapter Block Diagram

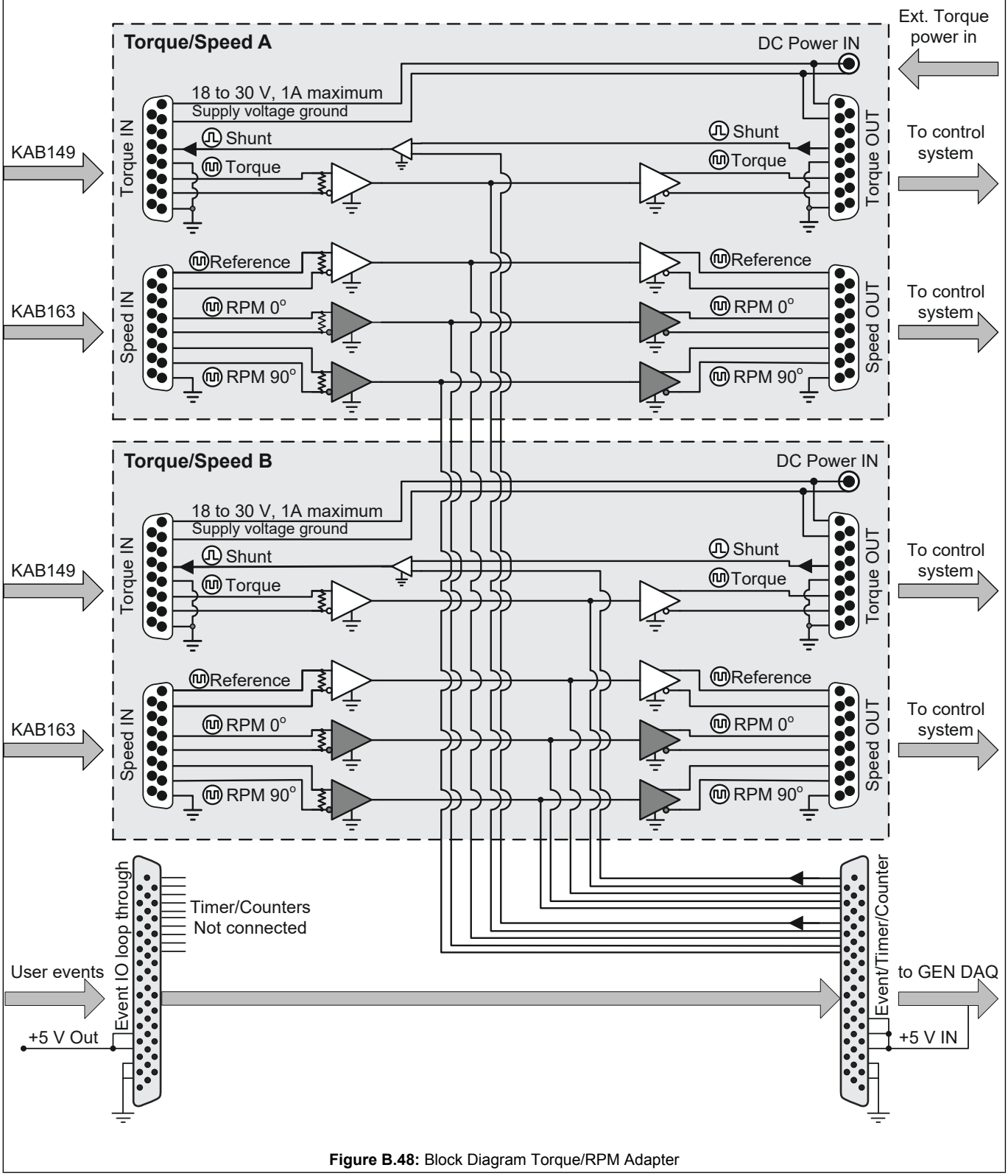


Figure B.48: Block Diagram Torque/RPM Adapter

Torque/RPM Adapter	
Connects a T12, T40 or similar torque transducer to GEN3i, GEN3t, GEN7i and GEN7tA Digital Event/Timer/Counter connector	
Torque sensor connection	
Number of torque sensors	2
Torque interface support	Torque and Shunt (A-Txx CON1 Torque IN & B-Txx CON1 Torque IN)
Speed interface support	RPM, Direction and Reference (A-Txx CON2 Speed IN & B-Txx CON2 Speed IN)
Inputs	
Signal type	Differential RS422
Maximum nondestructive input voltage	- 4 V to + 8 V input to ground - 12 V to + 12 V -input to +input (differential input)
Signal termination	100 Ω
Propagation delay (Input to GEN DAQ)	16 ns (typical)
Input buffers	AM26LV32C
Torque sensor loop through	
Number of torque sensors	2
Torque interface output	Torque (A-Txx CON1 Torque OUT & B-Txx CON1 Torque OUT)
Speed interface output	RPM, Direction and Reference (A-Txx CON2 Speed OUT & B-Txx CON2 Speed OUT)
Outputs	
Output type	Differential RS422, electronic retransmitted from input signals
Output voltage	- 0.3 V to + 6 V
Output current	± 25 mA
Propagation delay (Input to Output)	23 ns (typical)
Maximum signal frequency (Input to Output)	30 MHz
Output drivers	AM26C31C
Connectors	
Digital Event/Timer/Counter	HD22 sub-D 44 pin male (connecting cable included)
Loop through event input	44 pin, female D-type connector, AMP HD-22 series (Tyco/TE Connectivity: 5748482-5)
Loop through cable connector type	44 pin, male D-type connector, HDP-22 series (Tyco/TE Connectivity: 1658680-1), to be ordered separately
Torque, Speed/RPM interface IN	15 pin, female sub-D type (matches 1-KAB149-6 and 1-KAB163-6)
Torque, Speed/RPM interface OUT	15 pin, male sub-D type
Torque power input	Switchcraft L712A Matching cable connector Switchcraft 761KS17 (LD-024-1000911). Two cable connectors included
Cables	
Torque/RPM adapter to GEN DAQ mainframe	0.7 m (2.30 ft), included with Torque/RPM adapter
Torque sensor to Txx Torque IN	1-KAB149-6 (other lengths available), to be ordered separately
Torque sensor to Txx Speed IN	1-KAB163-6 (other lengths available), to be ordered separately
Power	
Adapter	Power by GEN DAQ mainframe
Torque sensors	Requires separate power supply Check the manual of the used torque sensor to select proper power supply

Torque/RPM Adapter Connector Layout

Figure B.49: G070A front view

Front side connectors	
Sensor A input	Torque and Speed
Sensor A output	Torque and Speed
Sensor A power input	Optional sensor A power, supplied on Torque input connector
Event input	All remaining events not used for sensor A and B torque and RPM measurements

Figure B.50: G070A back view

Back side connectors	
Sensor B input	Torque and Speed
Sensor B output	Torque and Speed
Sensor B power input	Optional sensor B power, supplied on Torque input connector
Digital Event/Timer/Counter output	Connections to GEN DAQ mainframe, includes power from GEN DAQ to G070A

Torque Sensor Connector Pin Assignment

Pin 5 : Supply voltage ground (not connected to signal ground)
Pin 6 : Supply voltage 18 V to 30 V
Pin 8: Ground
Pin 12: + Torque Signal
Pin 13: - Torque Signal
Pin 14: Shunt Signal trigger 5 V to 30 V

Shielding connected to connector housing
All other pins not connected

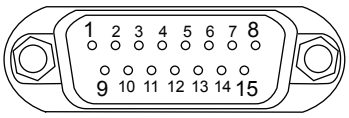


Figure B.51: Torque IN and OUT connector pinning

Pin 2: + Reference Signal
Pin 3: - Reference Signal
Pin 8: Signal ground
Pin 12: + Rotational Speed 0° Signal
Pin 13: - Rotational Speed 0° Signal
Pin 14: - Rotational Speed 90° Signal
Pin 15: + Rotational Speed 90° Signal

Shielding connected to connector housing
All other pins not connected

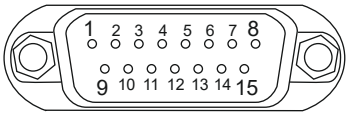


Figure B.52: Speed IN and OUT connector pinning

Torque Sensor Power Connector Assignment

Power connector	Switchcraft L712A
Cable connector	Switchcraft 761KS17, included in shipment
Connector pinning	
Outer shield	Supply voltage ground
Inner pin	Supply voltage (18 V to 30 V)

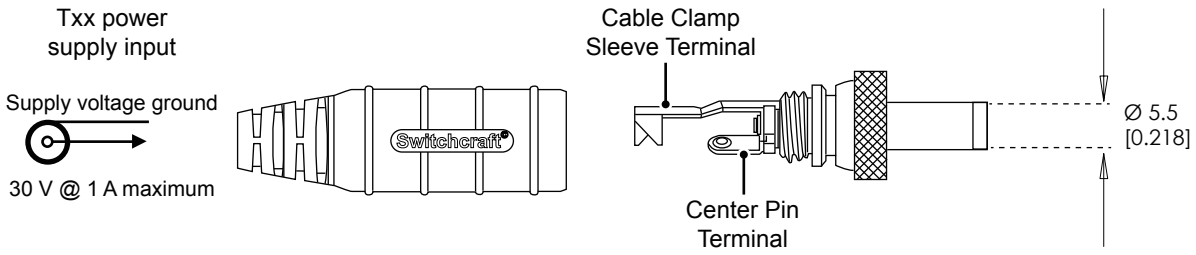
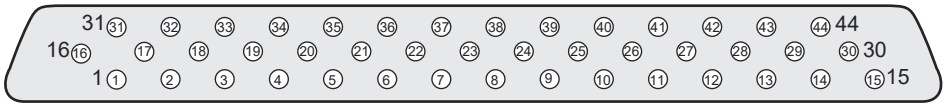


Figure B.53: Cable connector details

Loop through Connector Pin Assignment



PIN 1 - Not connected
PIN 2 - Not connected
PIN 3 - Not connected
PIN 4 - Event Input 4A
PIN 5 - Event Input 5A
PIN 6 - Event Input 6A
PIN 7 - Event Input 7A
PIN 8 - Event Input 8A
PIN 9 - Event Input 9A
PIN 10 - Not connected
PIN 11 - Not connected
PIN 12 - Not connected
PIN 13 - Not connected
PIN 14 - Not connected
PIN 15 - Not connected
PIN 16 - Event Input 4B
PIN 17 - Event Input 5B
PIN 18 - Event Input 6B
PIN 19 - Event Input 7B
PIN 20 - Event Input 8B
PIN 21 - Event Input 9B
PIN 22 - Not connected
PIN 23 - Not connected
PIN 24 - Not connected
PIN 25 - Event Input 13B
PIN 26 - Event Input 14B
PIN 27 - Ground
PIN 28 - Ground
PIN 29 - Ground
PIN 30 - Ground
PIN 31 - Event Input 15B
PIN 32 - Event Input 16B
PIN 33 - Event Input 13A
PIN 34 - Event Input 14A
PIN 35 - Event Input 15A
PIN 36 - Event Input 16A
PIN 37 - Event Output 2B
PIN 38 - Event Output 1B
PIN 39 - Event Output 2A
PIN 40 - Event Output 1A
PIN 41 - Ground
PIN 42 - Ground
PIN 43 - +5 V Power output
PIN 44 - +5 V Power output

Figure B.54: Pin diagram for loop through connector

Application Examples

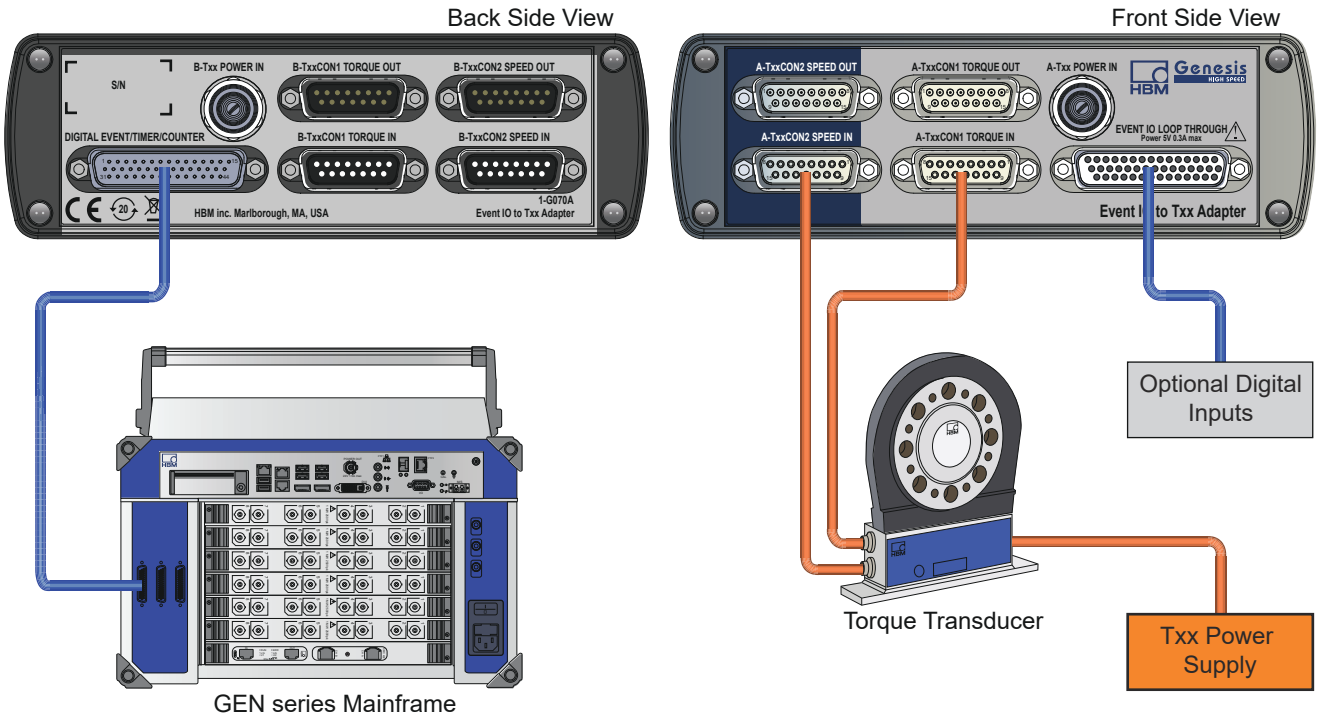


Figure B.55: External powered torque transducer connected to GEN DAQ

Note *GEN series connection supported for GEN3i, GEN3t, GEN7i (shown), GEN7tA or GEN17tA.*

Example 1: Connection of a single Torque transducer with torque and speed to GEN DAQ input A using the G070A adapter; Torque transducer powered directly; no control system output

Application Examples

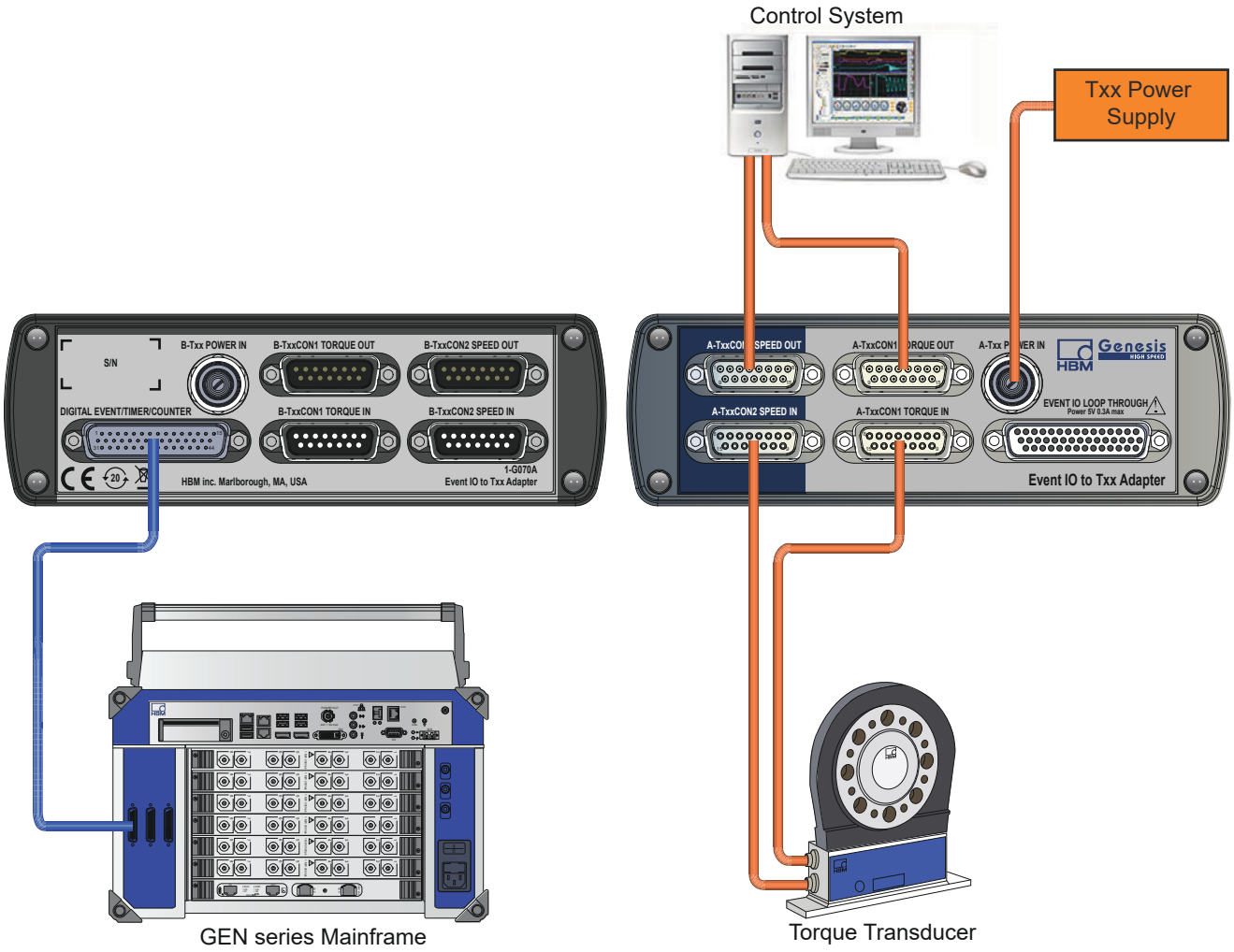


Figure B.56: G070A powered torque transducer connected to GEN DAQ and control system

Note *GEN series connection supported for GEN3i, GEN3t, GEN7i (shown), GEN7tA or GEN17tA.*

Example 2: Connection of a single Torque transducer with torque and speed to GEN DAQ (input A); Torque transducer powered using G070A; torque and speed output to control system

Application Examples

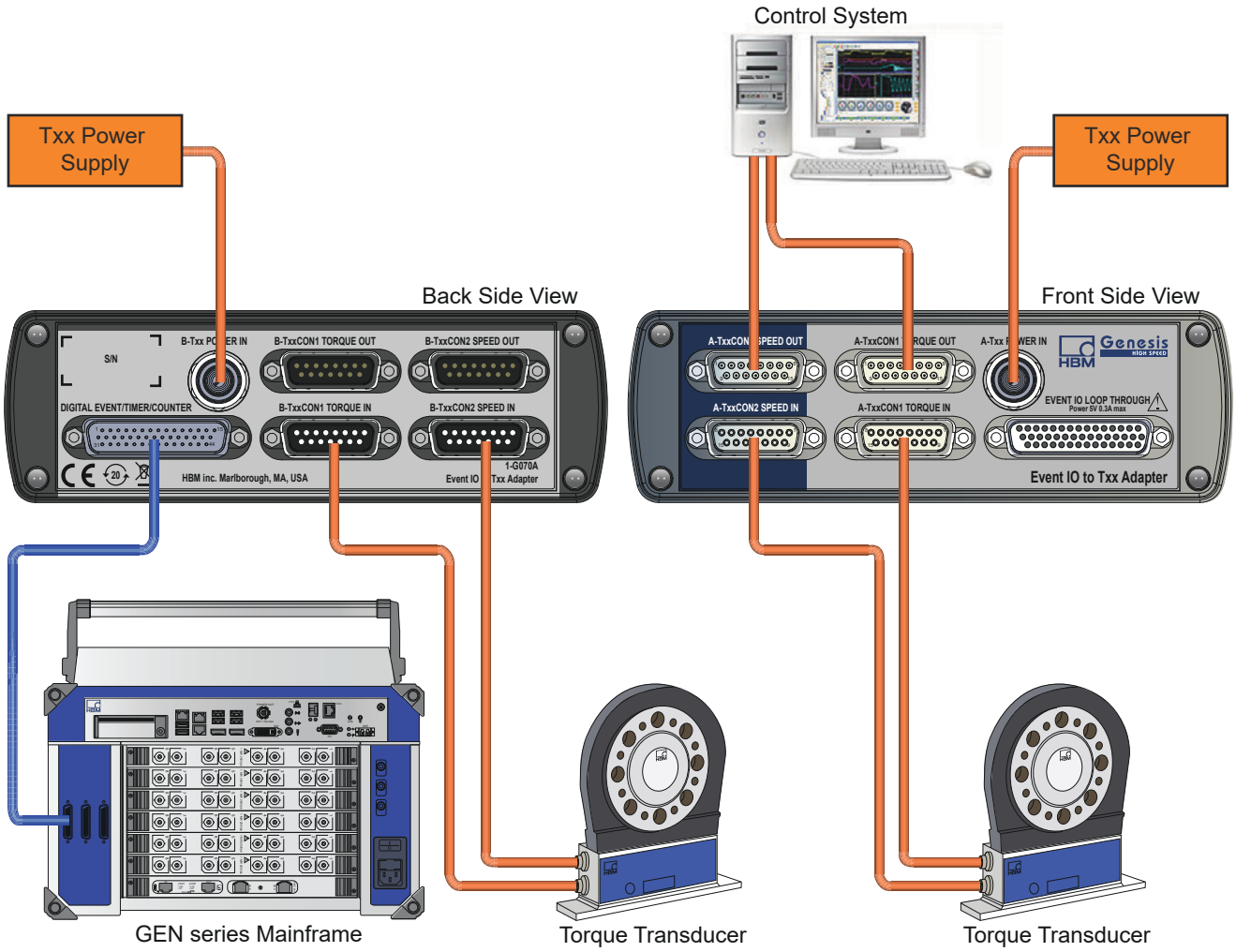


Figure B.57: Two torque transducer connected to GEN DAQ and control system

Note *GEN series connection supported for GEN3i, GEN3t, GEN7i (shown), GEN7tA or GEN17tA.*

Example 3: Connection of two torque transducers connecting torque and speed to GEN DAQ (input A and B); both torque transducers powered using G070A; torque and speed of transducer A output to control system

Application Examples

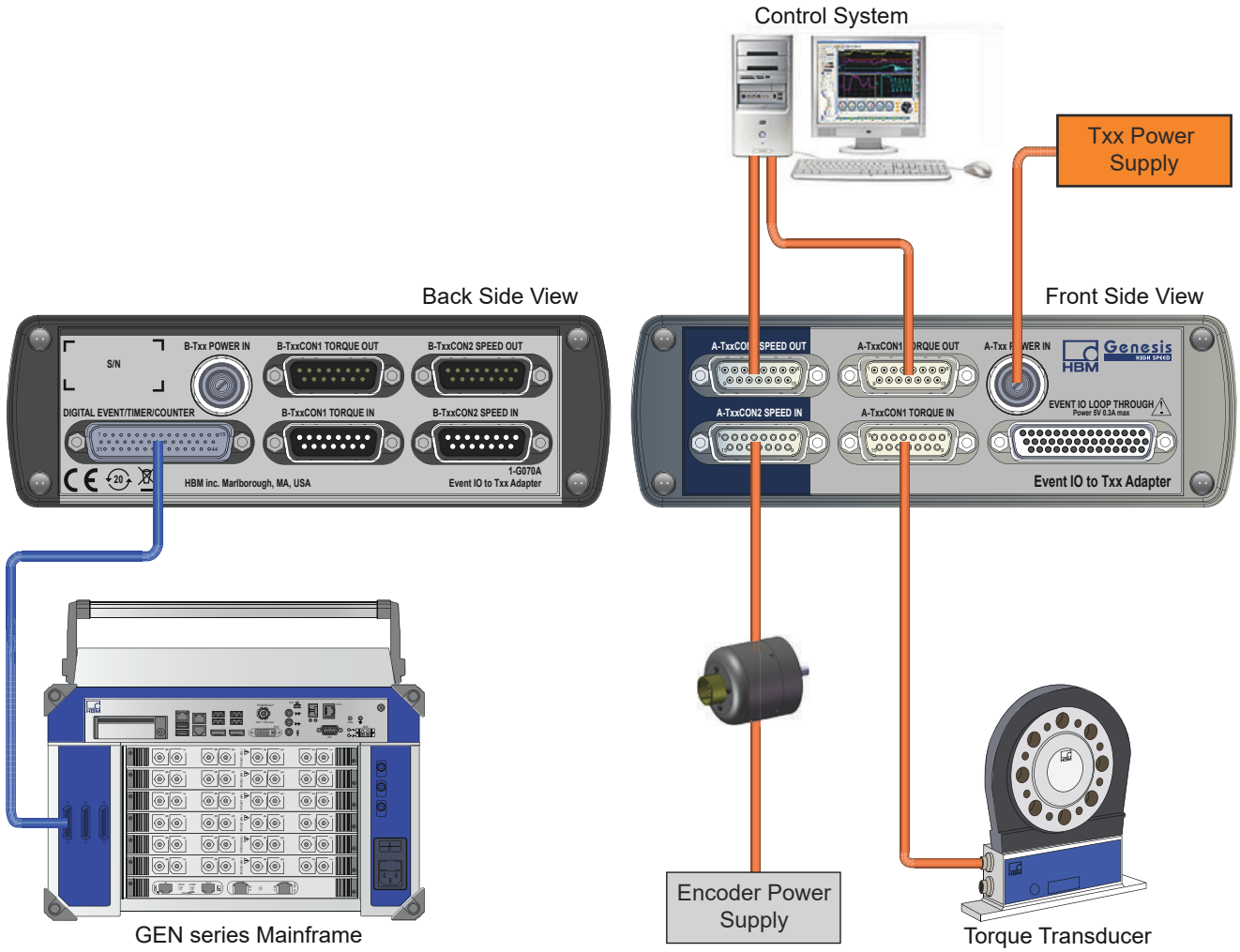


Figure B.58: Torque transducer and speed encoder connected to GEN DAQ and control system

Note *GEN series connection supported for GEN3i, GEN3t, GEN7i (shown), GEN7tA or GEN17tA.*

Example 4: Connection of a single torque transducer with torque only to GEN DAQ (input A); torque transducer powered using G070A; separate incremental encoder used for speed, encoder directly powered; torque and speed output to control system

Physical, Weight and Dimensions	
Weight	
Mainframe	0.75 kg (1.65 lb)
Dimensions	
Height	55 mm (2.2")
Width	172 mm (6.8")
Depth	124 mm (4.9")
Grounding	Using shield of GEN DAQ cable connection
Casing	Aluminum
Accessories	Cable to connect adapter to GEN DAQ mainframe event connector, included with Torque/RPM adapter

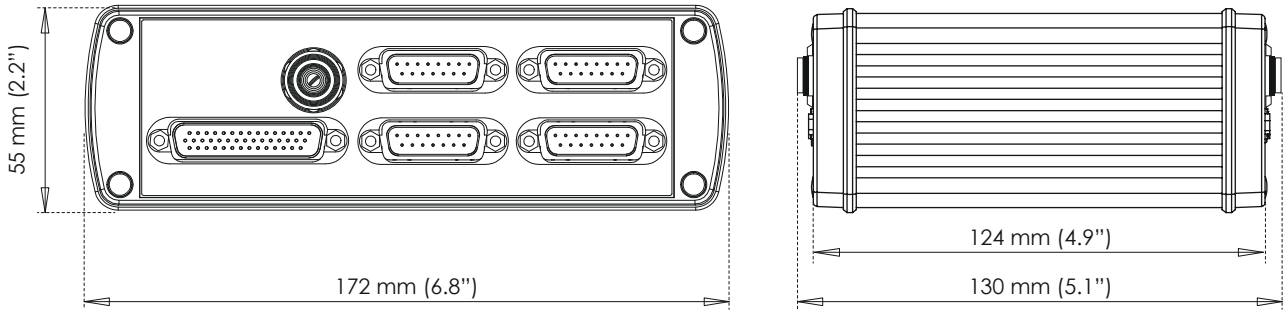


Figure B.59: G070A Dimensions

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC-60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC-60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC-60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity >95/90% RH 6 Cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives	
Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

B.10.2 G072 Isolated Digital Event Adapter

- **32 digital event input channels**
- **4 digital event output channels**
- **230 V RMS event channel isolation**
- **Full channel to channel isolation**
- **Removable screw terminals for quick cable connections**
- **Direct interface to GEN DAQ mainframe event connector**
- **GEN DAQ mainframe to adapter cable included**
- **No external power supply required**
- **Optional cable set to connect to GN6470 or GN4070**

The isolated Digital Event Adapter provides an isolation barrier for up to 32 digital event input channels. Furthermore 4 event output channels are available if the adapter is connected to the Digital Event/Timer/Counter connector of GEN DAQ mainframes. The adapter can optionally be connected directly to the GEN DAQ Binary Marker Timer/Counter card.
Using the isolated Digital Event Adapter allows the user to avoid ground loops and improves immunity to electrical noisy environments.
The channel to channel and channel to ground isolation voltage is 230 V RMS. The standard input voltage of 4.5 – 11.5 V for logic “1” can be increased by using external resistors. Therefore higher voltage levels can be used for logic “0” and “1”.
The wiring of the signal cable is easy due to the pluggable screwed joint connectors of the adapter.
For easy connectivity the adapter is powered by the GEN DAQ mainframe or the GEN DAQ Binary Marker Timer/ Counter card to avoid the need for a separate power supply.

Isolated Digital Event Adapter Block Diagram

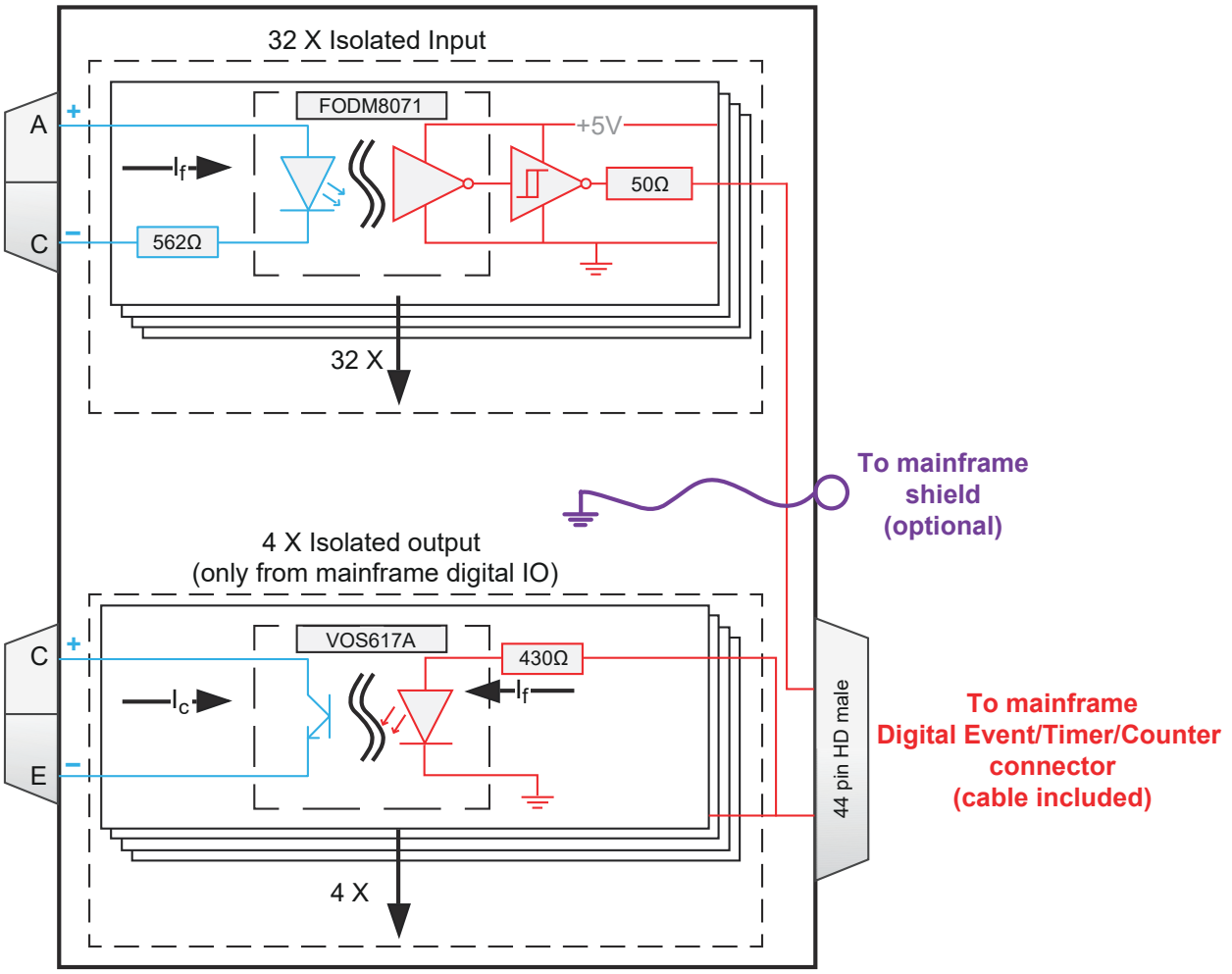


Figure B.60: Block diagram adapter

Event Inputs	
Inputs	32 event channels (Anode (A), Cathode (C) optocoupler with 562 Ω series resistor)
Isolation voltage	230 V AC RMS or DC (channel to channel and channel to chassis/earth)
Isolation device	Fairchild FOD8071 optocoupler (or comparable)
Switching frequency	10 MHz input block signal tested. The highest frequency supported for the system is limited by the isolator box or acquisition system, whichever is the lowest
Maximum propagation delay	55 ns
Common mode transient voltage	Typically 20 kV/µs
Input switching voltages (see Figure B.61 and Figure B.62)	
Logic 0	< 1.0 V + 0.0015 A (562 Ω + R_{ext})
Logic 1	> 1.3 V + 0.0050 A (562 Ω + R_{ext})
Maximum nondestructive voltage	1.8 V + 0.0150 A (562 Ω + R_{ext})
Minimum nondestructive reverse voltage	-5.0 V

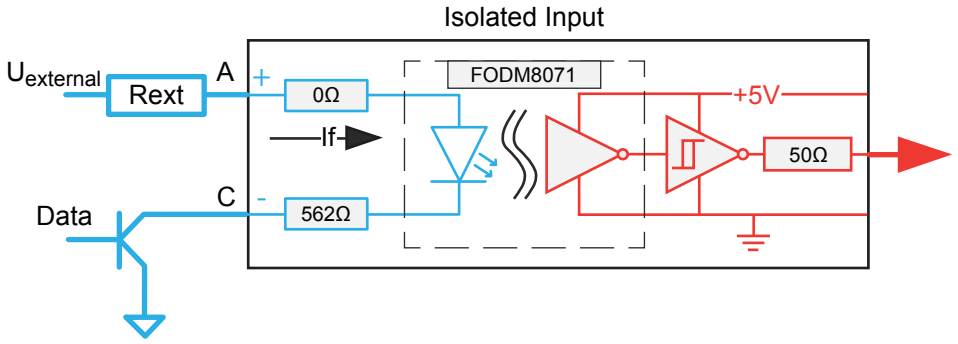


Figure B.61: Add an external resistor to change input voltage levels

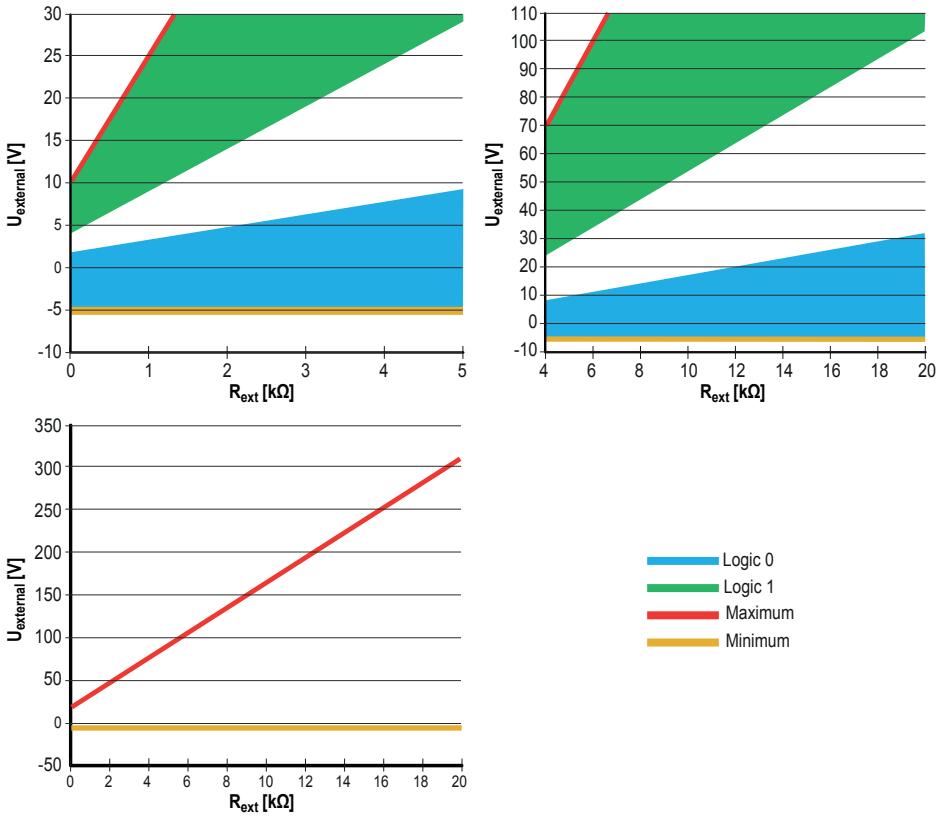


Figure B.62: Detailed input voltage levels (top graphs)/nondestructive input voltages (below)

Event Outputs	
Output channels	4 digital isolated output channels (open Collector, Emitter) Only supported by Digital Event/Timer/Counter connector
Isolation device	Vishay VOS617A optocoupler (or comparable)
Output frequency	170 kHz output signal tested. Maximum useable frequency for the system is limited by the Isolated Digital Event Adapter or acquisition system, whichever is the slowest.
Nondestructive control voltages (see Figure B.63 and Figure B.64)	
Maximum voltage	0.007 * R_{ext} and < 80 V
Minimum voltage	-7.0 V

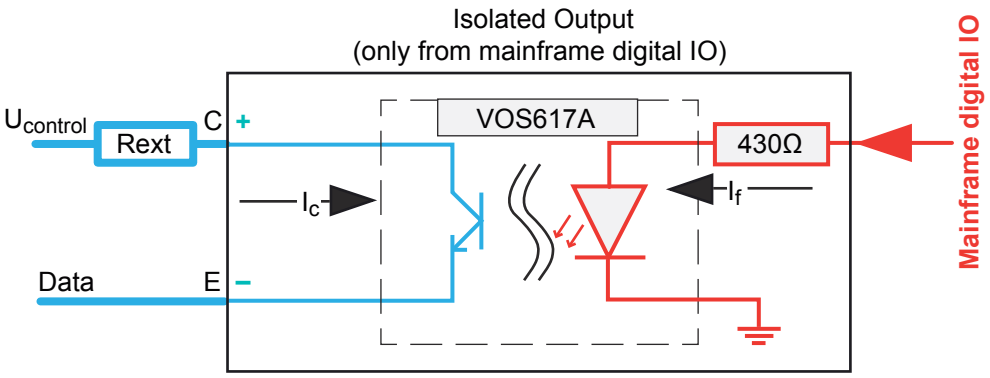


Figure B.63: Add an external resistor to change output voltage levels

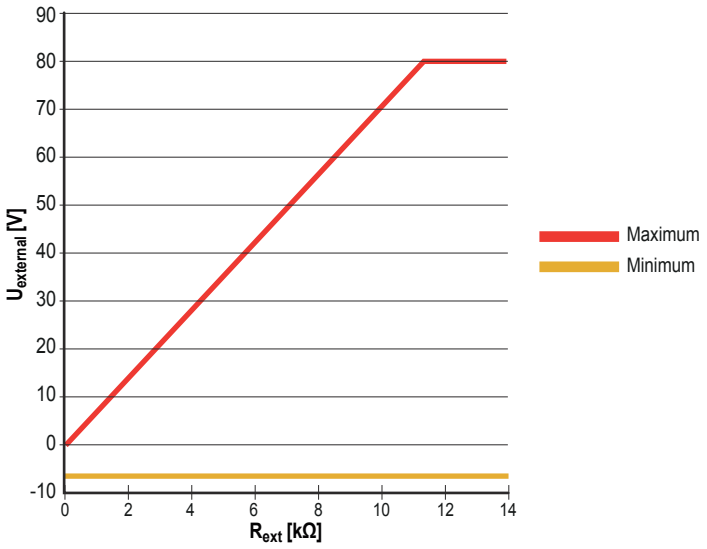


Figure B.64: Nondestructive output voltages

Output Connectors (Only one output connector option can be used at the same time)	
Digital Event/Timer/Counter	HD22 sub-D 44 pin male (connecting cable included)
Digital marker group A and B	15 pin, female sub-D type (connecting cable 1-KAB2116-1.5, to be ordered separately)
Output Cables	
GEN DAQ mainframe to adapter	0.7 m (2.30 ft), included with adapter
GEN DAQ marker card to adapter	1-KAB2116-1.5, 1.5 m (4.92 ft) needs to be ordered separately
Power	
GEN DAQ mainframe to adapter	Powered by GEN DAQ mainframe or marker card

Adapter Front Connector Pinning

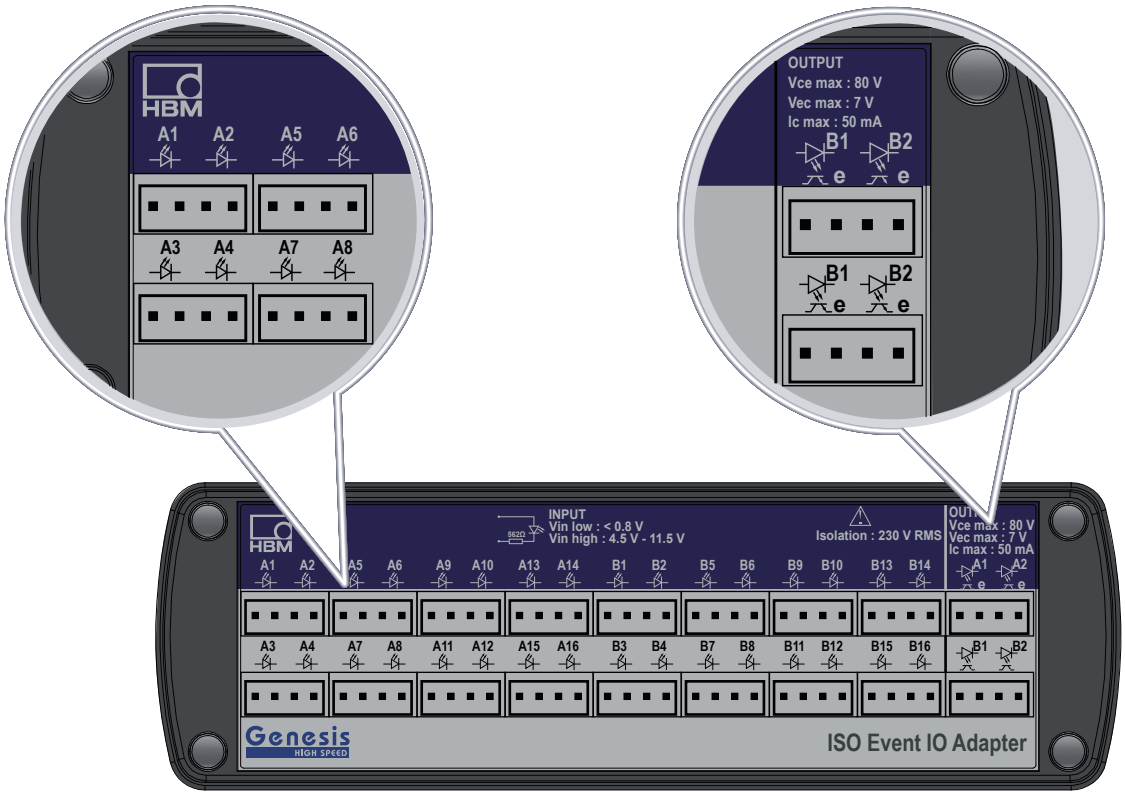


Figure B.65: G072 front connectors

Isolated Digital Event Input Cable Connector Details

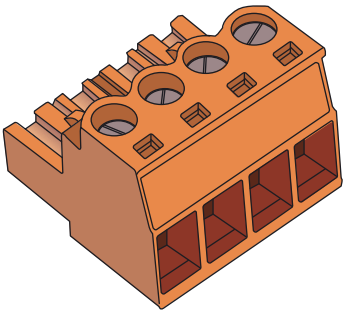


Figure B.66: Input connector

Cable connector type	Weidmuller BL 3.50/04/180 SN or BX (Weidmuller order number 1597380000) 1x4 pole cable screw clamp (included with adapter, 18 pieces altogether)

Adapter Rear Connector Pinning

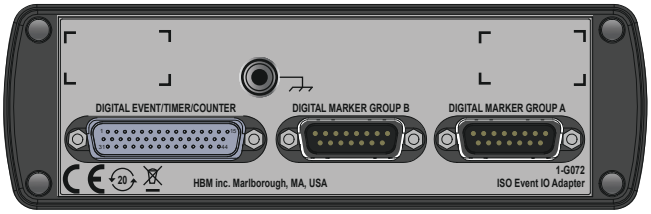
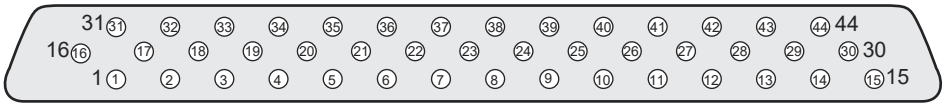
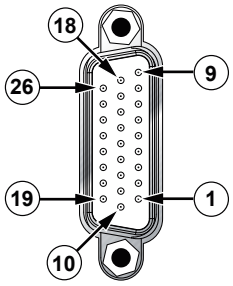


Figure B.67: G072 rear connectors



PIN 1 - Event Input 1A & Reset Timer/Counter 2A
PIN 2 - Event Input 2A & Direction Timer/Counter 2A
PIN 3 - Event Input 3A & Clock Timer/Counter 2A
PIN 4 - Event Input 4A
PIN 5 - Event Input 5A
PIN 6 - Event Input 6A
PIN 7 - Event Input 7A
PIN 8 - Event Input 8A
PIN 9 - Event Input 9A
PIN 10 - Event Input 10A & Reset Timer/Counter 1A
PIN 11 - Event Input 11A & Direction Timer/Counter 1A
PIN 12 - Event Input 12A & Clock Timer/Counter 1A
PIN 13 - Event Input 1B & Reset Timer/Counter 2B
PIN 14 - Event Input 2B & Direction Timer/Counter 2B
PIN 15 - Event Input 3B & Clock Timer/Counter 2B
PIN 16 - Event Input 4B
PIN 17 - Event Input 5B
PIN 18 - Event Input 6B
PIN 19 - Event Input 7B
PIN 20 - Event Input 8B
PIN 21 - Event Input 9B
PIN 22 - Event Input 10B & Reset Timer/Counter 1B
PIN 23 - Event Input 11B & Direction Timer/Counter 1B
PIN 24 - Event Input 12B & Clock Timer/Counter 1B
PIN 25 - Event Input 13B
PIN 26 - Event Input 14B
PIN 27 - Ground
PIN 28 - Ground
PIN 29 - Ground
PIN 30 - Ground
PIN 31 - Event Input 15B
PIN 32 - Event Input 16B
PIN 33 - Event Input 13A
PIN 34 - Event Input 14A
PIN 35 - Event Input 15A
PIN 36 - Event Input 16A
PIN 37 - Event Output 2B
PIN 38 - Event Output 1B
PIN 39 - Event Output 2A
PIN 40 - Event Output 1A
PIN 41 - Ground
PIN 42 - Ground
PIN 43 - +5 V Power
PIN 44 - +5 V Power

Figure B.68: Pin assignment for Digital Event/Timer/Counter connector



Pin number	GROUP A	GROUP B	Pin number	GROUP A	GROUP B
PIN 1	A 16	B 16	PIN 14	A 3	B 19
PIN 2	A 15	B 15	PIN 15	A 2	B 18
PIN 3	A 14	B 14	PIN 16	A 1	B 1
PIN 4	A 13	B 13	PIN 17	Ground	Ground
PIN 5	A 12	B 12	PIN 18	Ground	Ground
PIN 6	A 11	B 11	PIN 19	Ground	Ground
PIN 7	A 10	B 10	PIN 20	Ground	Ground
PIN 8	A 9	B 9	PIN 21	Ground	Ground
PIN 9	A 8	B 8	PIN 22	Ground	Ground
PIN 10	A 7	B 7	PIN 23	Ground	Ground
PIN 11	A 6	B 6	PIN 24	Ground	Ground
PIN 12	A 5	B 5	PIN 25	+ 5 V	+ 5 V
PIN 13	A 4	B 4	PIN 26	+ 5 V	+ 5 V

Figure B.69: Digital marker group A/B pinning

Isolated Input Application Examples

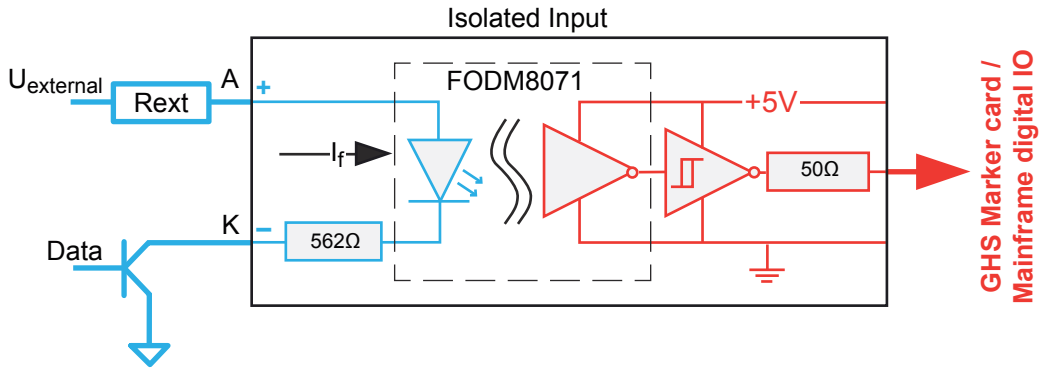


Figure B.70: Isolated input switched to negative input

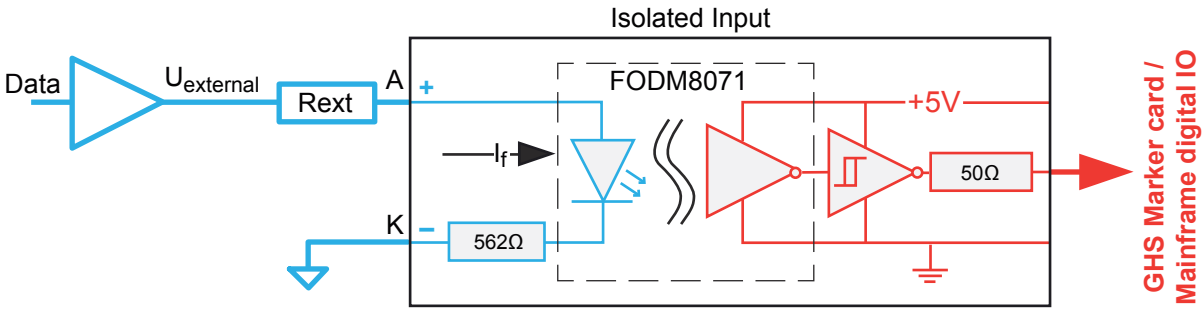


Figure B.71: Isolated input switched to positive input

Isolated Output Application Examples

(Only supported by Digital Event/Timer/Counter connectors)

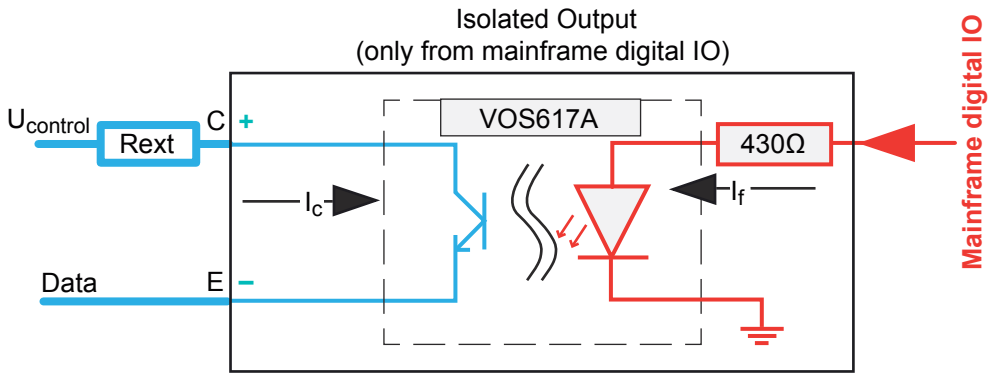


Figure B.72: Isolated output switched to negative output

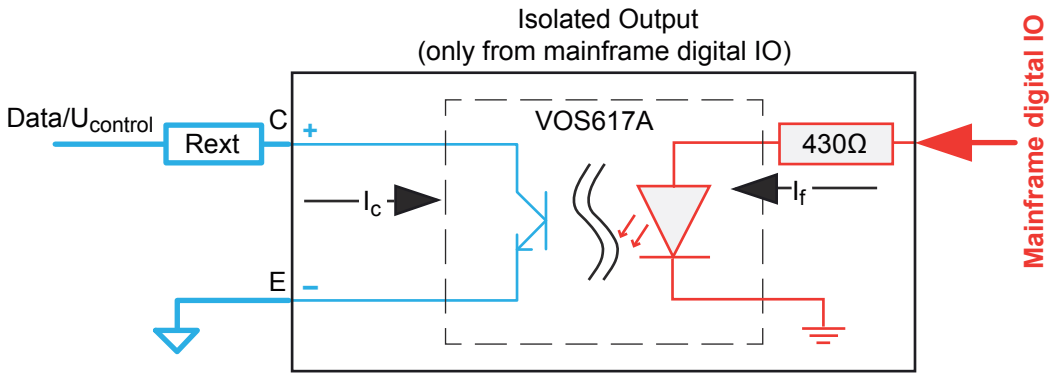


Figure B.73: Isolated output switched to positive output

Physical, Weight and Dimensions	
Weight	
Adapter	0.75 kg (1.65 lb)
Dimensions	
Height	54.6 mm (2.15”)
Width	171.6 mm (6.76")
Depth	130.14 mm (4.86")
Grounding	Uses shield for GEN DAQ cable connection
Casing	Aluminum

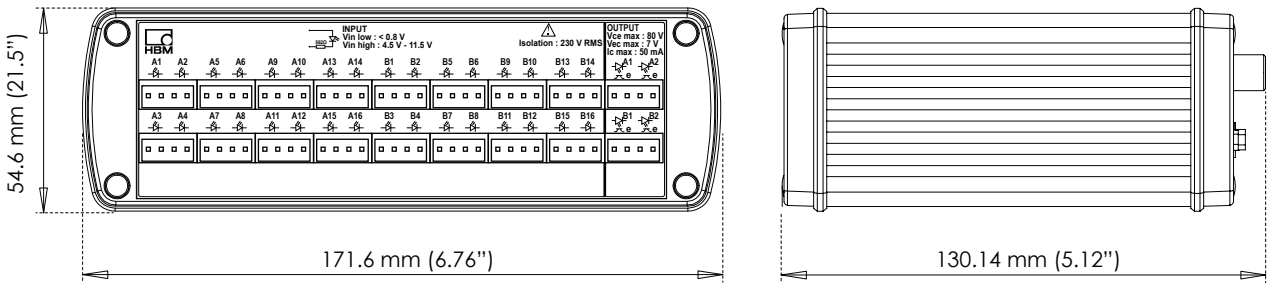


Figure B.74: G072 dimensions

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-64	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC-60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC60068-2-3 Test Ca	+40 °C (+104 °F), humidity > 93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC-60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC-60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity >95/90% RH 6 Cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives	
Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Radiated disturbance: class A
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 MHz to 2.7 GHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test All input and output connections ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 150 kHz to 80 MHz, 1000 Hz AM; 10 V RMS @ all inputs, both using clamp: performance criteria A

B.10.3 Isolated digital event adapter to marker card cable

1-KAB2116-1.5: Isolated digital event adapter to marker card cable (Option, to be ordered separately)

Set of two cables to connect the digital marker A and digital marker B output connectors of the G072 isolated digital event adapter to either a GN6470 or a GN4070 marker card. Cable length of 1.5 m (4.92 ft)

Figure B.75: Isolated digital event adapter to marker card cable

B.11 Measurement cables

B.11.1 Shielded 2 Wire 600 V RMS CAT II cable

KAB290: Shielded 2 Wire 600 V RMS CAT II Cable (Option, to be ordered separately)	
This cable is specially designed to be used with the GN610B, GN611B cards. Significantly reduces signal disturbance pickup by using two identical signal wires with earthed shield. This cable must not be used for three wire measurements. The shield is not a standard signal wire.	
Cable setup	2 wires with shield and isolation. Signal wires terminated on both sides using (red, black) shrouded banana plugs. Shield connected on one side using (yellow) shrouded banana plug. **Note:** First cable shipments have shield connected on both sides.

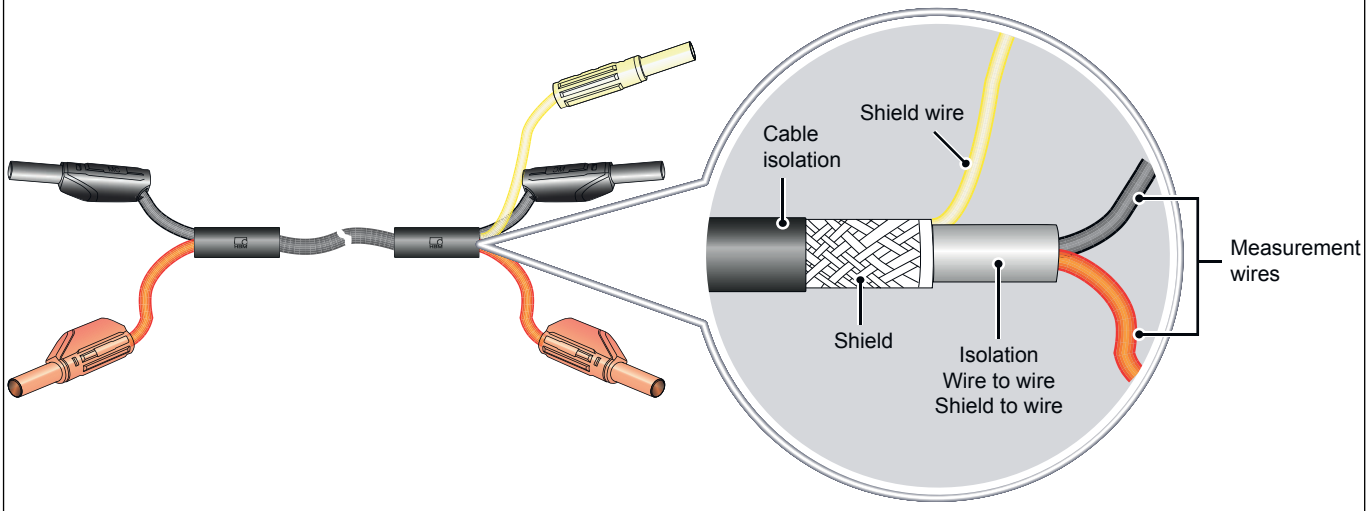


Figure B.76: Two wire shielded cable setup

Maximum current	10 A RMS
Wire thickness	2 * 0.75 mm^2 (0.00116 in^2)
Maximum wire resistance	25 mΩ / m (7.6 mΩ / ft) ± 5%
Weight	Approximately 143 g/m (1.54 oz/foot)
Outside cable diameter	Approximately 9 mm (0.354 inch)
Minimum bend radius	10 times that of the cable diameter
Isolation	
Resistance	20 MΩ / km (32.19 MΩ/ mile)
Voltage	600 V RMS CAT II; wire to wire; wire to shield; shield to outside
Capacitance	
Wire to wire	130 pF/m (39.6 pF/ft) ± 10%
Wire to shield	200 pF/m (61 pF/ft) ± 10%
Temperature range	
Operational	-15 °C (+5 °F) to +80 °C (+176 °F)
Non-operational (storage)	-40 °C (-40 °F) to +80 °C (+176 °F)
Available lengths	1.5 m (4.92 ft), 3.0 m (9.84 ft), 6.0 m (19.7 ft)

KAB290: Shielded 2 Wire 600 V RMS CAT II Cable (Option, to be ordered separately)

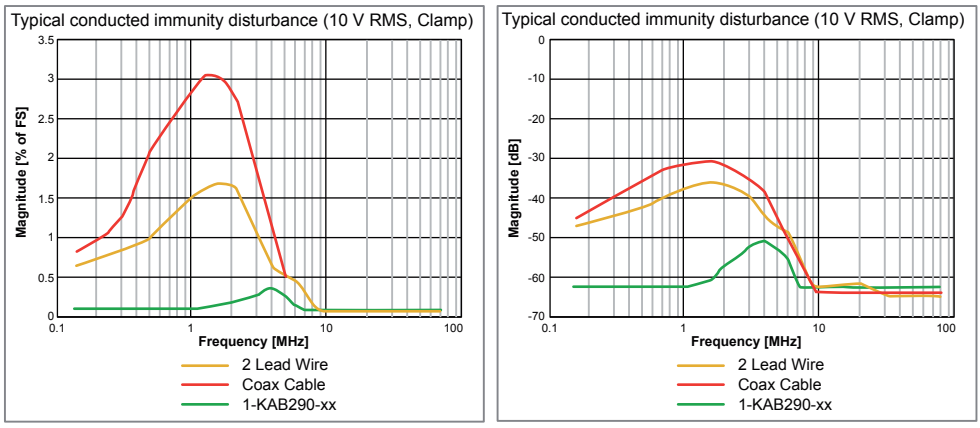


Figure B.77: Typical conducted immunity, tested using ± 10 V range

KAB2128: Shielded 3 Wire 600 V RMS CAT II Cable (Option, to be ordered separately)

This cable is specially designed to be used with the GN610B and GN611B cards. Significantly reduces signal disturbance pickup by using three identical signal wires with earthed shield.

Cable setup	3 wires with shield and isolation. Signal wires terminated on both sides using (brown, grey, black) shrouded banana plugs. Shield connected on one side using (yellow) shrouded banana plug.

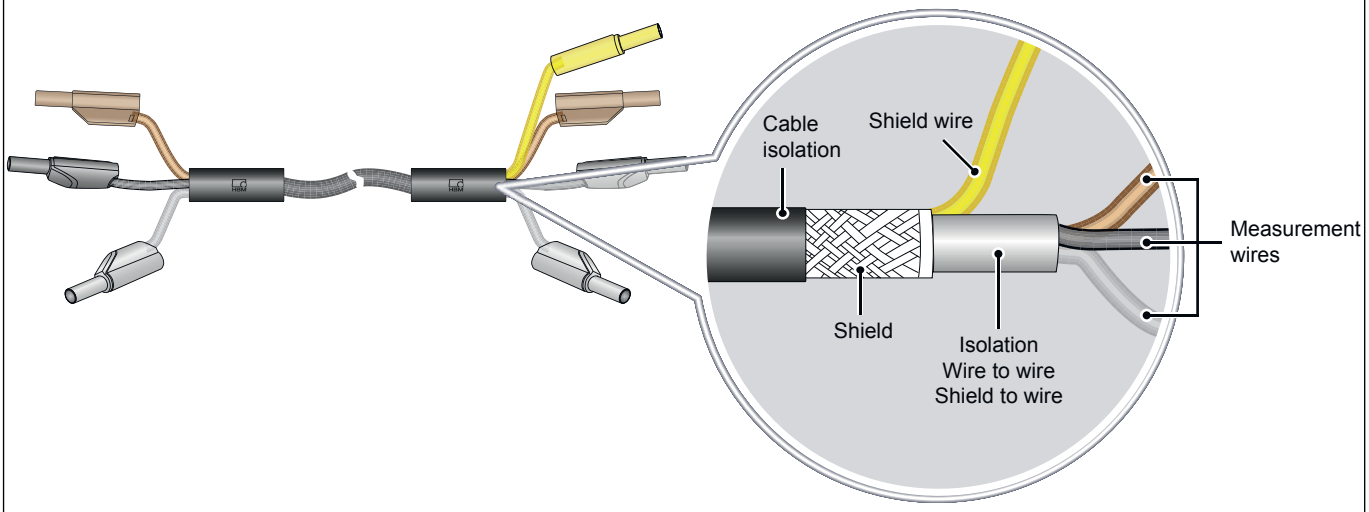


Figure B.78: Three wire shielded cable setup

Maximum current	1 A RMS
Wire thickness	AWG19 0.65 mm^2 (0.001 in^2)
Maximum wire resistance	25.4 mΩ / m (8.0 mΩ / ft) ± 5%
Weight	Approximately 155 g/m (1.67 oz/foot)
Outside cable diameter	Approximately 9.1 mm (0.36 inch)
Minimum bend radius	10 times that of the cable diameter
Isolation	
Resistance	20 MΩ / km (32.19 MΩ/ mile)
Voltage	600 V RMS CAT II; wire to wire; wire to shield; shield to outside
Capacitance	
Wire to wire	110 pF/m (39.6 pF/ft) ± 10%
Wire to shield	140 pF/m (61 pF/ft) ± 10%
Temperature range	
Operational	-15 °C (+5 °F) to +80 °C (+176 °F)
Non-operational (storage)	-40 °C (-40 °F) to +80 °C (+176 °F)
Available lengths	1.5 m (4.92 ft), 3.0 m (9.84 ft), 6.0 m (19.7 ft),12 m (39.37 ft), 20 m (65.62 ft)

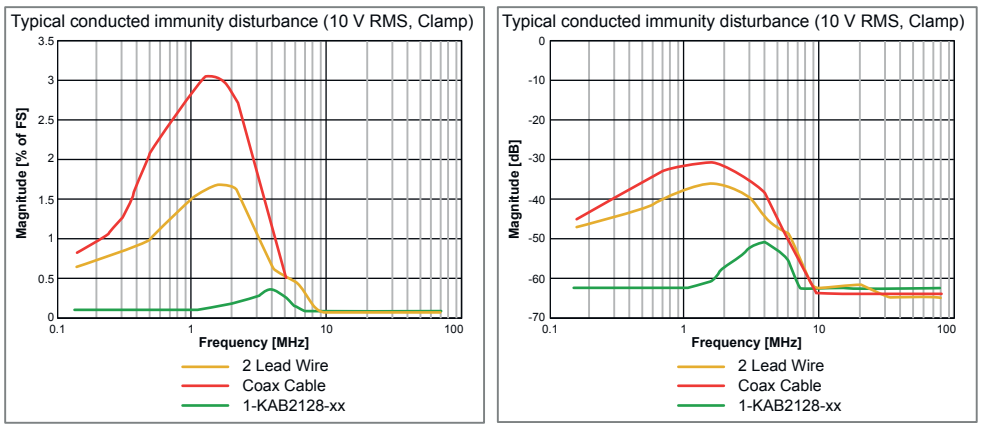


Figure B.79: Typical conducted immunity, tested using ± 10 V range

B.11.2 Test leads and clips

1-KAB282-1.5: Test leads and clip (Option, to be ordered separately)
Black/red lead set 600 V RMS CAT II, 1.5 meter (4.9 ft) with safety-shrouded banana plugs and alligator clips

Figure B.80: Test leads and clip

B.12 PTP equipment

B.12.1 IRIG to PTPv2 convertor

G001B: IRIG to PTPv2 convertor

External IRIG to PTPv2 convertor in a compact housing. Using the PTPv2 time source output GEN DAQ then synchronizes to IRIG time source. The solution comes as a complete package including cables,, 19" rack mount kit and CD with user manual and installation instructions.

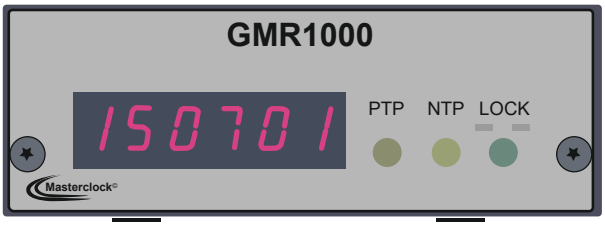


Figure B.81: External IRIG to PTPv2 convertor (1-G001B)

B.12.2 GPS to PTPv2 receiver

G002B: GPS to PTPv2 receiver

External GPS time synchronization using PTPv2 network communication.
The solution comes as a complete package, including a power over Ethernet (PoE) powered GPS antenna (OTMC 100i), a 50 m (164 ft) IP67 CAT6 outdoor RJ45 network cable, an outdoor RJ45 network surge protector (PD-OUT/SP11), a 20 m (65 ft) CAT6 RJ45 network cable, a RJ45 to Optical SFP convertor with PoE injection on the RJ45 network, two G062 SFPs (For GEN DAQ SFP network and the SFP convertor), a KAB280-10 optical cable and CD with user manual and installation instructions.

Figure B.82: External GPS time synchronization using PTPv2 (1-G002B)

B.13 Rack mount kit

B.13.1 Rack mount kit

G071: Rack Mount Kit (Option, to be ordered separately)

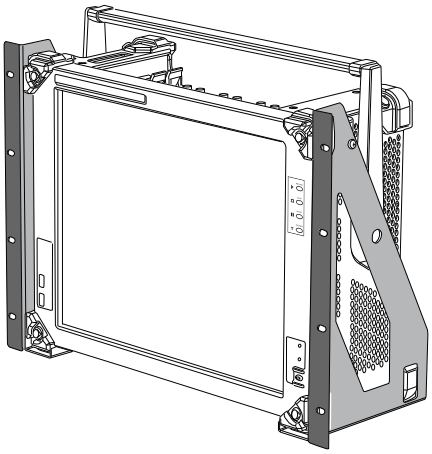


Figure B.83: GEN3i Rack Mount Kit

Rack Mount Kit	Mounting a GEN3i mainframe in a standard 19” rack. Does not support the mouse and keyboard delivered with the GEN3i. Requires no additional mounting materials. User installed option.

B.14 Shipping case

B.14.1 Shipping case

G054: Shipping Case (Option, to be ordered separately)

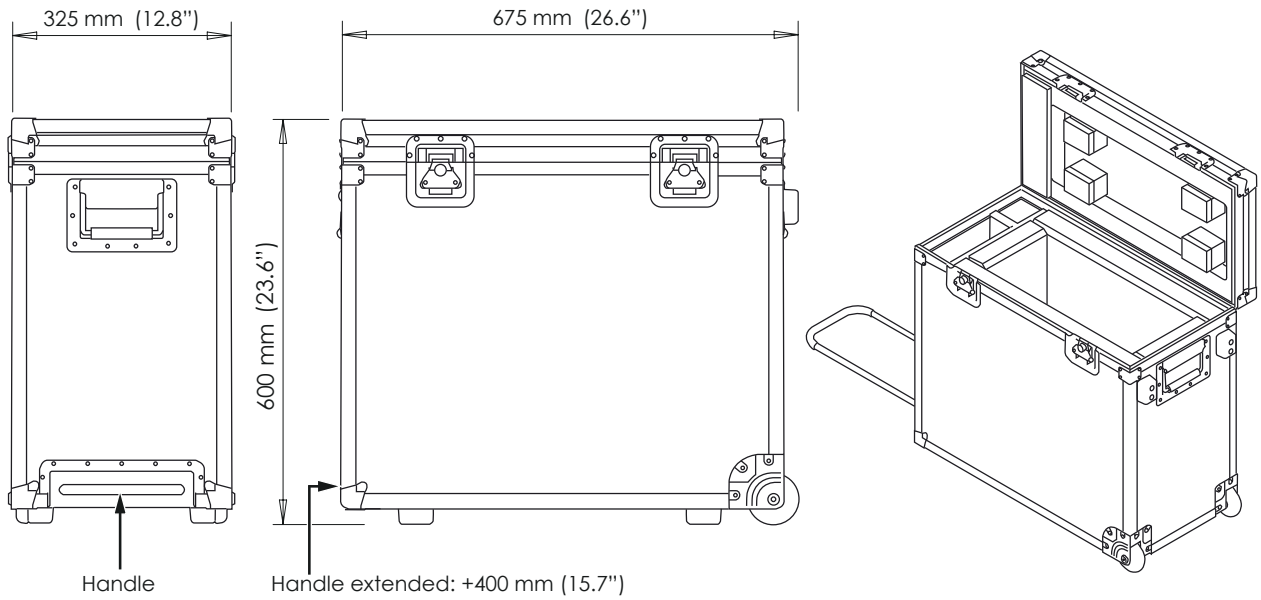


Figure B.84: Reusable hardcover shipping case with wheels and transport handle

Outside Dimensions	600 mm (23.6") x 325 mm (12.8") x 675 mm (26.5") (HxWxD)
Weight Empty Case	16.5 kg (36.3 lb)
System Storage Area	Special area for system, slides in from the top for easy storage and easy removal from the shipment case. Protects the system from impact during drops, shocks and vibrations
Accessories Area	Separate area for keyboard, mouse, power cable and additional cables
Reliable Case Transport	Wheels and extendable handle constructed for stable transportation with a low gravitation point to prevent the case from tumbling in any direction during roll transport
Case Extras	Two lift handles and locks on side of the case for easy transport
Shock and Vibration	Tested with system inside case in accordance with ASTM D4728 E
Drop Test	Tested with system inside case in accordance with ASTM D4169-04 Level I

B.15 Software

B.15.1 Perception standard software

DAQ software, Perception standard software included with GEN3i (Option, to be ordered separately)
Perception standard software package. Refer to the Perception data sheet for details.

B.15.2 Perception professional

1-PERC-PRO-01-2: DAQ software options, Perception Professional (Option, to be ordered separately)
Analysis, Advanced Report, Video Playback, Multiple Workbooks, Information, Basic FFT, Sensor Database and more

B.15.3 Instrument Panel languages

DAQ software and Instrument Panel languages (Option, to be ordered separately)
English, German, French, Chinese, Japanese, Korean, Russian, Portuguese (Brazilian)

B.15.4 PNRF free viewer

1-PERC-VW-01-2: PNRF Free Viewer (free of charge) (Option, to be ordered separately)
Same as Perception Standard but without mainframe setup and control. Opens every PNRF and NRF recording to review the recorded data. Supports display cursors and display markers, quick word reporting, print display, print settings, export to ASCII, Excel, imPRESSion, RTPro and TEAM Data. Does not support any of the standard Perception options.

B.15.5 Free viewer

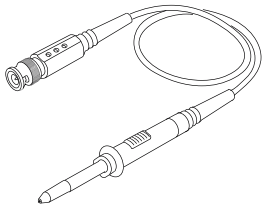
1-PERC-VA-01-2: Free Viewer (free of charge) Advanced (Option, to be ordered separately)
Same as Perception Advanced but without mainframe setup and control. Opens every PNRF and NRF recording to review the recorded data. Supports display cursors and display markers, quick word reporting, print display, print settings, export to ASCII, Excel, imPRESSion, RTPro and TEAM Data. Does not support any of the standard Perception options.

B.16 Voltage probes

B.16.1 Passive, single-ended voltage probes

G901, G902: Passive, Single-Ended Voltage Probe (Option, to be ordered separately)

To be used with single-ended non-isolated amplifiers or with differential non-isolated amplifiers in single-ended mode



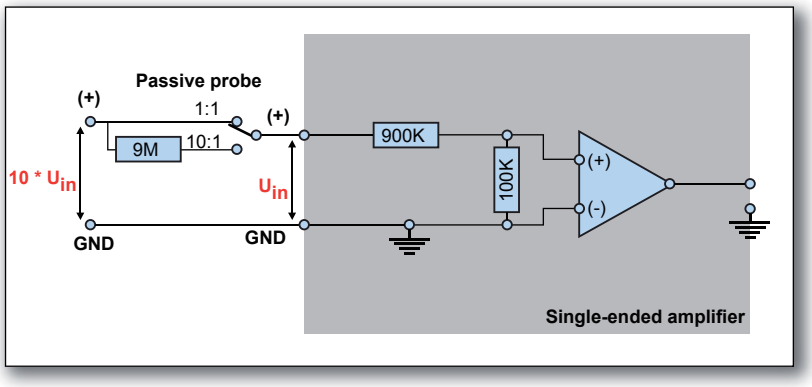


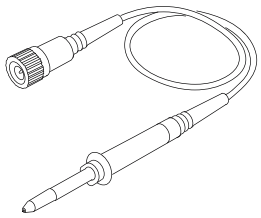
Figure B.85: Block diagram passive, single-ended voltage probe

Isolation	Not supported			
Capacitive compensation range	7 to 75 pF			
DC inaccuracy	2%			
	G901		**G902**	
Divide factors	1:1	10:1	1:1	10:1
Probe impedance (connected to channel)	1 MΩ	10 MΩ	1 MΩ	10 MΩ
- 3 dB Bandwidth	12 MHz	200 MHz	6 MHz	100 MHz
Maximum input voltage	55 V RMS	300 V RMS CAT II	55 V RMS	300 V RMS CAT II
Probe cable length	1.2 m (3.9 ft)		3 m (9.8 ft)	
Probe weight	Typically 59 g (2.1 oz)		Typically 88 g (3.1 oz)	
Original manufacturer's part number	PMK 869-923900		PMK 869-924900	
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)			

Figure B.86: Probe and probe accessories

G903: Passive, Single-Ended Voltage Probe (Option, to be ordered separately)

To be used with single-ended amplifiers or with differential amplifiers in single-ended mode



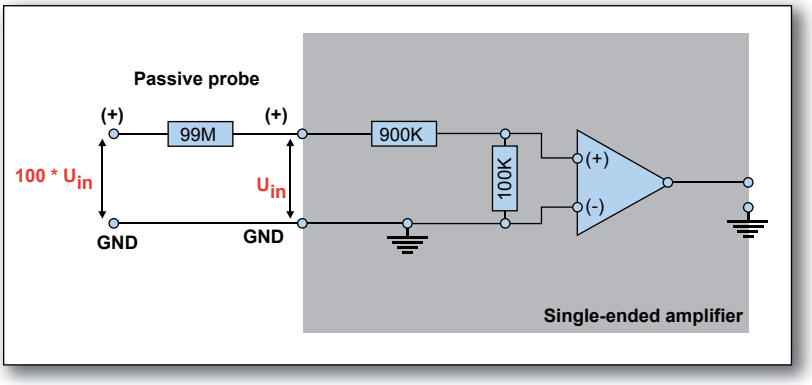


Figure B.87: Block diagram passive, single-ended voltage probe

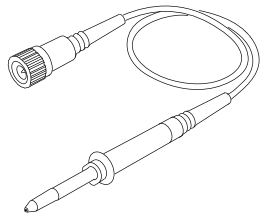
Isolation	Not supported
Capacitive compensation range	7 to 45 pF
DC inaccuracy	2%
Divide factors	100:1
Probe impedance (connected to channel)	100 MΩ
-3 dB Bandwidth	400 MHz
Maximum input voltage	1000 V RMS CAT II
Probe cable length	1.2 m (3.9 ft)
Probe weight	Typically 67 g (2.4 oz)
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturer's part number	PMK PHV1000-1-45

Figure B.88: Probe and probe accessories

Note *The compensation range of the G903 probe does not match that of GN1610/GN1611/GN3210/GN3211 cards. For the limited bandwidth of GN1610/GN1611/GN3210/GN3211, this has no noticeable effects. When using the G903 probe in combination with this card select the sensor "G903_NoCapacitiveCheck" from the Perception Sensor Database.*

G904: Passive, Single-Ended Voltage Probe (Option, to be ordered separately)

To be used with single-ended amplifiers or with differential amplifiers in single-ended mode



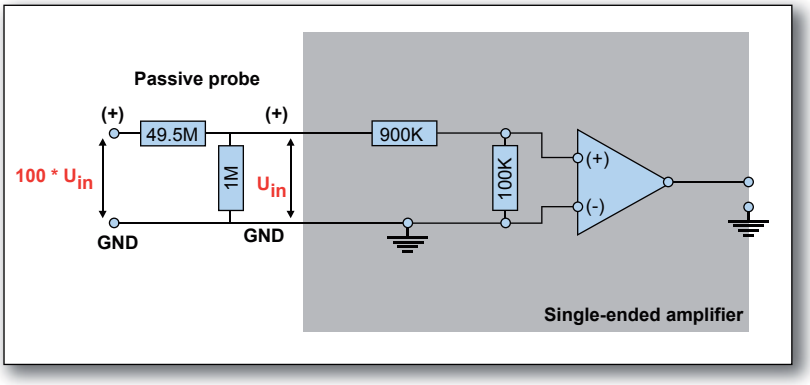


Figure B.89: Block diagram passive, single-ended voltage probe

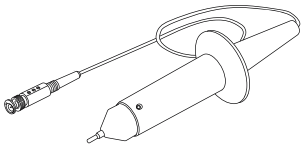
Isolation	Not supported
Capacitive compensation range	10 to 50 pF
DC inaccuracy	2%
Divide factors	100:1
Probe impedance (connected to channel)	50 MΩ
-3 dB Bandwidth	300 MHz
Maximum input voltage	2 kV RMS @ 50/60 Hz 3 kV DC
Probe cable length	2 m (6.7 ft)
Probe weight	Typically 68 g (2.4 oz)
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturer's part number	PMK 117-901600

Figure B.90: Probe and probe accessories

Note *The compensation range of the G904 probe does not match that of GN1610/GN1611/GN3210/GN3211 cards. For the limited bandwidth of GN1610/GN1611/GN3210/GN3211, this has no noticeable effects. When using the G904 probe in combination with this card select the sensor "G904_NoCapacitiveCheck" from the Perception Sensor Database.*

G906: Passive, Single-Ended Voltage Probe (Option, to be ordered separately)

To be used with single-ended amplifiers or with differential amplifiers in single-ended mode



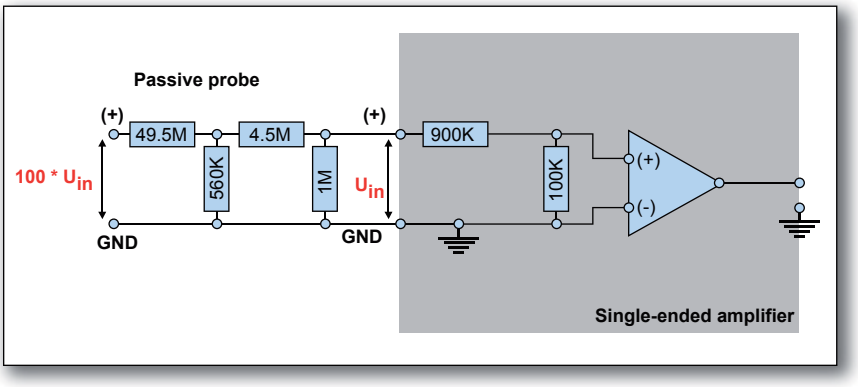


Figure B.91: Block diagram passive, single-ended voltage probe

Isolation	Not supported
Capacitive compensation range	10 to 50 pF
DC inaccuracy	2%
Divide factors	1000:1
Probe impedance (connected to channel)	100 MΩ
-3 dB Bandwidth	100 MHz
Maximum input voltage	14 kV RMS @ 50/60 Hz, 20 kV DC
Probe cable length	Typically 3 m (9.8 ft)
Probe weight	Typically 465 g (16.4 oz)
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturer's part number	PMK PHV 4002-3

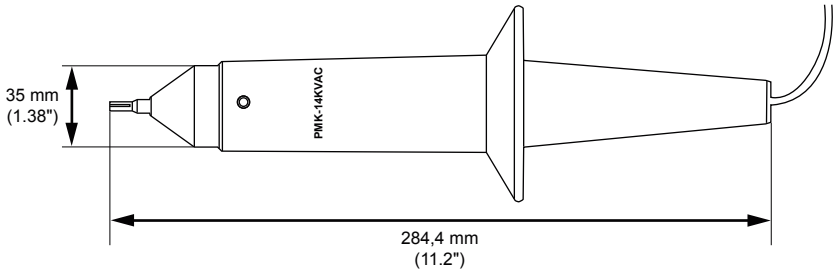


Figure B.92: Dimensions

To be used with single-ended amplifiers or with differential amplifiers in single-ended mode

Figure B.93: Probe and probe accessories

Note *The compensation range of the G906 probe does not match that of GN1610/GN1611/GN3210/GN3211 cards. For the limited bandwidth of GN1610/GN1611/GN3210/GN3211, this has no noticeable effects. When using the G906 probe in combination with this card select the sensor "G906_NoCapacitiveCheck" from the Perception Sensor Database.*

B.16.2 Passive, single-ended isolated probes

G057: Passive, Single-Ended Isolated Voltage Probe (Option, to be ordered separately)

To be used with single-ended amplifiers or with differential amplifiers in single-ended mode

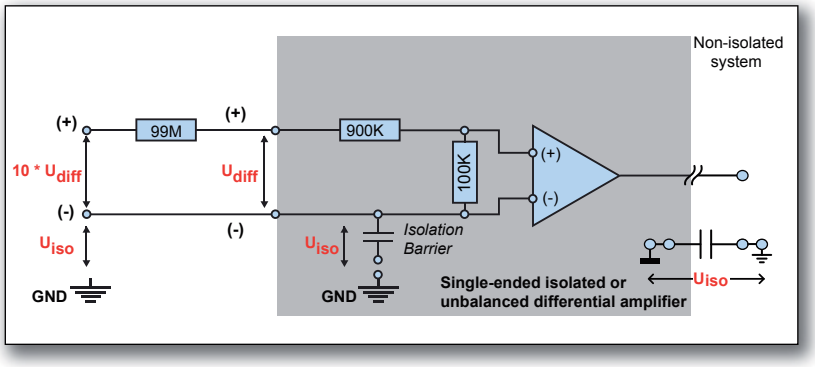


Figure B.94: Block diagram passive, single-ended isolated voltage probe

Isolation	Supported if the acquisition card uses isolated amplifiers
Capacitive compensation range	30 to 70 pF
DC inaccuracy	2%
Divide factors	100:1
Probe impedance (connected to channel)	100 MΩ
-3 dB Bandwidth	50 MHz
Maximum input voltage	600 V RMS CAT III, 1000 V RMS CAT II, 3540 V RMS CAT I
Probe cable length	1.2 m (3.9 ft)
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturer's part number	Multi-Contact Isoprobe II - 100:1 55pF

Figure B.95: Probe and probe accessories

B.16.3 Passive, differential matched isolated voltage probes

G025: Passive, Differential Matched Isolated Voltage Probe (Option, to be ordered separately)

To be used with differential isolated or non-isolated amplifiers

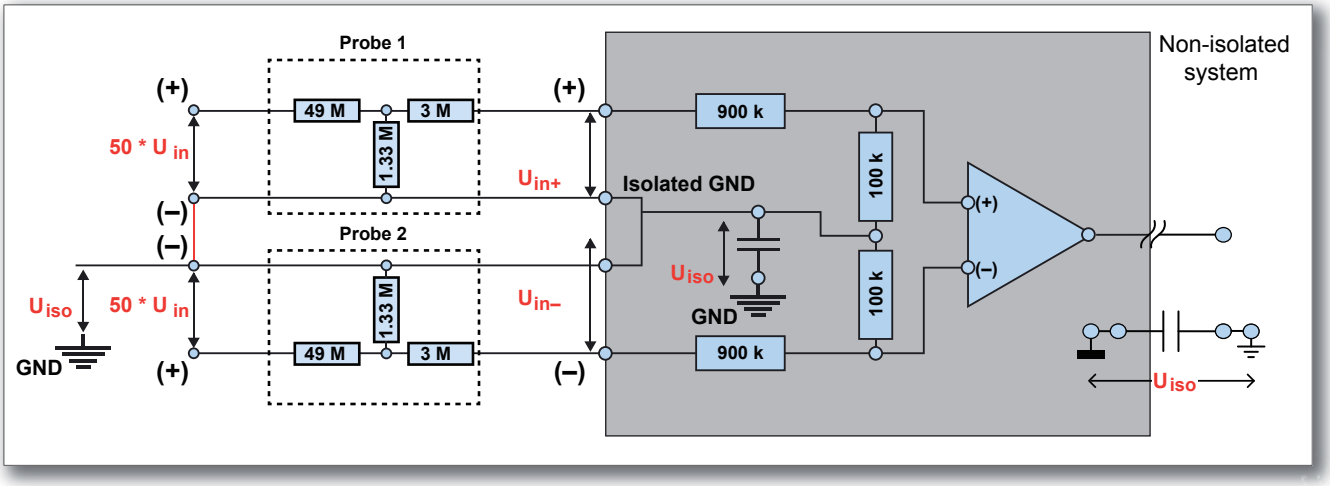


Figure B.96: Block diagram passive, differential matched isolated voltage probe

Isolation	Supported if the acquisition card uses isolated amplifiers. Keep ground of probe below isolation level of input channel.
Capacitive compensation range	100 to 140 pF
DC inaccuracy	2%
Divide factors	200:1
Probe impedance (connected to channel)	50 MΩ for each probe
-3 dB Bandwidth	20 MHz
Maximum input voltage	2.8 kV RMS CAT II
Probe cable length	3 m (9.8 ft)
Probe weight	Typically 90 g (3.2 oz) for each probe
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturers part number	PMK PFDF 4263-L-140 (LDS: 869-929500)

Figure B.97: Probe and probe accessories

G026: Passive, Differential Matched Isolated Voltage Probe (Option, to be ordered separately)

To be used with differential isolated or non-isolated amplifiers

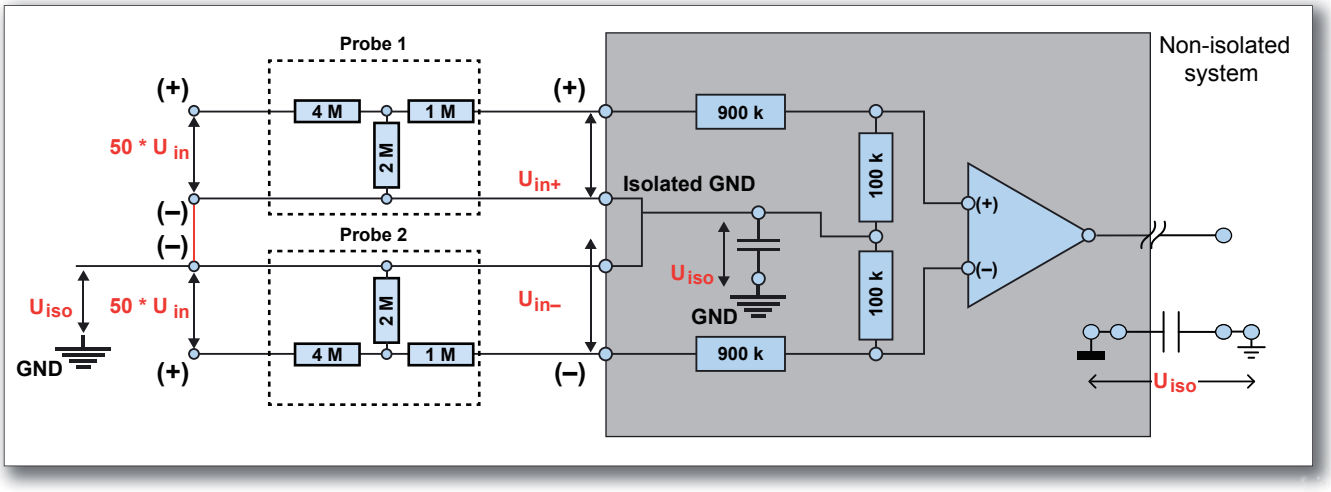


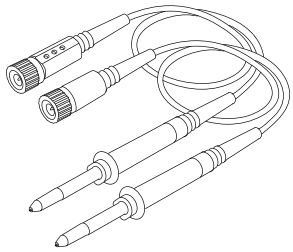
Figure B.98: Block diagram passive, differential matched isolated voltage probe

Isolation	Supported if the acquisition card uses isolated amplifiers. Keep ground of probe below isolation level of input channel.
Capacitive compensation range	105 to 140 pF
DC inaccuracy	2%
Divide factors	10:1
Probe impedance (connected to channel)	5 MΩ for each probe
-3 dB Bandwidth	100 MHz
Maximum input voltage	300 V RMS CAT II
Probe cable length	3 m (9.8 ft)
Probe weight	Typically 90 g (3.2 oz) for each probe
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturers part number	PMK PDD 4013A-140 (LDS: 869-929600)

Figure B.99: Probe and probe accessories

G907: Passive, Differential Matched Voltage Probe (Option, to be ordered separately)

To be used with differential isolated or non-isolated amplifiers



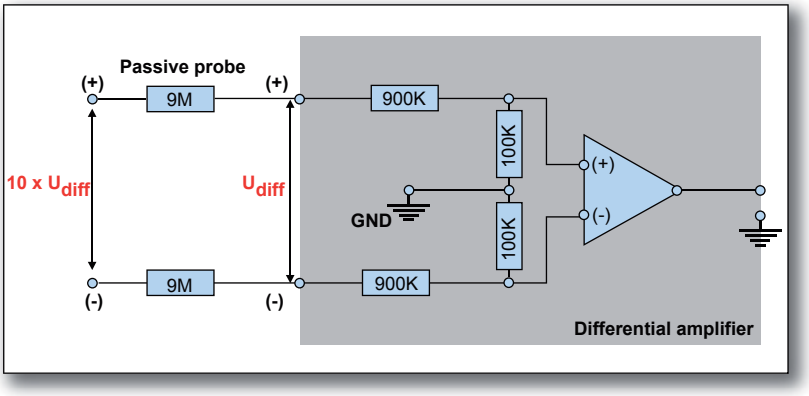


Figure B.100: Block diagram passive, differential matched isolated voltage probe

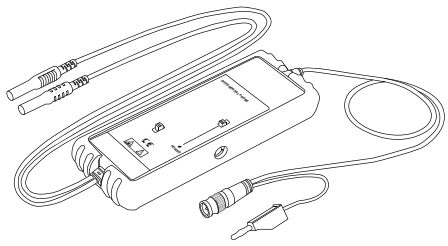
Isolation	Not supported
Capacitive compensation range	35 to 75 pF
DC inaccuracy	2%
Divide factors	10:1
Probe impedance (connected to channel)	10 MΩ for each probe
- 3 dB Bandwidth	100 MHz
Maximum input voltage	300 V RMS CAT II
Probe cable length	3 m (9.8 ft)
Probe weight	Typically 90 g (3.2 oz) for each probe
Probe operating temperature range	0 °C to +50 °C (32 °F to 122 °F)
Original manufacturers part number	PMK PDD 4013A-70

Figure B.101: Probe and probe accessories

B.16.4 Active, differential voltage probe

G909: Active, Differential Voltage Probe (Option, to be ordered separately)

To be used with differential isolated or non-isolated amplifiers



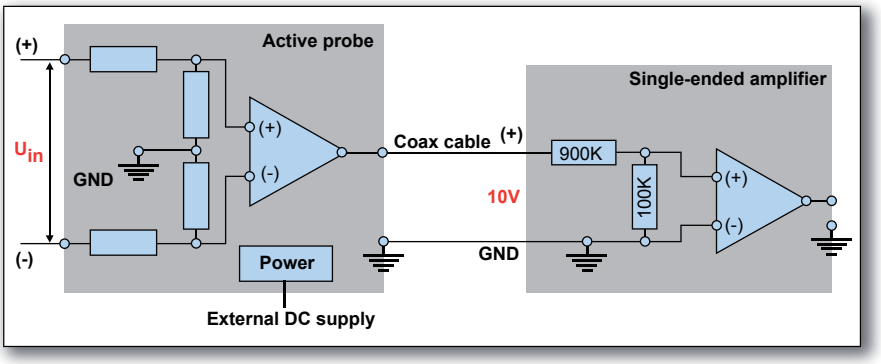


Figure B.102: Block diagram active, differential voltage probe

Isolation	Not supported	
Capacitive compensation range	Not required as this is an active output	
DC inaccuracy	2%	
Probe impedance	4 MΩ for each input	
- 3 dB Bandwidth	25 MHz	
Rise time	14 ns	
CMRR (typical)	-80 dB @ 50 Hz, -60 dB @ 20 kHz	
Output voltage	±7 V (50 kΩ load)	
Output typical offset	< ±5 mV	
Output typical noise	0.7 mV RMS	
Output source impedance	50 Ω	
Divide factor	20:1	200:1
Maximum measuring voltage	140 V RMS CAT III	1000 V RMS CAT III
Common mode voltage	1000 V RMS	1000 V RMS
Maximum voltage on each input (Common mode + measurement voltage)	1000 V RMS	1000 V RMS
Probe power	4 * AA cell battery or external power	
External power source	Regulated voltage between 4.4 V DC and 12 V DC	
Power usage	60 mA @ 6 V DC 40 mA @ 9 V DC	
Probe cable length	Input leads 0.45 m (1.48 ft) BNC output cable 0.95 m (3.12 ft)	
Probe weight	Typically 265 g (3.6 oz)	
Probe operating temperature range	-10 °C to +40 °C (14 °F to 104 °F)	
Original manufacturers part number	Probe Master Inc™, 4231-20X/200X	

Figure B.103: G909 Probe

B.16.5 High precision differential probe

5 kV RMS High Precision Differential Probe (Option, to be ordered separately)

5 kV RMS, 20 MΩ, 50:1, typical 0.1 % high precision, differential probe to be used in combination with GN610B and GN611B acquisition cards. The built-in earthing monitor system increases safety of the user and protects the GEN series inputs for isolation overloads.
The probe and output cable are optimized to match the 33 pF input capacitance when using the ranges ± 10 V, ± 20 V, ± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1000 V. In the lower ranges passband attenuation exceeds the HDP specified amplitude response.

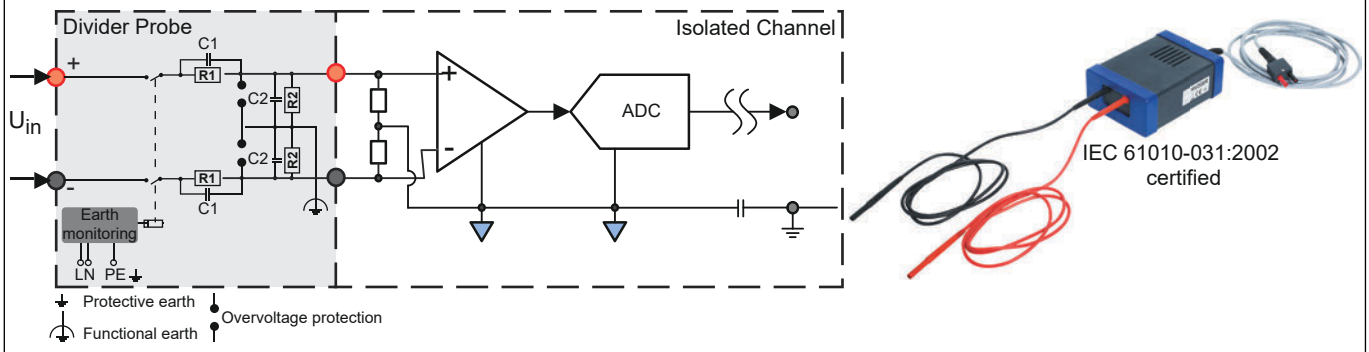


Figure B.104: Block diagram and image

Maximum input to earth voltage IEC 61010-031:2002, CB Test certificate CA/ 20325/CSA	1000 V RMS or DC CAT IV 5 kV RMS (No measurement category defined for nominal voltage above 1 kV RMS)
Maximum DC input to earth voltage IEC 61010-031:2015	1500 V DC CAT IV
Divider ratio	50:1
Measurement ranges	± 500 V up to ± 1500 V (1 kV RMS) CAT IV ± 1 kV RMS up to ± 5k V RMS (Full safety rated)
Inaccuracy (divider, cable and GN610B)	± 0.2% @ 1000 V, 50 Hz, 25 °C (0.1% typical)
Input impedance	20 MΩ ± 0.2%
Temperature coefficient	± 10 ppm / °C (± 18 ppm / °F)
Bandwidth	-0.5 dB @ 100 kHz, phase match 0.1°
Input cable/pins	High voltage insulated 4 mm safety connector (similar to Stäubli Electrical Cable MC XHM-5000)
Output pins	Cable with 4 mm banana plugs
Earth monitoring	If functional earth is not attached divider is floating and inputs are disconnected from the output
Original manufacturers part number	HVD50R
Operating temperature range	5 °C to +40 °C (41 °F to 104 °F)

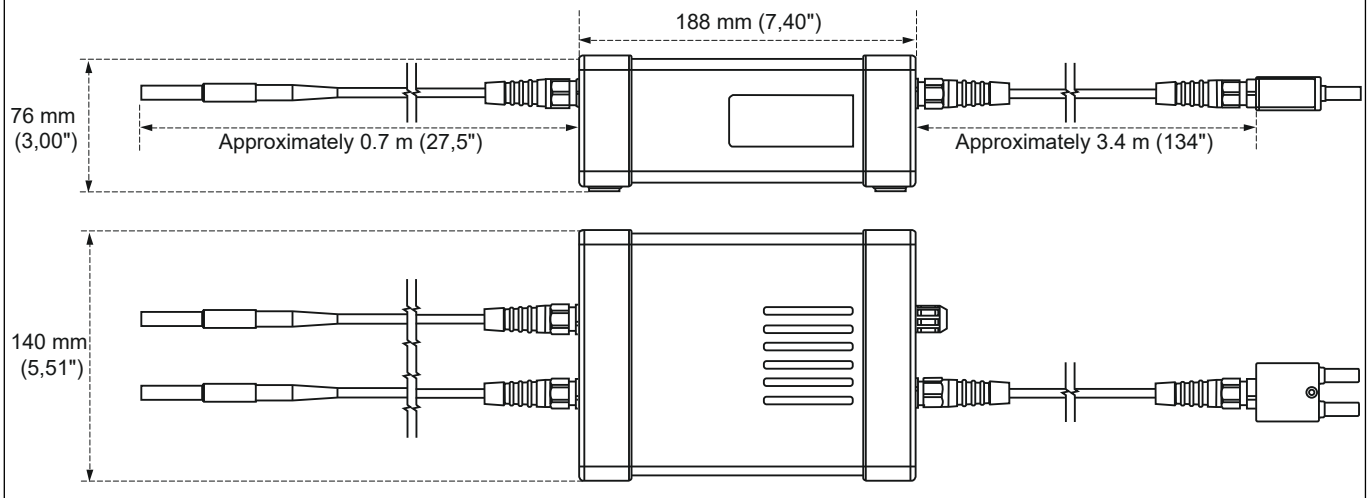


Figure B.105: Dimensions

1 kV RMS and DC CAT IV Differential Probe (Option, to be ordered separately)

1 kV RMS/DC CAT IV, 4 MΩ, 10:1, typical 0.1% high precision, differential probe to be used in combination with GN610B and GN611B acquisition cards.
The probe is optimized to match the 33 pF input capacitance when using the ranges ± 10 V, ± 20 V, ± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1000 V. In the lower acquisition card ranges passband attenuation exceeds the specified amplitude response.

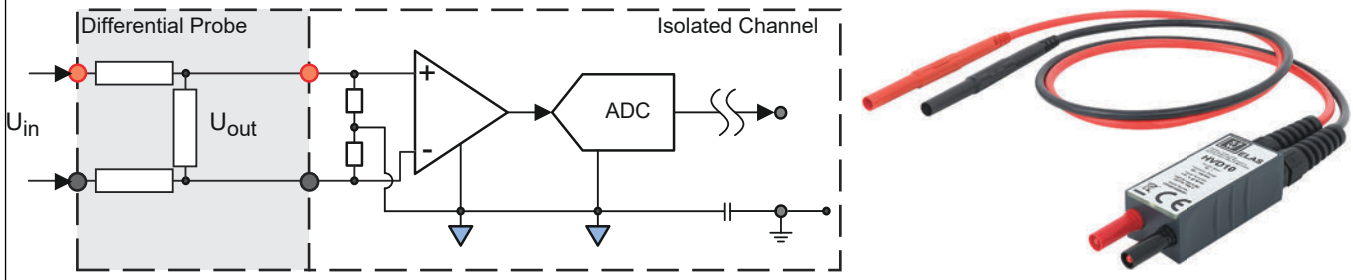


Figure B.106: Block diagram and image

Maximum input to earth voltage IEC 61010-031:2015	1000 V RMS or DC CAT IV 1500 V DC CAT III
Divider ratio	10:1
Measurement ranges	± 100 V up to ± 1500 V (1 kV RMS) (common mode < 1000 V RMS)
Inaccuracy including GN61xB card	± 0.2% @ 1000 V, 50 Hz, 25 °C (0.1% typical)
Input impedance	4 MΩ ± 0.2%
Temperature coefficient	± 25 ppm / °C (± 45 ppm / °F)
Bandwidth	-0.3 dB @ 100 kHz, phase match 1°
Input cable/pins	High voltage insulated 4 mm safety connector (similar to Stäubli Electrical Cable MC XHM-5000)
Output pins	4 mm safety banana, 19 mm (0.75") spacing
Isolation (terminals – earth)	1000 V RMS
Resistor technology	Metal foil
Original manufacturers part number	HVD10
Weight	Approximately 53 g (1.87 oz)
Operating temperature range	+5 °C to +40 °C (41 °F to 104 °F)

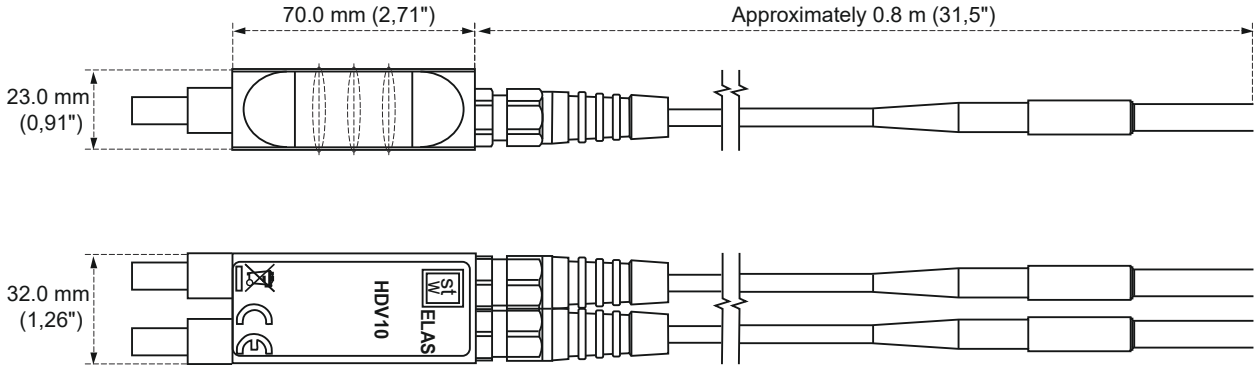


Figure B.107: Dimensions

B.16.6 High precision impedance probe

Gxxx: 10 MΩ Impedance Probe (Option, to be ordered separately)

High precision 10 MΩ impedance probe (HDP) to be used in combination with GN610B and GN611B acquisition cards. Reduces the resistive/current load on the device under test by increasing the input impedance to 10 MΩ with 0.2% inaccuracy. The use of the 10:1 divider reduces the lowest user range to ± 0.1 V. The highest input range is ± 1000 V due to the maximum voltage rating of the probe.
The HDP10H probe is optimized to match the 33 pF input capacitance when using the ranges ± 10 V up to ± 1000 V.
The HDP10L probe is optimized to match the 57 pF input capacitance when using the ranges ± 10 mV up to ± 5 V.

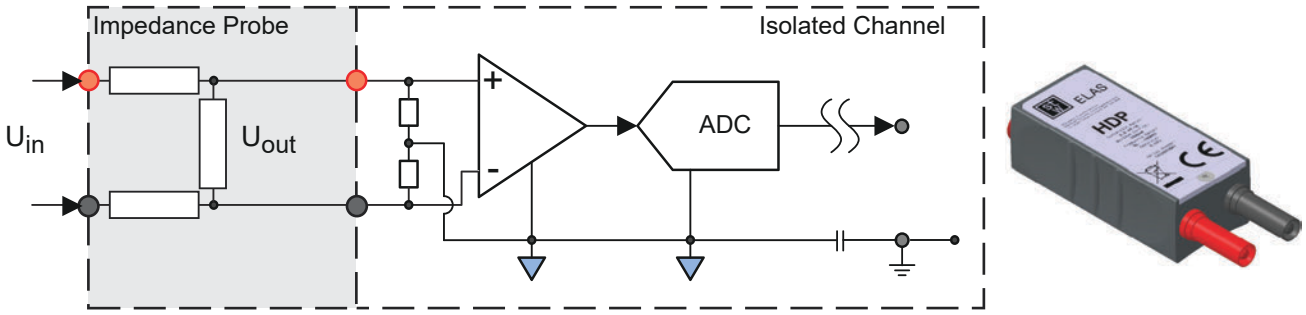


Figure B.108: Block diagram and image

Maximum input voltage	± 1000 V DC, ± 600 V RMS CAT II
Divider ratio	10:1
Measurement ranges	
HDP10H	± 100 V up to ± 1000 V
HDP10L	± 100 mV up to ± 50 V
Inaccuracy	± 0.2%
Input impedance	10 MΩ ± 0.2%
Temperature coefficient	± 25 ppm / °C (± 45 ppm / °F)
-0.5 dB Bandwidth	100 kHz
Output capacitive match	HDP10H 33 pF HDP10L 57 pF
Input pins	4 mm safety banana, 13 mm (0.51") spacing
Output pins	4 mm safety banana, 19 mm (0.75") spacing
Isolation (terminals – earth)	1000 V RMS
Resistor technology	Metal foil
Original manufacturers part number	HDP
Weight	53 g (1.87 oz)
Operating temperature range	0 °C to +40 °C (32 °F to 104 °F)

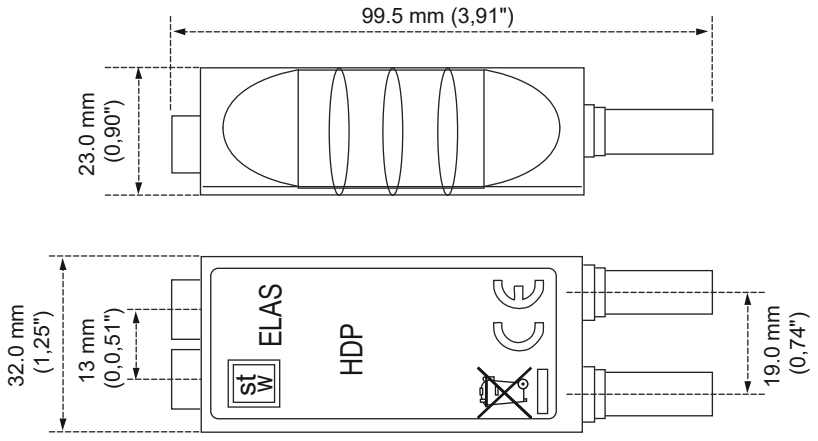


Figure B.109: Dimensions

B.16.7 High Voltage Cable extension

5 kV RMS High Voltage Cable Extension (Option, to be ordered separately)

The High Voltage Cable (HVC) is an extension for measurement cables with voltages up to 5 kV RMS. This device is designed to be connected with a cable on the input terminal of the high precision differential probe HVD10 and HVD50R. The HVC is designed according IEC 61010-031:2015 compliant to 1000 V RMS CAT IV and 1500 V DC CAT IV.

Figure B.110: Cable

Maximum Current	5A
Maximum Input to earth voltage IEC 61010-031:2015	1 kV RMS CAT IV 1.5 kV DC CAT IV 5 kV RMS (No measurement category defined for nominal voltage above 1 kV RMS / 1.5 kV DC)
Impedance Input --> Output	< 0,1 Ω
Original manufacturers part number	HVC
Operating temperature range	+5 °C to +40 °C (+41 °F to +104 °F)
Input cable connector	High voltage insulated 4 mm safety connector (similar to Stäubli Electrical Cable MC XHM-5000)
Output cable connector	Female connector compatible with: ● HVD50R ● HVD10 ● Stäubli Electrical Cable XHM-5000 ● Stäubli Electrical Cable XHL-5000 ● Schützinger HSPL 7576 / 1
Available cable lengths	1,5 m (59") / 3m (118") / 4,5m (177") / 6m (236")

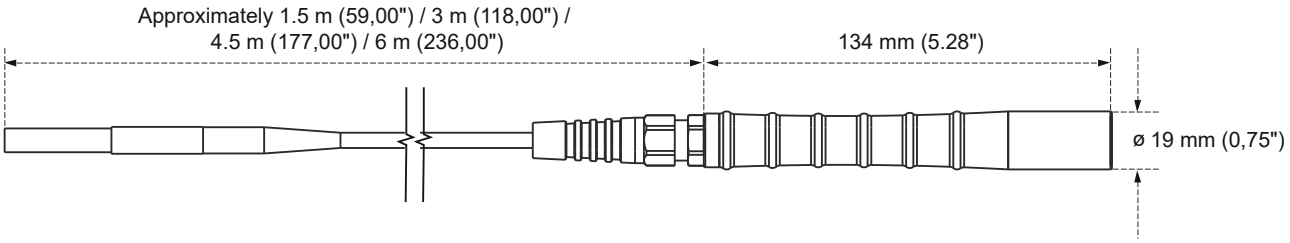


Figure B.111: Dimensions

C G001B Specifications

C.1 GPS time synchronization (G001B)

G001B: IRIG Receiver with PTP Output (Option, to be ordered separately)

External IRIG to PTPv2 convertor in a compact housing. Using the PTPv2 time source output GEN DAQ then synchronizes to IRIG time source. The solution comes as a complete package including cables,, 19" rack mount kit and CD with user manual and installation instructions.

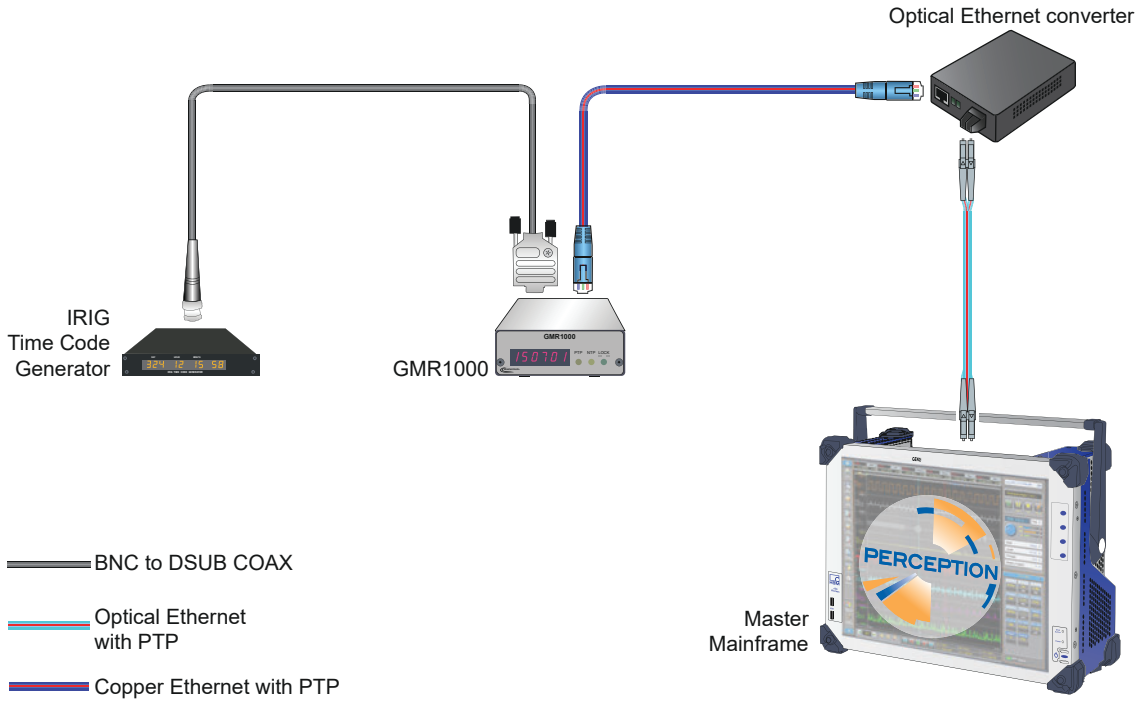


Figure C.1: Example setup IRIG time synchronization

Included in G001B option	
IRIG receiver	GMR1000
IRIG input	2.5 m (8.2 ft) BNC to DSUB COAX
Ethernet cables	4.5 m (14.8 ft) CAT6 Ethernet cable to PoE adapter 20 m (65 ft) Fiber cable standard MM LC-LC 1-KAB280-20
Optical Ethernet converter	Converts the electrical Ethernet signal to an optical SFP Ethernet output signal.
Optical SFP	2 * G062 for optical Ethernet converter and GEN DAQ mainframe optical ethernet option
IRIG receiver GMR1000	
DC input	9-28 V DC
AC input	External wall mount power supply
Dimensions	164 mm (width) x 103 mm (height) x 36 mm (depth) (6.45" x 4.05" x 1.41")
Weight	0.45 kg (16 oz)
Rack mount	19", 1U height included
IRIG protocols supported	IRIG-B0 (DCLS), IRIG-B1 (AM), IRIG-A0 (DCLS), IRIG-A1 (AM), IRIG-E0 (DCLS), IRIG-E1 (AM)
Time synchronization accuracy	< 50 µs to IRIG time (Measured on GEN DAQ mainframe)
GEN DAQ series functions	Capture start of recording time Synchronize master time base oscillator frequency
Time required to full synchronization	
No recording active	< 1 min
Recording or pause active	< 1 min plus 25 s per ms recording time deviation from IRIG time source
Supported PTPv2 timing protocol	PTP according to IEEE1588-2008 (1 step, End-to-End, UDP, IPv4)

D G002B Specifications

D.1 GPS time synchronization (G002B)

G002B: GPS Receiver with PTP Output (Option, to be ordered separately)

External GPS time synchronization using PTPv2 network communication.
The solution comes as a complete package, including a power over Ethernet (PoE) powered GPS antenna, all required RJ45 network cable, an outdoor RJ45 network surge protector, a PoE injector, two G062 SFPs and CD with user manual and installation instructions.

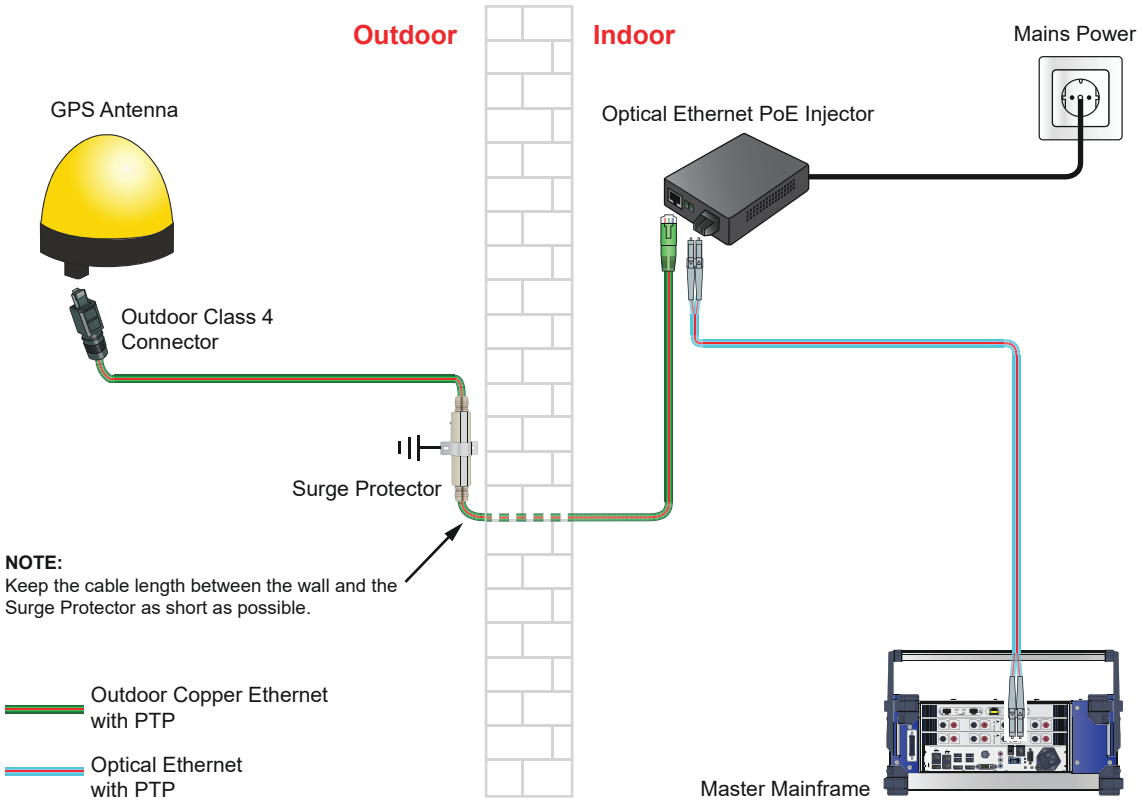


Figure D.1: Example setup GPS time synchronization

Included in G002B option	
GPS antenna	OTMC 100
GPS antenna cables	50 m (164 ft) Outdoor CAT6 Ethernet cable to Surge Protector 20 m (65 ft) Outdoor CAT6 Ethernet cable to PoE adapter 20 m (65 ft) Fiber cable standard MM LC-LC 1-KAB280-20
Surge Protector	UL497B standard
Optical Ethernet PoE Injector	Power over Ethernet (PoE) injector. Supplies power to GPS antenna and converts the electrical Ethernet signal to an optical MM 50/125 um Ethernet output signal.
Optical SFP	2 * G062 for PoE injector and GEN DAQ mainframe optical ethernet option
GPS antenna safety	IEC60950-1:2005 2 Ed. +A1:2009 IEC60950-22:2005
GPS antenna connector	RJ45 waterproof connector according to IEC61076-3-106 (Variant 4)
Time synchronization accuracy	<150 ns to reference time (UTC) (Measured on GEN DAQ mainframe)
GEN DAQ series functions	Capture start of recording time Synchronize master time base oscillator frequency
GPS localization time	4 to 10 minutes after power on of antenna
Time required to full synchronization after GPS localization completed	
No recording active	<1 min
Recording or pause active	<1 min plus 25 s per ms recording time deviation from UTC time
User notifications while recording	Time marks on PTP time synchronization lost/restored, Mac Address of Master
Antenna Supported Timing Protocols PTPv2	PTP according to IEEE1588–2008 (1 step, End-to-End, UDP, IPv4)

Example Setup: GPS Receiver with Master/Slave Connected Systems

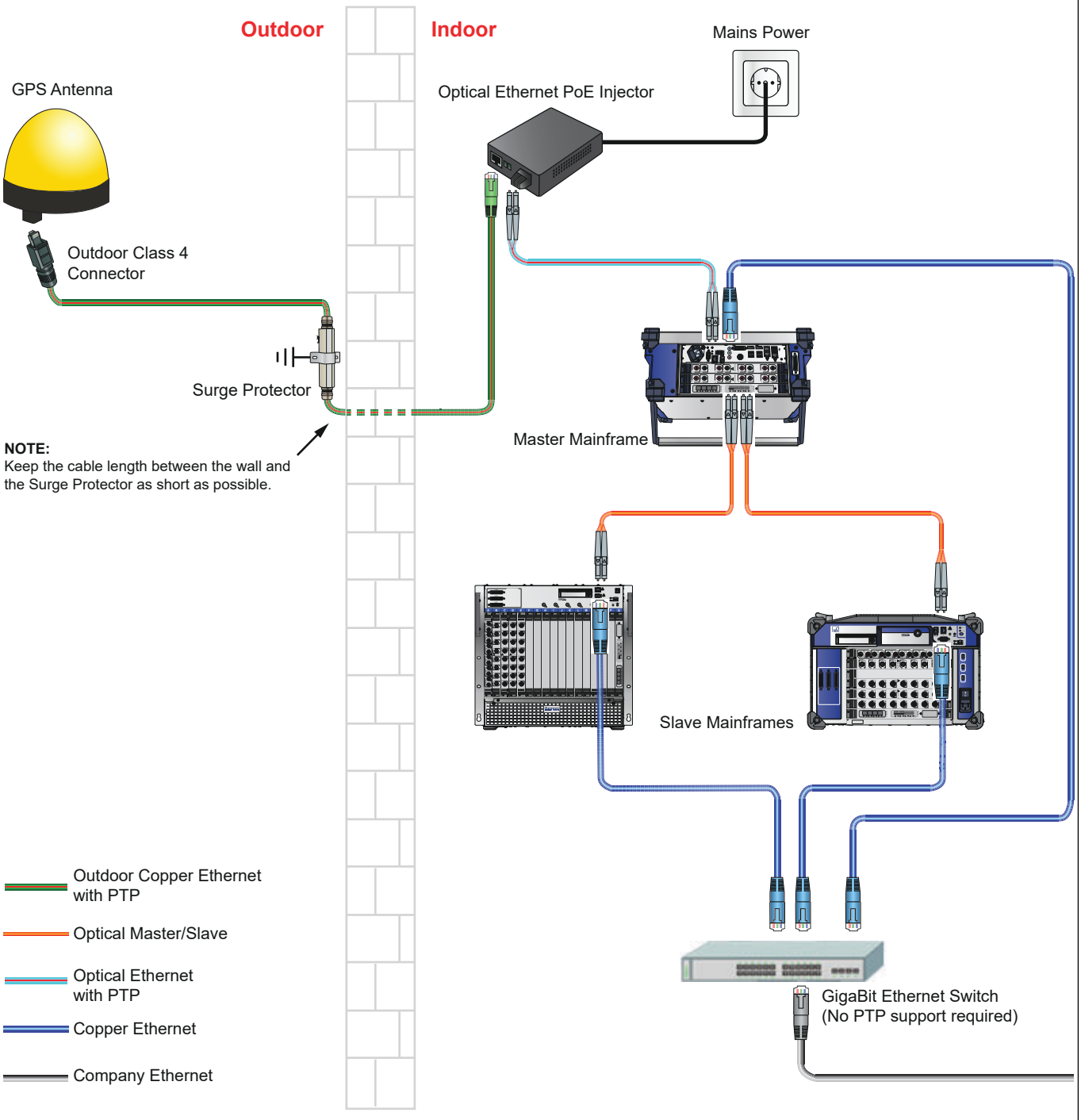


Figure D.2: GPS setup for tethered mainframe with Master/Slave connected slaves

Example Setup: GPS Receiver with Tethered Mainframes and QuantumX

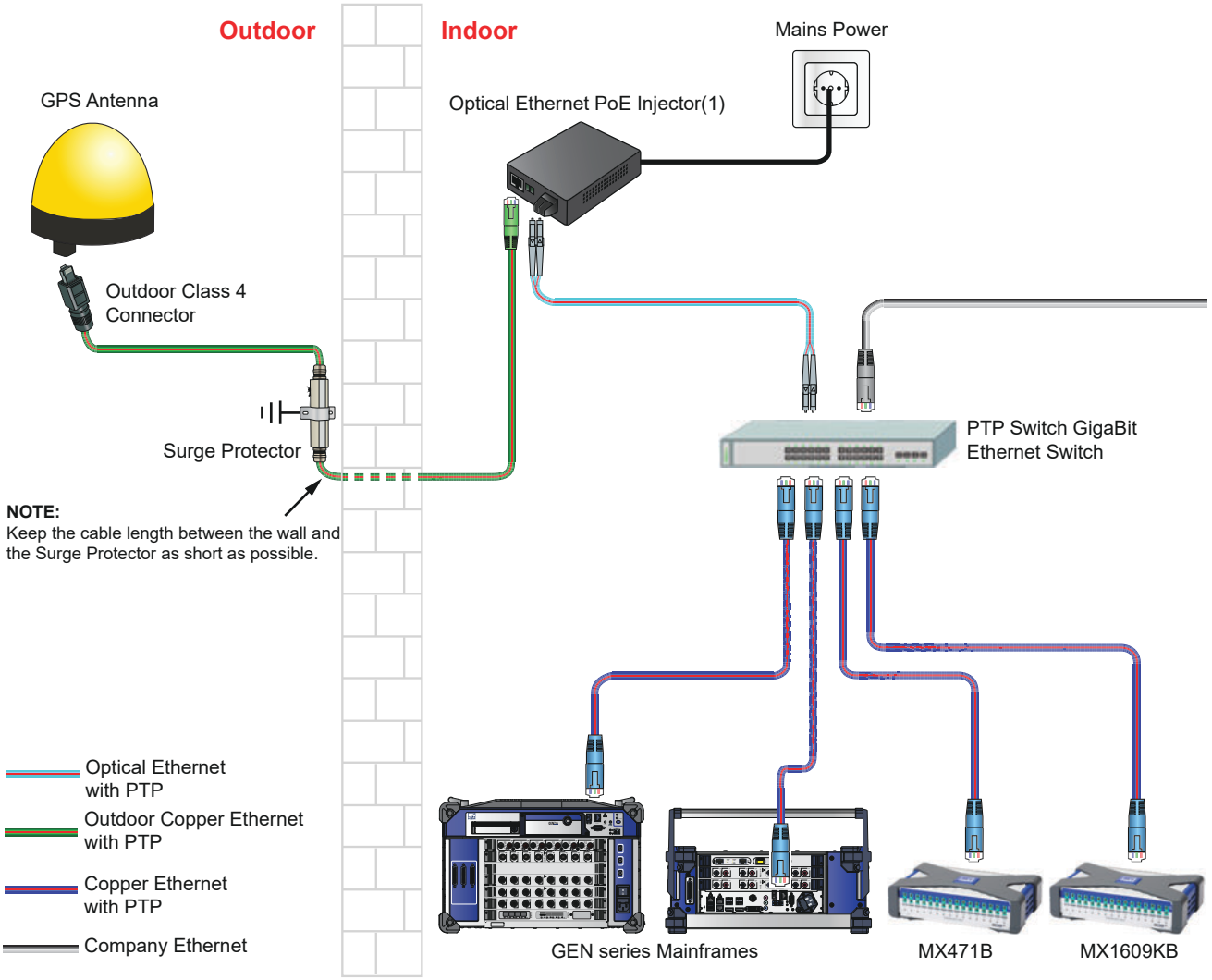


Figure D.3: GPS setup for tethered mainframes and QuantumX

(1) Ethernet PoE injectors using dual RJ45 electrical connections can be ordered through customs systems. Contact custom systems at: customsystems@hbm.com

E Maintenance

E.1 Preventive maintenance

Regularly scheduled HBM preventive maintenance services that include cleaning, adjusting, inspection and calibration will help to:

- Assure that the instrument is available whenever it is needed
- Maintain optimum performance
- Avoid expensive unplanned downtime and repair

Also, regularly scheduled maintenance is a predictable expenditure.

Except for the batteries, the instrument is a maintenance-free product; no preventive maintenance is required.

Inspect the instrument's batteries at least twice a year, but preferably every month. Damaged batteries and batteries with reduced capacity should be replaced to meet the batteries' specified capacity and consequently the instrument's specified run-time using the battery. The main benefit of this inspection will result in reliable use of the instrument.

If the instrument has been stored for four weeks or longer, first inspect the battery before putting the instrument back to use.

How often preventive maintenance needs to be performed depends on your application, workload, and regulatory requirements.

E.2 Preventive drive replacement

When installed in the instrument, the drive is the "data center" of the instrument. It contains all of the programs and recorded data. The CPU may be the "brain" of the system, but the drive is its memory and personality; it is what makes the instrument what it is.

CAUTION

Do not to exceed the drives warranty period.

Contact HBM service for more details.

E.2.1 Hard disk drive

The reliable service life of a typical hard disk drive is around three to five years. Some drives work for a decade or longer, but every year that passes after three years increases the chances of a failure.

If the instrument uses a hard disk drive, HBM therefore advises replacing it at least every two years to prevent loss of data or inactivity of the instrument.

Note *This recommendation is based on 24/7 use of the instrument at full drive write speeds. Reduced use of the instruments drive allows for a longer replacement period.*

E.2.2 Solid State Drive (SSD)

Solid State Drives have no mechanical parts that can fail. However, each block of data on a Solid State Drive can only be erased and written a defined number of times before the data block fails. The Solid State Drive manages this limitation so that drives can last for many years with normal use. Very intensive use of the Solid State Drive to record and store new data will shorten the drive's life expectancy.

The reliable service life of a typical Solid State Drive drive is around three to five years. Some drives work for a decade or longer, but every year that passes after three or so increases the chances of a failure.

If the instrument uses a solid state drive, HBM therefore advises replacing it at least every two years to prevent loss of data or inactivity of the instrument.

Note *This recommendation is based on 24/7 use of the instrument at full drive write speeds. Reduced use of the instruments drive allows for a longer replacement period.*

E.3 Cleaning

To clean the instrument, disconnect all power sources. Lightly wipe the surfaces with a clean, soft cloth dampened with water.

The GEN3i does not require additional routine cleaning. If the cooling inlets on the side of the instrument become clogged with dust, use a small brush and/or vacuum cleaner to remove the dust.

F Service Information

F.1 General - Service Information

HBM offers comprehensive factory servicing for all HBM Data Acquisition products. Extended warranties for calibration, repair or both are available. Installation, on-site or factory training are also available. Contact the factory or local sales person for more information. For local contact information, visit www.hbm.com/support.

If servicing is needed on the equipment, contact the factory with the model and serial numbers, a description of the problem, and your contact information. A Return Material Authorization (RMA) number will be issued. Attach this number and the accompanying paperwork to the unit.

During the warranty period, the customer pays for shipping to HBM. HBM pays to return the equipment in the same fashion as it was received. Outside of the warranty period, a quote for the shipping costs is issued. A purchase order must be received before work can be performed.

It is recommended that the unit always be shipped in the original shipping container.

For the frequent shipping of some products, HBM offers hard shipping containers specifically designed for frequent transportation.

F.2 Calibration/verification

The GEN series Data Acquisition System is factory calibrated when delivered to the customer. Swapping, replacing or removing the cards may result in minor deviations to the original calibration. HBM recommends that the GEN series system should be tested and, if necessary, calibrated once a year or after any major event that may affect calibration. When in doubt, consult your local supplier.

G Trouble-shooting

G.1 Boot setup

GEN3i is an acquisition system with a built-in PC. As with any PC, this implies that the system consists of a set of tools that allow the setup of the PC and its hard disk to be set up.

These tools can only be accessed immediately after **Power on**. Make sure that the mouse and keyboard are attached prior to powering on the system.

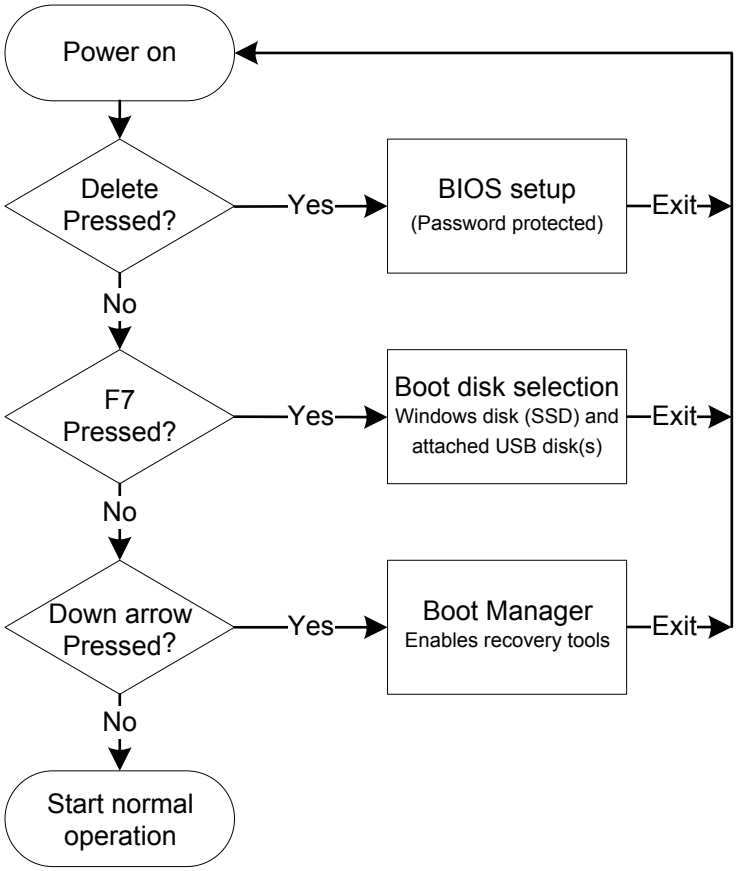
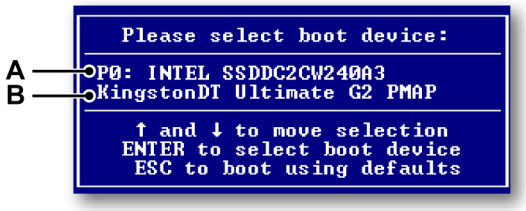


Figure G.1: Boot selections

To access the BIOS setup, press the delete key during the boot process. The BIOS setup is password protected to prevent accidental changes to the BIOS. As GEN3i is a fixed system setup, no BIOS changes are required. HBM service can make BIOS changes if the system setup ever requires them.

If an external disk needs to be booted, press the F7 key while the BIOS is booting. BIOS displays a selection of all available bootable disks. Select the disk of choice and continue booting from this disk.



Note *Text displayed in this dialog can be different, depending on which SSD/RAID disk and USB disk are used.*

A Name of installed (RAID) Solid State Drive

B Name of USB disk/stick attached to your system

Recovery tools can be accessed by pressing the down arrow key during the boot process. A selection menu of recovery tools available appears. These recovery tools are available on the recovery partition. This partition is not available during normal instrument operation and can only be accessed during the boot process. For more details, please refer to the section "Recovery tools disk" on page 724.

Solid State Drive layout

The Solid State Drive is partitioned in two partitions.

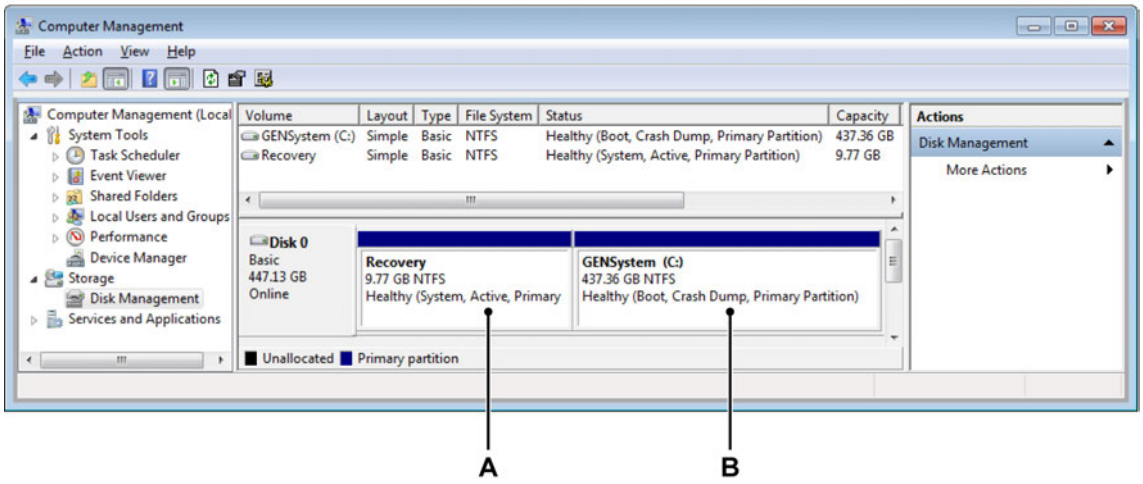


Figure G.2: Solid State Drive

A Partition 1: Recovery

B Partition 2: GENSystem (standard boot partition)

The GENSystem partition has Windows® 7 Ultimate 64 bits installed and all HBM software installed on it. It is not a standard Windows® 7 Ultimate installation, as HBM pre-loads all required drivers to operate the GHS Integrated system. If the GHS Integrated system ever fails to properly boot into Windows® and/or operate the Perception software without problems, a GHS Integrated system image restore is required to get the system working properly again.

Installing a regular Windows® 7 Ultimate license and loading standard Perception software will not install the GHS Integrated system drivers. Perception software will not be able to find the acquisition hardware.

HBM does not supply separate driver installation packages. Ultimately, HBM service can supply a recovery disk to restore the recovery partition if this is damaged or lost due to any unforeseen reason.

For more information on GHS Integrated system image restore, please refer to "GHS Integrated system image restore" on page 725.

Recovery tools disk
When pressing the down arrow key during the Integrated system boot process, the recovery partition tools are started.
Use the arrow keys to select the tool and press enter to start the tool.

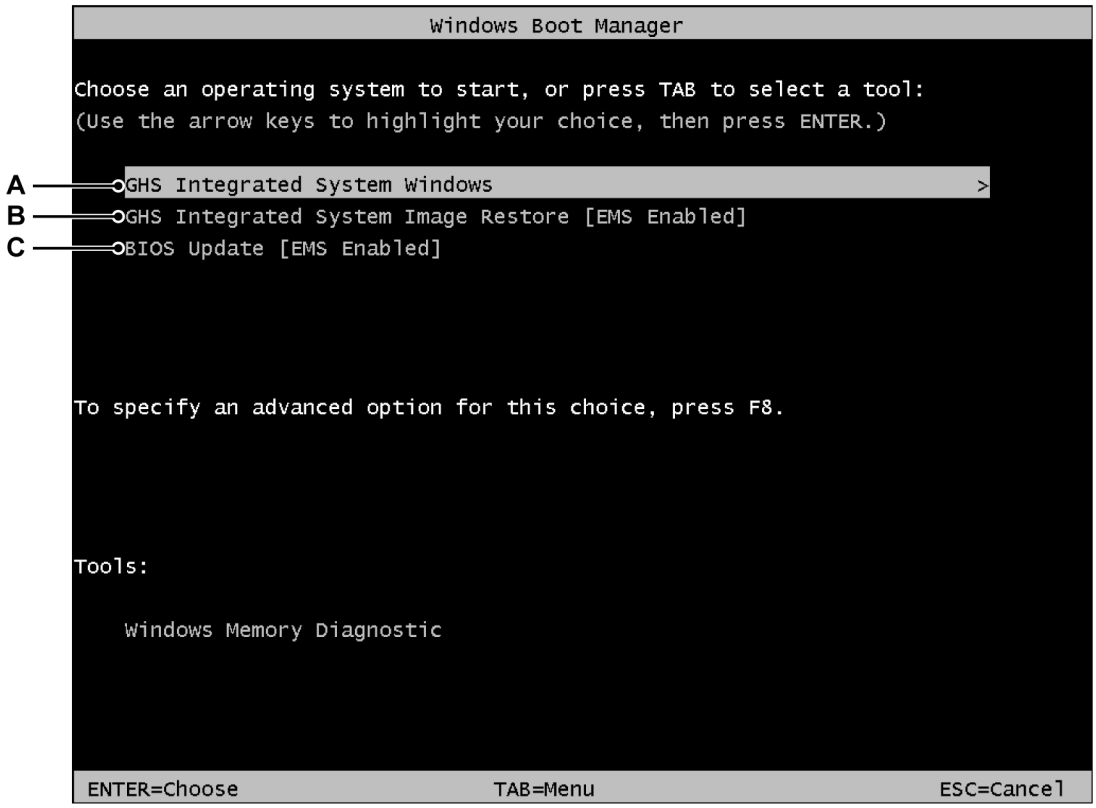


Figure G.3: Recovery partition boot manager

A **GHS Integrated System Windows**
Boots the standard Windows® software and starts the Perception software.

B **GHS Integrated System Image Restore [EMS enabled]**
Starts the Windows® recovery process to restore the GENSystem Partition to its original factory setup.
For more information on GHS Integrated system image restore, please refer to "GHS Integrated system image restore" on page 725.

C **BIOS Update [EMS Enabled]**
Restores the GHS Integrated system BIOS to its factory defaults.
For more information on Restoring the GHS Integrated system BIOS, please refer to "GHS Integrated system BIOS update" on page 773.

Note *EMS enabled is a technical step to allow both BIOS Update and image restore to run their process correctly. This is of no concern for the user of the system.*

G.2 GHS Integrated system image restore

Image restore is only useful when the GHS Integrated system has problems booting the Windows® operating system or when unexplainable Perception software errors occur while using the integrated system.

No extra tools are required to restore the system. Restoring the system to the Windows® factory default setup requires the Windows® 7 or 10 license to be reactivated.

The system disk has a hidden partition that holds an image of the GENSystem partition. The version of the image matches the way the mainframe was originally shipped. That is, if the system was running Perception 6.40.13201 when it was shipped, this is included in the recovery partition.

WARNING

All data, including Perception recordings, will be deleted during the GHS Integrated image restore process. Back up valuable data before starting this process.

G.2.1 Boot menu preparation

In order to reimage the system, proceed as follows:

WARNING

Do not power off or reboot the system while restoring the image.

1. Power off the mainframe
2. Make sure that a keyboard is connected to a USB 2.0 port.

Note *Windows® 7: USB 3.0 ports are not supported during the image restore process.*
Windows® 10: USB 3.0 ports are supported system image restore.

3 Turn the mainframe back on and then continually push the up and down arrow keys on the keyboard. This makes the system stop at the boot menu. Use the arrow keys to select the **GHS Integrated System Image Restore [EMS Enabled]** item in the list.

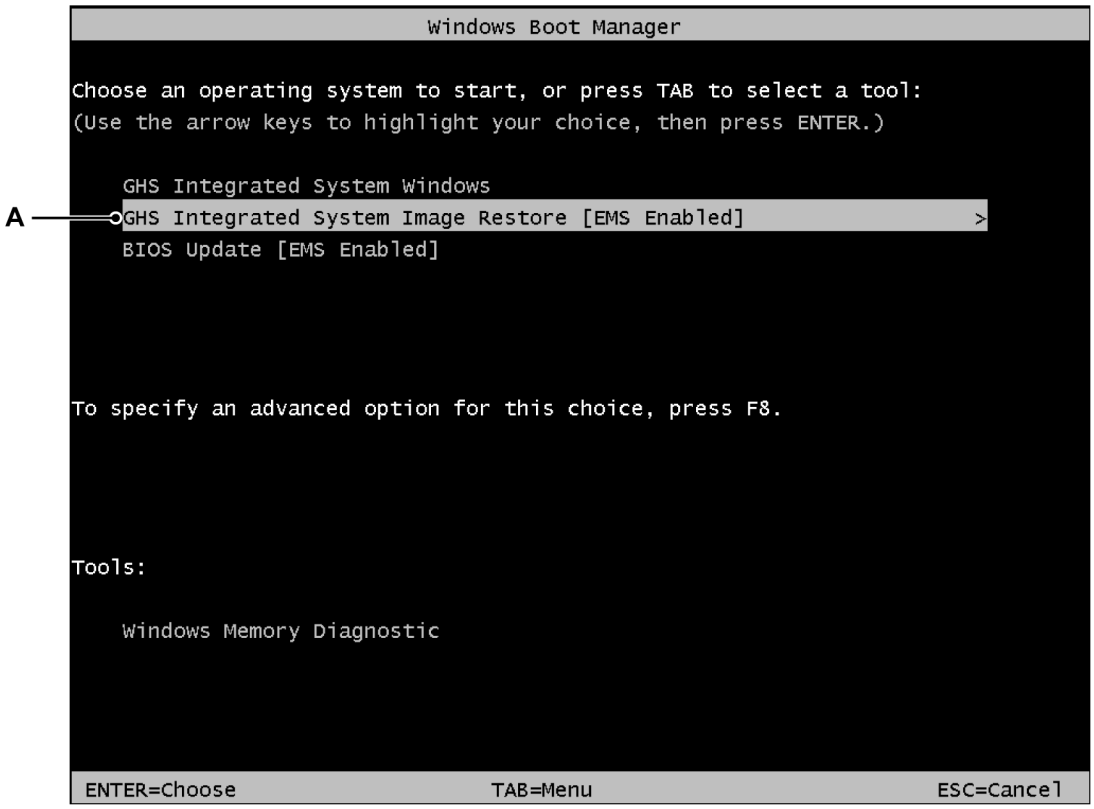


Figure G.4: Windows Boot Manager - Restore selection

A GHS Integrated System Image Restore

HINT/TIP

If the options listed in Figure G.4 do not appear the GHS integrated system drive is either corrupted or replaced with a new empty system drive.

See appendix "Recovery partition creation" on page 768 to recreate the recovery partition as a starting point to rebuild the system drive.

G.2.2 Starting image restore

1 The system starts the image restore process.
Check the **I understand the consequences** box and select **Yes**.

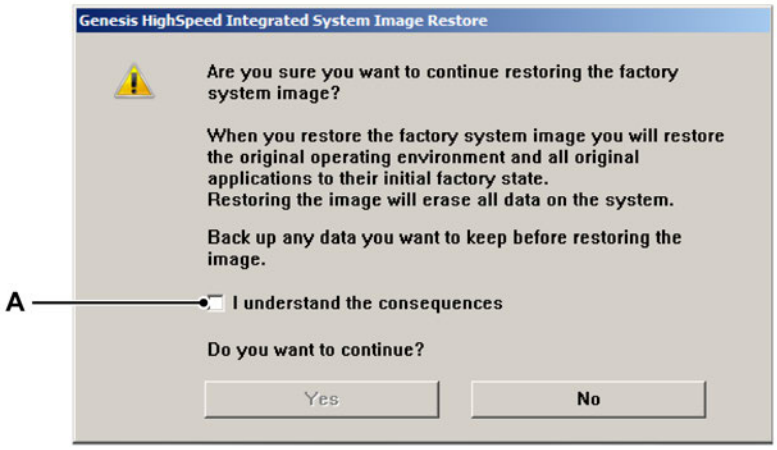


Figure G.5: Confirmation to start image restore and erase data

A I understand the consequences

2 The image is applied to the Solid State Drive. The window shows the progress.

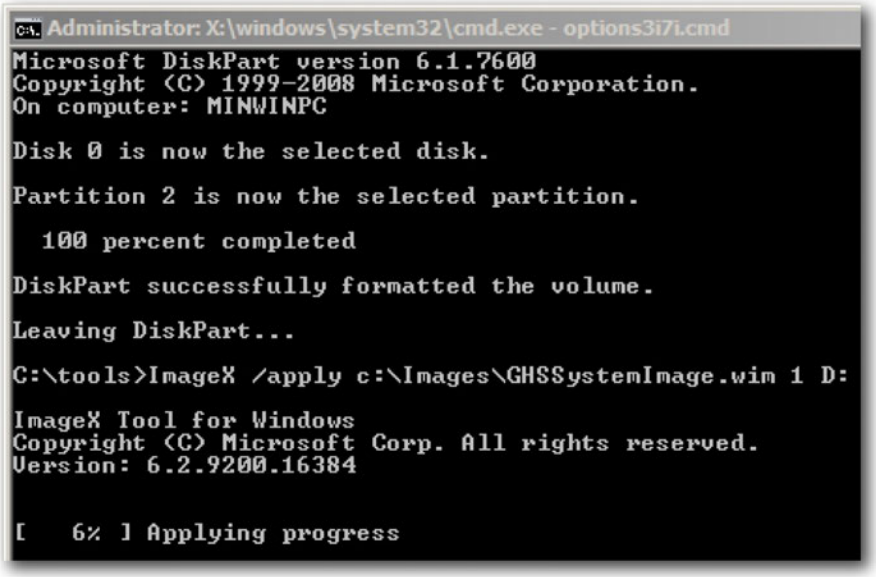


Figure G.6: Image restore progress

3 After the image has been applied, a key must be pressed to restart the system. Press any key that the process is complete when prompted.

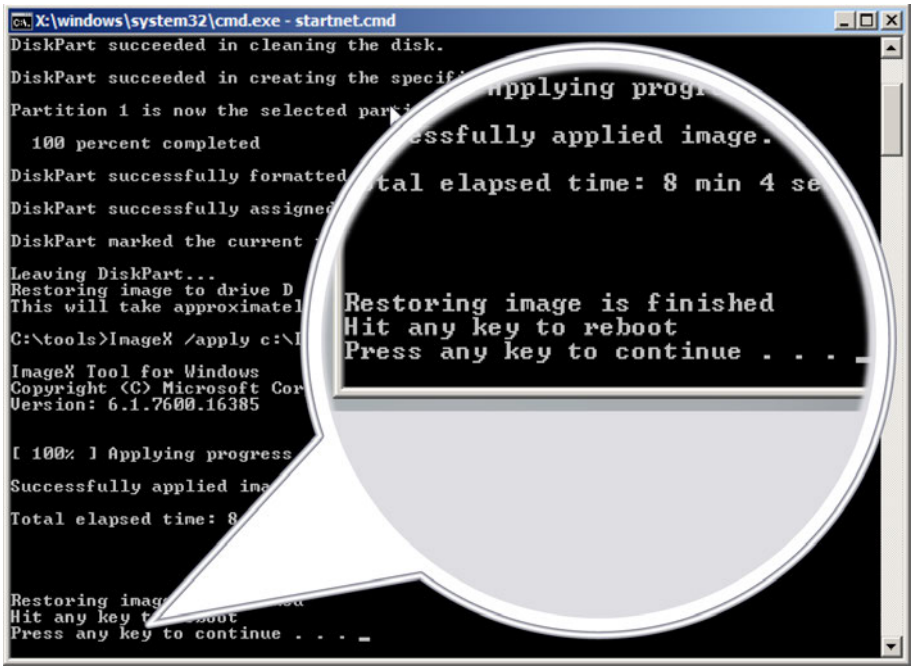


Figure G.7: Image restore completion

4 After the reboot is complete, the following screen appears temporarily:

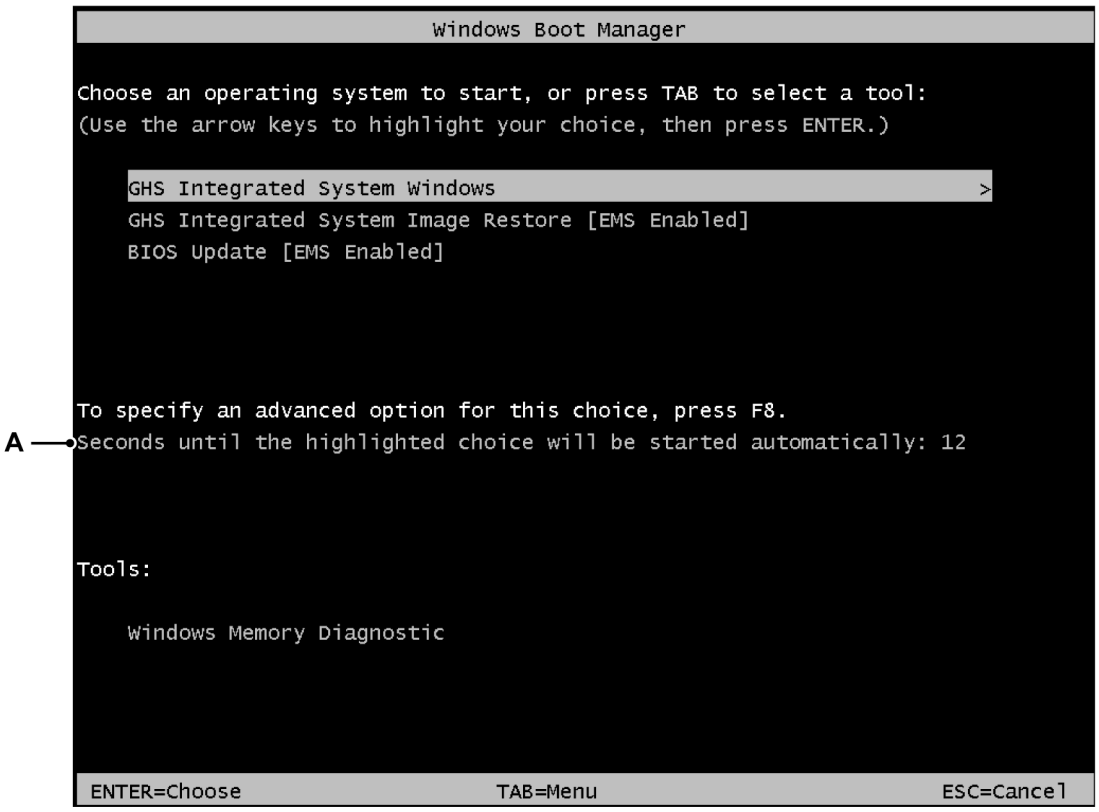


Figure G.8: Windows Boot Manager - Automatic boot

A Time remaining until automatic boot starts

Note *No selection is required. The system automatically boots to the GHS Integrated system Windows® and starts the initialization of the restored image.*

WARNING

Do not power off the mainframe while the system is installing.

G.2.3 Image restore phase 1 - Installing devices

The installation first initializes the system and scans for devices.

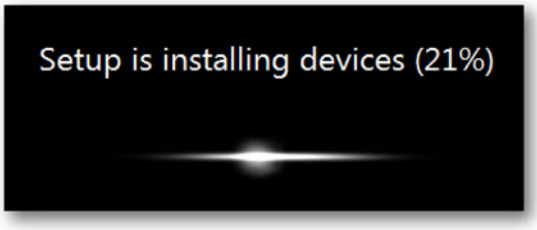


Figure G.9: Image restore phase 1 progress

After the devices have been installed, the system reboots. The boot menu appears (see Figure G.9) for 30 seconds before it continues. No selection is required; simply wait.

Note *Windows® 10: System doesn't reboot but continues with "Image restore phase 2 - Measuring video performance" (see chapter below).*

G.2.4 Image restore phase 2 - Measuring video performance

The system is prepared for first use and the video performance is tested.

Note *Windows® 10: Phase 2 is now getting ready. The system has installed the devices and is installing software components. After installing the components, the system reboots.*

Figure G.10: Image restore phase 2 progress

After checking the video performance, the system reboots. The boot menu (see Figure G.10) appears for 30 seconds again. No selection is required; simply wait.

IMPORTANT

The “Image restore phase 3 - Windows® welcome” process is different between Windows® 7 and Windows® 10. For more information about the Windows® 10 process, please refer to "Image restore phase 3 - Windows 10 welcome" on page 741.

G.2.5 Image restore phase 3 - Windows 7 welcome

1 Windows® 7 Language

Select the appropriate user interface language and click **Next**.

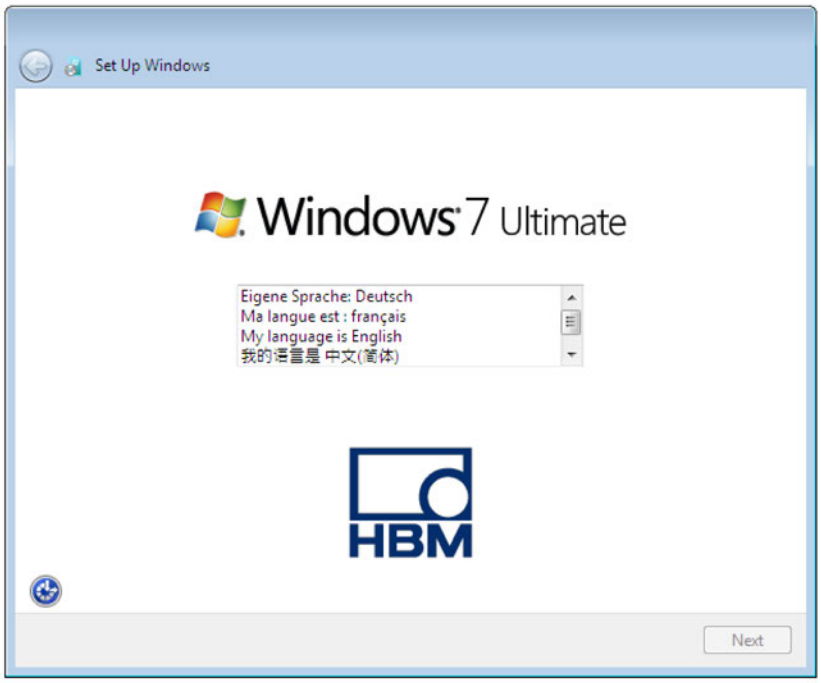


Figure G.11: Language selection

2 **Regional and keyboard**
Select the appropriate **Country or region**, **Time and currency** and **Keyboard layout** and click **Next**.

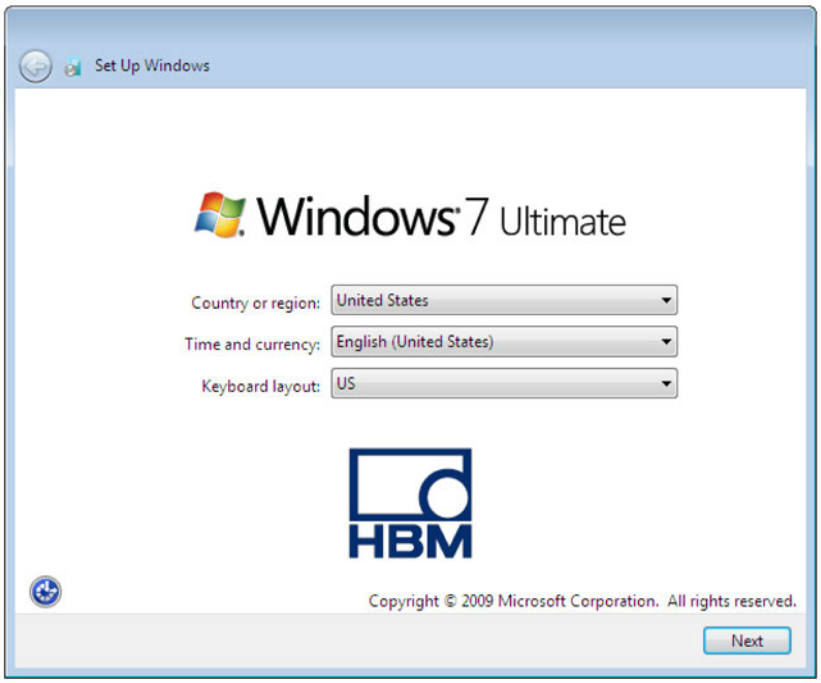


Figure G.12: Region and keyboard

3 Computer name

Enter the computer name.

HBM uses your system's serial number as a factory default setting. The serial number can be found near the power inlet of your system (see Figure G.13).

Figure G.13: GEN3i serial number

A Location of GEN3i serial number

Once the computer name has been entered correctly, click **Next.**

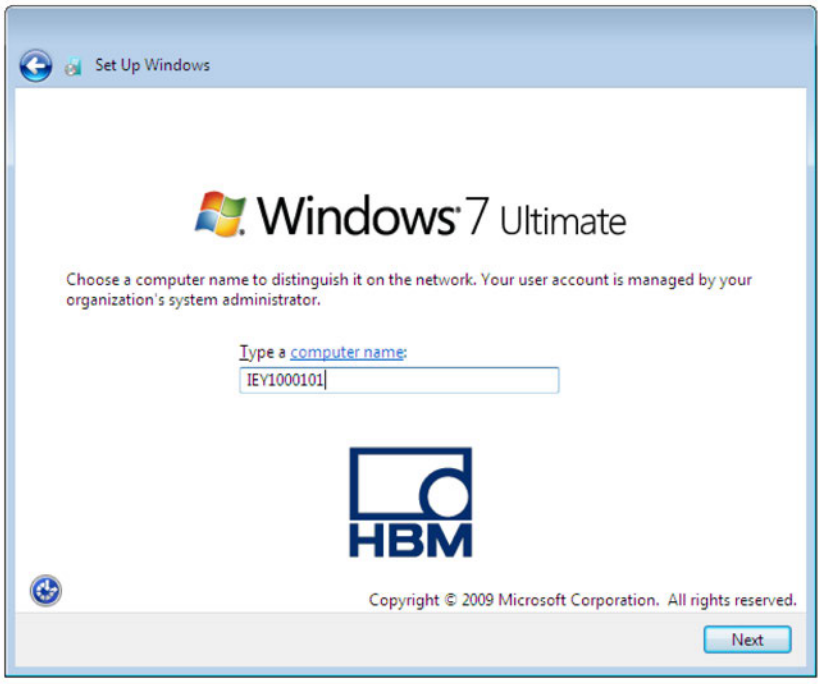


Figure G.14: Computer name

4 Windows product key

The Windows® product key can be found on the Microsoft® sticker on the top or back of the instrument. Locate this sticker and enter the Windows® product key.

The Windows® product key that has just been entered needs to be activated. Even if no internet connection is available during this step, Windows® be installed and work correctly for the next 30 days.

The check mark "Automatically activate Windows when I'm online" should be selected. As soon as Windows® detects a working internet connection, the Windows® product key is activated.

If an internet connection is not available within the next 30 days, alternative activation by phone or fax is offered when Windows® is completely configured.

When the information has been entered correctly, click **Next**.

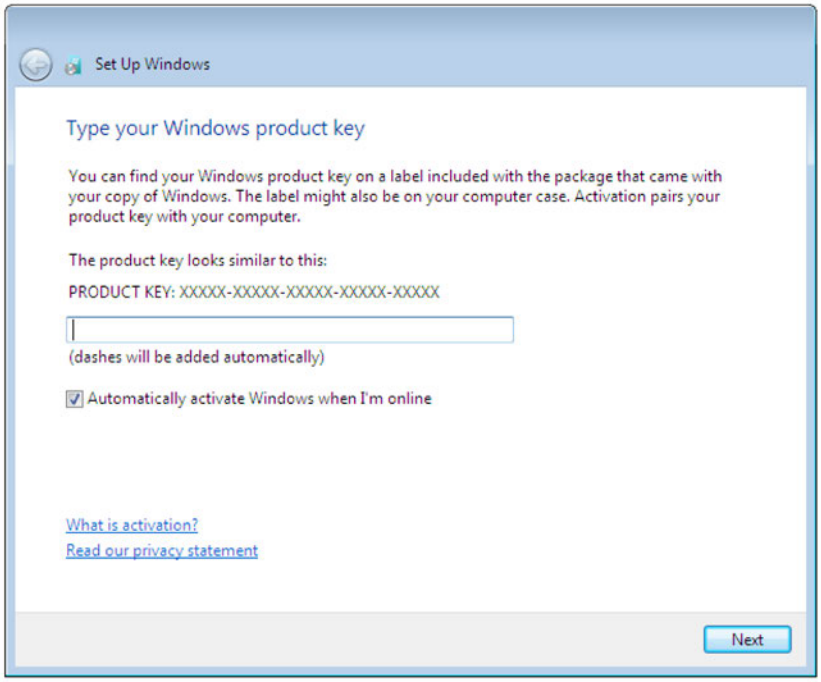


Figure G.15: Windows® 7 product key and activation

5 Microsoft® software license terms

Carefully read the Microsoft® software license terms. Check the **I accept the license terms** box and click **Next**.

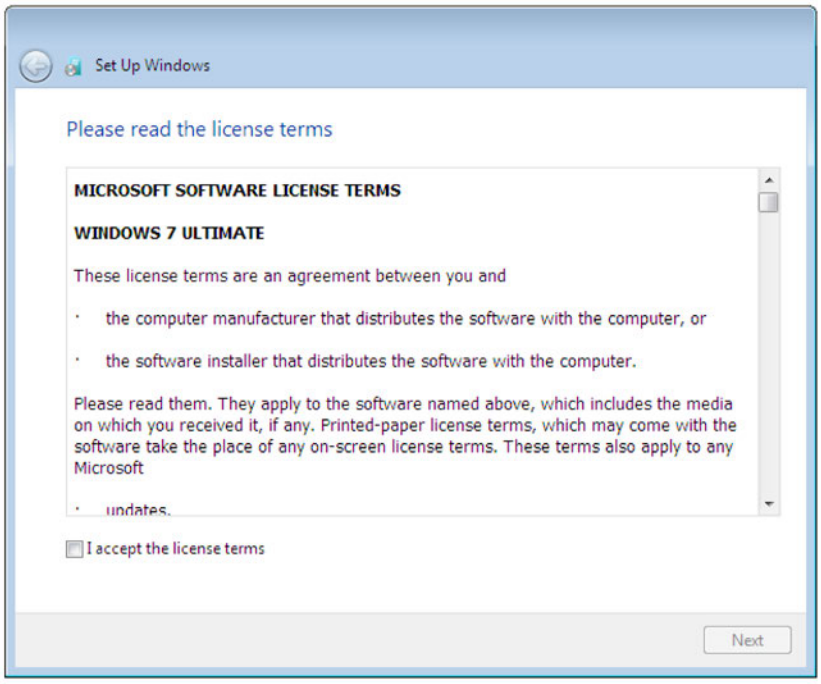


Figure G.16: Microsoft® license terms

6 Time and date settings

Select the correct time zone that the system will be used in and adjust the date and time. Click **Next**.

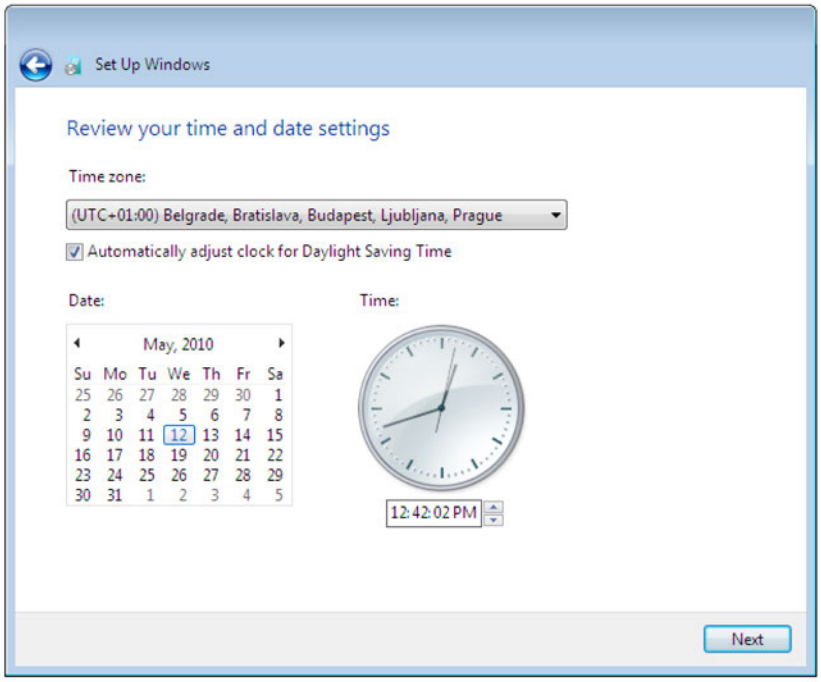


Figure G.17: Time and date settings

WARNING

Using the incorrect time zone settings results in incorrect date and time information in the recordings.

7 Join wireless network

Wireless networks can be configured during normal system operation. Select **Skip** to skip the wireless network configuration.

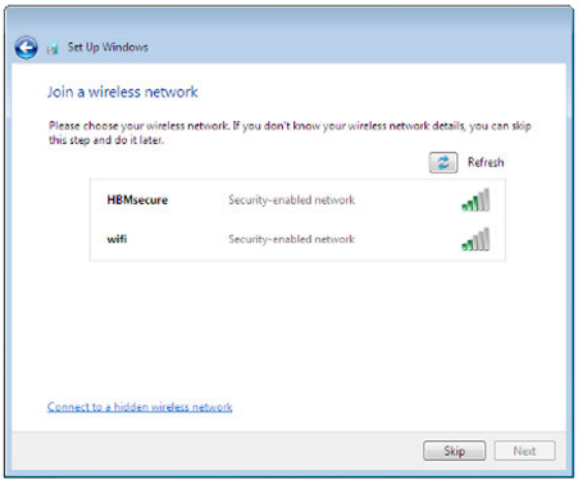


Figure G.18: Wireless network setup

8 Finalizing

This screen appears while Windows® 7 finalizes the setup.

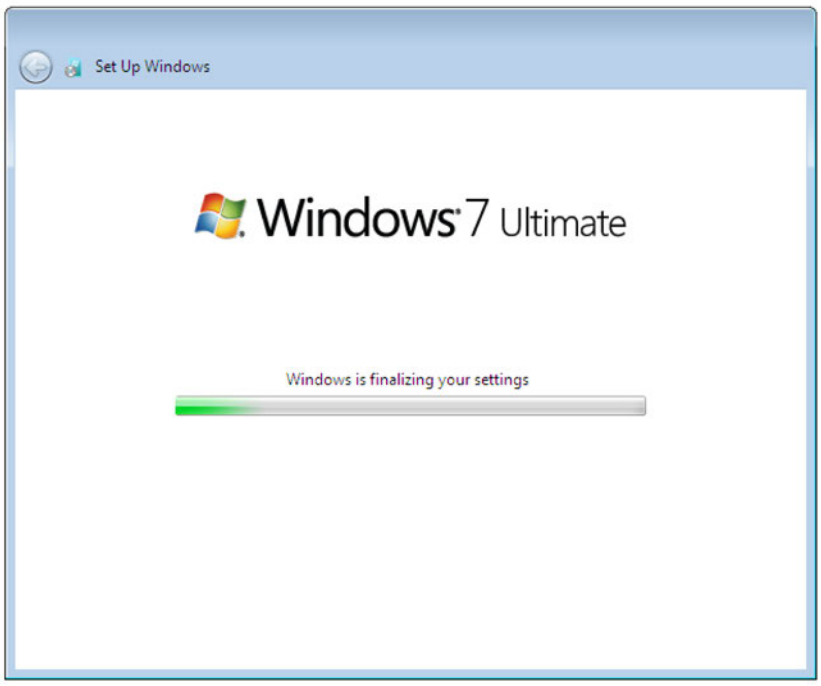


Figure G.19: Windows® 7 finalization progress status

9 Ready

When the settings have been finalized, the Windows® 7 Welcome screen appears:

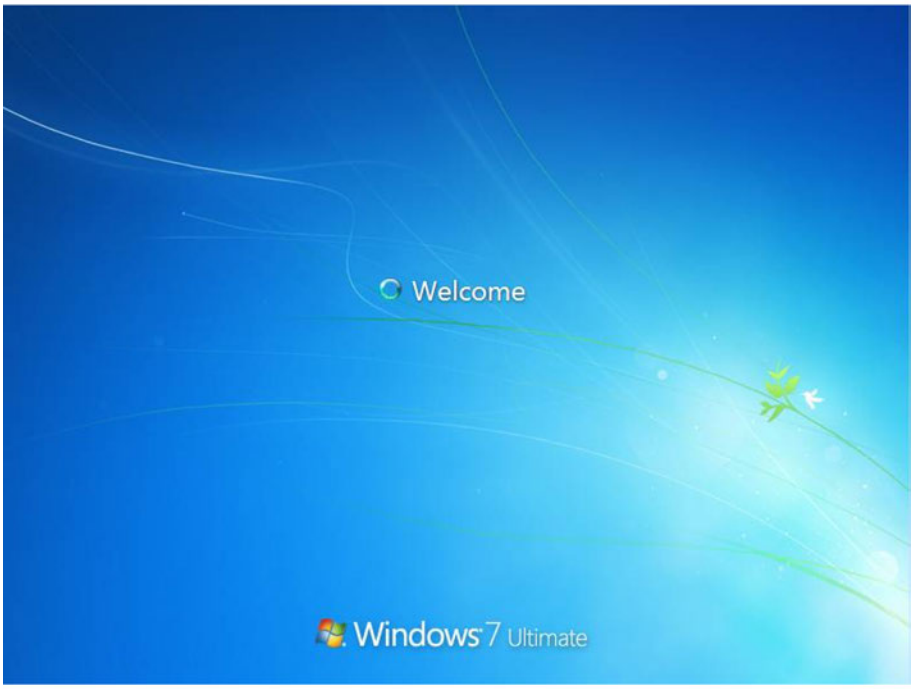


Figure G.20: Windows® 7 Welcome screen

10 When the installation is finished, the touch screen calibration starts automatically. For more information, please refer to "Touch screen calibration" on page 751.

G.2.6 Image restore phase 3 - Windows 10 welcome

1 Windows® 10 language

Select the appropriate user interface language and click **Next**.

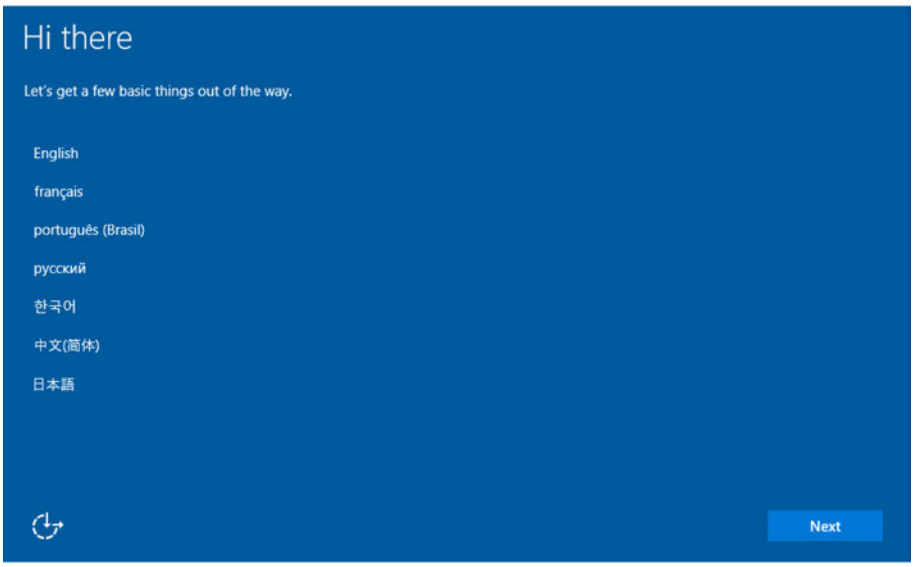
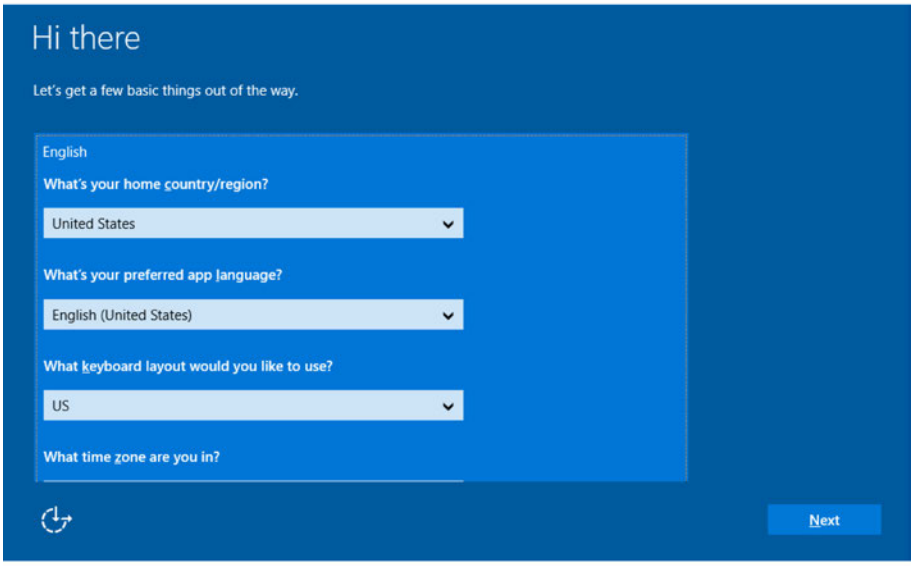


Figure G.21: User interface language selection

2 **Country/region, application language, keyboard**
Select the appropriate **country or region**, **app language** and **keyboard layout** and click **Next**.



3 **Windows® product key**

The Windows® product key can be found on the Microsoft® sticker on the top or back of the instrument. Locate this sticker and enter the Windows® product key.

If the system was previously running an activated version of Windows® 10 and the PC hardware has not changed, it is possible to select **Do this later**. The activation process will contact the Microsoft® activation servers to check for an existing activation and automatically activate the system.

As soon as Windows® detects a working internet connection, the Windows® product key is activated.

If an internet connection is not available within the next 30 days, alternative activation by phone or fax is offered when Windows® is completely configured.

When the information has been entered correctly, click **Next**.

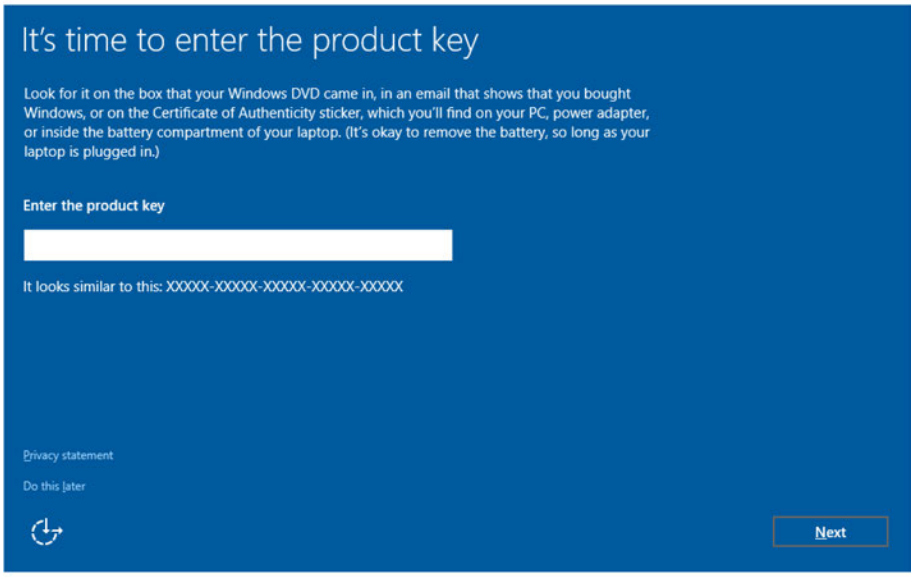


Figure G.22: Windows® product key and activation

4 **Microsoft® software license terms**

Carefully read the Microsoft® software license terms. Click **Accept** to continue.

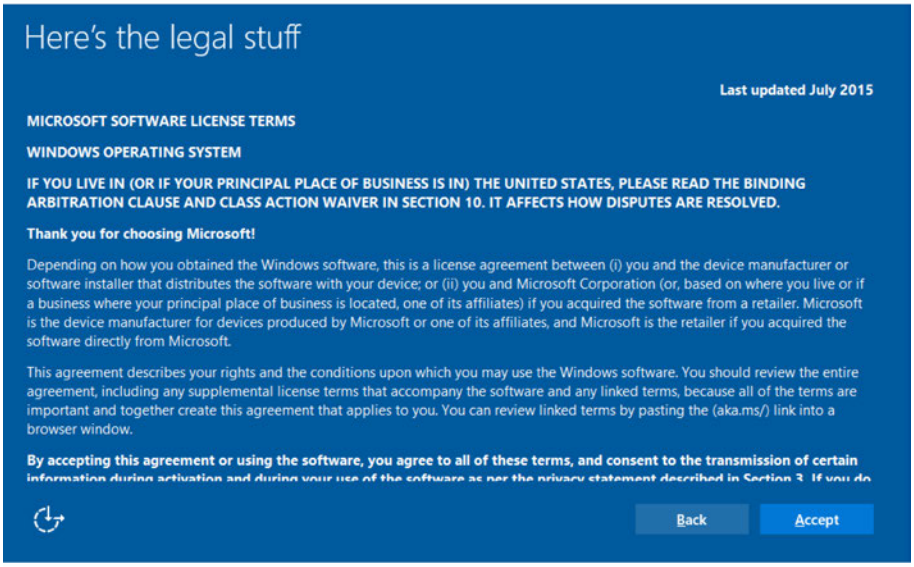


Figure G.23: Microsoft® license terms

5 Finalizing

This screen appears while Windows® 10 finalizes the setup.

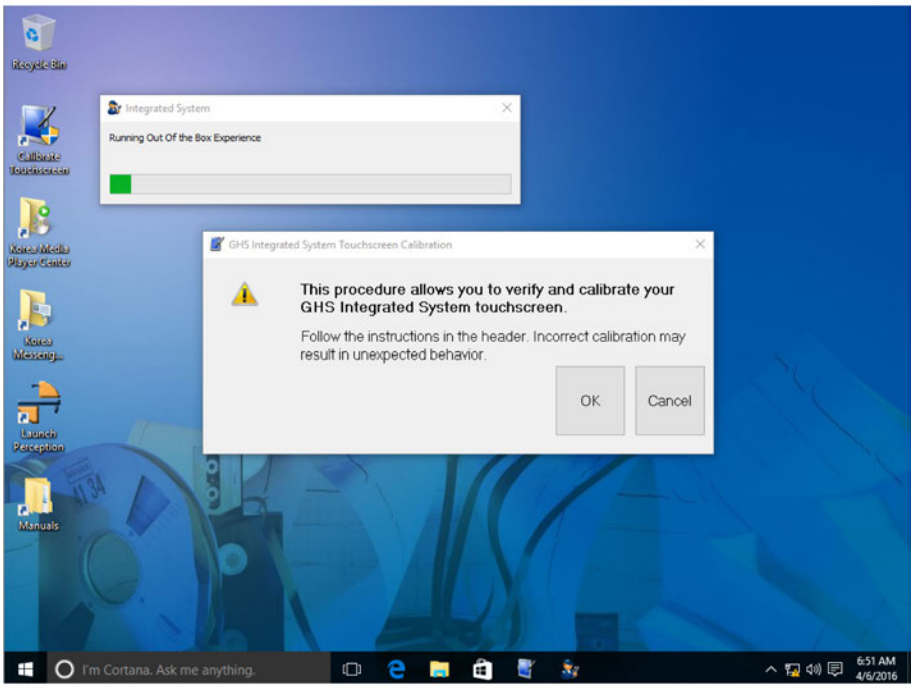
Figure G.24: Windows® 10 finalization

6 Ready

When the settings have been finalized, the Windows® 10 Welcome screen appears:

Figure G.25: Windows® 10 Welcome screen

7 When the installation is finished, the touch screen calibration starts. The calibration asks for a confirmation before the process starts. For more information, please refer to "Touch screen calibration" on page 751.



After the touch screen calibration the system reboots and Perception automatically starts after signing in.

G.2.7 Potential problems after restore

After running the GHS Integrated system image restore, the following problem can occur (see Figure G.26).

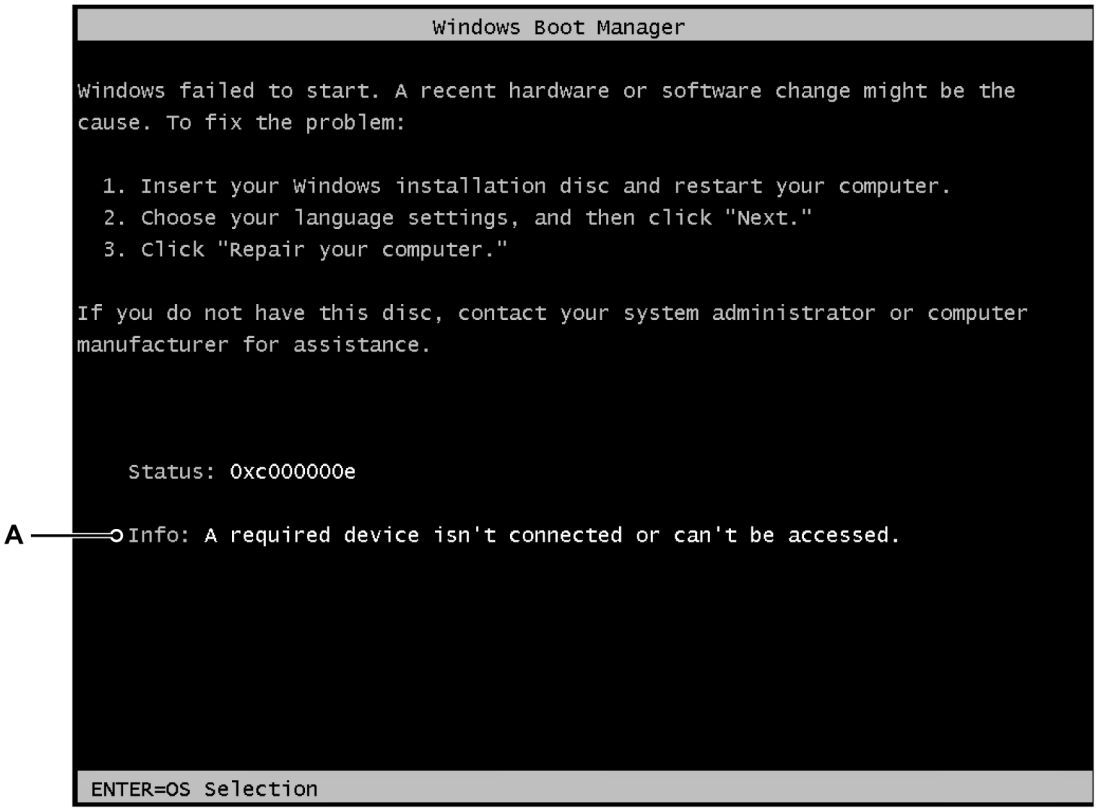


Figure G.26: A required device is not connected or can not be accessed

A Device is not connected - error message

This problem is typically caused after a Windows® 10 upgrade and later restoring the Windows® 7 system image. Windows® 10 modified the bootloader of your drive and the image did not restore the original bootloader.

This problem can be fixed by performing the following steps:

1. Using a Windows PC, download the repair file form the HBM website: www.hbm.com/fileadmin/mediapool/support/genesishighspeed/GEN3i/BootMenuRecovery.zip
2. Extract the zip file to the USB drive.

3 (Re-)boot the GHS system and select the Image Restore option in the boot menu.

Note *The blue USB ports are USB 3.0 ports and do not work in this procedure. Make sure keyboard and mouse are in a black USB port.*

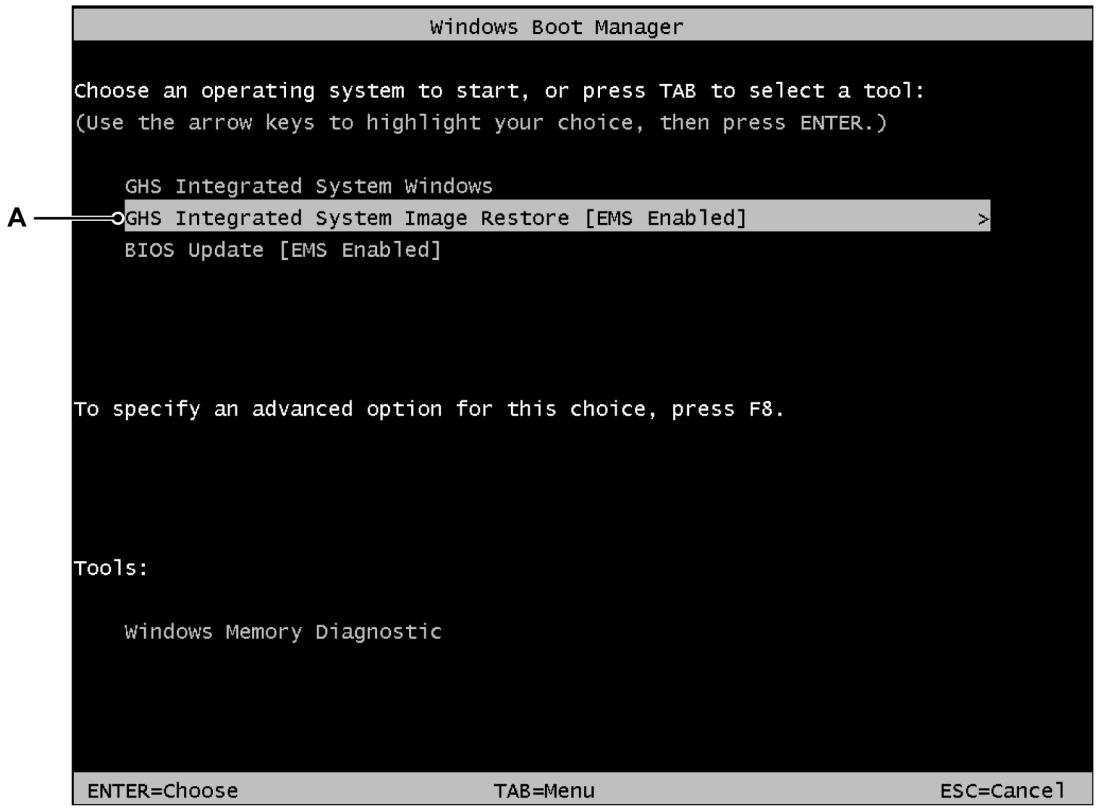


Figure G.27: Windows Boot Manager - Restore selection

A GHS Integrated System Image Restore

4 When the message about the consequences of the restore appears (see Figure G.28), press the TAB key to check that the keyboard is recognized (this can take a few seconds).

5 Press the TAB key until the **No** button is highlighted.
Press the shortcut **Ctrl+Shift+Spacebar**. When available press the **No** button.

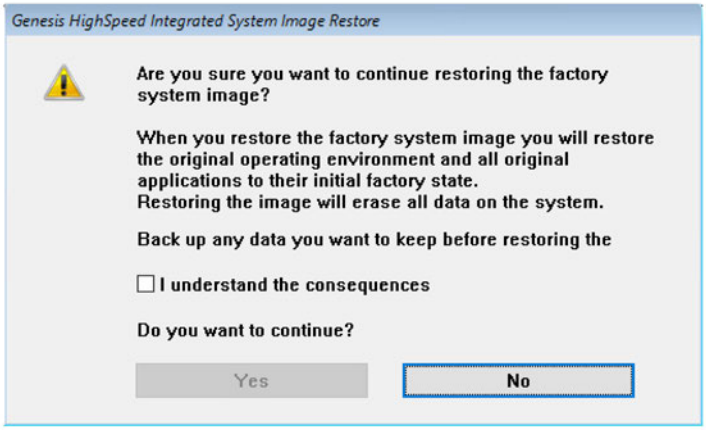


Figure G.28: Genesis HighSpeed Integrated System Image Restore

6 Put the USB stick in a black or white (front) USB port.
7 Find the drive letter which is assigned to the USB stick by typing the following commands:

“E” (usually “E” or “F”).

Note *If you get the message “The system cannot find the drive specified” continue with the next letter in the alphabet until the USB device is found.*

8 Type “FixBootMenu” to repair the bootloader.
9 Wait until the process completes and reboot the system.

G.3 Touch screen calibration

The following startup link is available on the Windows® desktop.

Figure G.29: Calibration touch screen startup

HINT/TIP

The touch screen calibration can also be started manually whenever re-calibration is required.

IMPORTANT

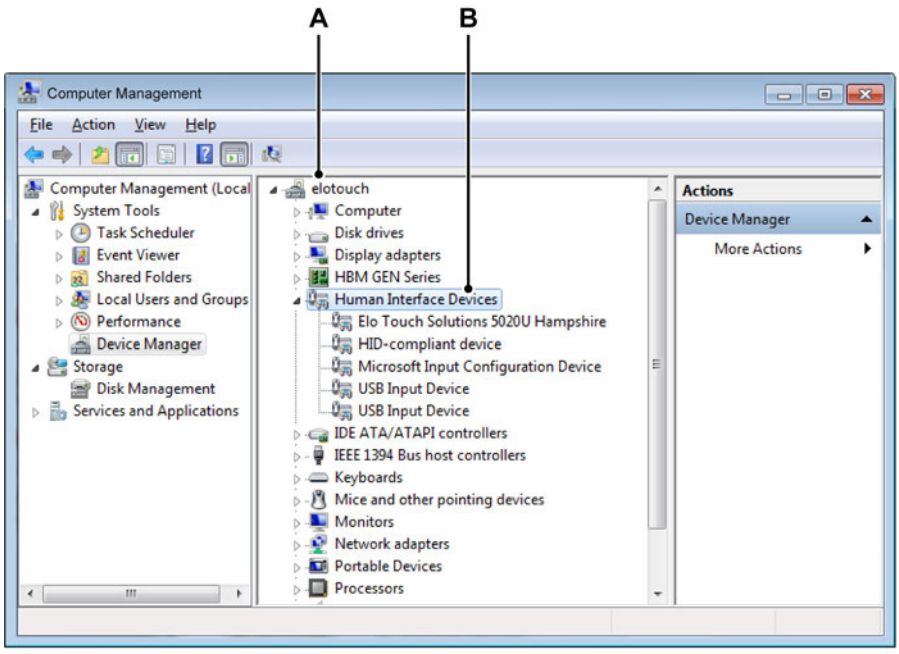
The touch screen calibration procedure depends on the type of touch screen.

GEN7i always comes with an ELO touch screen. GEN3i/GEN3iA come with either a WACOM touch screen or an ELO touch screen. The **Calibrate Touchscreen** shortcut on the Windows® desktop automatically selects the correct calibration procedure for the touch screen installed.

To verify the type of touch screen installed in GEN3i/GEN3iA manually, take the following steps:

1 Go to **Start Control ► Panel Hardware and Sound ► Device Manager**

2 Select the **Human Interface Devices**



A ELO touch screen installed

B WACOM touch screen installed

3 If an **ELO Touch solutions** device is listed, the system has an ELO touch screen.

4 If a **HID-Compliant device** is listed, the system has an ELO WACOM touch screen.

a Open the properties of the **HID-Compliant device** by right-clicking the item.

b In the **Details** tab, select the Hardware Ids propterty.

c The WACOM device starts with **HID\VID_056A**

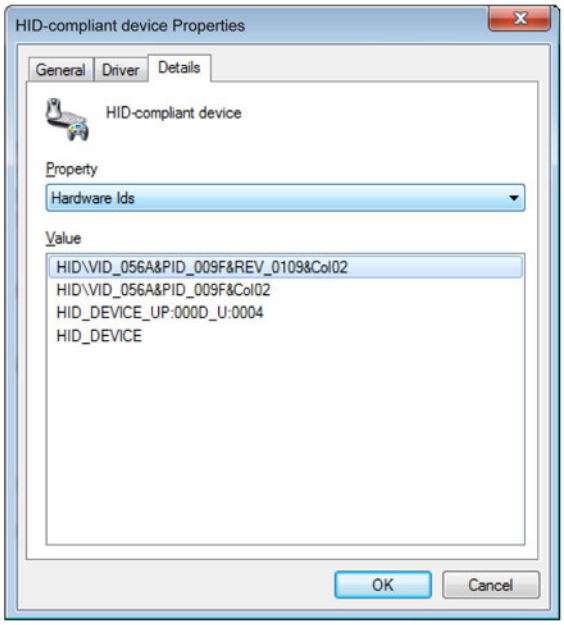


Figure G.30: To check which type of touch screen is installed

G.3.1 WACOM touch screen

Note *Be as accurate as possible when tapping with your finger. Any deviation from the indicated point will result in misaligned touch screen operation.*

The first part of the utility tests for possible jitter caused by external radiation source.

Note *For the screen operation to work more accurately, make sure that the user is connected to a conductive ground connection.*

1 Use your finger to tap somewhere on the screen and hold still until the countdown in the header has finished.
The countdown takes approximately 5 seconds. The utility may interpret finger movements during the countdown as a power source distortion. Therefore, moving your finger during the countdown will cause the test to fail.

Note *If any finger movement happens during this process, please exit the application and start it again.*

Figure G.31: Touch screen calibration (Step 1)

If the test failed, a warning dialog appears. This dialog will also allow you to redo the test.

Note *Initial test failures mostly occur due to external influences.*
Check the conductive ground connection of the user. Use a wrist-wrap or simply grab the protective earth pin of the system and repeat the test.
If the test passes now, an external radiation source with a frequency of approximately 270 kHz is present in the environment, causing the touch screen to detect misaligned touches.
Remove the external radiation source or operate the system in another area away from the radiation source.
If you cannot remove the radiation source or operate the system in a different area, using the touch screen will be very difficult. The system will detect misaligned touches and respond with unexpected reactions.

Figure G.32: Touch screen calibration - Failure dialog (step 2 optional)

A Next step

B Exit program

C Redo verification

The failure dialog has a red caption. A red line indicates that the movement was detected during the test.

- Select **Redo Verification** to restart the jitter detection.
- Select **Exit Program** to stop the touch screen validation. When exit is selected, no calibration adjustment has been performed.
- Select **Next Step** to continue to the calibration steps. Do not progress to the next step if this step fails.

2 Twenty (20) points need to be tapped on a grid. The tap positions are indicated on the screen by a crosshair.

The crosshair starts at the top left point, moves from left to right and then to the next row of points below until all points have been tapped. A margin is applied to detect whether the tap is in the immediate area around the point that is expected to be tapped.

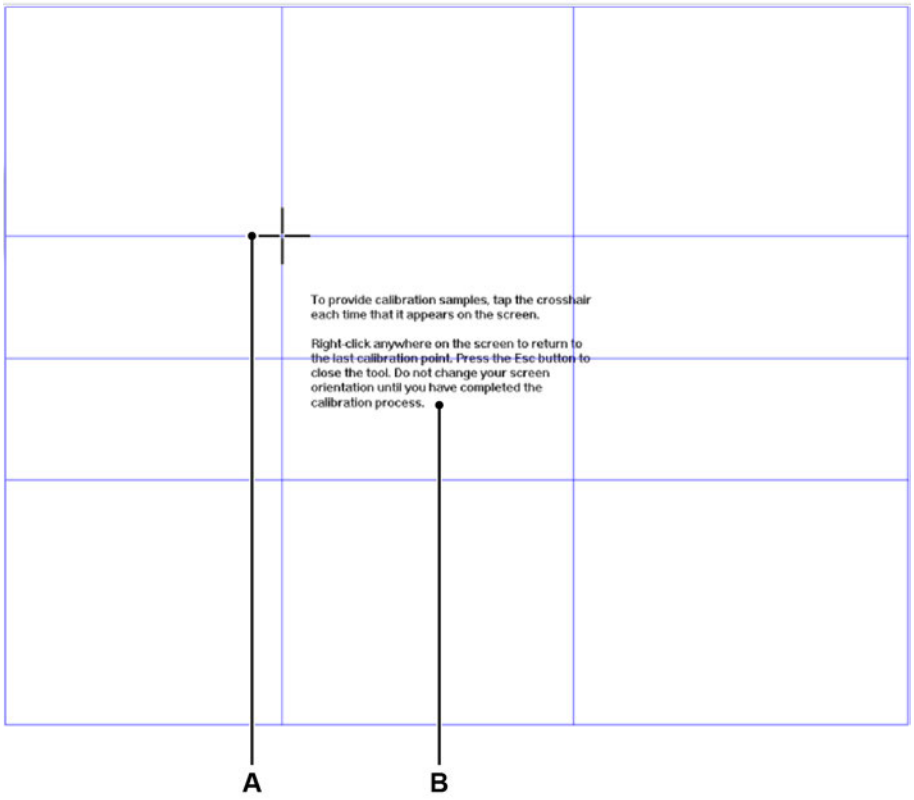


Figure G.33: Touch screen calibration - Grid with crosshair (step 3)

A **Crosshair** Moved from start point in the top left-hand corner.

B **Description** To provide calibration samples, tap the crosshair each time that it appears on the screen.
Right-click anywhere on the screen to return to the last calibration point. Press the Esc key to close the tool. Do not change the screen orientation until the calibration process is completed.

3 After all points on the grid have been tapped, the calibration data can be saved. If the calibration was successful, select **Save** to save the new data.

Note *The calibration assumes that the factory calibrated touch screen is correct for the touch screen to operate properly. If the tap test continues to fail, contact HBM service to redo the factory calibration using the Wacom utility.*

4 After the calibration, a small verification of the new calibration data is shown to check whether the new verification data is meaningful and to make sure that the data will not cause problems using device:

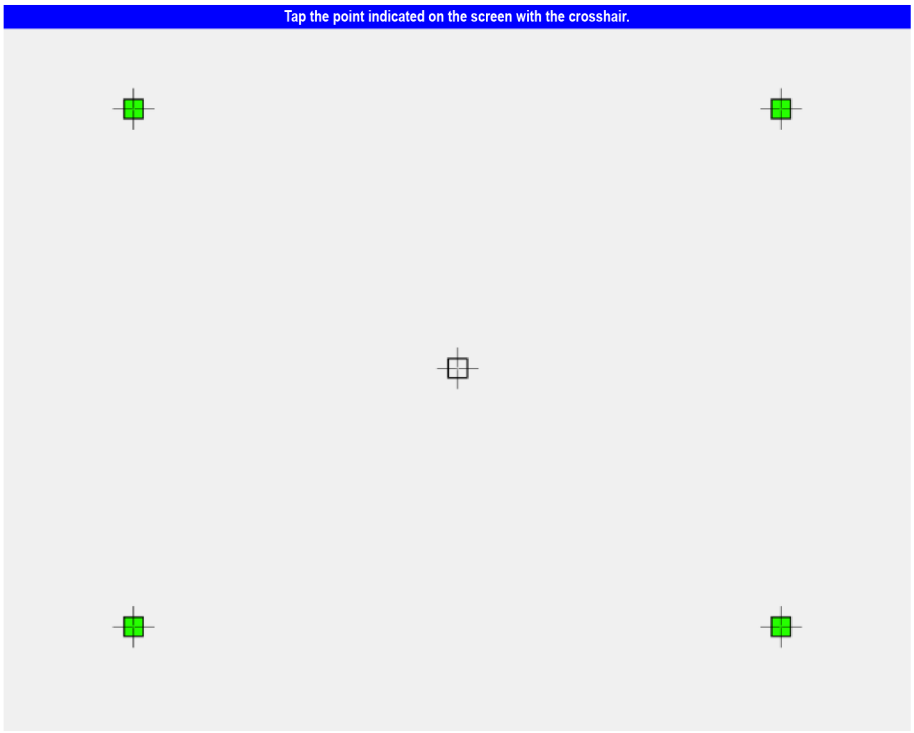


Figure G.34: Touch screen calibration verification (step 5)
Five (5) rectangles appear on the screen. Tap each rectangle individually. If tapped accurately, the rectangle turns green.

5A If a rectangle is tapped incorrectly (either by accident or due to an incorrectly calibrated touch screen), the rectangle turns red. A red circle indicates the position that really was tapped.

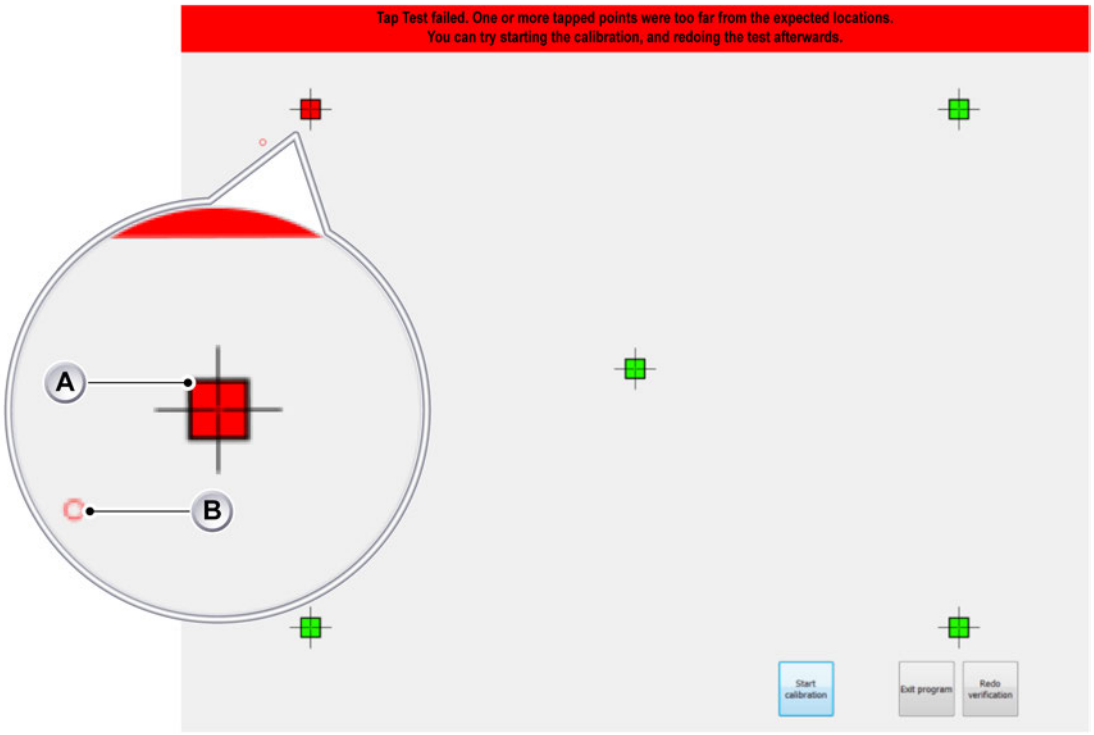


Figure G.35: Touch screen calibration - Missing rectangle

A Missed tap point

B Detected touch position

5B When all rectangles have been tapped correctly, the screen looks like this:

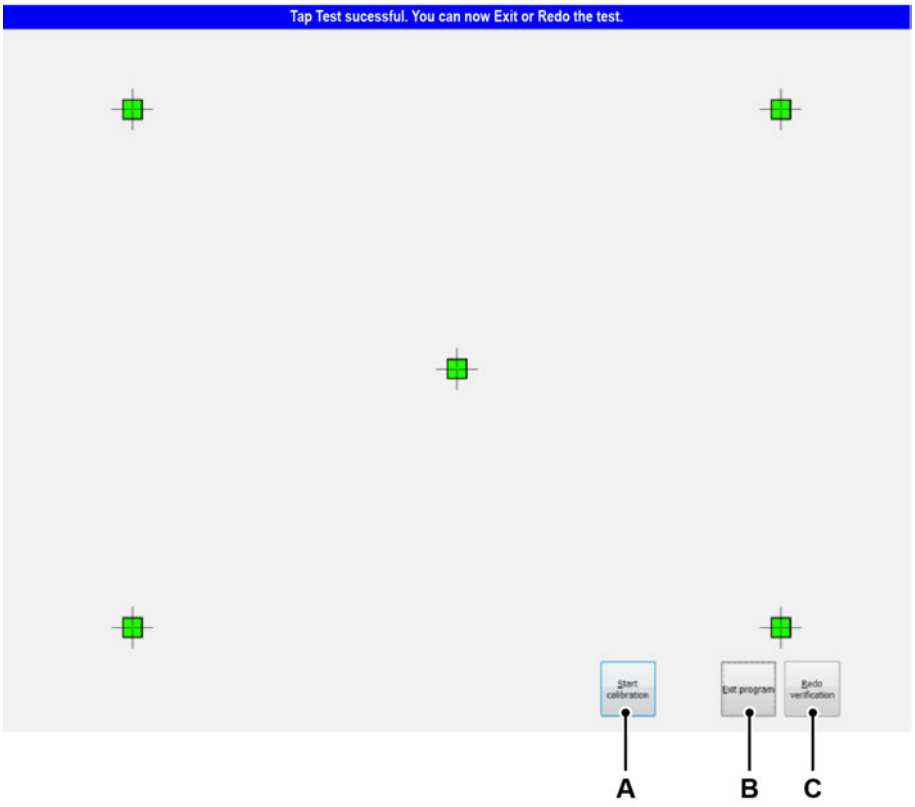


Figure G.36: Touch screen calibration - Final (step 5)

A Start calibration

B Exit program

C Redo verification

Options to continue:

A **Start calibration**
Redo the ccalibration by clicking the **Start calibration** button.
This action would be appropriate if the tap test failed when the center of rectangle had been tapped correctly but it turned red anyway. Before recalibrating, please complete the tap test at least twice.

B **Exit program**
Exit program, this will exit the application.
This action would be appropriate if the tap test passed (blue caption, all rectangles are green).

C Redo verification
Redo the tap test by selecting the **Redo Verification** button.
This selection would be appropriate if the test had failed and a rectangle had accidentally been missed or if this had been the first time the tap test failed.

This completes the GEN3i reimage process.

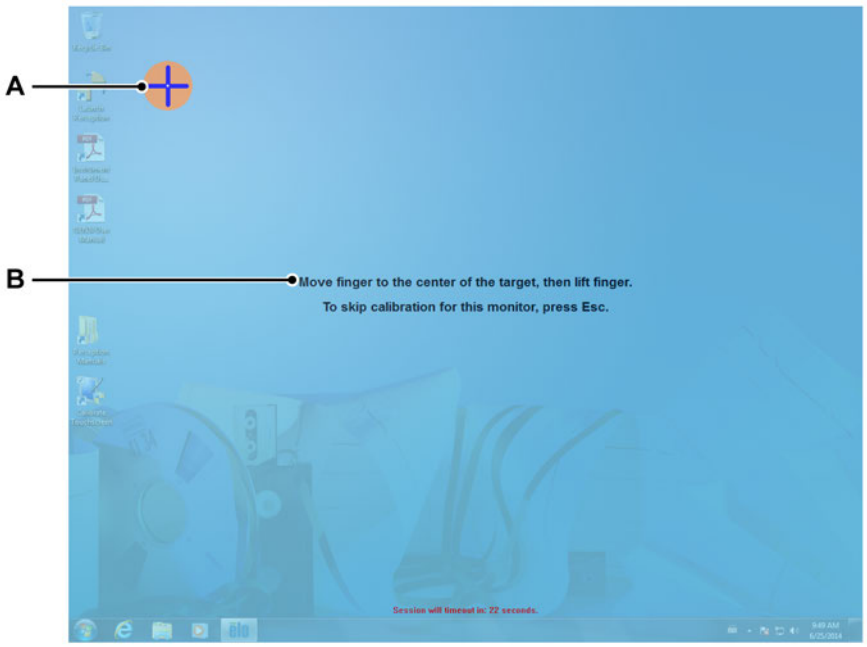
G.3.2 ELO touch screen

Note *Be as accurate as possible when tapping with your finger. Any deviation from the indicated point will result in misaligned touch screen operation.*

The calibration process can be redone to make adjustments for personal usage. Three (3) points need to be tapped on the screen. The tap positions are indicated on the screen with a circle that has a blue crosshair.

After starting the calibration process, follow the instructions listed on the screen. Press the Esc key to cancel the calibration process at any time. No changes are made when this process is canceled.

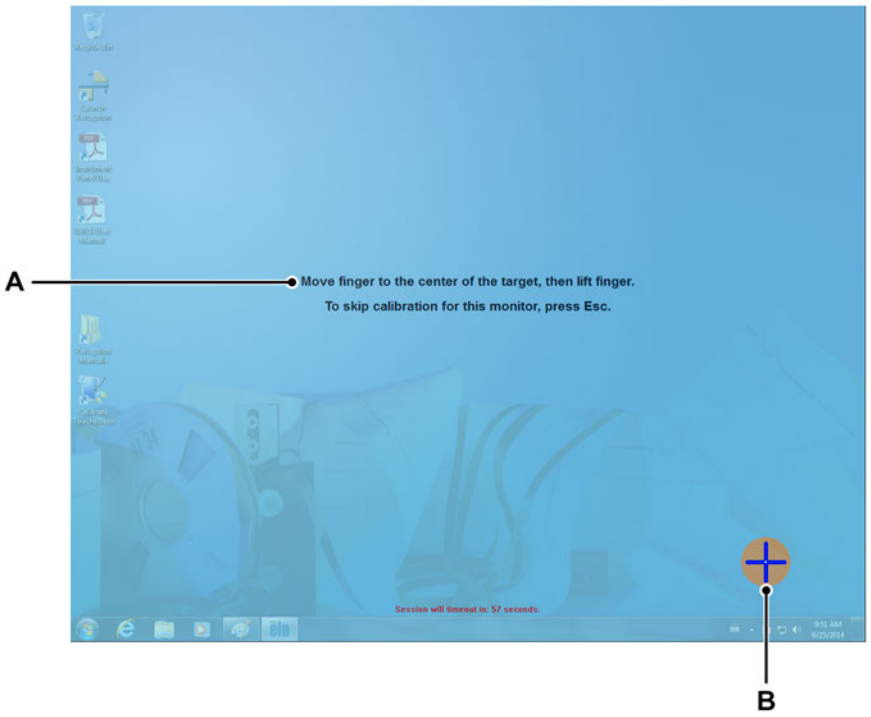
1 The first crosshair appears in the upper left-hand corner of the screen.



A **Crosshair** First crosshair for calibration.

B **Description** Move your finger to the center of the target, then lift your finger.
To skip calibrating for this monitor, press Esc.

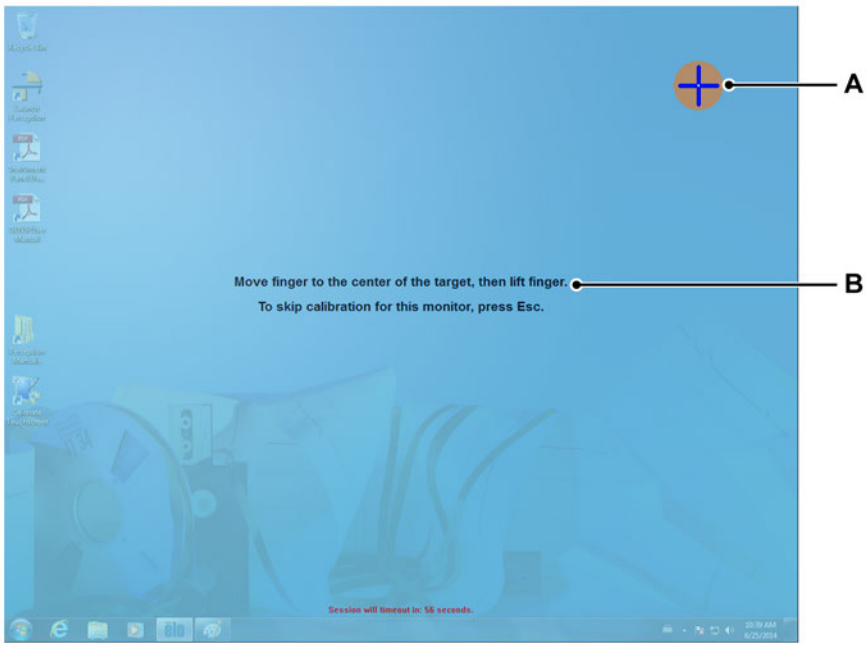
2 After tapping the first crosshair, the second crosshair appears in the bottom right-hand corner of the screen.



A **Description** Move your finger to the center of the target, then lift your finger.
To skip calibrating this monitor, press Esc.

B **Crosshair** Second crosshair for calibration.

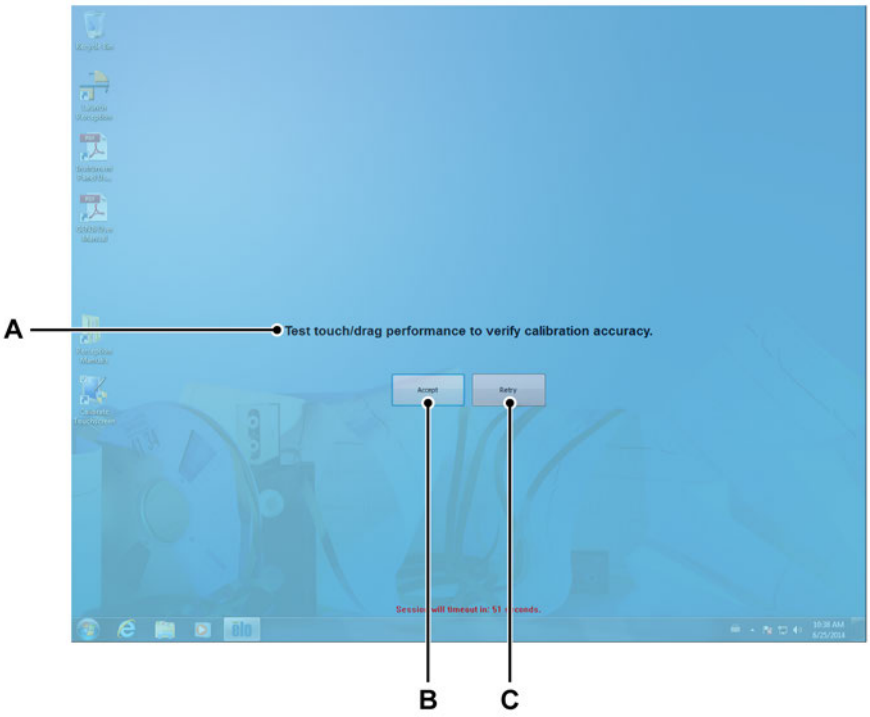
3 The final crosshair appears in the upper right-hand corner of the screen.



A **Crosshair** Third crosshair for calibration.

B **Description** Move your finger to the center of the target, then lift your finger.
To skip calibrating this monitor, press Esc.

4 After all points on the grid have been tapped, the calibration can be verified by tapping and dragging on the screen.



A **Description** Test touch/drag performance to verify calibration accuracy.

B **Accept** Calibration process

C **Retry** Calibration process

New calibration data is only stored after the **Accept** button has been clicked.

G.4 Backing up the recovery partition

HINT/TIP

For archive reasons a bootable USB stick which contains the original image of the systems recovery partition can be created. Restore of the original Recovery image might be needed because the system drive failed and/or the partition was damaged.

The archive copy can also be used to restore the system without the support of HBM service. A copy of the system's recovery partition can always be ordered from HBM service. Even if no copy has been made and the system boot fails, HBM can supply a copy to restore the system to standard operation.

Prerequisites

The recovery image back-up requires a USB disk or stick with a least 16 GB of disk space.

Boot the GEN3i into standard Windows® operation. (If this fails, a back-up copy must already be available or requested from HBM service).

Creating the back copy

You can create a bootable USB stick that contains the original image of the system. You might need to restore the original image if Windows® does not start or if your system drive has failed.

In order to create an Integrated System Recovery USB disk, you need a USB stick that can store 16 GB or more.

1 Start the **Create Integrated System Restore USB** tool.

2 Go to **All Programs ► HBM ► Integrated System**

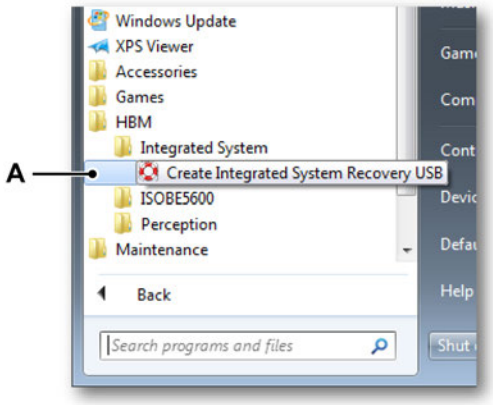


Figure G.37: Create Integrated System Recovery USB

A Create Integrated System Recovery USB option

WARNING

All data on the USB stick will be removed.

3 Select the drive that contains the USB disk and confirm with **Create**.

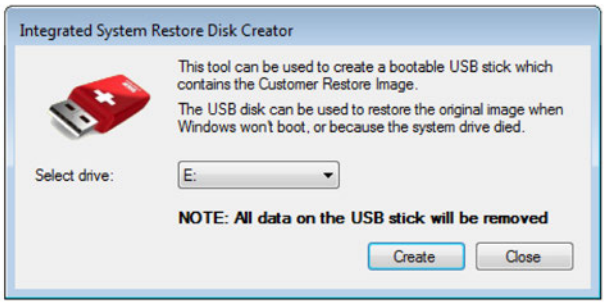


Figure G.38: Integrated System Restore Disk Creator dialog

The disk will be initialized and formatted and the recovery partition files will be copied to the USB disk.

A dialog (see Figure G.39) will show the progress and notify you when the disk creation process is finished.

Figure G.39: Formatting progress window

G.5 Recovery partition creation

To create/restore the recovery partition, a USB disk/stick with a back-up copy of the recovery partition is required. If this back-up copy has not been made or is lost, a copy can be ordered from HBM service.

G.5.1 Using the Integrated System Recovery USB Disk

1. Power off the mainframe.
2. Connect the mouse and keyboard.
3. Insert the USB disk in one of the USB 2.0 ports (The USB3.0 ports will not allow the restore process to finish correctly).
4. Power on the system and keep the **F7** function key pressed until the following dialog appears.

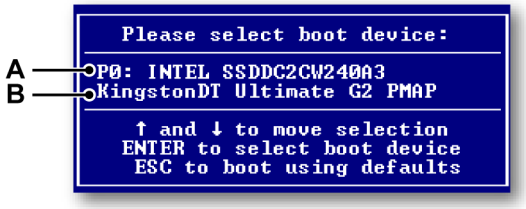


Figure G.40: Listed boot devices

A Name of installed Solid State Drive

B Name of USB disk/stick attached to your system

If the attached USB disk/stick does not appear, it was installed the system was powered on or the USB disk/stick is not bootable. Correct the issue, power off the system and restart from the beginning.

Use the arrow keys to select the USB disk/stick in the list of boot devices and press enter. The system will boot the recovery partition creation.

A disk partition inspection is started.

- If a recovery partition is detected, the **Recovery Partition Restore** is started. For more information, please refer to "Starting recovery partition restore" on page 770.
- If the Recovery partition is not detected, the **Recovery Partition Creation** is started. For more information, please refer to "Starting recovery partition creation" on page 769.

G.5.2 Starting recovery partition creation

If no recovery partition is found, the recovery partition creation is started.

WARNING

All data on the disk will be erased. This includes the GENSystem partition that contains Windows® installation and any previously recorded data.

Check the **I understand the consequences** box and confirm with **Yes**.

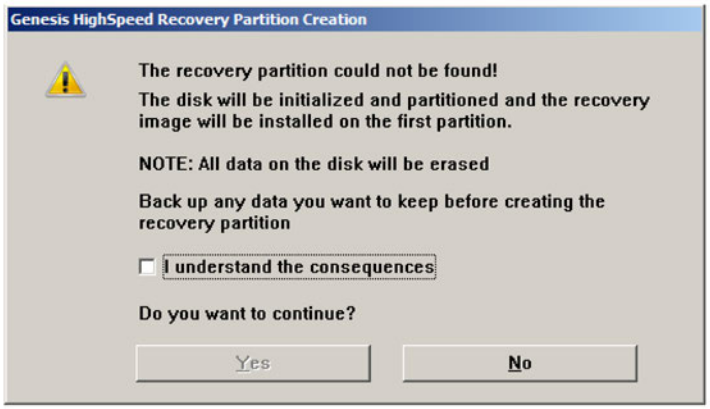


Figure G.41: Genesis HighSpeed Recovery Partition Creation

The recovery partition creation process initializes the disk and creates the partition. When the partition is created, the process automatically continues with the recovery partition restore steps.

G.5.3 Starting recovery partition restore

The recovery partition restore process starts with a confirmation request.

WARNING

All data on the recovery partition will be erased. The GENSystem partition that contains Windows® installation and any previously recorded data is not erased.

Check the **I understand the consequences** box and confirm with **Yes**.

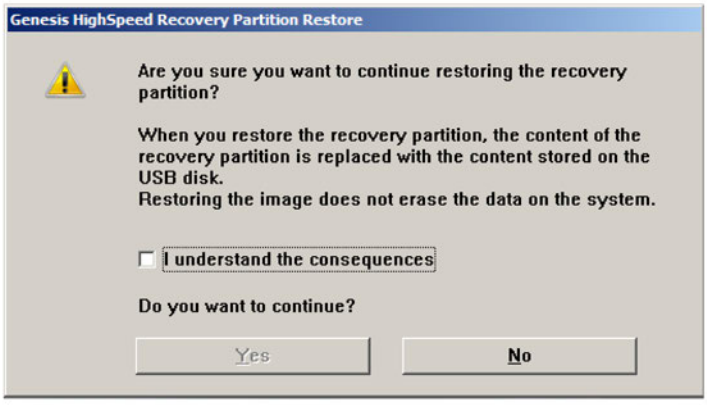


Figure G.42: Genesis HighSpeed Recovery Partition Restore

The recovery partition image is copied to the first partition of the Solid State Drive. A progress window is shown during the copying process (see Figure G.43).

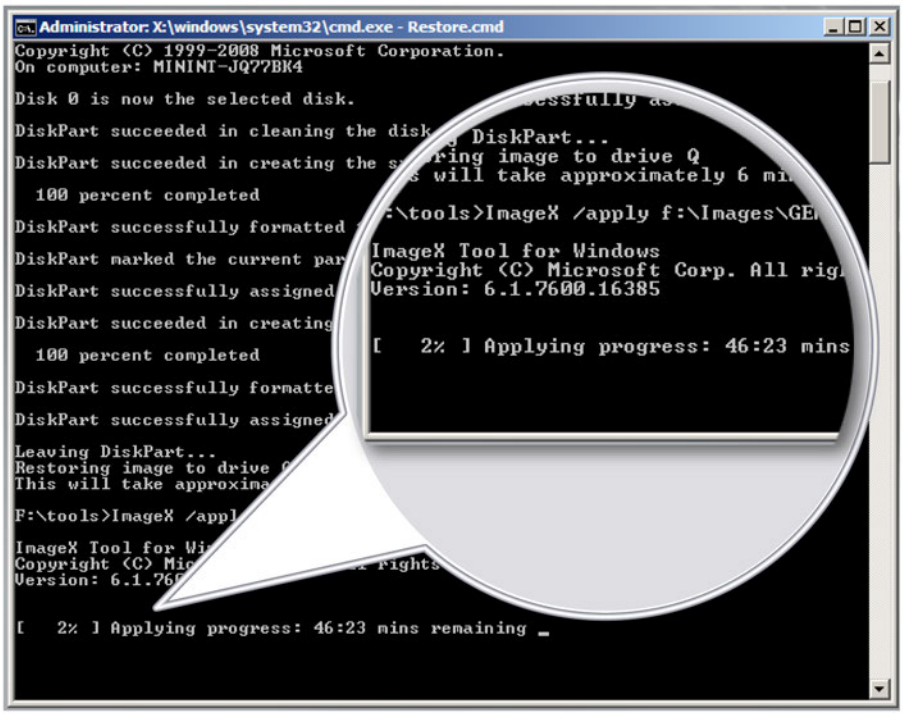


Figure G.43: Recovery partition image copying progress

After the image has been copied, the sentence **Restoring image is finished** appears in the progress window (see Figure G.44).

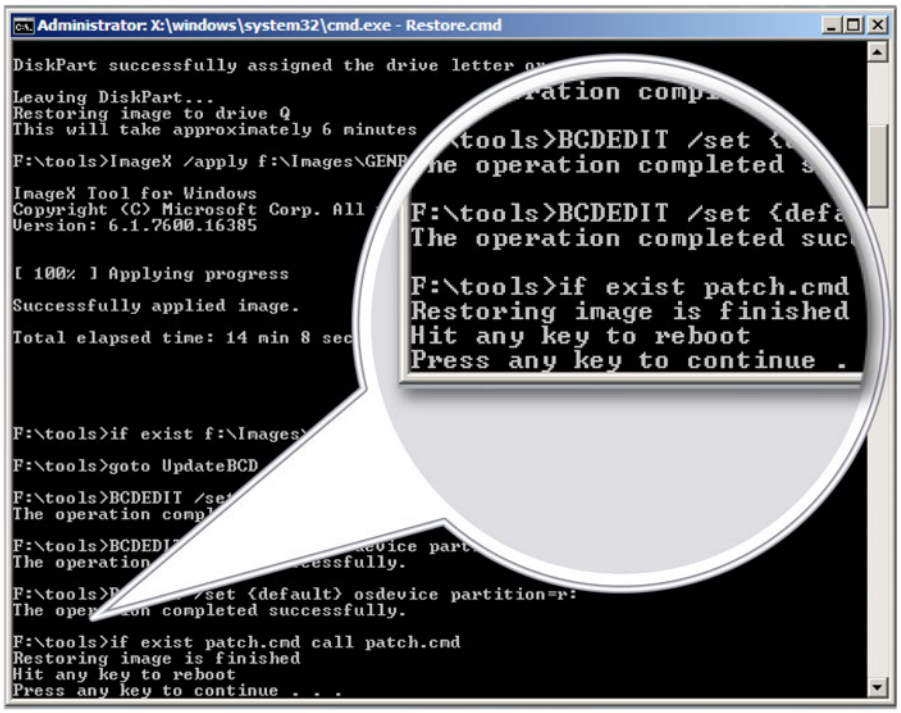


Figure G.44: Recovery partition image finished

Press any key to end the recovery partition restore and reboot the system.

G.6 GHS Integrated system BIOS update

The BIOS is password protected. The settings from the manufacturing process ensure the best operation of the system.

WARNING

Do not power off the system during the BIOS update.

1. Power off the mainframe.
2. Make sure that a keyboard is connected.
3. Turn the system back on, continually push the arrow down key on the keyboard to start the Boot Manager.
4. Use the arrow keys to select the **BIOS Update [EMS Enabled]** item from the list.

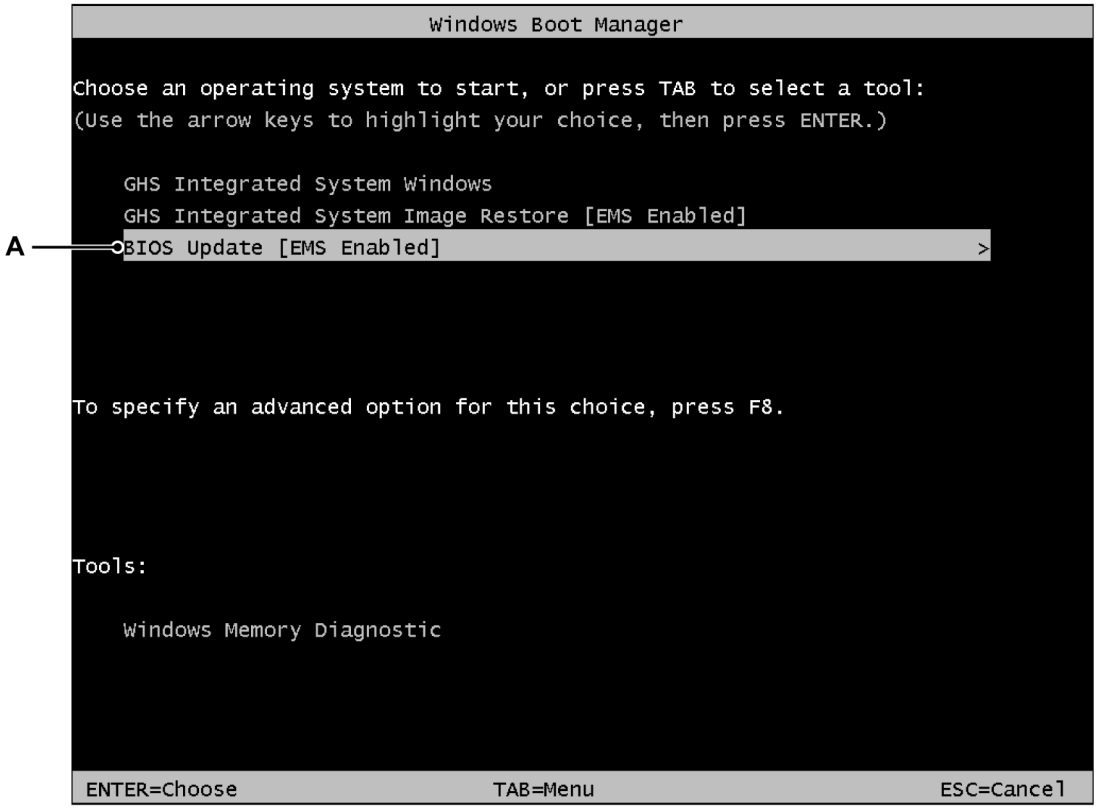


Figure G.45: Windows Boot Manager - BIOS update

A BIOS Update (EMS Enabled)

5. Press Enter to start the BIOS update.

6 The BIOS update is started and the BIOS is restored with the BIOS version and settings that were used when this system was manufactured.
A progress window (see Figure G.46) appears during the BIOS update.

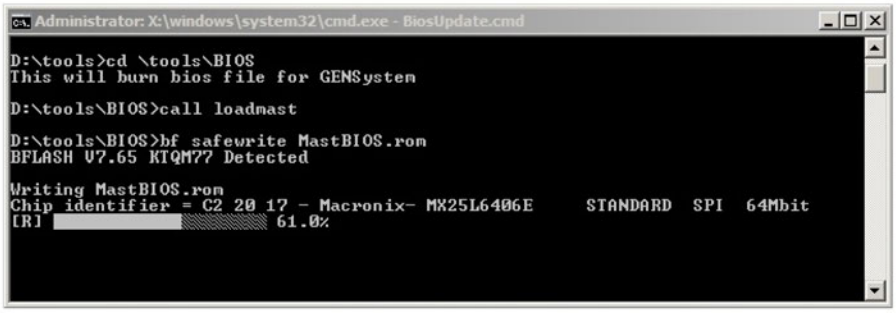


Figure G.46: BIOS update progress window

7 After the BIOS update is finished, the sentence **BIOS has been updated** appears in the progress window (see Figure G.47).

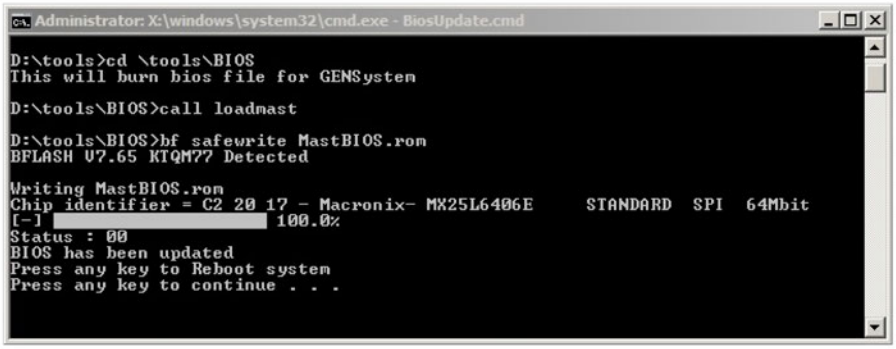


Figure G.47: BIOS update finished

8 Press any key to end the BIOS update and reboot the system.

G.7 Language settings in Windows

G.7.1 How to change the Windows 7 display language

1 Go to **Start ▸ Control Panel ▸ Clock, Language, and Region** / **Change the display language**.

2 Change the display language in the **Choose a display language** dropdown list.

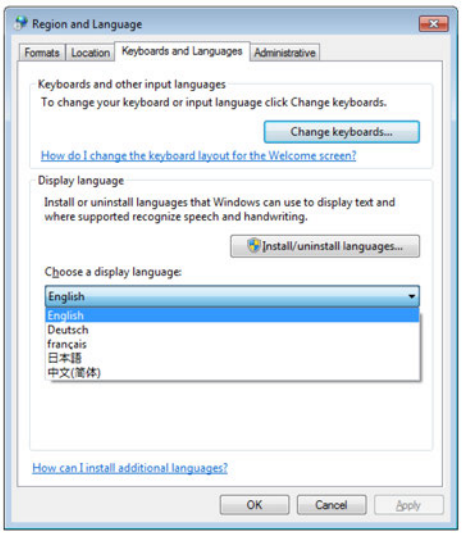


Figure G.48: Choose a display language

3 Click **OK**.

4 Windows® 7 will install the language, as shown in Figure G.49.

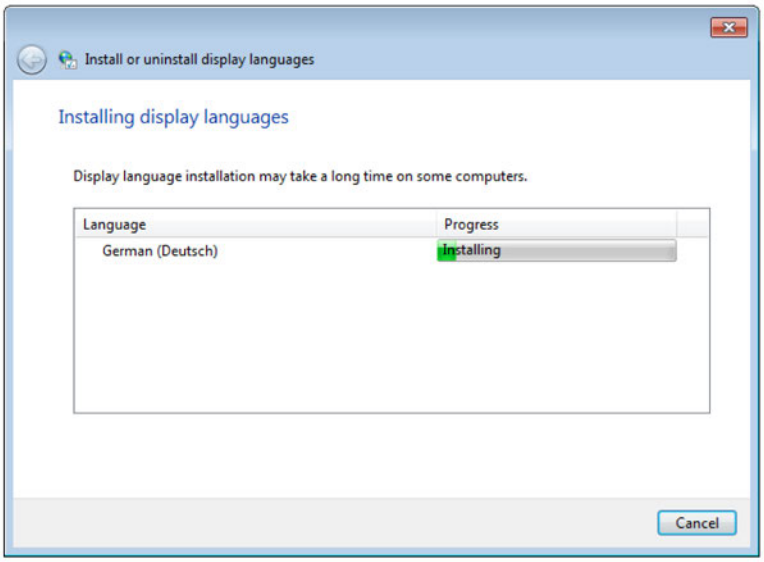


Figure G.49: Installing display languages

5 Log off for the changes to take effect (this will affect only the user profile under which you are currently logged on).

Note *If the required language is not listed, install the required language as described in "Installing a Language Pack in Windows 7 Ultimate" on page 780.*

G.7.2 How to change the Windows 10 display language

Note *Windows® 10 removed all language packs at the end of a Customer Image Restore. Therefore the user must always install the language pack in Windows® 10 to make the change of the Windows® 10 display language obsolete.*

1 Go to **Start** ▸ **Settings**, select **Time & language**.

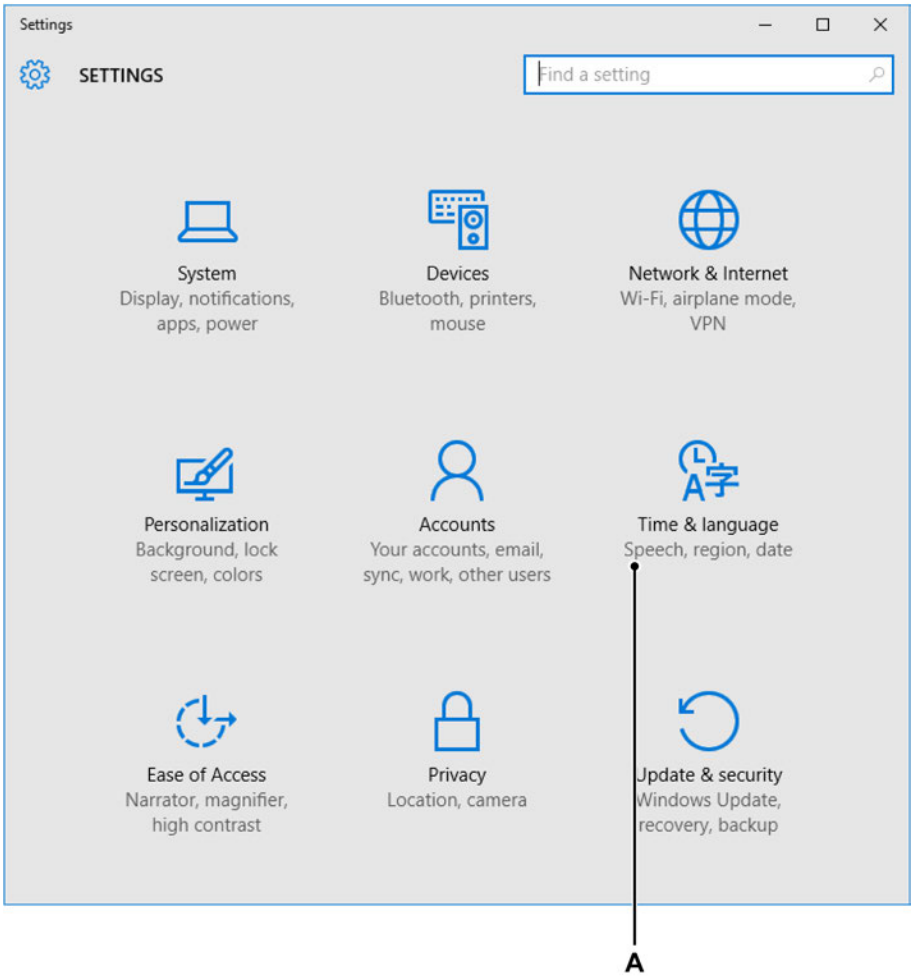


Figure G.50: Windows® 10 Settings window

A Time and language option

2 In the **Time & Language** window, select the **Region & language** option. Select the **Add a language** button for the appropriate language and confirm with **Set as default**.

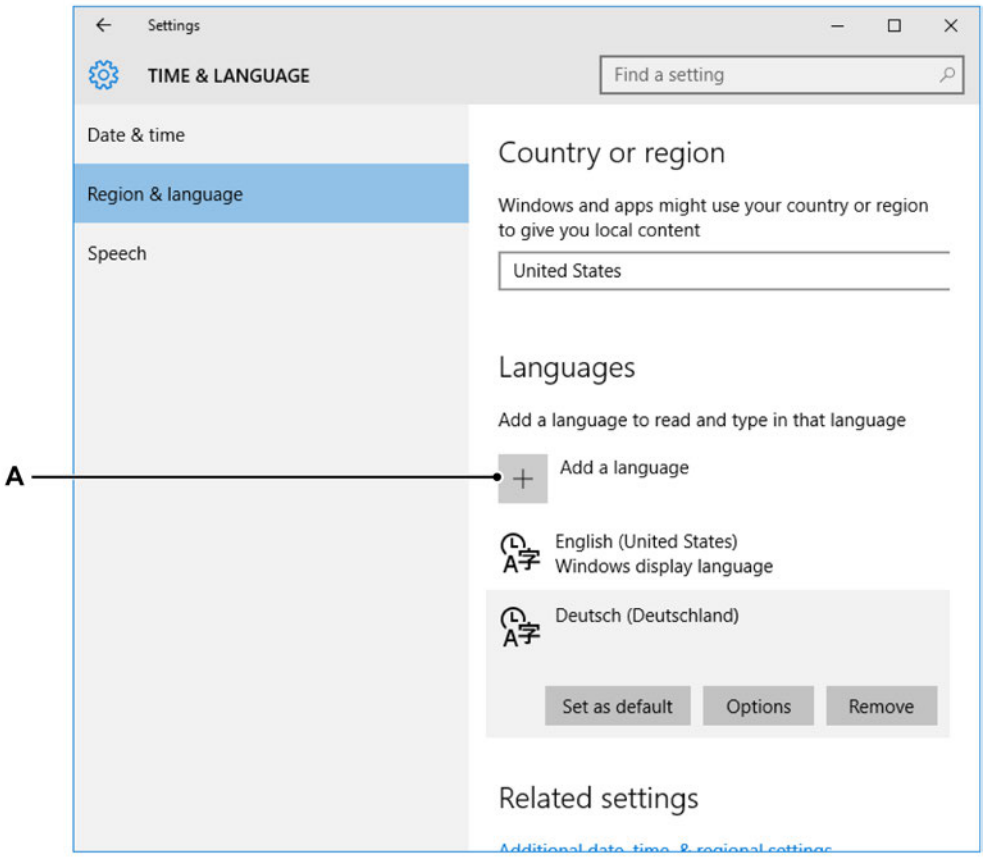


Figure G.51: Windows® 10 Time & Language window

A Add a Windows ® 10 display language.

3 The selected language will be used after the next sign-in.

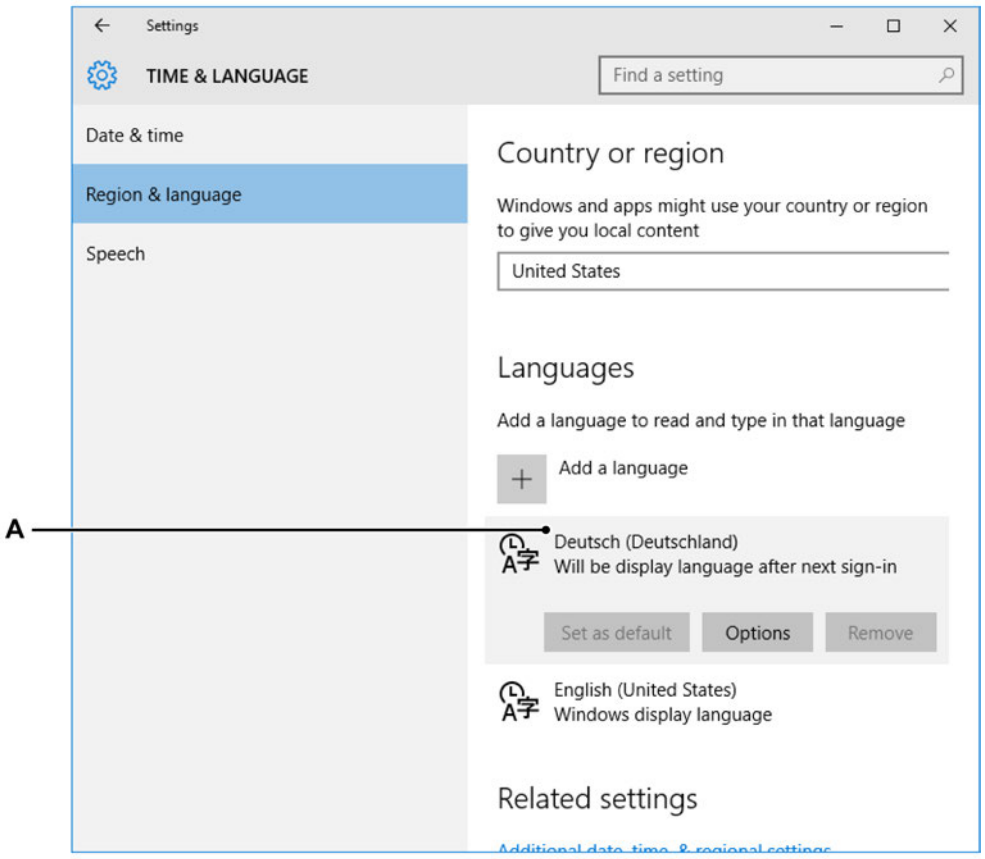


Figure G.52: Windows® 10 Time & Language window

A Windows® 10 display language when system is rebooted.

G.7.3 Installing a Language Pack in Windows 7 Ultimate

Note *Make sure that GEN3i has access to an internet connection. The Windows® update needs access to Microsoft® servers to download the selected language pack.*

1 Go to **Start ▸ All Programs ▸ Windows Update ▸ Optional Updates.**
2 Open optional updates and go to the section **Windows 7 Language Packs**.

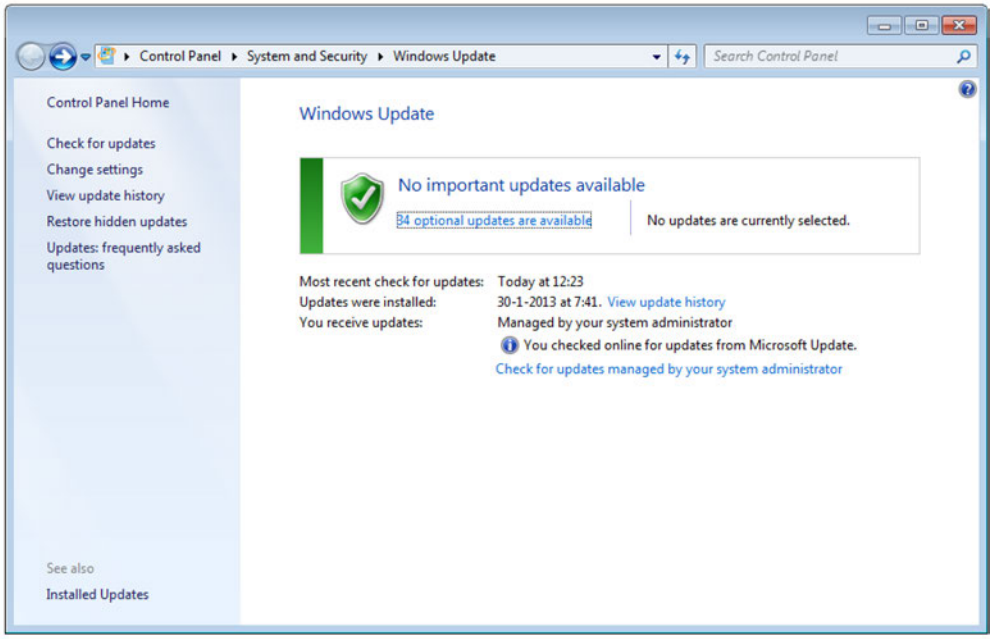


Figure G.53: Optional updates

3 Check the box to select a Language Pack and confirm by clicking **OK**.

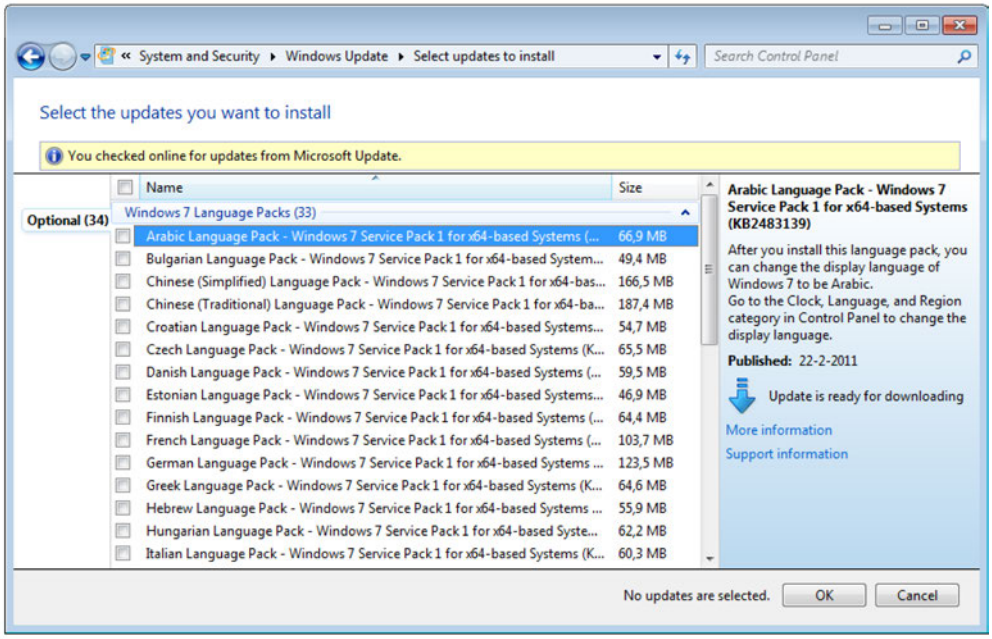


Figure G.54: Windows® 7 Language Packs

4 Proceed with **Install updates**.

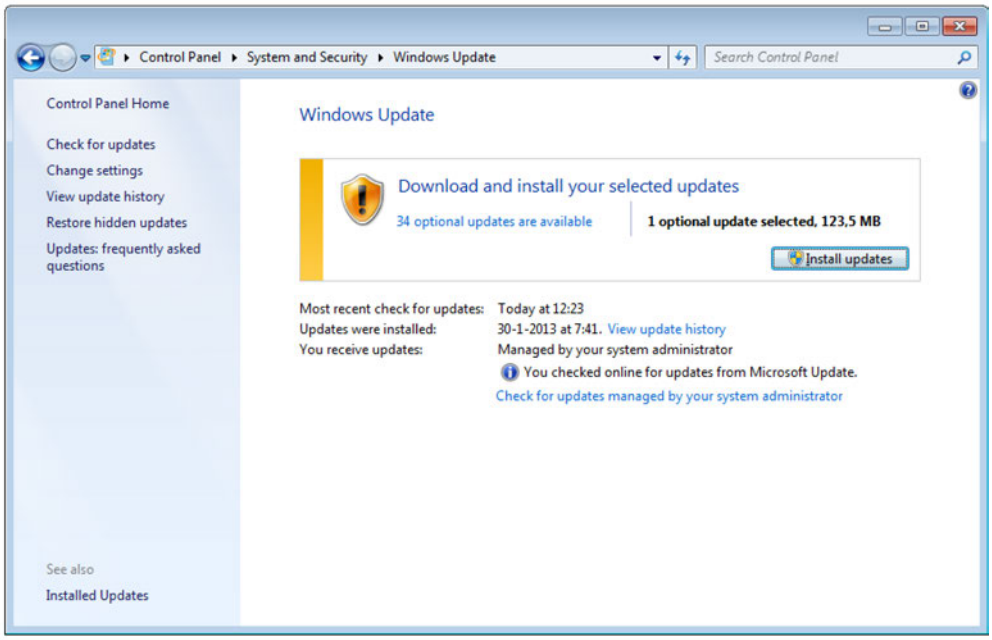


Figure G.55: Install updates

5 Windows® 7 will download the Language Pack.

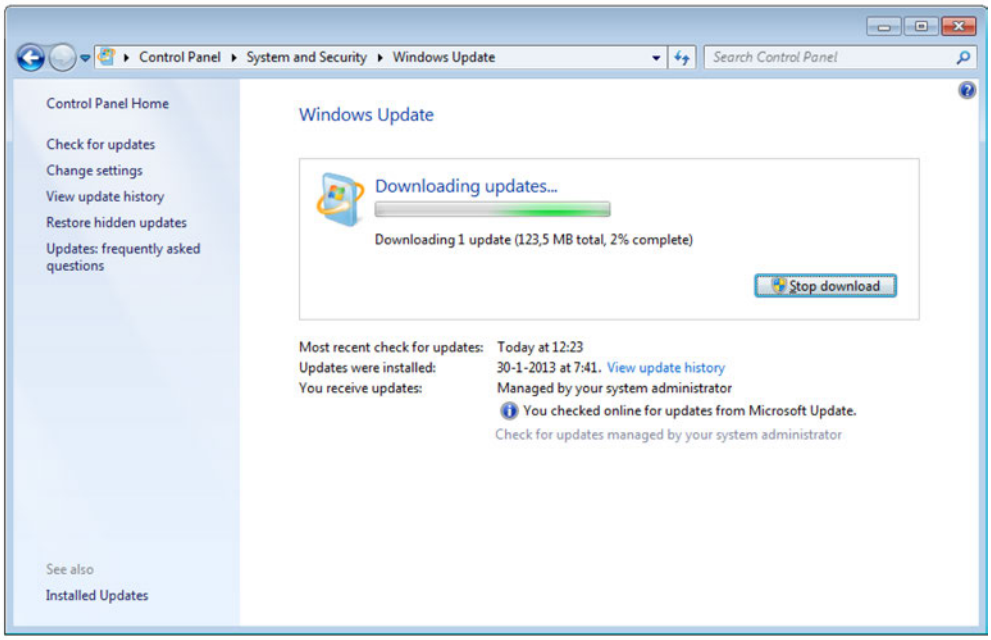


Figure G.56: Downloading updates

6 The installation of the update will automatically be initiated after the download is complete.

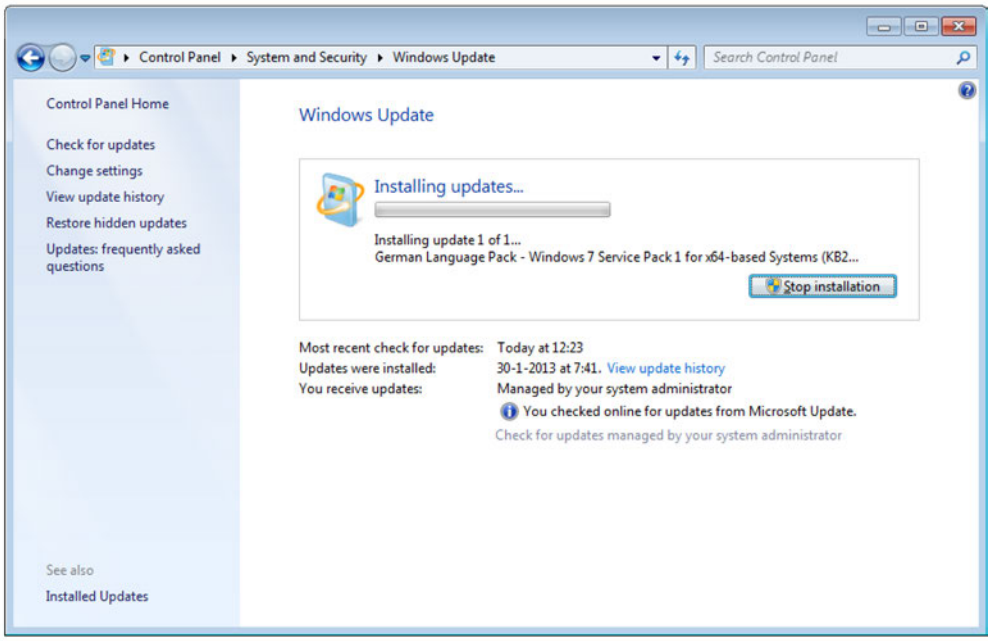


Figure G.57: Installing updates

G.7.4 Installing a Language Pack in Windows 10

Make sure the GEN3i has access to an internet connection. Windows® 10 update needs access to Microsoft® servers to download the selected language pack.

1 Go to **Start ► Settings**

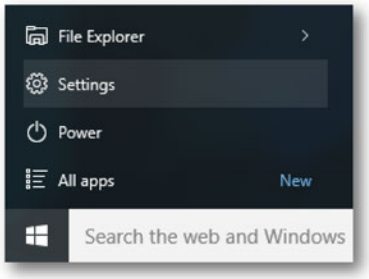


Figure G.58: Settings option

2 Select **Time & language** from the Settings panel.

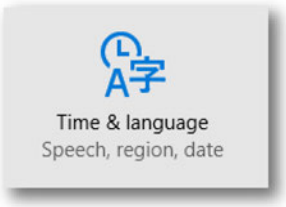


Figure G.59: Time and language option

3 The **TIME & LANGUAGE** windows opens. Select the **Region & Language** option and select **Add a language** in the **Languages** area.

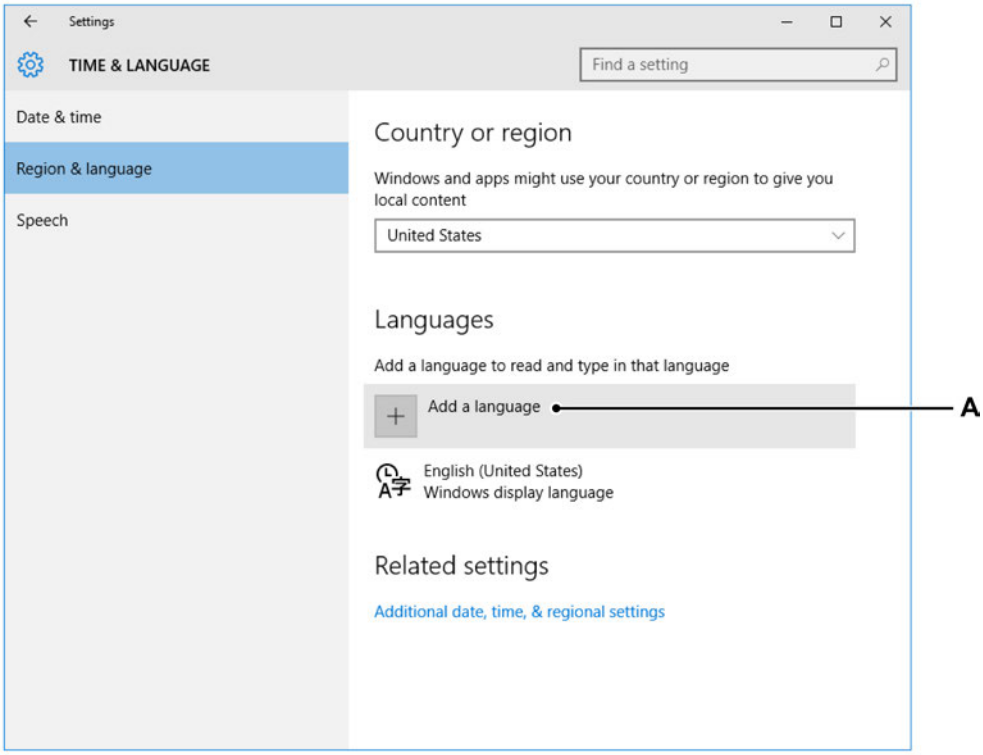


Figure G.60: Time and language window

A Add a language

4 Select the desired language from the list of languages. The languages are sorted using the English name of the language.

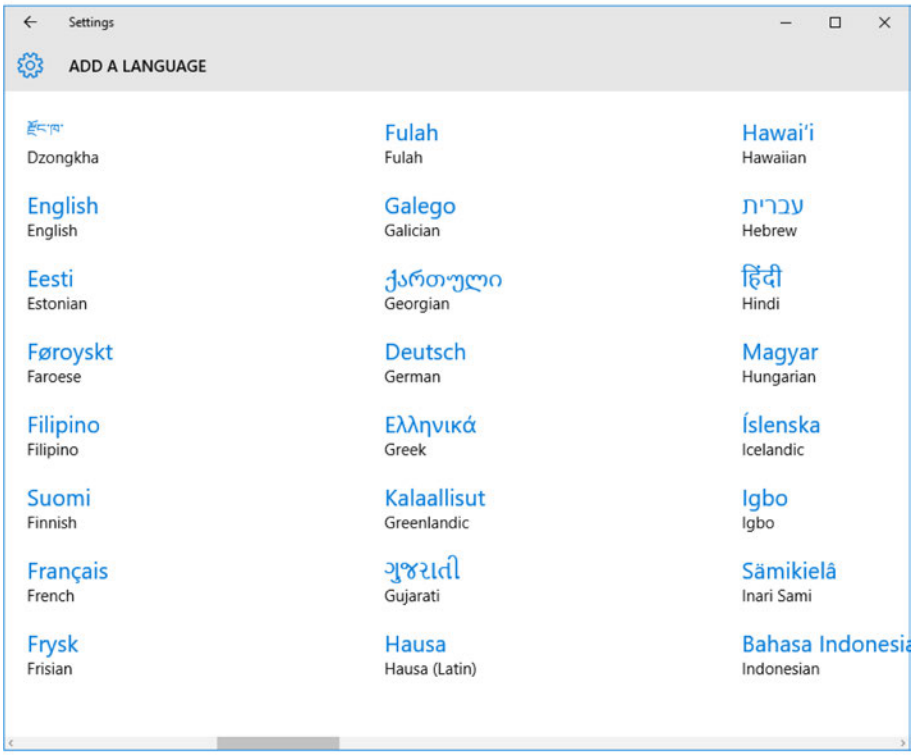


Figure G.61: Languages window

5 Some languages require the selection of a country/region specific dialect.

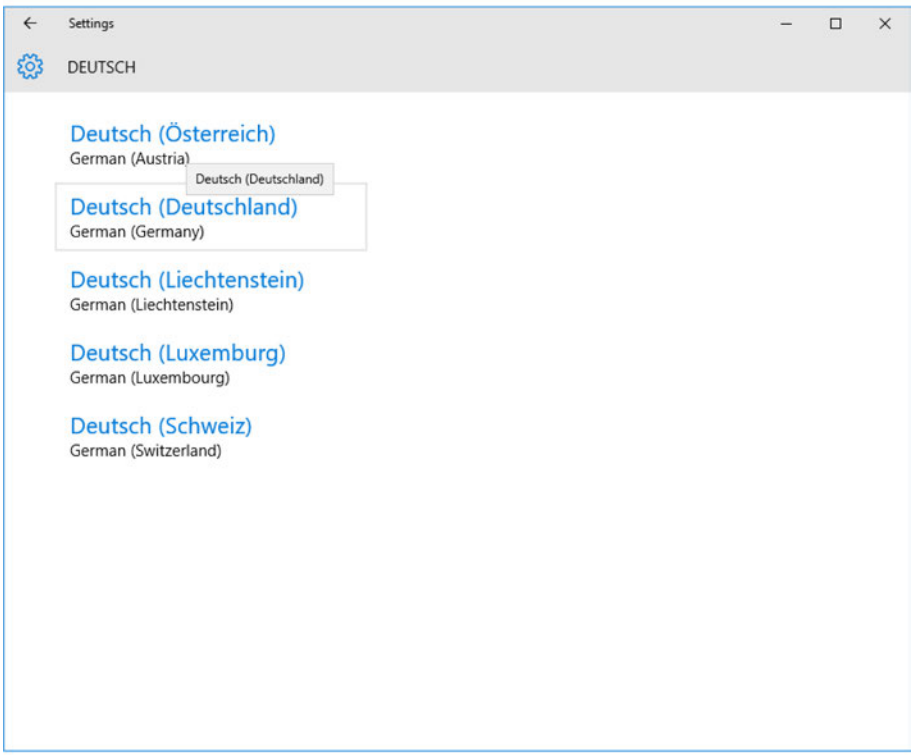


Figure G.62: Languages window/dialects

6 Select the language in the **Languages** area and click **Options**.

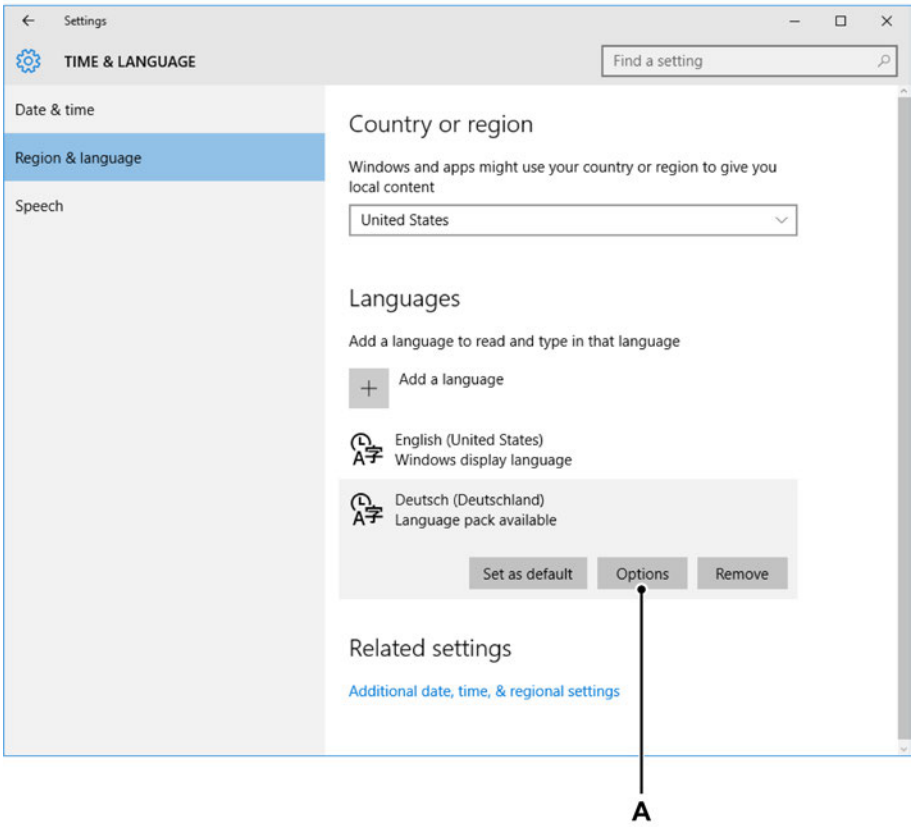


Figure G.63: Time and language window - Country or region options

A Options of the added language

7 Select **Download** of **Downlaoad language pack** option.

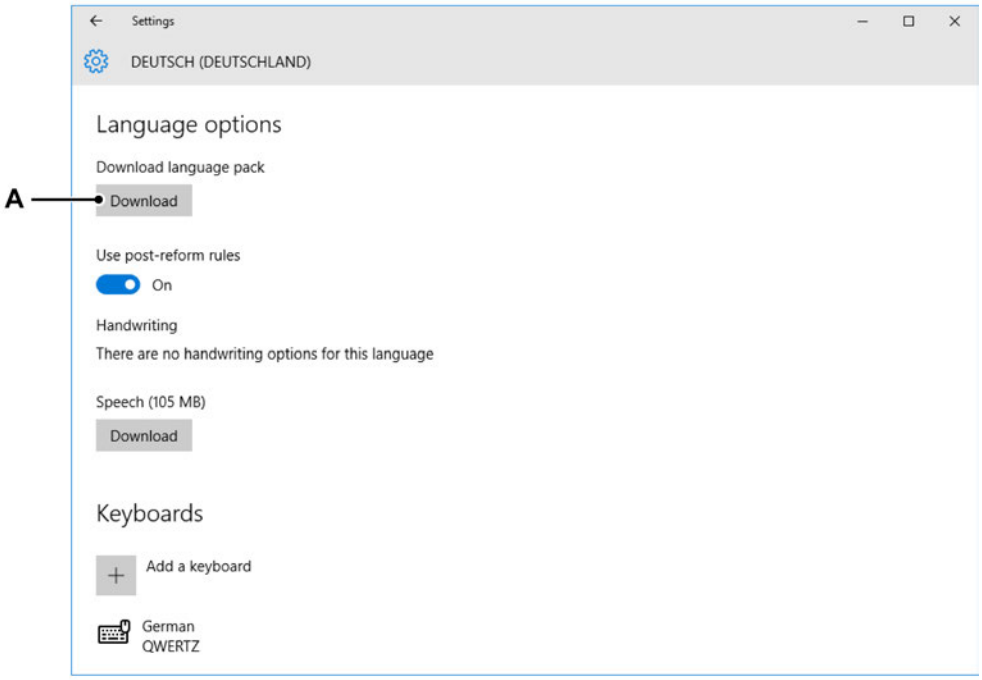


Figure G.64: Language options - Download language pack

A Download option

8 Windows® 10 downloads and install the language pack.

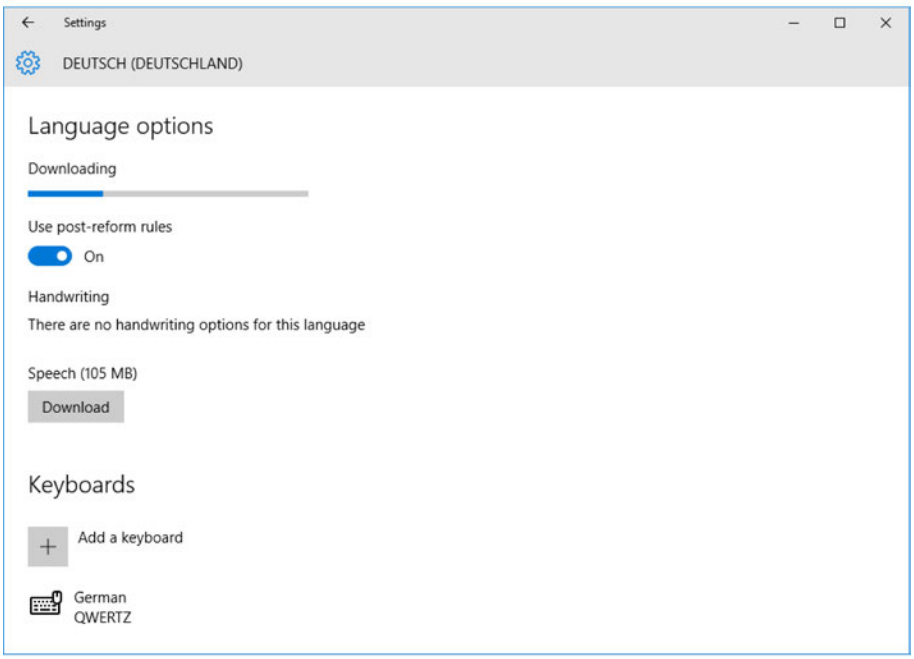


Figure G.65: Download progress status

9 Click on the ← arrow in the upper left corner to get back to the **TIME & LANGUAGE** window. Select the **Region & language** option. After the language pack has been installed, select **Set as default**.

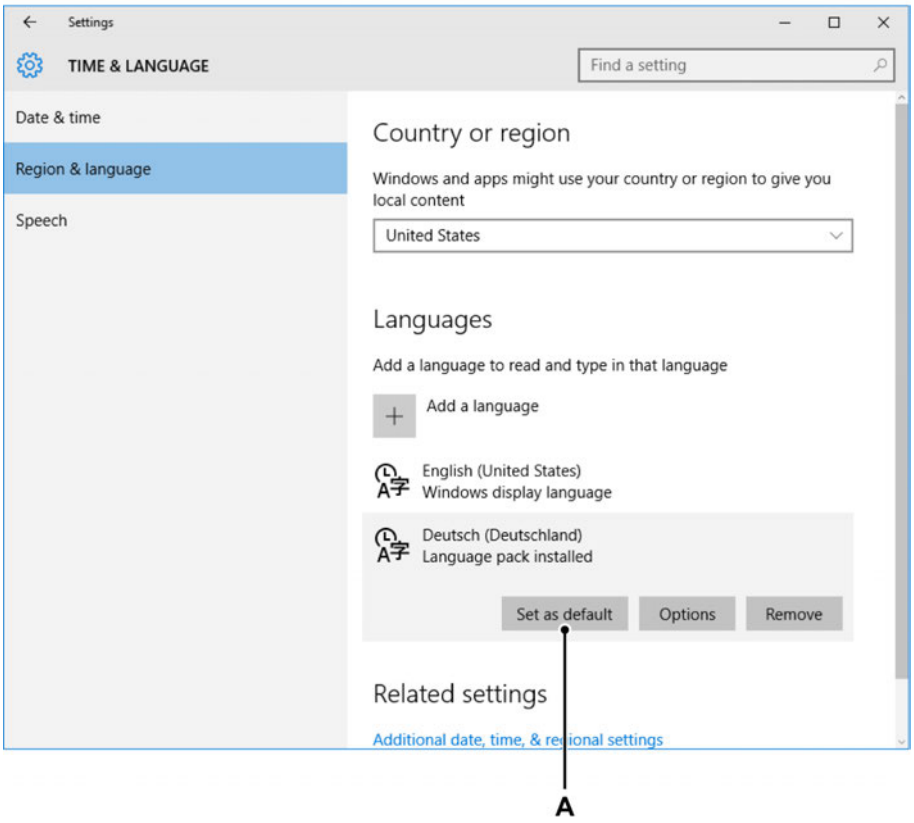


Figure G.66: Set region and language as default

A Set as default

10 The selected language becomes active after signing out and signing in again.

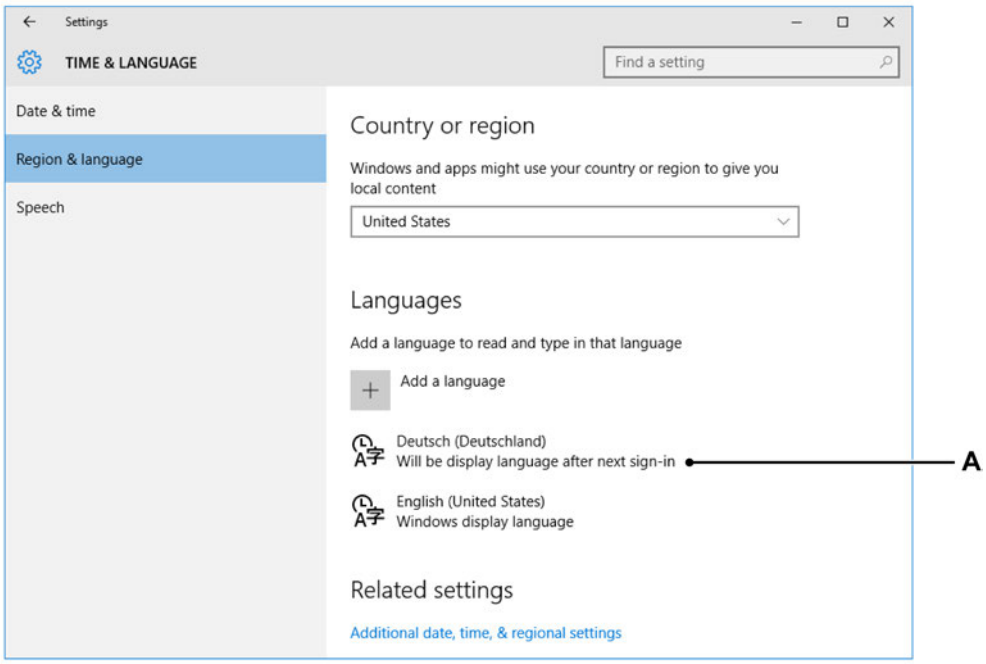


Figure G.67: Default language

A Will be display language after next sign-in

G.8 Upgrading GEN3i, GEN3iA and GEN7i to Windows 10

1 When checking for Windows® updates, one of the offered updates is the upgrade to Windows 10®. Once this update is installed, a new icon appears (see Figure G.68) in the Windows® taskbar.

Figure G.68: Windows® 10 update icon

Note *If this icon is not present check appendix "Enable the Windows 10 upgrade on GEN3i/GEN3iA/GEN7i" on page 802.*

2 When clicking on the icon the following window (see Figure G.69) is shown. Select **Upgrade now** to start the upgrade to Windows® 10.

Figure G.69: Upgrade recommendation

3 The download of the Windows® 10 installation starts.

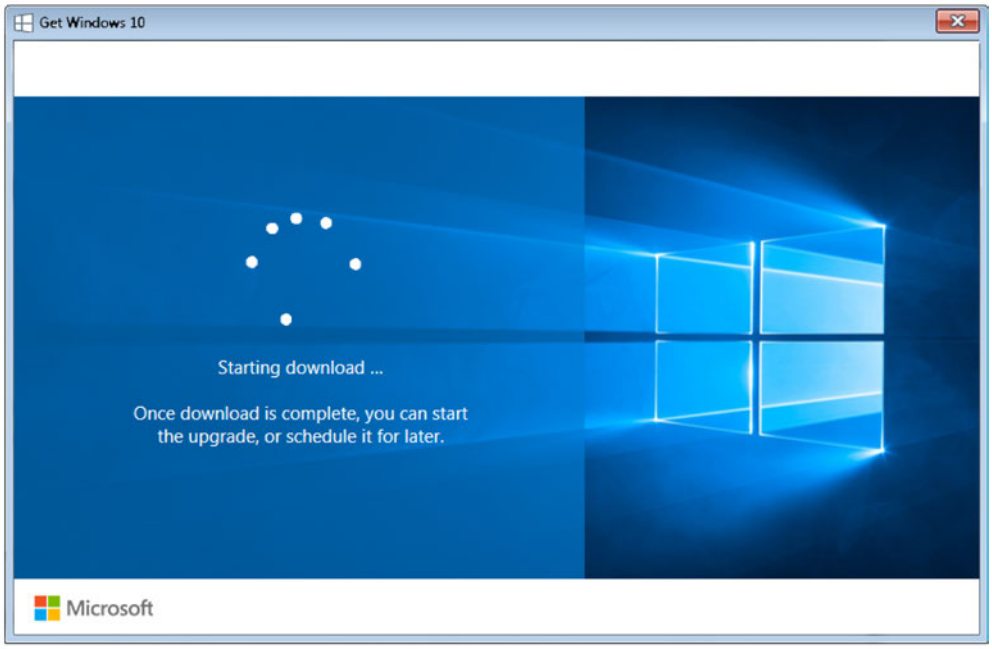


Figure G.70: Windows® 10 download start

4 The starting download screen automatically switches to **Windows Update** progress bar.

Note *The GEN series system must have access to Internet for this process to work. As the download is very big (almost 3 GB) an internet connection with 50 Mbit/s or more is strongly recommended. Even with a fast internet connection the download takes several hours to complete.*

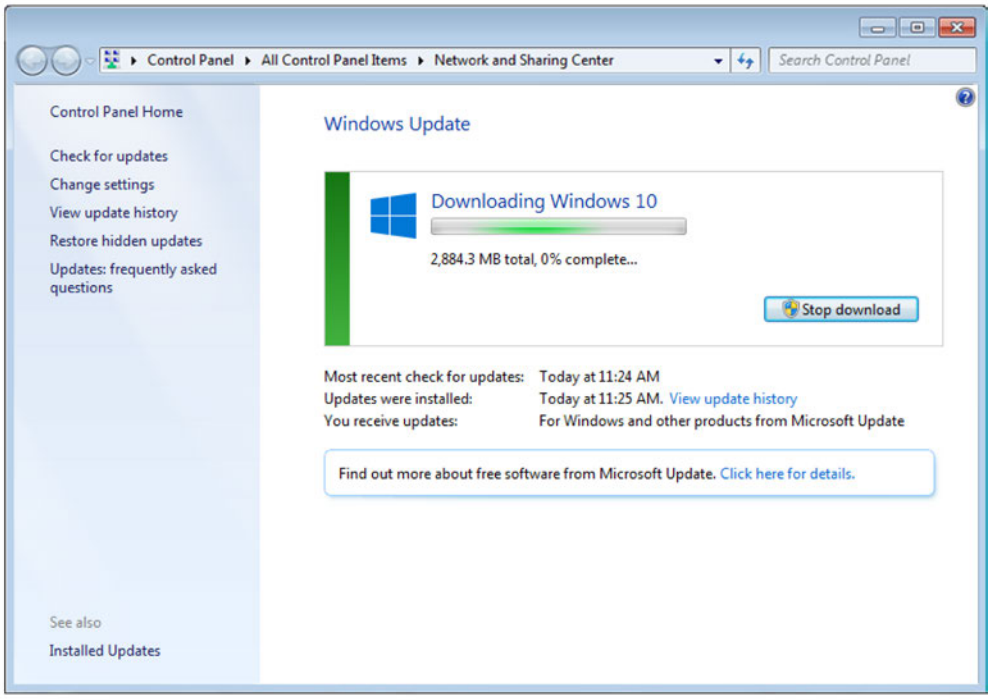


Figure G.71: Downloading Windows® 10 progress bar

5 Once the installation package has been downloaded, Windows® Update prepares the installation.

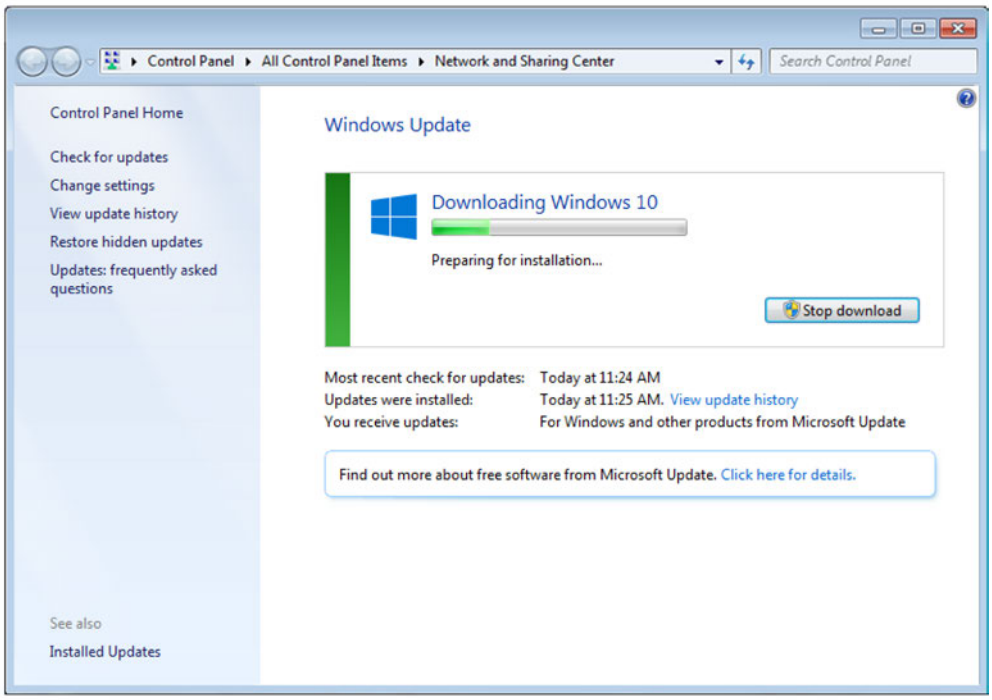


Figure G.72: Preparing for installation...

6 Before Windows® 10 is installed, the End User License Agreement has to be accepted. Select **Accept**.

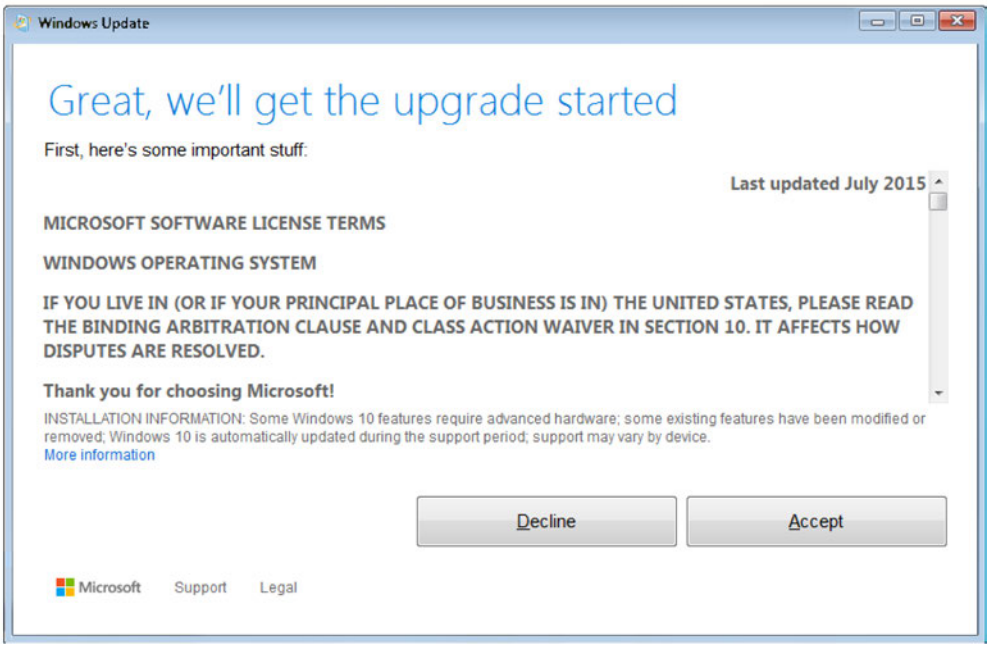


Figure G.73: Microsoft® Software Licence Terms

7 Now the Windows® 10 upgrade can be started. Select **Start the upgrade now**.

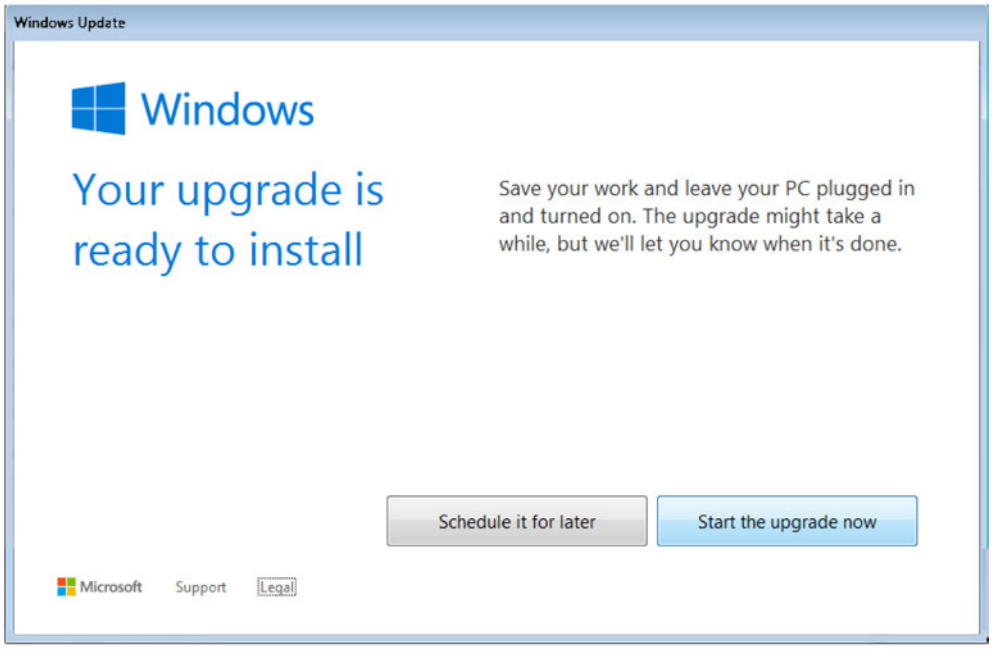


Figure G.74: Windows 10® upgrade is ready to install

8 The installation of the upgrade might take a while and during this step the system cannot be used and will reboot several times.

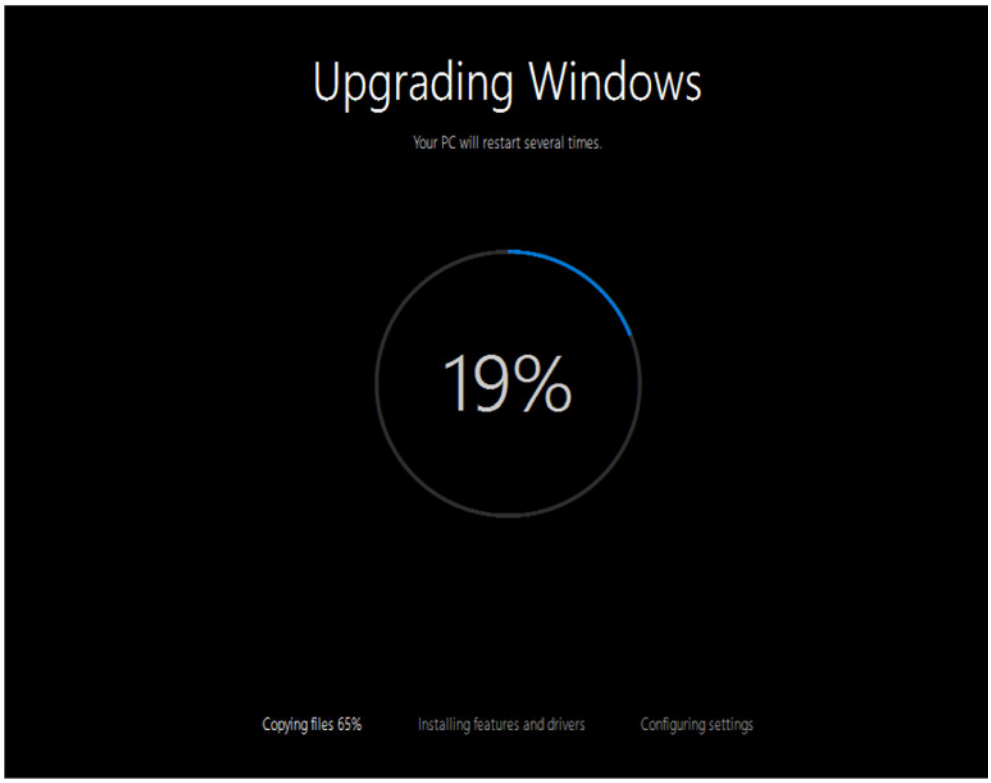


Figure G.75: Upgrade status

9 After Windows® 10 has been installed, a few questions have to be answered before the system can be used. Select **Next**.

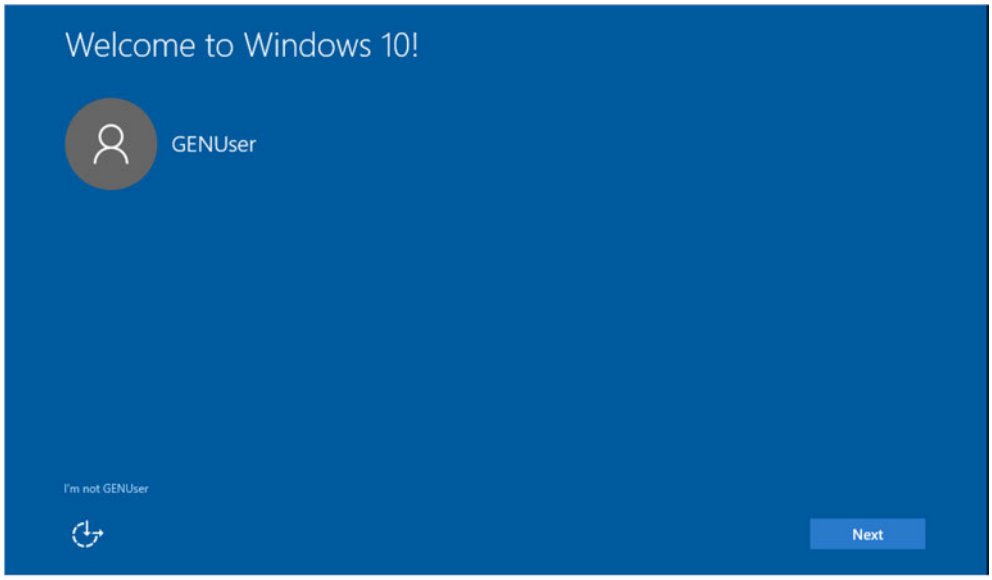


Figure G.76: Windows® 10 welcome message

10 Select **Use Express settings** to continue.

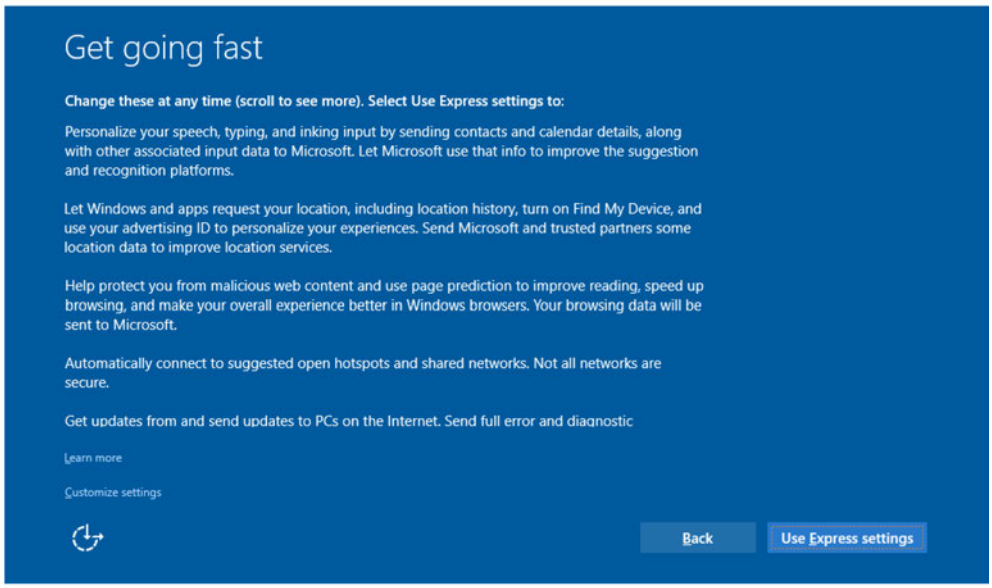


Figure G.77: Windows® 10 express settings

11 The presence of the Cortana personal assistant depends on the language of the operating system.

HINT/TIP

HBM recommends not to enable the Cortana personal assistant as a GEN series system typically is not used with personal application like agenda, email and messaging services.

If this screen appears, select **Not now**.

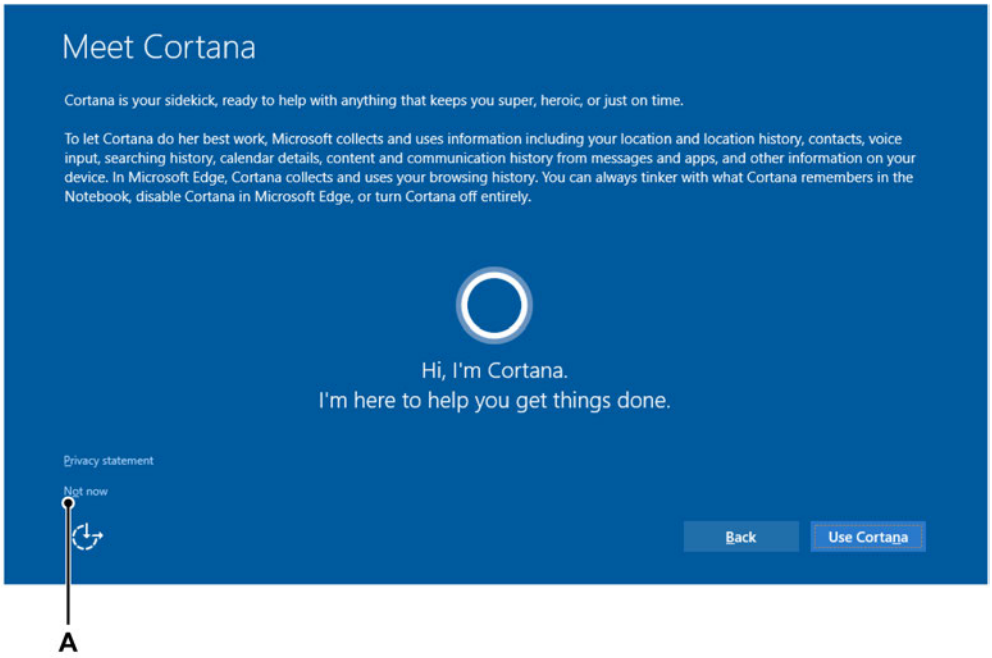
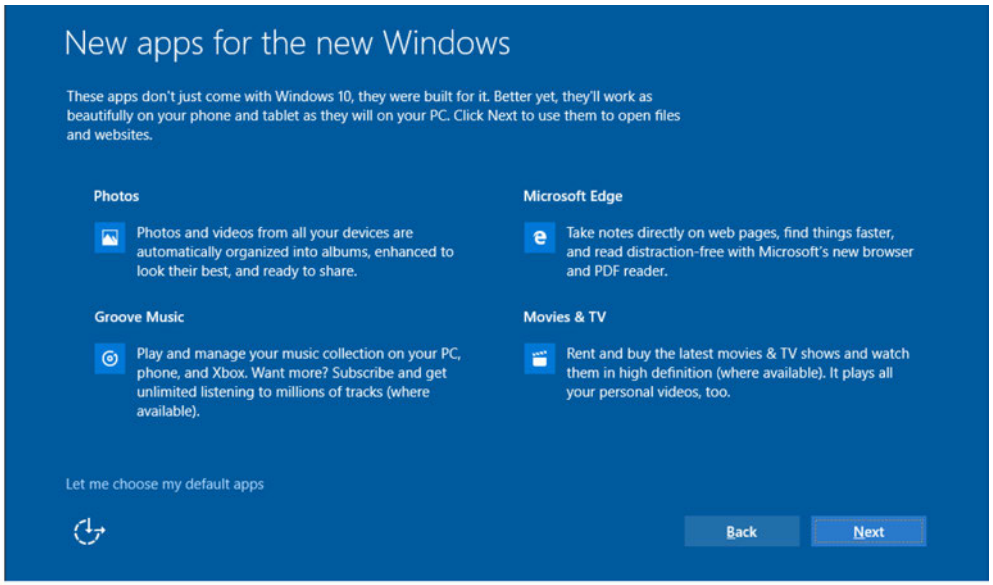


Figure G.78: Cortana personal assistant

A Not now

12 Select **Next** to finish the installation.



IMPORTANT

The Windows® 10 upgrade does not install all drivers required for the Genesis Highspeed Acquisition Hardware.

13 Download the latest GEN3i/GEN3iA/GEN7i Update Package from the HBM website: www.hbm.com/en/2475/support-downloads-perception/

Install the package on the integrated system. Follow the instructions of the update package.

G.9 Enable the Windows 10 upgrade on GEN3i/GEN3iA/GEN7i

IMPORTANT

GEN3i/GEN3iA/GEN7i mainframes are factory configured not to enable the free Windows® 10 upgrade offered by Microsoft®.

At time of release of this manual the Windows® 10 upgrade has been validated by HBM and can now be performed. Follow the steps documented in this appendix to enable the Windows® 10 upgrade.

1 Click on the Windows® **Start** button to open the Start Menu and select **All Programs**.

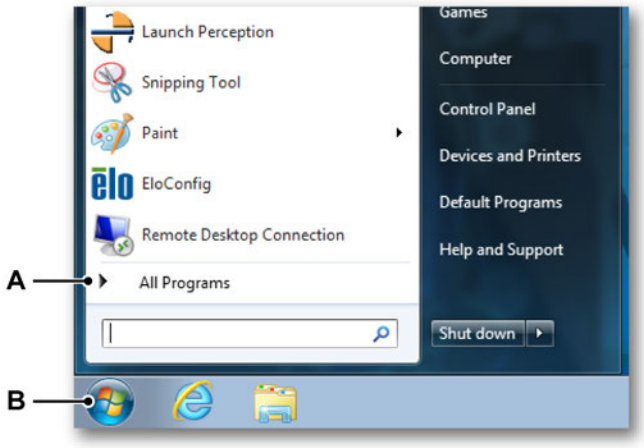


Figure G.79: Windows ® task bar and Start menu (detail)

A All Programs

B Start button

2 In the list of Programs select **Windows Update**.

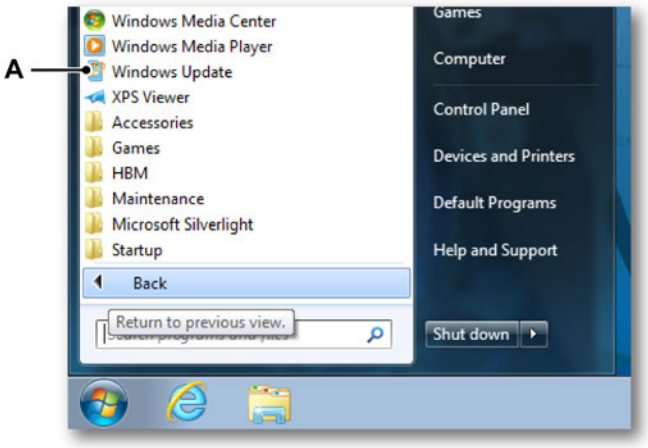


Figure G.80: Windows ® task bar and Start menu (detail)

A Windows Update option

3 Select **Restore hidden updates** to view the list of hidden updates.

Note *The GEN series system must have access to Internet for this process to work.*

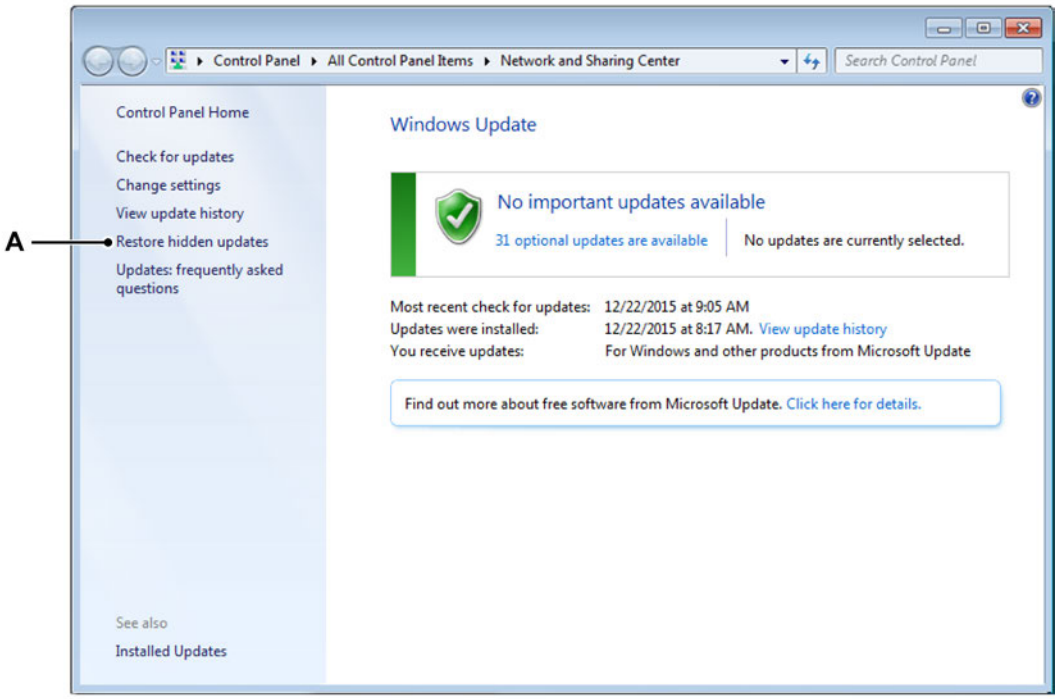


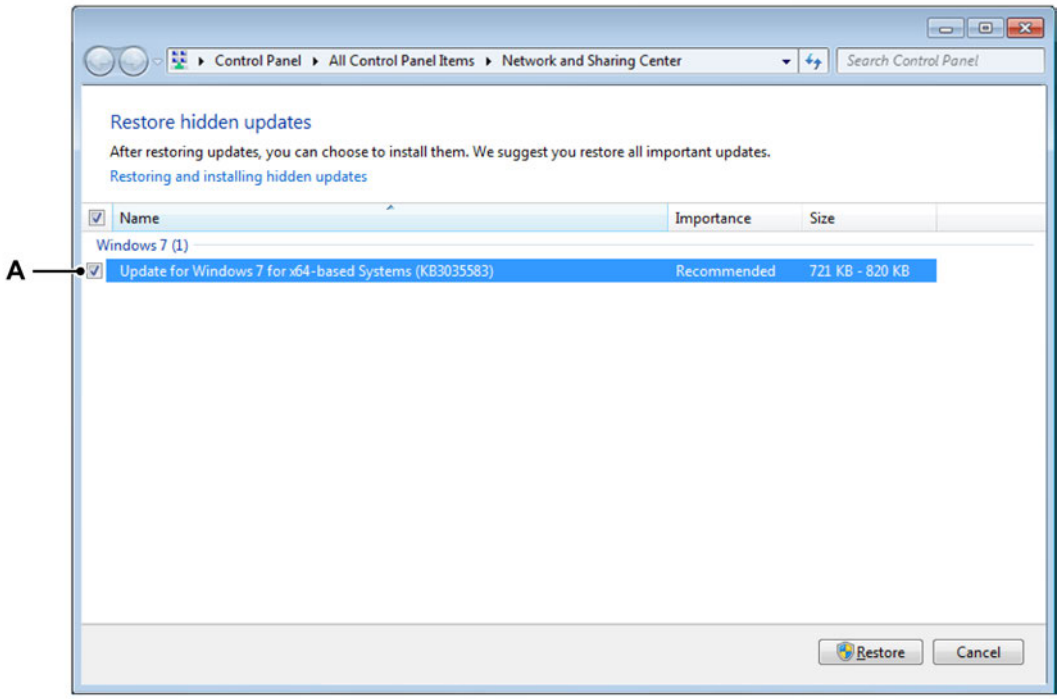
Figure G.81: Windows® Control Panel Home options

A Restore hidden updates

4 Windows® Update will now check for all available updates including the Windows® 10 update. In the list for **Restore hidden updates**, check all items (avoids searching the list) and select **Restore**.

IMPORTANT

When selecting individual items to be restored, make sure that the item "Update for Windows 7 for x64-based Systems (KB3035583) is selected. This item enables the Windows® 10 upgrade process.



A Hidden update to start the Windows® 10 upgrade process

5 Once the selected update is installed, the system requires a reboot. After the system is rebooted, it might take a few minutes before the Windows® 10 Upgrade icon appears in the taskbar.

G.10 Embedded Software upgrades

When a new version of Perception is installed, the embedded software of the mainframes is automatically updated when Perception connects to the mainframe.

Note *Some upgrades may take more than ten minutes.*

IMPORTANT

Do not power off the mainframe, do not disconnect network cables and do not shut down Perception during an embedded software upgrade.

When the software upgrade process does not complete within 30 minutes, power off the mainframe by keeping the Power-On button pressed for five seconds. Wait for 30 seconds and turn the unit back on.

Wait until the unit has completed the boot process. If the new software version is booted, Perception will connect and start using the mainframe as normal. In rare cases, the upgrade might have failed. This could result in:

- The mainframe using the old software.
- The mainframe using the “minimum mode” software.

In both cases, Perception software will automatically detect an old software version during the connection attempt and will restart the upgrade procedure.

In the very unlikely event that the mainframe does not reboot, turn the unit off again and retry the boot process. If the mainframe keeps failing to boot, contact your HBM service agent for enhanced support.

G.10.1 Boot recovery switch

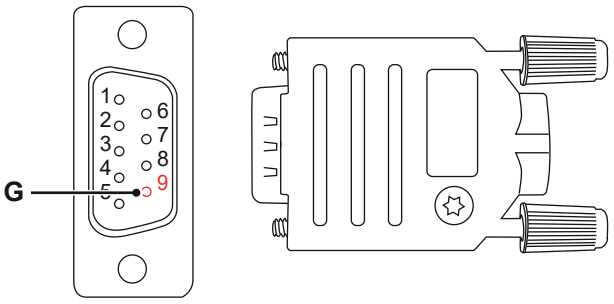
In the very unlikely event the GEN DAQ mainframe fails to boot correctly and/ or a firmware update is not possible, the mainframes supports a minimum boot mode recovery switch.

IMPORTANT

Use this switch only when instructed by HBM support. The GEN DAQ mainframe normally should boot in the recovery mode automatically whenever the normal boot fails.

+5 V Power Out

PIN Signal
PIN 1 - External Time base In
PIN 2 - External Event Out
PIN 3 - External Trigger In
PIN 4 - Ground
PIN 5 - Ground
PIN 6 - External Start In
PIN 7 - External Trigger Out
PIN 8 - External Stop In
PIN 9 - +5V



Output power	
Voltage	5 ± 0.5 V DC
Maximum current	0.1 A, continues short circuit protected

When instructed to use the minimum boot mode switch:

1 Power off the mainframe and remove the power cord.
2 Remove all acquisition cards to allow access to the mainframes backplane
See "Removing and installing input cards" on page 99 for more details.

3 Locate the boot mode switch on the mainframes backplane.

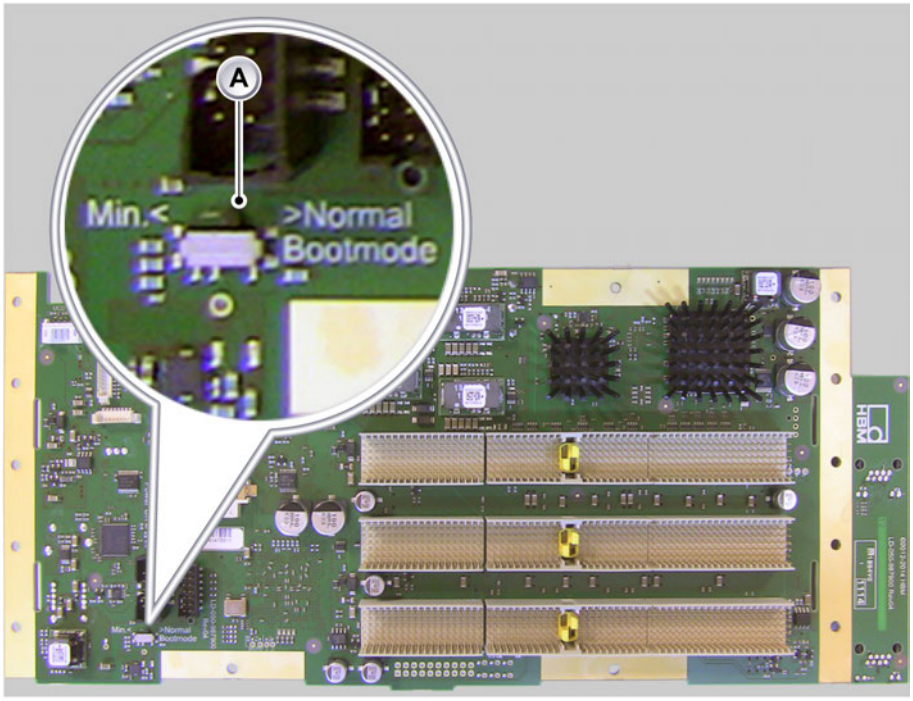


Figure G.82: Location of boot mode recovery switch

Note *Details might look slightly different depending on mainframe version.*

4 To enable the recovery mode, use a pointy object (e.g. screwdriver) and move the lever to the side labeled **Min**.

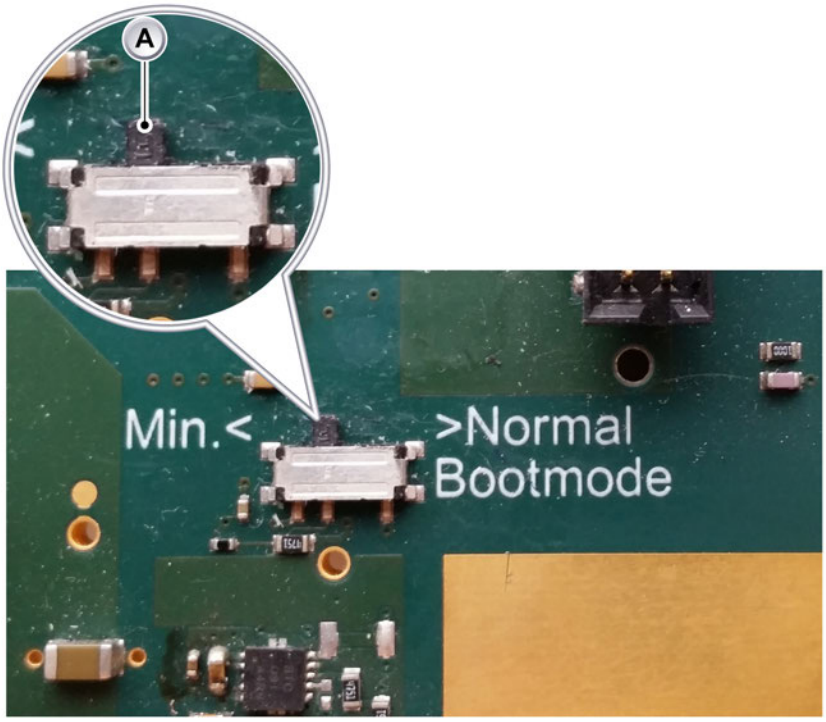


Figure G.83: Lever to switch the boot mode

A Lever

5 Re-insert all acquisition cards.
6 Insert the power cord and power on the mainframe.
7 Use Perception software to perform a firmware upgrade.
8 When Perception completes the mainframe will automatically reboot.
9 When reboot is completed power off the mainframe and remove the power cord.
10 Remove all acquisition cards to allow access to the mainframes backplane.
11 Shift the black lever to the side labeled **Normal**.
12 Re-insert all acquisition cards.
13 Insert the power cord and power on the mainframe.

The GENDAQ mainframe should now work in normal mode.

Note *If the mainframe still fails to work correctly after this recovery process the unit must be send back to HBM service for a repair.*

G.11 Unexpected mainframe shutdown

If the mainframe has shut down unexpectedly, this can have several causes:

- **Power interruption**
  - Check if the mains cable is still firmly connected.
  - Check if other devices on the same mains group have experienced a power interruption.
- **Over-temperature or over-voltage:**
  - If this happens while Perception is connected, a message is shown that tells the reason for the shutdown. Apart from that, a message is shown when connecting the next time, even if Perception was not connected at the time of the shutdown.
  - If the cause was over-temperature, please check the airflow around the mainframe; the mainframe must be able to attract cool air to avoid over-heating.
  - If the cause was over-voltage, please contact HBM service.

G.12 The Master/Slave connection does not synchronize

If this happens, check the following:

- Check whether the Master/Slave mode setting for each mainframe matches the role of that mainframe. There should be one (and only one) Master and one or more Slave(s).
- Check the optical Master/Slave cables. Both LEDs at the connector should be lit.
- Verify the cable type. The Master/Slave cables should be Multi Mode, 850 nm optical cables.
- Very long cables and optical couplers in the cable degrade the optical signal. For information on how to calculate optical losses, please refer to the chapter "Calculating maximum fiber cable length" on page 853.
- The optical connections should not be damaged and should be free of dust and lint.

G.13 The IRIG/GPS does not synchronize

- Verify the settings. Is the correct synchronization source selected?
- For IRIG, does the IRIG mode (such as “IRIG B AM”) match the IRIG signal?
- Check whether the connections are correct. For more information, please refer to the corresponding chapter.
- GPS synchronization can take a long time. Be patient. You may try switching back to RTC and starting all over again.
- Check whether the signal (IRIG) is free of distortions (e.g. record the IRIG signal and check whether the amplitude-modulated sine wave is clean).
- Check the positioning of the GPS antenna. The GPS synchronization needs signals from at least three satellites for correct operation. Walls can distort the signals from the satellites by blocking or reflecting them.

G.14 Optical Network (SFP)

If no connection is present on the fiber optic channel, first check the following:

1. Check whether the **cable wavelength** and **SFP module wavelength** are the same.
   Check the wavelength printed on the label of the SFP module with the specification of the cable used.
2. Check whether the communication speed at both ends of the fiber optic connection are the same.
3. Inspect the cable and connectors for any possible faults or breaks that could impede communication.
4. The optical connections should not be damaged and should be free of dust and lint.

G.15 Master/Slave synchronization verification procedure

To verify the correct operation of the Master/Slave configuration, proceed as follows:

Hardware setup

1. Set up two GEN series mainframes, each with at least one recorder card installed.
2. For GEN3i/GEN3iA/GEN3t/GEN7i/GEN7tA and GEN17tA the system synchronization connector can be used.
3. Connect a TTL level, 1 Hertz signal to the top input in the first recorder card of the master mainframe and to the top input in the first recorder card of the slave mainframe.
4. Switch on both GEN series mainframes and wait until they have completed the boot process.
5. Using the fiber optic cable, connect any Master/Slave card's connector of the master mainframe to Master/Slave card's top connector, labelled **M/S IN**, of the slave mainframes (For GEN3i/GEN3iA/GEN3t/GEN7i/GEN7tA and GEN17tA use the Master/Slave synchronization connector).
6. Check if both LEDs on both Master/Slave cards are illuminated green. (For GEN3i/GEN3iA/GEN3t/GEN7i/GEN7tA and GEN17tA, check the LEDs near the Master/Slave synchronization connector).

Software setup

1. If it is not already active, start Perception.
2. In the start dialog, select **New blank experiment**.
3. Make sure you are connected to the required mainframes. Use the *Hardware Navigator* to do this.
4. In the **Settings** sheet, go to the **General** group in the task pane and select **Mainframe**. A list of available mainframes is displayed in the settings area.
5. Set the master mainframe operating mode to Master in the **Master/ Slave mode** column.
6. Set the slave mainframe operating mode to Slave in the **Master/ Slave mode** column.
7. The slave mainframe will now be synchronized to the master mainframe. The status palette will show a box with the synchronization status of the Master/Slave system. This box is labelled **MASTER SLAVE**.

8 The synchronization status will first be **Synchronizing** for up to three minutes before becoming **Synchronized**.

Figure G.84: MASTER SLAVE Synchronizing

Figure G.85: MASTER SLAVE Synchronized

9 In the **Settings** sheet, go to the **Trigger** group in the task pane and select **Channel**.
10 In the **Trigger mode** column, set all triggers to **Off**.

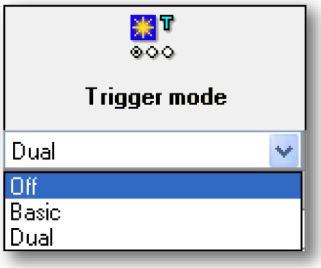


Figure G.86: Trigger mode list

11 Select the input with the connected TTL level, 1 Hertz signal on the master mainframe and set the trigger of this channel to **Basic**.
12 In the **Trigger** group, select **Recorder**.
13 Double-click on the **Master/Slave trigger** cell to open it for modification.

14 In the drop-down list that comes up, select **Transceive** for all recorders.

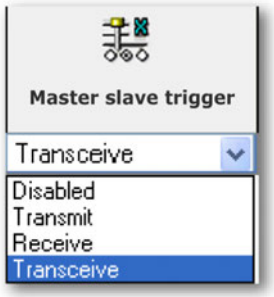


Figure G.87: Master/Slave trigger list

15 Set the filter mode of both channels to "Wideband".
16 Set up a display with the first channel of the first recorder card in the master mainframe and the first channel of the first recorder card in the slave mainframe.

Making a multi-mainframe recording

1 Wait for the “MASTER SLAVE” status to display **Synchronized** before proceeding to the next step.

Figure G.88: MASTER SLAVE Synchronized

2 Press **Run** in the acquisition control panel to start a recording.
3 The signal on the master mainframe will now generate a trigger event. This trigger event will be relayed to the slave mainframe.
4 The recording will now show the rising edge of the TTL level 1 Hertz signal recorded by the master mainframe and the slave mainframe.
5 The recordings in both mainframes are started at the same time.
6 All recorded signals will match in time to within ± 150 ns.

If all signals match in time, the recordings were completed successfully.

H Rack Mount Instructions

H.1 Mount GEN3i in a 19-inch rack

A 19-inch rack is a standardized (EIA 310-D, IEC 60297 and DIN 41494 SC48D) system for mounting various electronic units in a rack, 19-inches (482.6 mm) wide. Equipment designed to be placed in a rack is described as rack-mount or a rack-mounted system.

The GEN3i by itself cannot directly be mounted into a 19-inch rack. For this, you need to use the optional 19-inch rack mount kit.

19-inch brackets installation

1 Install both side brackets

2 Install front panel bracket

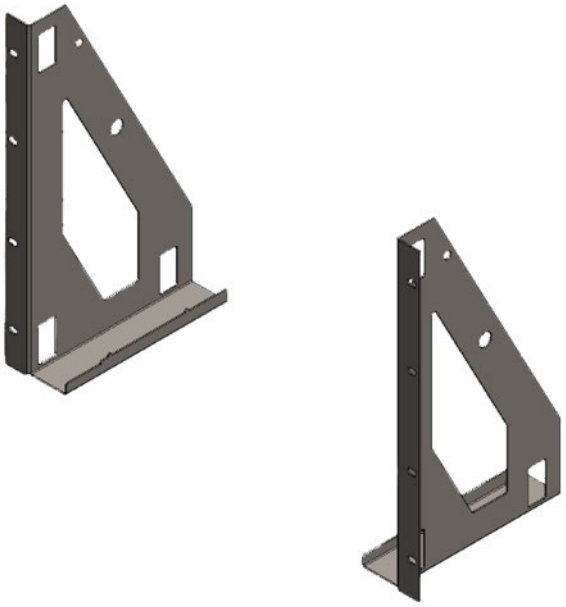


Figure H.1: 19-inch brackets

3 SCR/M5x16 (2x)

There are only two screws that fastened to the upper portion of both sides of the brackets as shown in Figure H.2.

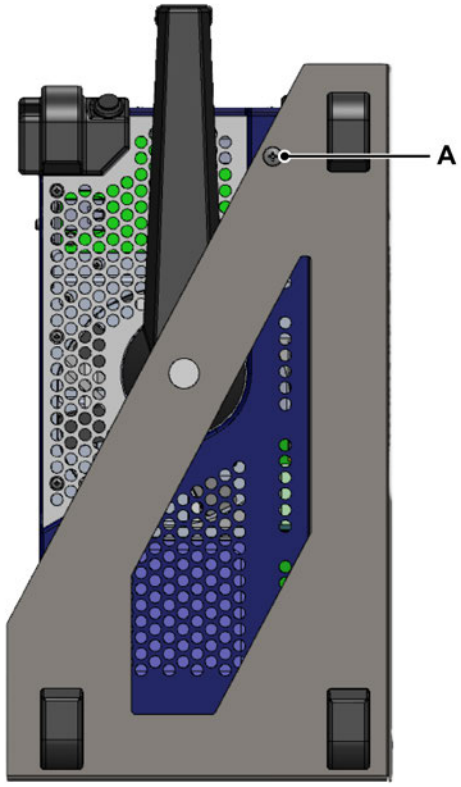


Figure H.2: GEN3i with installed 19-inch brackets

A Screw location

I PTP Synchronization

I.1 Mainframe PTP connections

I.1.1 GEN2i and GEN5i (No PTP support)

Within the GEN series mainframes, the GEN2i and GEN5i have no support for PTP time synchronization.

I.1.2 GEN7t and GEN16t

The GEN7t and GEN16t only support PTP time synchronization when using an Interface/Controller module IM2.

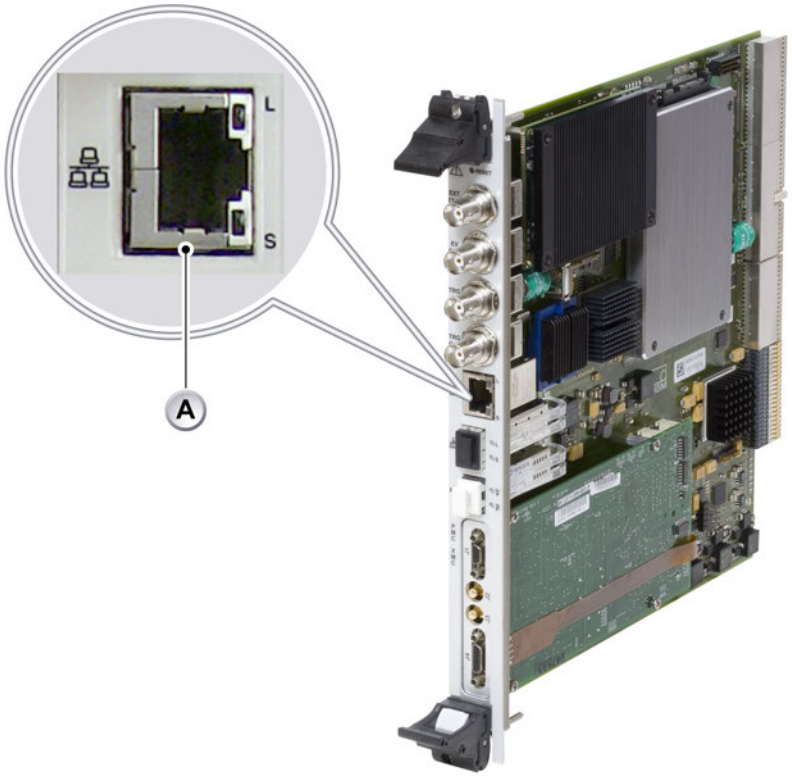


Figure I.1: GEN DAQ PTP enabled port (IM2 Module)

A PTP enabled network RJ45

I.1.3 GEN7i

Figure I.2: GEN7i PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

I.1.4 GEN7tA

Figure I.3: GEN7tA PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

I.1.5 GEN2tB

Figure I.4: GEN2tB PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

I.1.6 GEN3i and GEN3t

Figure I.5: GEN3i/GEN3t PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

I.1.7 GEN3iA

Figure I.6: GEN3i/GEN3t PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

I.1.8 GEN17tA

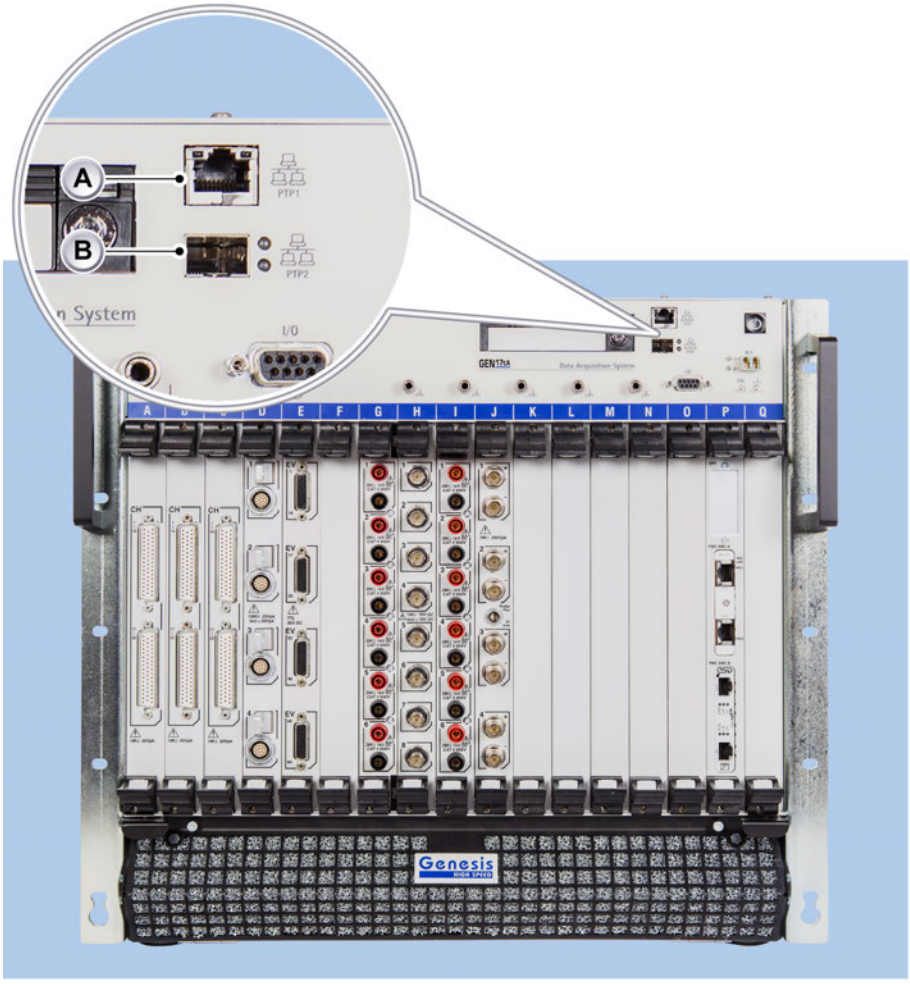


Figure I.7: GEN17tA PTP enabled ports

A PTP enabled network RJ45

B PTP enabled network optical SFP slot (SFP module is optional)

I.2 Perception settings

I.2.1 GEN7t/GEN16t - Perception settings

As the GEN7t and GEN16t only have 1 PTP port, set “Sync Source“ to PTP1:

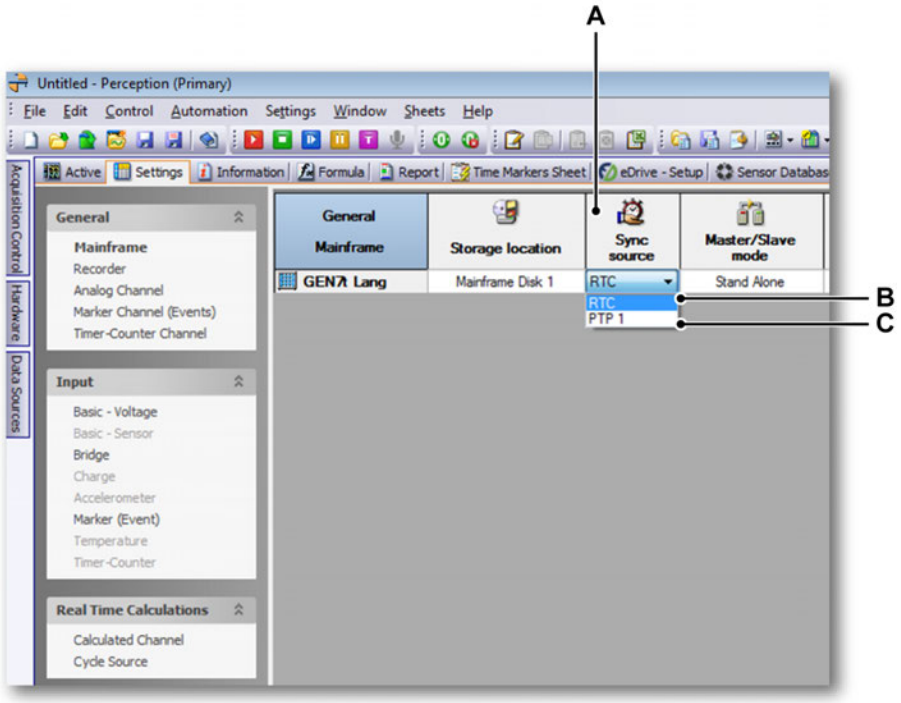


Figure I.8: Perception - Sync source option (PTP 1)

A Sync source option

B RTC

C PTP 1

I.2.2 GEN3i, GEN3iA, GEN7i, GEN3t, GEN7tA and GEN17tA - Perception settings

Set "Sync Source“ to PTP1 (RJ45) **or** to PTP2 (optical):

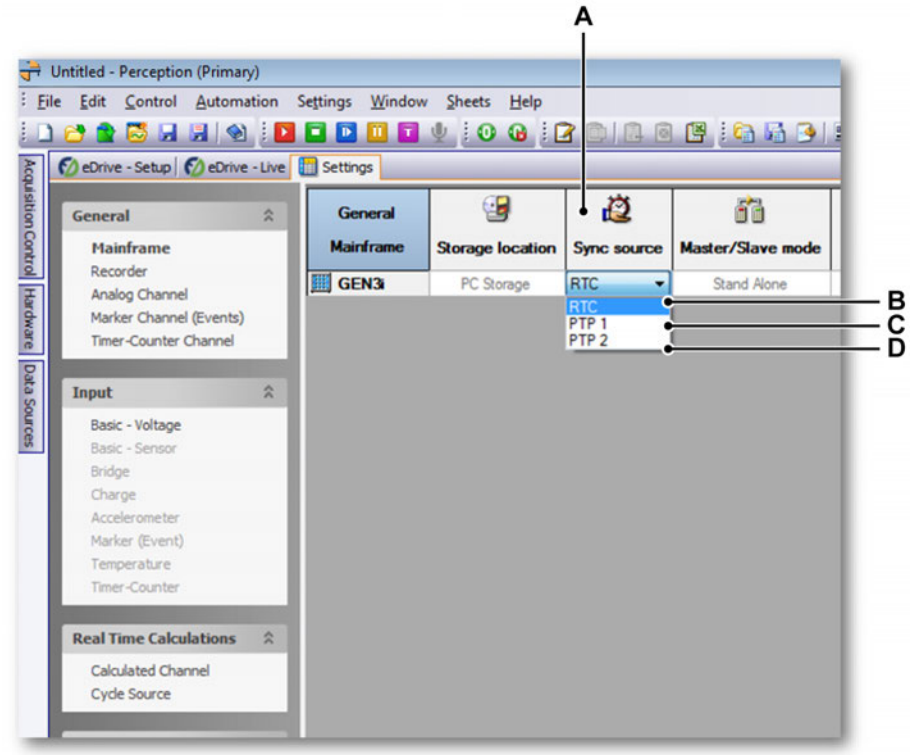


Figure I.9: Perception - Sync source option (PTP 1) or (PTP 2)

A Sync source option

B RTC

C PTP 1

D PTP 2

I.3 Synchronizing GEN series and QuantumX using PTP

I.3.1 GEN3i/GEN3iA/GEN7i with single QuantumX "B" version module

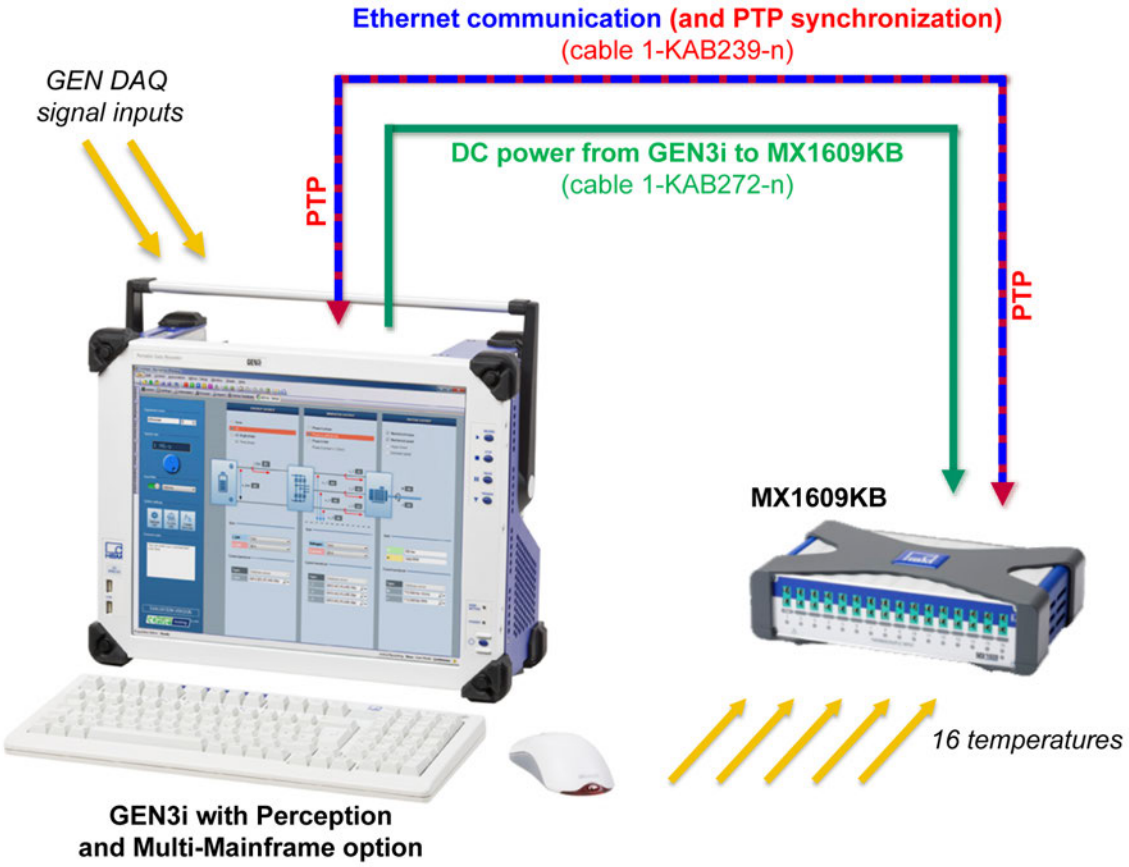


Figure I.10: GEN3i with single MX1609KB/MX1609TB - Overview

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i.*

Note *Setup only shows MX1609KB, MX471B (CAN) could also be used.*

I.3.2 GEN3i/GEN3iA/GEN7i with single Somat^{XR} "B" version module

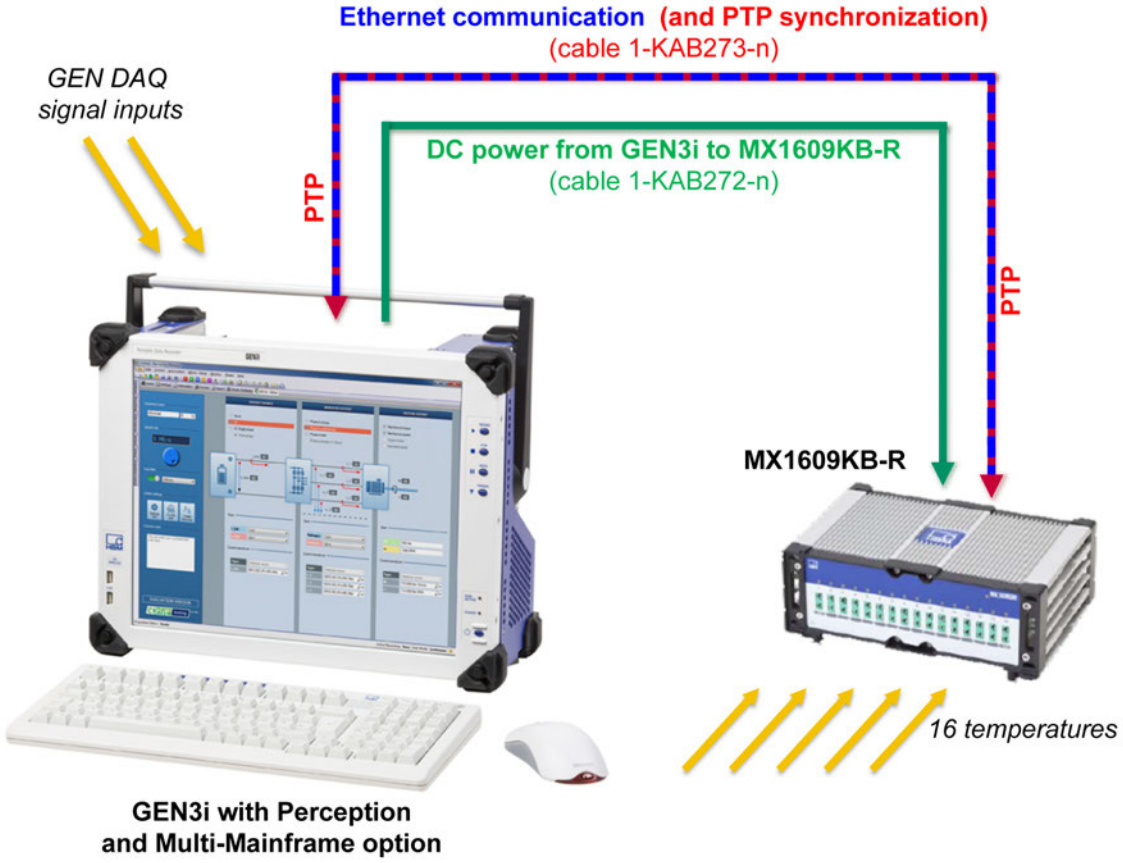


Figure I.11: GEN3i with single Somat^{XR} MX1609KB-R - Overview

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i.*

I.3.3 GEN3i/GEN3iA/GEN7i with up to three QuantumX "B" version modules

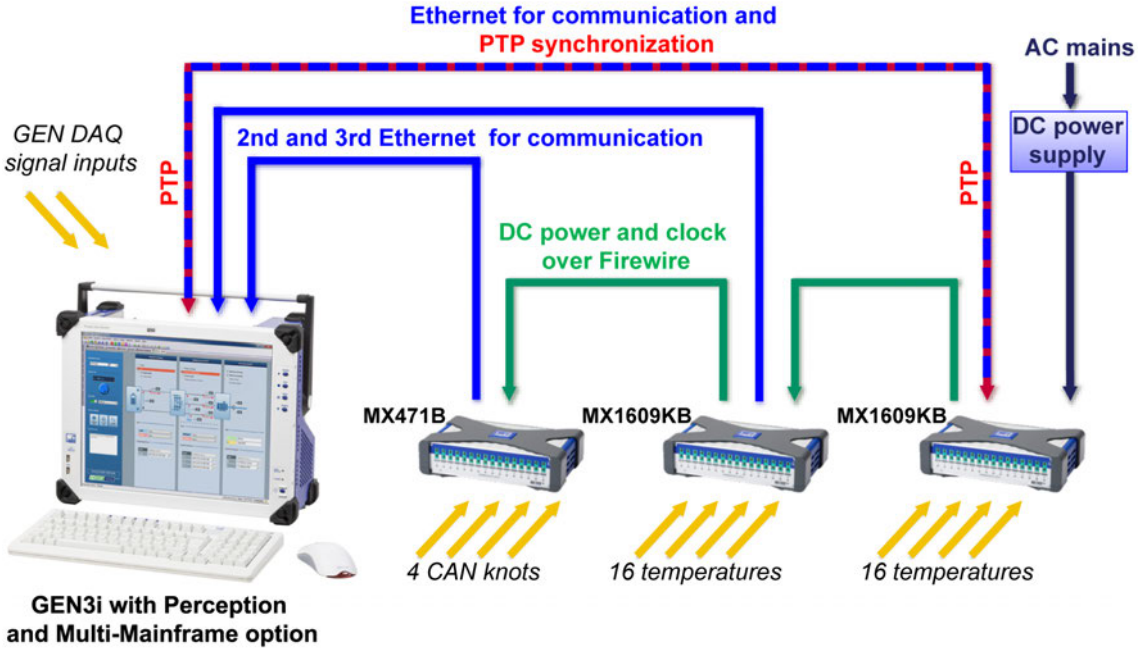


Figure I.12: GEN3i with a mix of three QuantumX "B" version modules

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i.*

Note **** All** modules must be "B" versions; one module must set to "clock master" and connected to the GEN3i PTP Ethernet.*

HINT/TIP

This setup uses multiple network ports on the GEN3i PC section.
Use fixed IP address setup with different base IP address and non-overlapping IP-ranges (Combination of base IP address and net mask) for each of the GEN3i network ports to make sure the setup always works.

Example setup:	
GEN3i network 1:	192.168.1.10 mask 255.255.255.0
GEN3i network 2:	192.168.2.10 mask 255.255.255.0
GEN3i network 3:	192.168.3.10 mask 255.255.255.0
QuantumX module 1:	192.168.1.11 mask 255.255.255.0
QuantumX module 2:	192.168.2.11 mask 255.255.255.0
QuantumX module 3:	192.168.3.11 mask 255.255.255.0

Background network details
If the network ports are configured for DHCP setup, each of the connections using the APIPA protocol to find a free IP address. As none of the network ports are linked together the APIPA protocol does not detect the address used any of the network devices in this setup. At random all QuantumX systems might end up with exactly the same network IP address. If this happens the systems are not uniquely addressable anymore and the communication fails.

I.3.4 GEN3i/GEN3iA/GEN7i with standard network switch and four or more of QuantumX "B" version modules

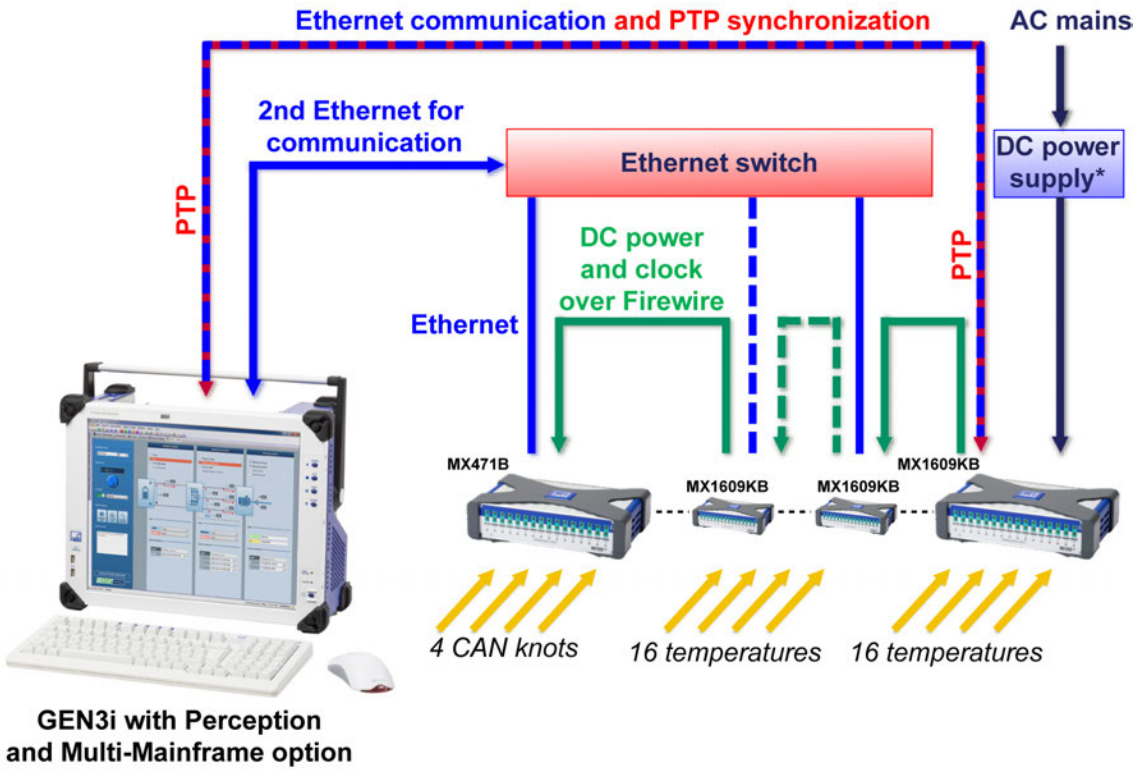


Figure I.13: GEN3i with multiple QuantumX "B" version modules

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i.*

Note ** Multiple QuantumX modules requires more than one power supply; see QuantumX documentation.*

Note *** **All** modules must be "B" versions; one module must set to "clock master" and connected to the GEN3i PTP Ethernet.*

HINT/TIP

This setup uses two network ports on the GEN3i PC section.
Use fixed IP address setup with different base IP address and non-overlapping IP-ranges (Combination of base IP address and net mask) for each of the GEN3i network ports to make sure the setup always works.

Example setup:	
GEN3i network 1:	192.168.1.10 mask 255.255.255.0
GEN3i network 2:	192.168.2.10 mask 255.255.255.0
QuantumX module 1:	192.168.1.11 mask 255.255.255.0
QuantumX module 2:	192.168.2.11 mask 255.255.255.0

Background network details
If the network ports are configured for DHCP setup, each of the connections using the APIPA protocol to find a free IP address. As the two network ports are not linked together the APIPA protocol on the PTP port does not detect the address used any of the network devices on the second network port. At random the PTP QuantumX system might end up with exactly the same network IP address as any of the other QuantumX systems. If this happens the two systems sharing the same IP address are not uniquely addressable anymore and the communication fails.

I.3.5 GEN3i/GEN3iA/GEN7i with PTP network switch and four or more of QuantumX "B" version modules

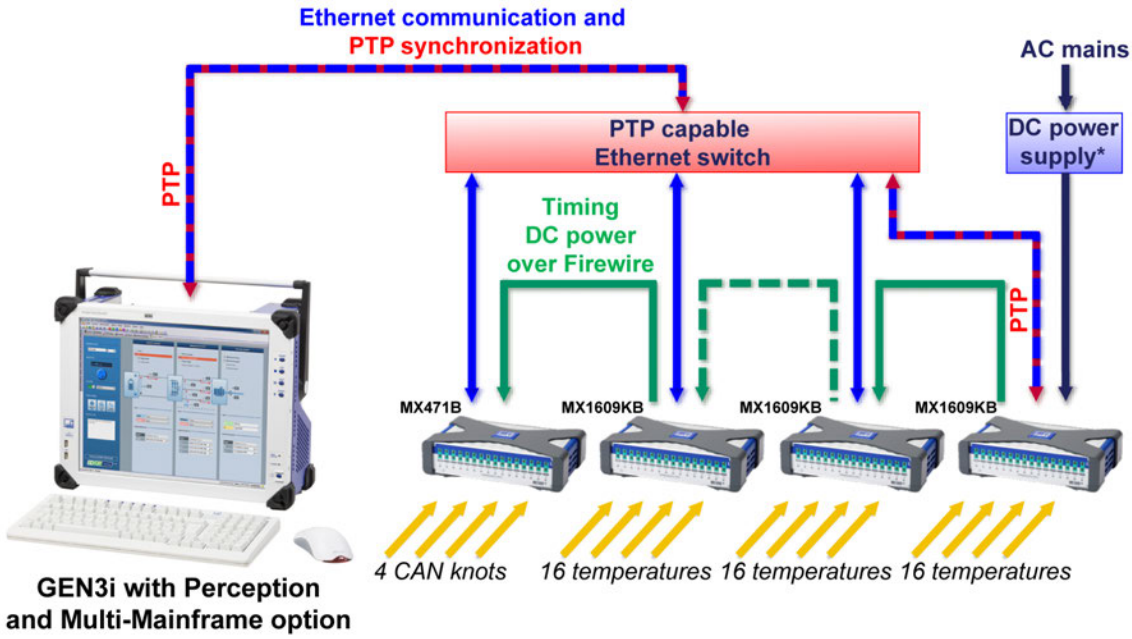


Figure I.14: GEN3i with multiple MX1609KB/MX1609TB - Using PTP switch

Note *Setup only shows GEN3i. GEN3i can be replaced by GEN3iA/GEN7i.*

Note ** Multiple QuantumX modules requires more than one power supply; see QuantumX documentation.*

HINT/TIP

This setup is preferred as it doesn't require any manual network setup. However it does require a PTP switch.

HINT/TIP

Perception V6.72 allows the PTP synchronization within the GEN series mainframes to be reduce to lower accuracies. With the lower sample rates used within the QuantumX this might be very acceptable within your application. Normal switches without PTP support can then be used without PTP synchronization error reports.

I.3.6 GEN3t/GEN7tA/GEN17tA with single QuantumX "B" version module

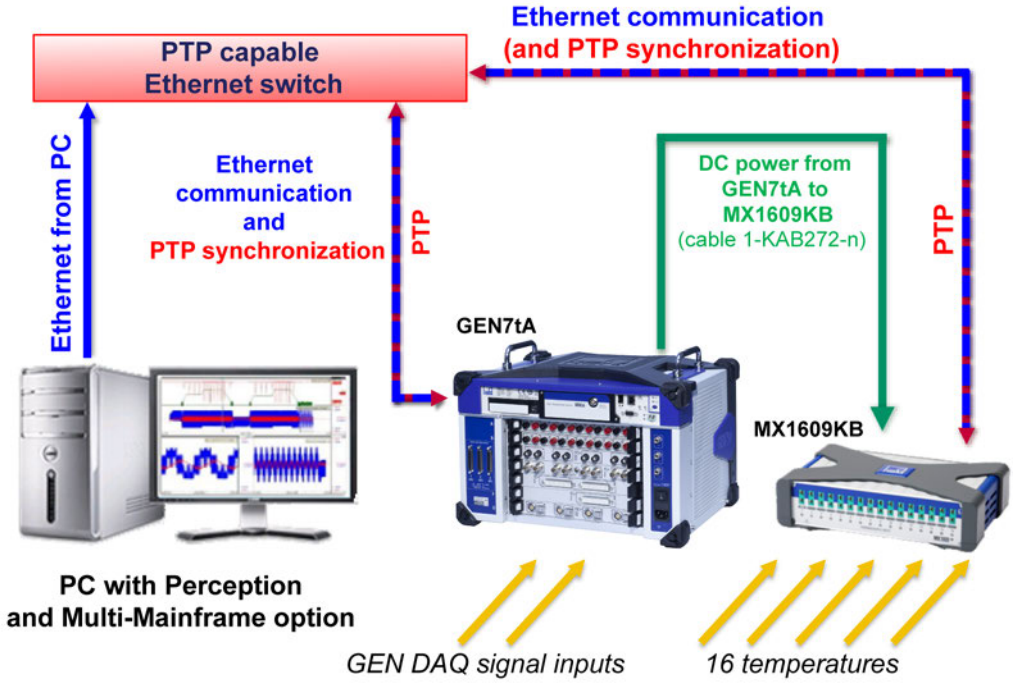


Figure I.15: GEN7tA with single QuantumX "B" version module

Note *Setup only shows GEN7tA. GEN7tA can be replaced by GEN3t or GEN17tA.*

I.3.7 GEN7tA with multiple QuantumX "B" version modules

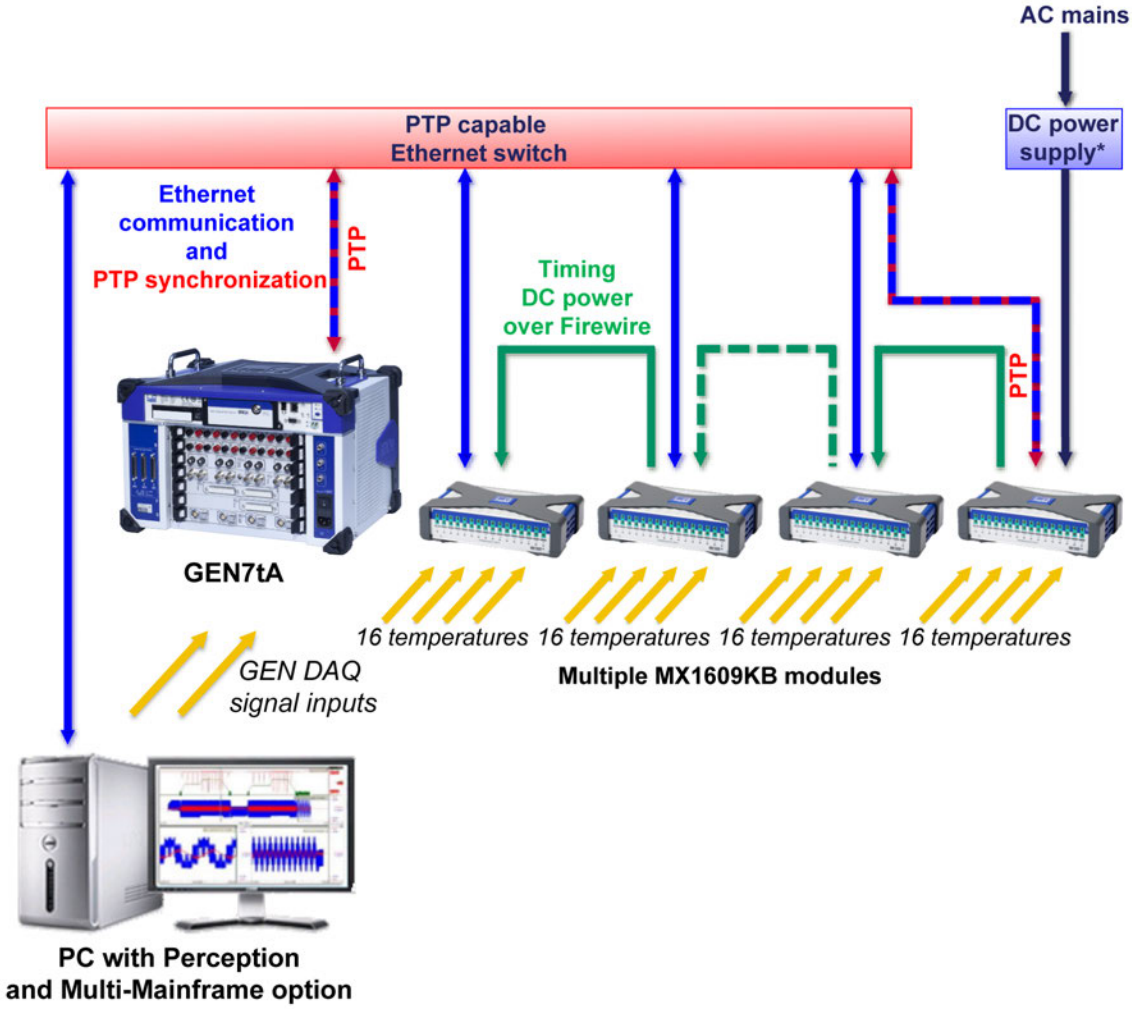


Figure I.16: GEN7tA with multiple MX1609KB/MX1609TB - Using PTP switch

Note *Setup only shows GEN7tA. GEN7tA can be replaced by GEN3t or GEN17tA.*

Note ** Multiple QuantumX modules requires more than one power supply; see QuantumX documentation.*

I.3.8 Genesis and QuantumX Setup using IRIG-to-PTP Bridge

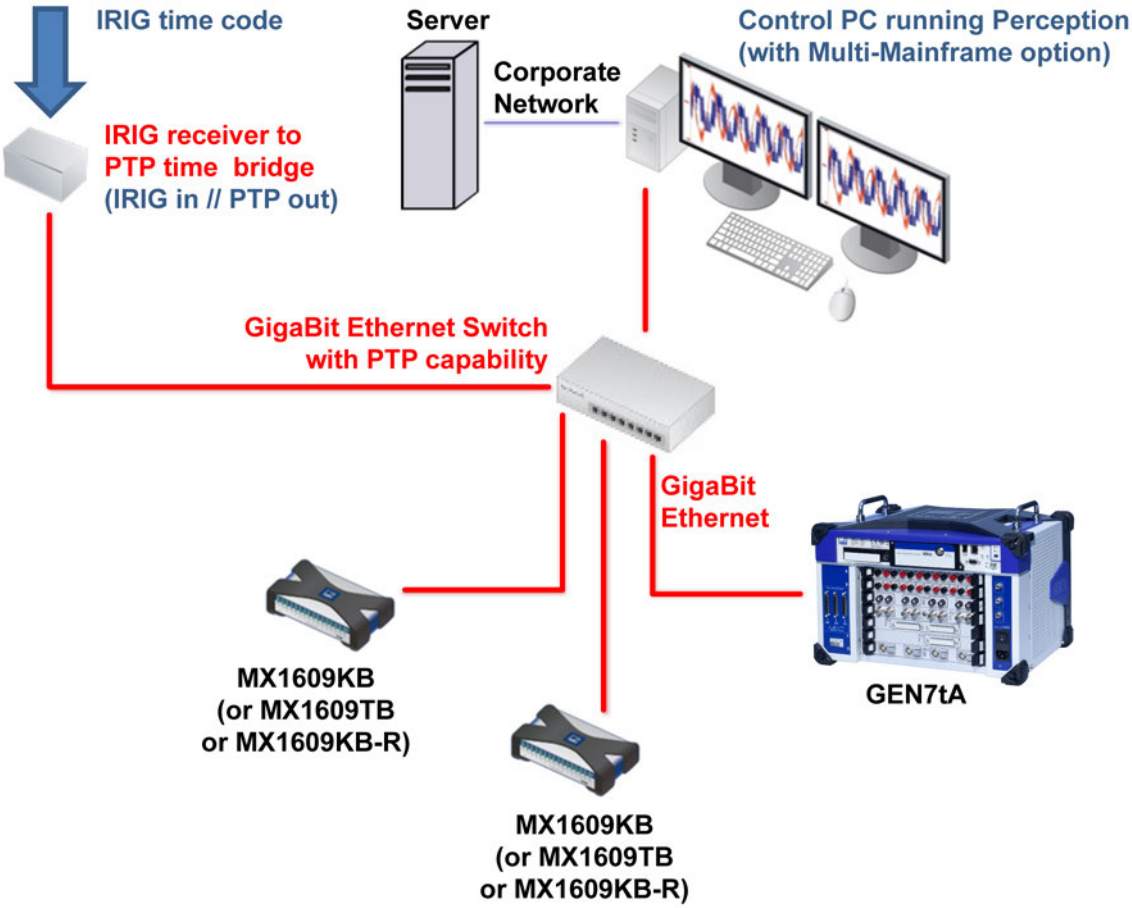


Figure I.17: Setup of IRIG-to-PTP Bridge

Note *GEN7tA can be replaced by GEN3t/GEN17tA/GEN3i/GEN3iA/GEN7i*

Settings in Perception

- Use the RJ45 connector for PTP support **(PTP 1)**.

I.3.9 PTP Grandmasters

IRIG or GPS to PTP bridge

- Successfully tested Symmetricom SyncServer® S350
- Equivalent model Symmetricom Xli GPS receiver (Model 1510-713)

Figure I.18: Symmetricom Xli GPS receiver

For more information please refer to: www.microsemi.com/

GPS to PTP Bridge
Successfully tested OTMC 100i Grand Master Clock

For more information, please refer to: www.omicron-lab.com/

I.3.10 PTP capable switch

- Successfully tested Siemens scalance xr324-12m

Figure I.19: Siemens scalance xr324-12m

For more information, please refer to the Siemens Scalance XR234-12M product page:
support.industry.siemens.com/cs/pd/515156?pdti=pi&dl=en&lc=en-NO

I.3.11 Using PTP and Master/Slave in combined setup

This is possible

- Master/Slave setup and PTP Synchronization.
- Set GEN3i as Master and GEN3t as Slave

Figure I.20: Example of correct PTP usage

Note *GEN3i can be replaced by GEN3iA/GEN7i.The GEN3t can be replaced by GEN7tA as slave.*

I.3.12 PTP configuration errors

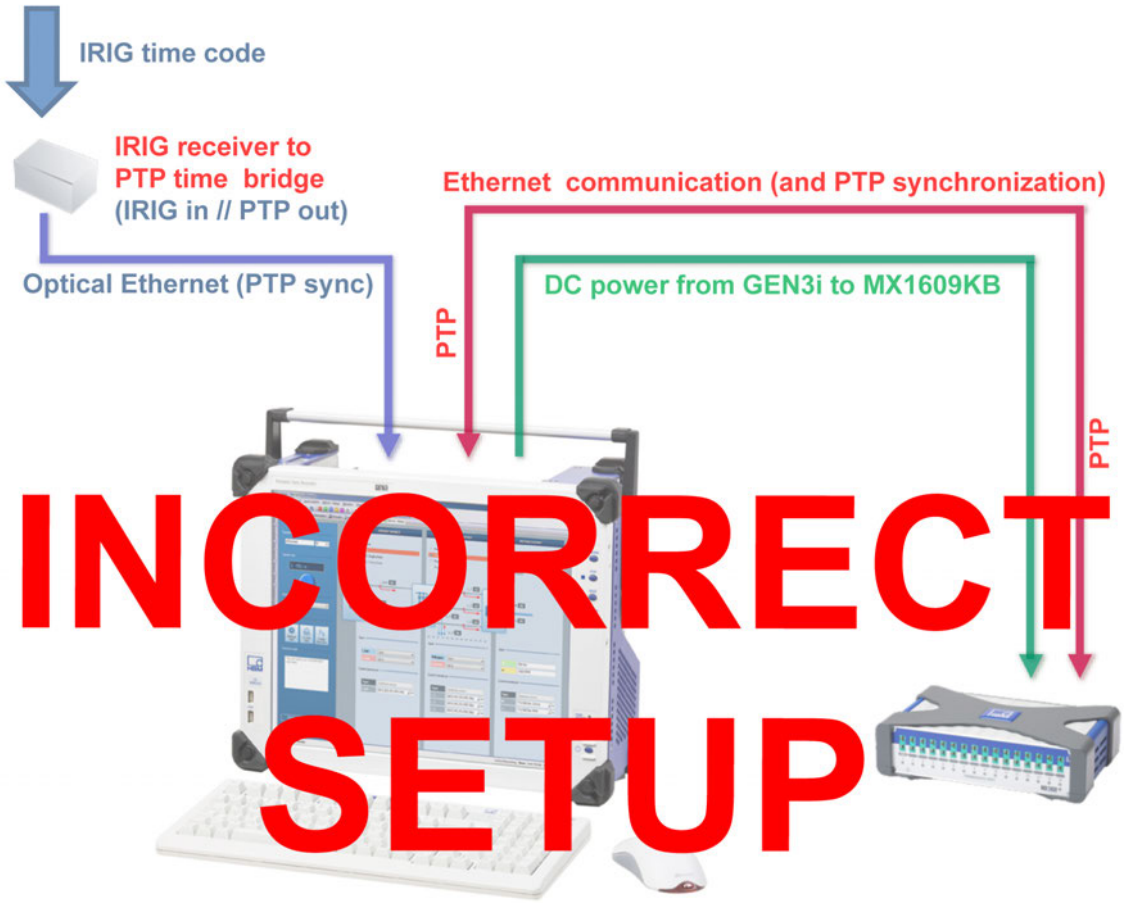


Figure I.21: Example of incorrect PTP usage

This is not possible!

- Set "Sync Source“ to PTP1 (RJ45) **or** to PTP2 (optical)
- Both at the same time is not possible: we don’t “bridge” PTP1 to PTP2

J Application Specific Usage

J.1 Rotational External Clock

GEN DAQ systems allow extensive setups for rotating external clock measurements. This document explains how to use the settings to get the job done.

J.1.1 GEN DAQ settings explained

All settings shown in this document can be found in the Perception software.

In Perception, activate the settings sheet as shown in Figure J.1.

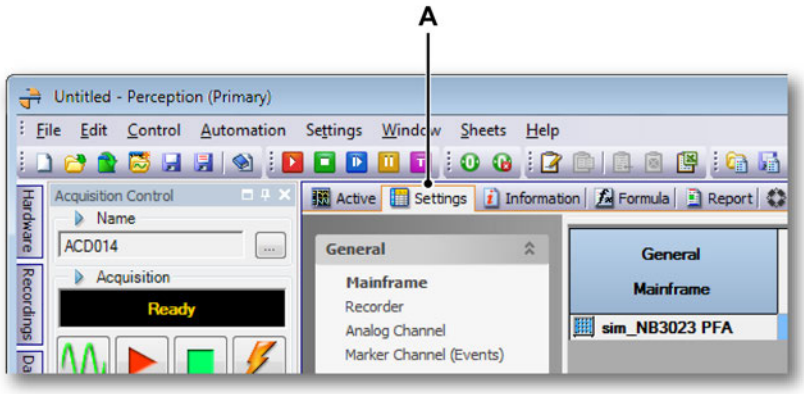


Figure J.1: Perception with activated settings sheet tab

A Settings sheet

Switch the settings sheet to show the advanced (dark grey) settings by using the Settings menu item **Settings ► Show Settings ► Advanced (All settings)**

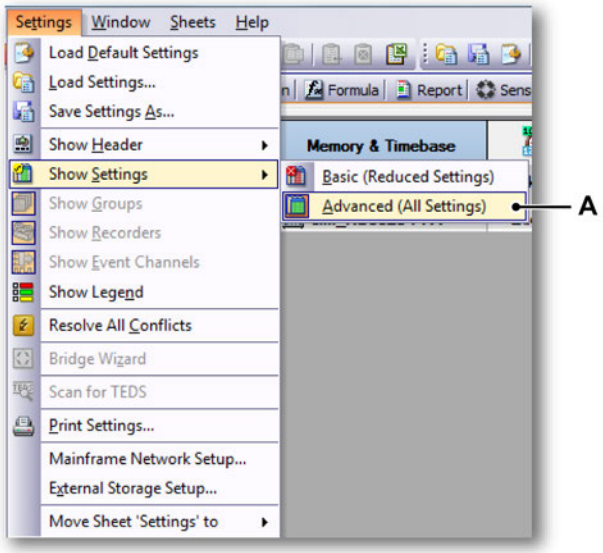


Figure J.2: Settings menu

A Advanced (All Settings)

J.1.2 Memory and Time base

Mainframe

In the settings sheet, select **Memory & Time base ▸ Mainframe**. The Mainframe setting sheet should look like Figure J.3.

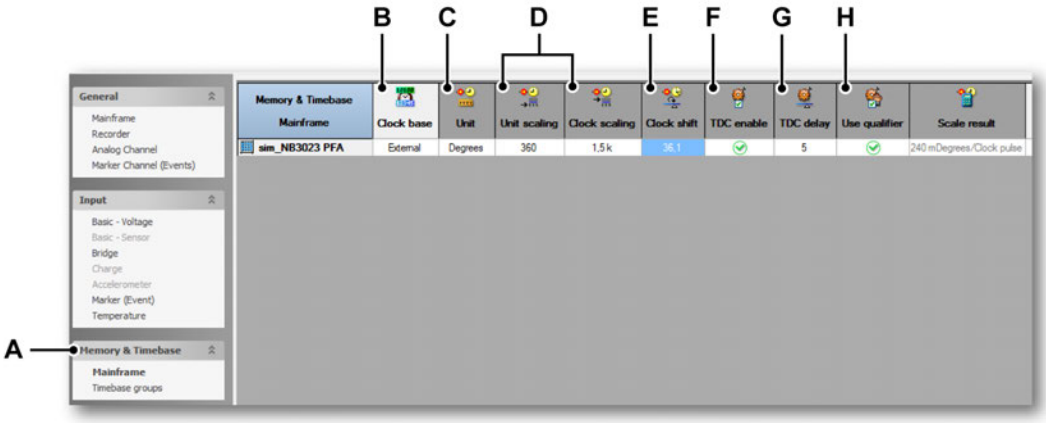


Figure J.3: Memory and Time base

A Memory and time base settings

B Clock base

C Unit

D Unit scaling/Clock scaling

E Clock shift

F TDC enable

G TDC delay

H Use qualifier

A Memory and time base settings

B Clock base
This setting must be set to “External”.

C Unit
During rotating measurements, this would be normally “Degrees”.

D Unit scaling and Clock scaling (Scale result)
These two settings define the relation between the external clock pulses and the units. The final setting is the division of these two settings. The setup uses two settings to ease the setup process and to avoid rounding errors whenever possible.
For example, when using a clock with 1500 pulses per 360 degrees cycle, then:

Unit scaling = 360
Clock Scaling = 1500

The result is shown in the read-only “Scale result”: 240 mDegrees/Clock pulse

E Clock shift: (TDC position)
This setting can be used to shift the position of the 0 degree indication on screen automatically. For example, if the TDC signal is not at the exact 0 degree position but comes in at 36.1 degrees, set the “Clock shift” to 36.1.

Note *Once the TDC point has been established, all samples recorded prior to TDC detection will be scaled backwards from this point.*

F TDC enable
When this setting is enabled, GEN DAQ systems will use the External Trigger input signal to automatically establish the 0 degree reference (TDC: Top Dead Center) for rotational measurements.

G TDC delay
The TDC delay parameter can be used to skip some of the beginning TDC signals, e.g. to avoid jitter TDC problems while starting engines.
Example: If this setting is set to 5, then the 0 degree position is linked to the 5^{th} occurrence of the TDC signal after start of recording in the GEN DAQ system.

H Use qualifier
This setting can be used to separate the ignition cycle from the exhaust cycle. Typically, the ignition and exhaust cycles are treated as a 720-degree rotation cycle together. For every 360-degree rotation, a TDC pulse will be generated by the engine. For the GEN DAQ system to separate the 0-degree TDC pulse from the pulse appearing at 360 degrees, we need a second signal, the TDC qualifier.

The TDC qualifier is implemented by using the alarm function of the GEN DAQ analog channels driving the alarm output of the GEN DAQ mainframe. The alarm status will be AND-ed with the external trigger input to produce the proper TDC signal selection. No additional wiring is required other than to measure the qualification signal of one of the analog channels.

To separate the ignition cycle from the exhaust cycle, we could measure the cylinder pressure, e.g. on Channel 1. Set the alarm level of Channel 1 to be active above 10 PSI. Disable all other alarm settings for all other channels in the system. Enable the Use Qualifier setting. If Channel 1 measures less than 10 PSI, the alarm output signal will disable the TDC detection. As soon as the pressure exceeds 10 PSI, TDC detection is enabled. If no TDC is detected before the pressure drops below 10 PSI again, the TDC detection is disabled again.

Recorder/Time base groups

Note *Perception V6.20 and earlier version use recorder settings for the next setting. In later version of Perception, these recorder settings have been replaced by Time base group settings. The basic behavior of the "External Clock Divider" is identical.*

External Clock Divider
This setting can be found in the Recorder Memory & Time base settings. The default value for this setting is 1, which means that samples are stored at each external clock pulse. If it is required that GEN DAQ only samples every third external clock pulse, setting the "External Clock Divider" to 3 will create the required sampling rate.

Note *GEN DAQ systems cannot sample at higher speeds than the external clock signal supplied.*

J.1.3 Calculating sample limits for external time base use

External sample rates are limited per card type. See the individual specification sheets of the different acquisition cards for details. Make sure and check that the maximum external sample rate is not exceeded. Exceeding the sample rate will results in missing samples at one or more external clock signal events.

Calculation example
Engine runs at 10 000 RPM maximum.

6 000 RPM equals 100 rotations per second.

For example, with a maximum external clock speed of 500 kS/s (all acquisition cards having a maximum sample rate of 1 MS/s), the maximum pulses per rotation are:

500 000 / 100 = 5 000 pulses per rotation maximum

However, it is not advaisable to exceed 10% of the maximum sample rate of the acquisition card used. When in external clock mode, GEN DAQ systems internally operate on the maximum sample rate, storing the next sample after an external clock has been detected.

Using a 1 MS/s acquisition card, an external clock at 500 kS/s would appear to contain jitter of up to 1 us. The jitter is then 50% of the external clock time period (1/500 kS/s = 2 µs).

Note *One way to overcome exceeding the maximum external sample rate of the card of choice might be to use the "External Clock Divider". The maximum external clock rate of the GEN DAQ mainframe is 2 MS/s. Using an "External Clock Divider" of 4 would allows the 1 MS/s card to run an external clock rate of 2 MS/s. It does not increase the measurement resolution, but it does allow a measurement at higher external clock rates.*

J.1.4 Perception Display settings explained

The Perception displays are capable of handling external time base recordings in different ways. The setup is controlled by using the display's X-Annotation Scaling settings.

These settings can be found by right clicking the mouse in the display of choice and by selecting "Display Setup" at the bottom of the menu.

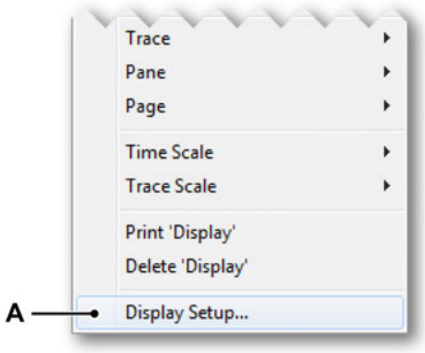


Figure J.4: Perception - Display setup

A Display setup

In the **Setup of Display** dialog, select the **Annotation & Grid** tab. For external time base recordings, select the X-Annotation scaling to **Position**. In this mode, there are three ways to show the X-axis.

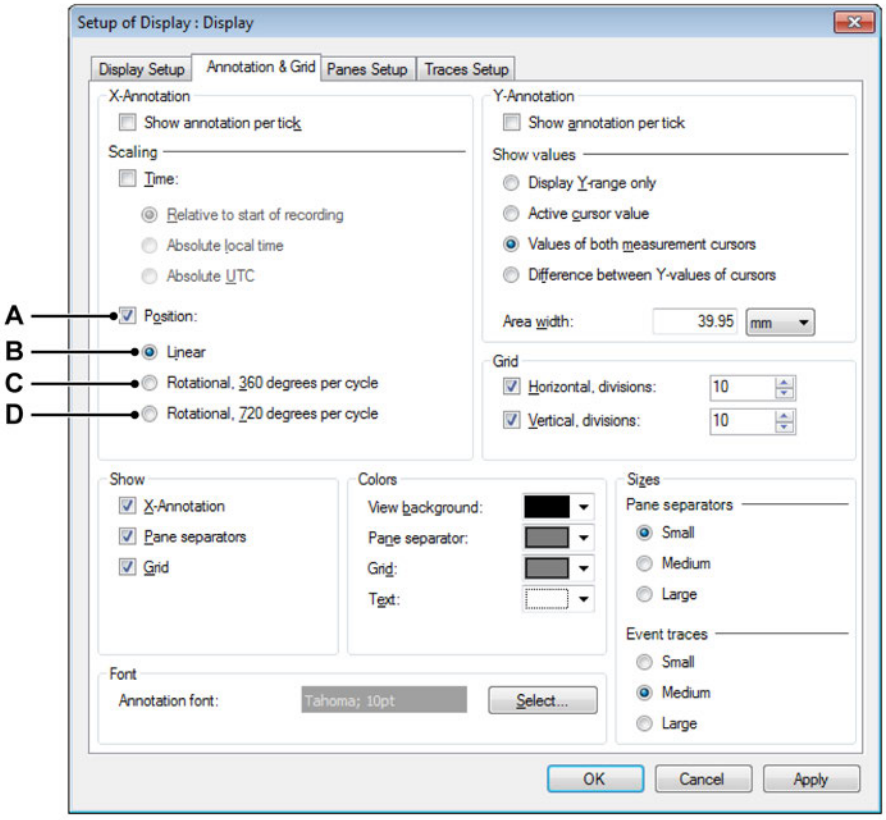


Figure J.5: Display Setup dialog - Annotation & Grid

A X-Annotation/Position check box

B Linear

C Rotational, 360 degrees per cycle

D Rotational, 720 degrees per cycle

A **Linear**
The X position is expressed in units as selected in the Mainframe – “Memory & Time base” settings dialog.
E.g. 1000 degrees will be shown as 1000 degrees on the X-axis.

B **Rotational, 360 degrees per cycle**
The X position is expressed by 360 degrees cycles and the number of remaining degrees.
E.g. 1200 degrees will be shown as 3:120, which means 3 cycles and 120 degrees.

C **Rotational, 720 degrees per cycle**
The X position is expressed by 720 degrees cycles and the number of remaining degrees.
E.g. 1200 degrees will show as 1:480, which means 1 cycle and 480 degrees.

Perception will use the TDC setup process to determine the proper 0 degree point. (For more information on how to use these settings, please refer to “TDC Enable” and “TDC qualifier”
(Figure J.3 "Memory and Time base" on page 842)).

J.1.5 Cylinder Pressure Analysis option package

HBM offers a special custom software package for Perception to analyze some parameters of combustion engines.

The basic purpose of the current program version is to receive the following information from a cylinder pressure measurement:

- Determine which cycle had the absolute maximum pressure peak during the full recording
- Determine which cycle had the absolute minimum pressure peak during the full recording
- Calculate the mean pressure cycle of all cycles during the full recording

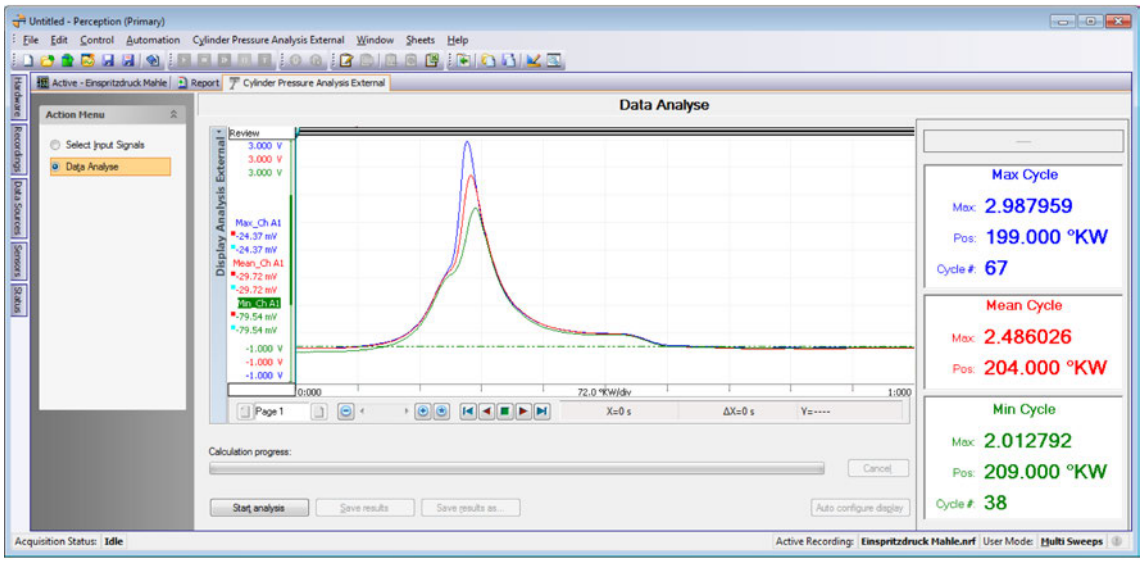


Figure J.6: Cylinder Pressure Analysis dialog

J.1.6 Cylinder Pressure Analysis customer evaluation

HBM offers a 30 day evaluation version of this special software to see if this meets the requirements.

Special wishes can be adapted as cost option after consulting our CSI programmer.

J.1.7 Cylinder Pressure Analysis and TDC settings

The Cylinder Pressure Analysis application is able to use all of the available TDC settings. When properly used during the recording process, the defined **Offset**, **Analysis interval** and **Cycle size** of the Cylinder pressure analysis CSI will automatically process every new recording without user interaction.

Defining the **Cycle Size**, the **Analysis Interval** and analysis **Offset** relative to the **TDC** signal is done using the configuration dialog of the Cylinder Pressure Analysis application as shown in Figure J.7.

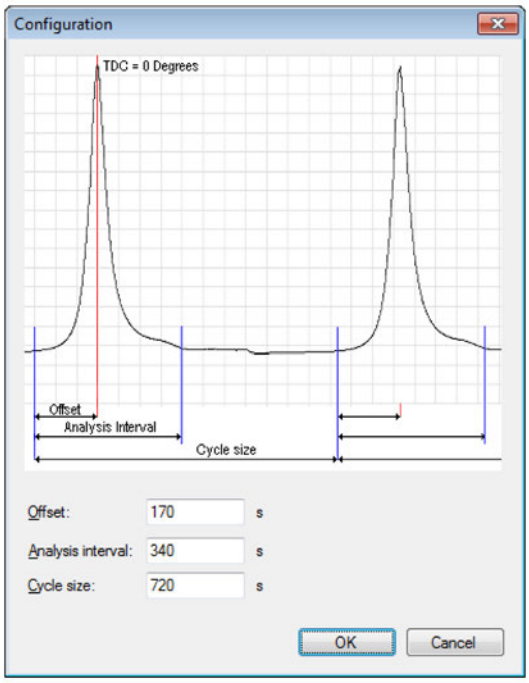


Figure J.7: Cylinder Pressure Analysis Configuration

J.2 dY/dT Triggering

Basic setting definitions:

dY: The result of subtracting two ADC values

dT: Specifies the time between the two samples subtracted

These two setting values are independent of each other. The user therefore needs to specify both settings explicitly for the trigger unit to do a correct job. Neither Perception nor the GEN series can recalculate the two settings to extract a useable setting. It is the user that needs to specify both settings within limits that the GEN series can use.

Notes on setting definitions:

dY: Specified in technical user units so the value scales with changes to technical units. Maximum dY depends on your amplifier range and technical unit scaling. Perception might turn the background yellow to inform of a change in the amplifier settings, which is required to be able to actually generate a trigger for you. Assuming the amplifier is set to a range of 100 V, and the dY of 110 V can never be measured with this sensitivity. Applying a technical unit multiplier of 10 or decreasing the amplifier sensitivity to 200 V range both would make this setting valid. Do not expect Perception to re-calculate the dY/dT of 110 V/10 ms to 55 V/5 ms. Recalculation would lead to completely different trigger behavior as the noise sensitivity goes down from 110 V to 55 V and this might not be what is expected.

dT: Specified in seconds, used in samples. Setting is sample rate dependent. Maximum dT in samples is 1023. For user convenience, entry in time is offered, but the hardware works in samples. Therefore, changing sample rates might make your setting unusable. For example, 1023 ms is OK as long as the sample rate is 1 kS/s. At 1 MS/s, the maximum dT time is 1.023 ms.
Whenever a dT is unusable with the selected sample rate, the background of this setting will turn yellow within Perception (Perception indicates this setting is not valid with the current time base settings that are dependent on this setting).

Remember:
Always specify your requested dY and dT values the way you expect to GEN series to look at your signals.

Example:

- dY set to -4 V
- dT set to 2 ms
- Basic trigger
- Falling edge

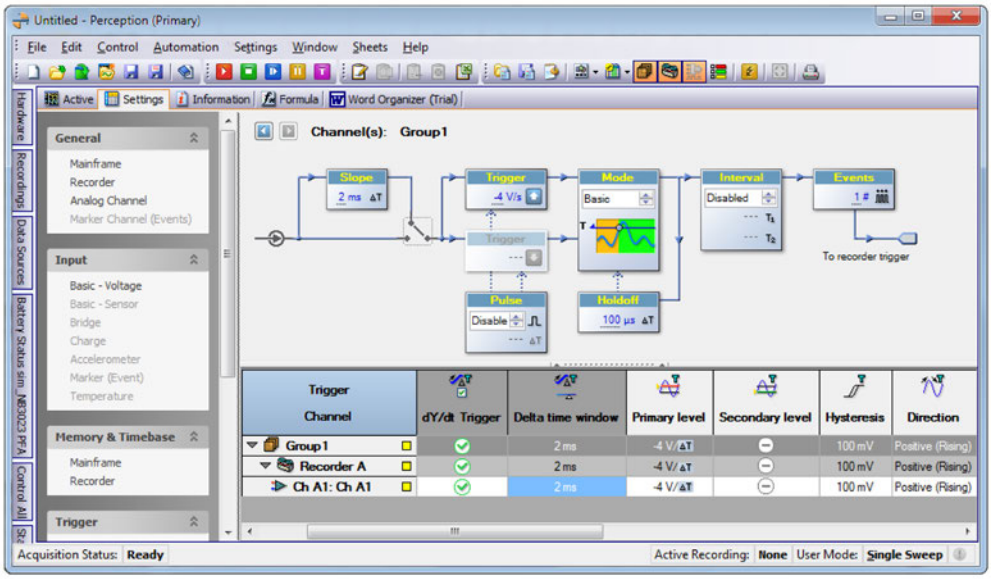


Figure J.8: Example of a dY/dT triggering

In the next images, the two cursors are set to 2 ms. This means the difference between the blue and the red cursor will be the value sent to the trigger unit.

- Next sample recorded (sample of blue cursors, see Figure J.9)
- Difference is -2.451 V
- dY not met, no trigger

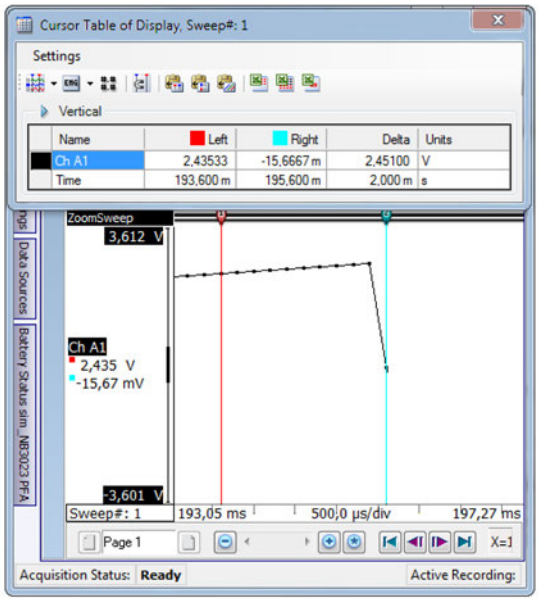


Figure J.9: Sample recording 1

- Next sample recorded (sample of blue cursors, see Figure J.10)
- Difference now is -3.81633 V
- dY not met, no trigger

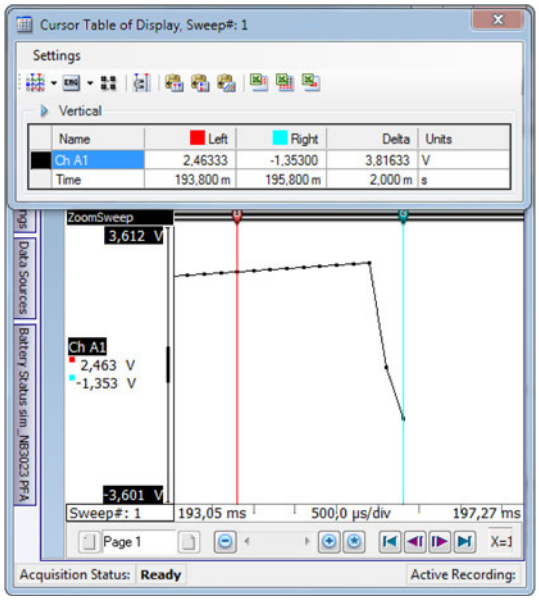


Figure J.10: Sample recording 2

- Next sample recorded (sample of blue cursors, see Figure J.11)
- Difference now is -4.49867 V
- dY met
- As previous dY was higher value, this is a falling edge: trigger

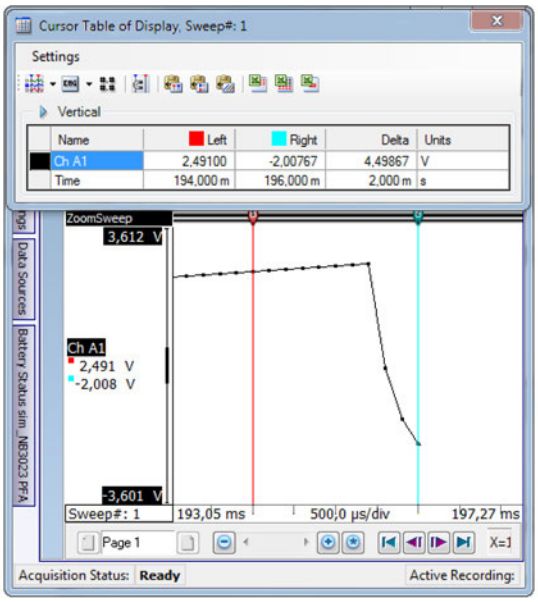


Figure J.11: Sample recording 3

Note *Trigger edge in this case is the edge of the differentiated signal, not the signal itself.*

J.3 Calculating maximum fiber cable length

Maximum optical fiber length is determined by two major factors: optical loss and bandwidth limit. These types of optical fiber performance and quality are defined in the ISO standard ISO/IEC 11801.

OMx/OCx = ISO/ IEC 11801 standard (optical fiber type)	For wave-length	Optical power budget	Cable loss	Coupler loss. ANSI/TIA/ EIA-568-A	BW Length limit
OM1 = Multi Mode 62.5/125 µm	850 nm	8 dB	-3.5 dB/km	-0.75 dB	200 MHz*km
OM2 = Multi Mode 50/125 µm	850 nm	8 dB	-3.5 dB/km	-0.75 dB	500 MHz*km
OM3 = Multi Mode 50/125 µm laser optimized fiber	850 nm	8 dB	-3.5 dB/km	-0.75 dB	2000 MHz*km
OM4 = Multi Mode 50/125 µm laser optimized fiber	850 nm	8 dB	-3.5 dB/km	-0.75 dB	4700 MHz*km
OS1 = Single Mode 9/125 µm	1310 nm	10 dB	-1 dB/km	-0.75 dB	N/A
OS2 = Single Mode 9/125 µm	1310 nm	10 dB	-0.4 dB/km	-0.75 dB	N/A

Note *Table shows worst-case specifications.*

Standard GHS systems use VCSEL 850 nm optical transmitters/receivers; they have an optical power budget of 8 dB. Calculating the maximum length of optical cable can be done in the following manner:

Optical budget GHS system 850 nm	:	8 dB
Maximum fiber cable length	:	$L_{optical}$ (km)
Fiber cable loss	:	-3.5 dB/km
Number of couplers	:	c
Coupler loss	:	-0.75 dB
Safety margin for aging and repair	:	-3 dB

$$L_{optical} = -\frac{8dB + (c * -0.75dB) + (-3\,dB)}{-3.5dB}\ (km)$$

This formula also applies to Single Mode systems

For example, if two couplers are used in the cable, c = 2, the maximum length would be $L_{optical}$ = 1 km

The second limiting factor for cable length is fiber cable bandwidth.
Bandwidth limit is caused by light pulse dispersion in the optical fiber; this only affects Multi Mode fiber systems.
This limit is the product of the GHS system's maximum signaling speed and the defined fiber cable bandwidth.

GHS signaling speed over optical fiber	:	1000 MHz
OM class defined bandwidth	:	BW
Maximum fiber cable length	:	L_{BW} (km)

$$L_{BW} = \frac{BW}{1000MHz} \ (km)$$

For example, if an OM2-type cable is used, the maximum length will be L_{BW} = 0.5 km

The maximum optical fiber length that can be used in a setup is the shortest outcome of $L_{optical}$ or L_{BW}

If the two examples above are followed, the optical fiber length must be limited to L_{BW} = 0.5 km

J.4 Wake On LAN support (WOL)

Several of the GEN series mainframes support Wake On LAN features (WOL). WOL is only supported on copper or optical networks. WOL is not supported by wireless networks.

At the time of this manual's release, the following mainframes support WOL:

- GEN3i
- GEN3iA
- GEN7i
- GEN3t
- GEN7tA
- GEN17tA

WOL can turn the GEN series mainframe on from the “S5”' power state when power is connected to the mainframe and the power switch at the net entry is switched to the “1” or “on” position. In this state, the power can be turned on by sending a “magic packet” to one of the mainframe's wired network ports. The magic packet must contain the MAC or Physical address of the connected network port.

Generating a magic packet can be done with third party tools or custom-built applications. Search the internet using “Wake On LAN” and several freeware tools show up. HBM is not responsible for any of the (freeware) tools found using this search method.

WARNING

Whenever a mainframe is powered off by using a forced power down (keeping the standby button pressed for five seconds), the WOL feature is disabled. Always allow the system to power down normally to enable the WOL feature.

HINT/TIP

When a mainframe's power is interrupted externally, re-applying power to the mainframe immediately starts the mainframe (no WOL magic packet is required).

WAN (Wide Area Network) support

As the name WOL indicates (Wake on LAN), there is no direct support outside the boundaries of your LAN (Local Area Network). A LAN typically ends as soon as routers or layer 3 switches are used to transfer network data from point A to point B. Routers are typically used to access the internet. Layer 3 switches are typically used to control network traffic within larger facilities to avoid unwanted network traffic on different segments within the network.

- Without using routers or layer 3 switches, magic packets can be sent within a LAN without problems.
- When your company uses layer 3 switches, your IT department might need to help you set up their layer 3 switches to allow WOL magic packets to reach your remote GEN series system.
- Sending the magic packets for WOL from a location outside the LAN (WAN setup) may require a VPN connection to the target LAN or special settings to the LAN internet router.

For additional information on Wake On LAN, please refer to:
en.wikipedia.org/wiki/Wake-on-LAN

J.4.1 Locating GEN3i, GEN3iA and GEN7i MAC/Physical address

For **GEN3i**, **GEN3iA** and **GEN7i**, the MAC/Physical address can be found in Windows® in the following manner:

1 Connect the required network port.

2 Go to Windows® **Network and Sharing Center**. Select **Local Area Connection (A)**.

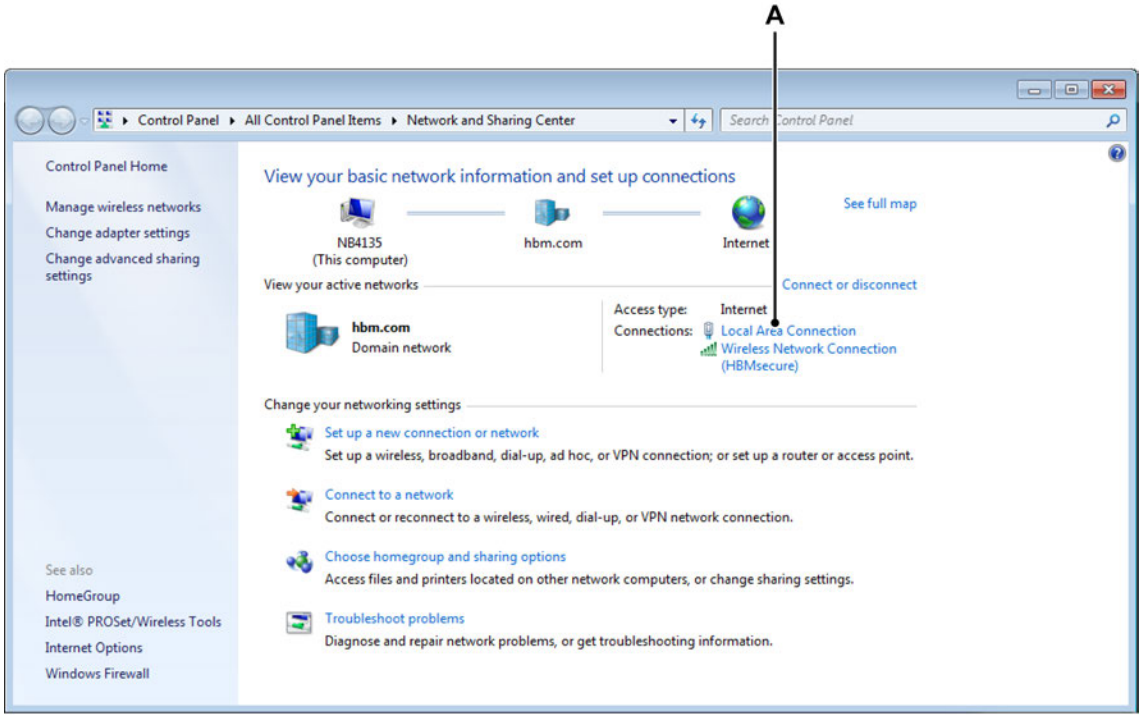


Figure J.12: Network and Sharing Center

A Local Area Connection

3 The **Local Area Connection Status** dialog opens. Select **Details**.

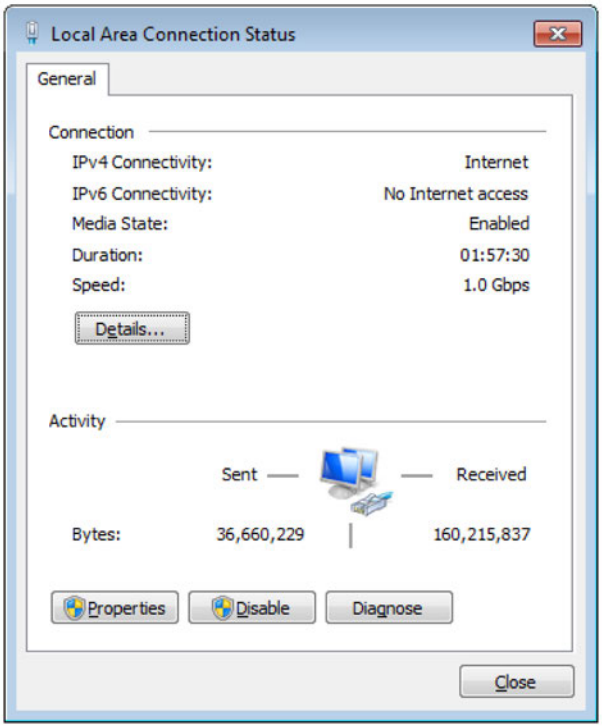


Figure J.13: Local Area Connection Status

4 The **Network Connection Details** dialog opens.

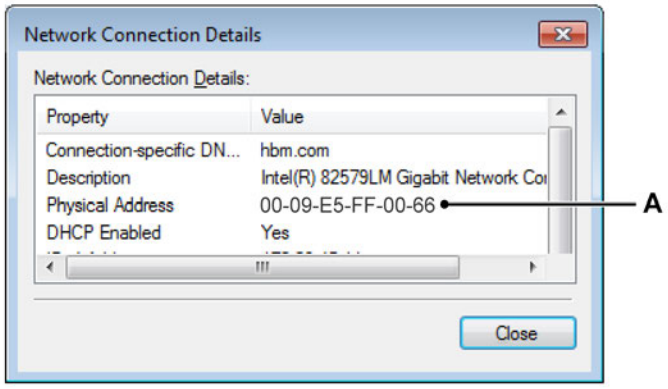


Figure J.14: Network Connection Details

A MAC/Physical address

The MAC/Physical address of the selected network connection is displayed in the **Network Connection Details** dialog as a twelve character string.

J.4.2 Locating GEN3t, GEN7tA and GEN17tA MAC/Physical address

For **GEN3t, GEN7tA** and **GEN17tA**, the MAC/Physical address can be found in Perception in the following manner:

1 Start the Perception software

2 Connect to either GEN3t, GEN7tA or GEN17tA.

3 Enable the **Properties Window** (see Figure J.16); this can be found in the Perception “Windows” menu.

4 Open the **Hardware** window. Select the target mainframe **(A)**. Right click on the mouse to open the context menu. Select **Mainframe view (B)**.

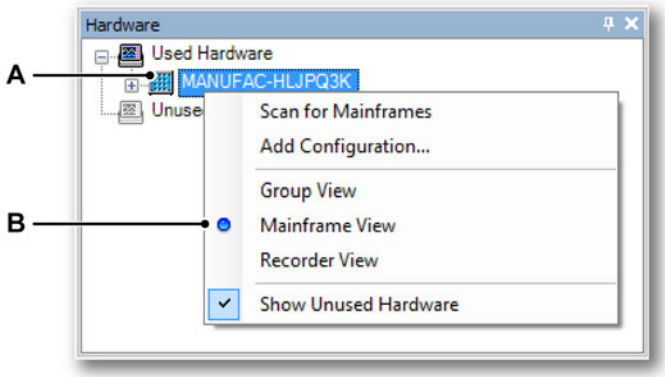


Figure J.15: Hardware window in Perception

A Target mainframe

B Mainframe view

5 The MAC/Physical address of the selected network connection is displayed in the **Properties window** as a twelve character string.

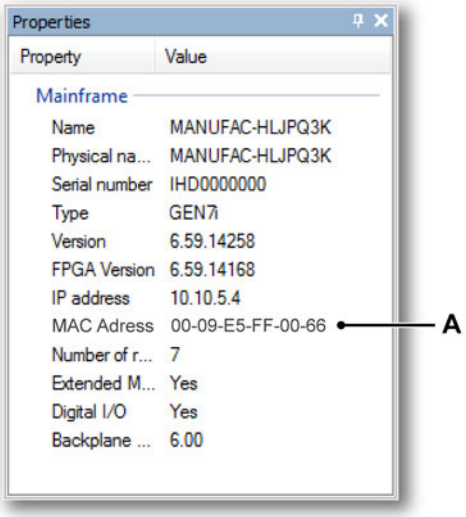


Figure J.16: Properties window in Perception

A MAC/Physical address

J.5 Configuring an encoder with direction and reset

Pins and Connectors:

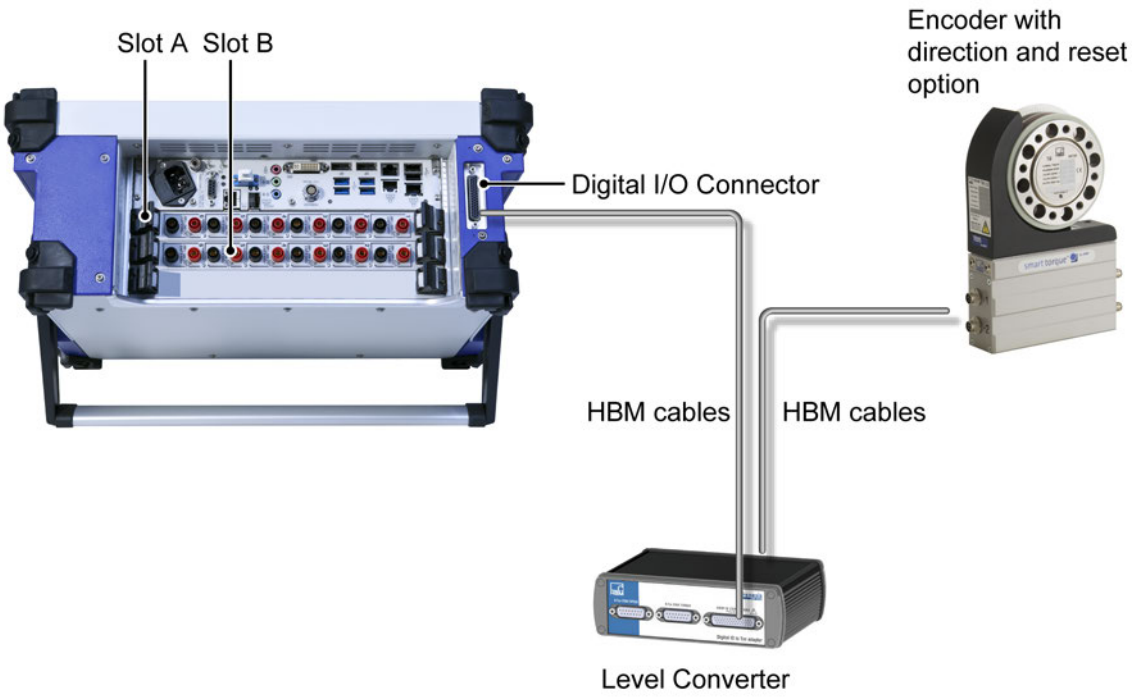


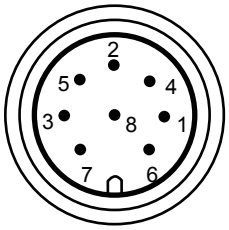
Figure J.17: Connecting Encoders with reset and direction options to a GEN3i

The following descriptions shows how to configure the encoder:

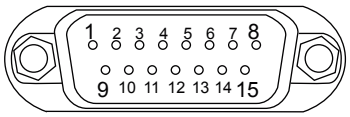
- Pins and connectors from encoder to level converter (see chapter "From encoder to level converter" on page 861)
- Pins and connectors from level converter to digital I/O connector on the mainframe (see chapter "From level converter to Digital I/O connector on the mainframe" on page 864)

J.5.1 From encoder to level converter

The Level converter 1-G070-2 offers the possibility to connect two speed connectors to two different encoders. In this example, the B-TxxCON2 Speed connector of the Level Converter is used. HBM cables 1-KAB149-6 and 1-KAB163-6 are designed to be used with the Level Converter. KAB149 is compatible with the Torque interface connector; KAB163 is compatible with the Speed/RPM interface connector.



Top view



T12 speed	Txx adapter speed

Plug pin	**Assignment**	**TXX adapter Speed**
1	Rotational speed measurement signal (pulse string, 5 V; 0°)	Pin 12
2	Reference signal (1 pulse/revolution, 5 V)	Pin 2
3	Rotational speed measurement signal (pulse string, 5 V; 90° phase shifted)	Pin 15
4	Reference signal (1 pulse/revolution, 5 V)	Pin 3
5	Not in use	
6	Rotational speed measurement signal (pulse string, 5 V; 0°)	Pin 13
7	Rotational speed measurement signal (pulse string, 5 V; 90° phase shifted)	Pin 14
8	Operating voltage zero	Pin 8
	Shielding connected to housing ground	

The signal from the encoder has the following characteristics:

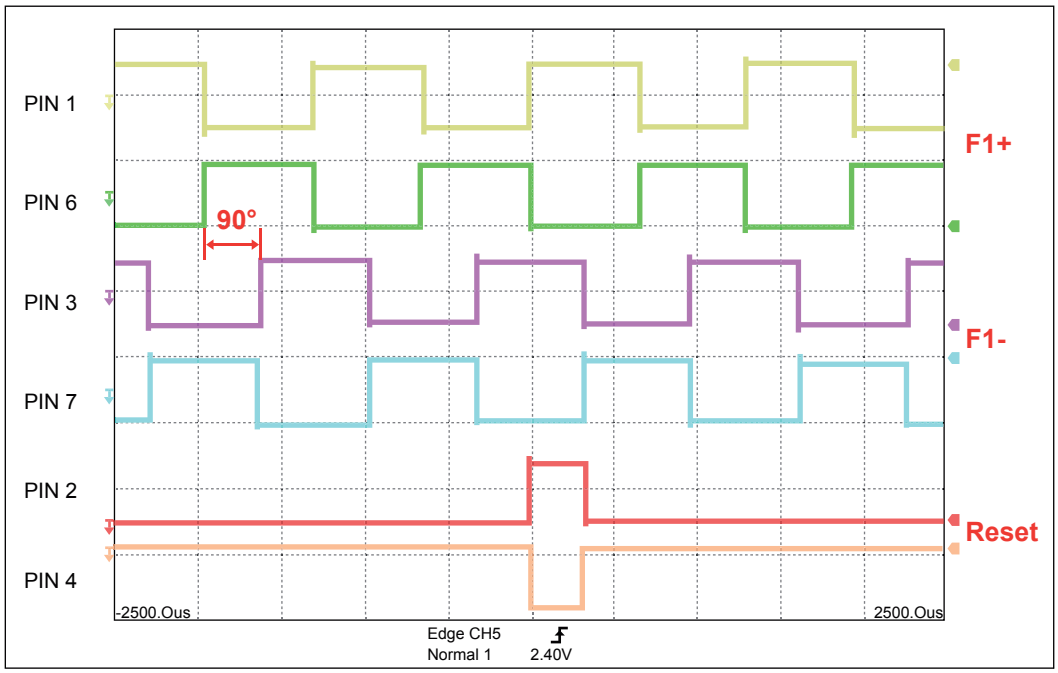


Figure J.18: Rotational speed signals at level converter

J.5.2 From level converter to Digital I/O connector on the mainframe

This cable is included with the level converter (1-G070-2).

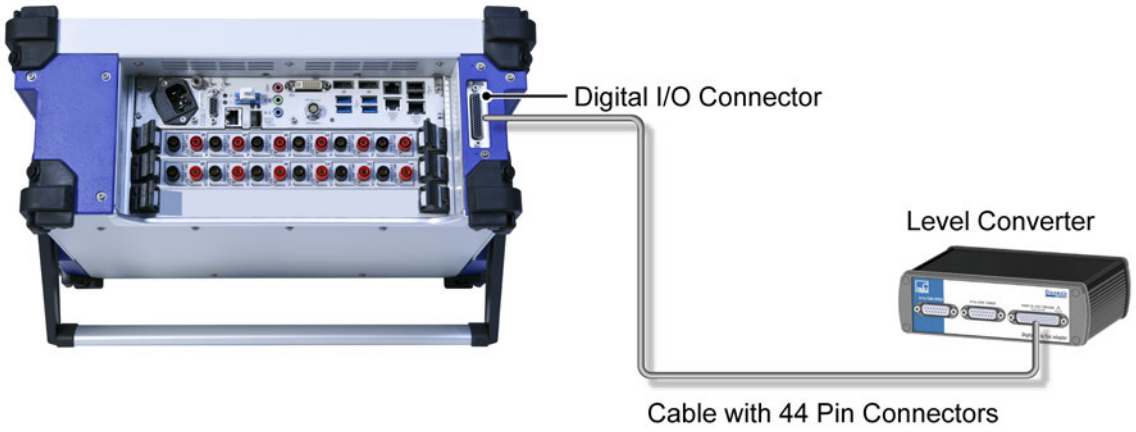
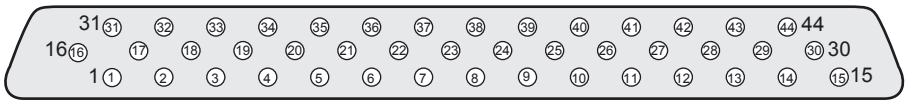


Figure J.19: Connecting a GEN3i from level converter to a digital I/O connector

J.5.3 Activate Digital I/O channels with Perception

In order to activate the Digital I/O channels, including the counter/timer channels, a module that supports the Digital I/O connector must be installed. Not all input modules in the GEN series family support the Digital I/O connector. In this example, the two 1kV modules which activate four counter timer channels (two counter channels per module) are used.

The Timer/Counter channels that are active depend on which pins of the Digital I/O connector are used:



A
- **PIN 1 - Event Input 1A & Reset Timer/Counter 2A**
- **PIN 2 - Event Input 2A & Direction Timer/Counter 2A**
- **PIN 3 - Event Input 3A & Clock Timer/Counter 2A**
- PIN 4 - Event Input 4A
- PIN 5 - Event Input 5A
- PIN 6 - Event Input 6A
- PIN 7 - Event Input 7A
- PIN 8 - Event Input 8A
- PIN 9 - Event Input 9A

B
- **PIN 10 - Event Input 10A & Reset Timer/Counter 1A**
- **PIN 11 - Event Input 11A & Direction Timer/Counter 1A**
- **PIN 12 - Event Input 12A & Clock Timer/Counter 1A**

C
- **PIN 13 - Event Input 1B & Reset Timer/Counter 2B**
- **PIN 14 - Event Input 2B & Direction Timer/Counter 2B**
- **PIN 15 - Event Input 3B & Clock Timer/Counter 2B**
- PIN 16 - Event Input 4B
- PIN 17 - Event Input 5B
- PIN 18 - Event Input 6B
- PIN 19 - Event Input 7B
- PIN 20 - Event Input 8B
- PIN 21 - Event Input 9B

D
- **PIN 22 - Event Input 10B & Reset Timer/Counter 1B**
- **PIN 23 - Event Input 11B & Direction Timer/Counter 1B**
- **PIN 24 - Event Input 12B & Clock Timer/Counter 1B**
- PIN 25 - Event Input 13B
- PIN 26 - Event Input 14B
- PIN 27 - Ground
- PIN 28 - Ground
- PIN 29 - Ground
- PIN 30 - Ground
- PIN 31 - Event Input 15B & External Stop B
- PIN 32 - Event Input 16B & External Start B
- PIN 33 - Event Input 13A
- PIN 34 - Event Input 14A
- PIN 35 - Event Input 15A & External Stop A
- PIN 36 - Event Input 16A & External Start A
- PIN 37 - Event Output 2B
- PIN 38 - Event Output 1B
- PIN 39 - Event Output 2A
- PIN 40 - Event Output 1A
- PIN 41 - Ground
- PIN 42 - Ground
- PIN 43 - +5 V Power
- PIN 44 - +5 V Power

Figure J.20: Pin diagram for Digital Event/Timer/Counter connector

A Card A-Txx CON2 Speed Channel A9

B Card A-Channel A8

C Card B-Txx CON2 Speed Channel B9

D Card A-Channel B8

In this example (see Figure J.20), Recorder A and Recorder B are 1kV modules (six channels each). The event channels supported by the module are assigned the next available channel number after the analog channels. In this case, that is Channel 7; for Recorder B, the event channels are assigned channel names of Ev B7-01 to Ev B7-16.

The two counter timer channels supported by Recorder B are Channel B8 (Timer/Counter2A, see Figure J.20) and Channel B9 (Time/Counter2A, see Figure J.20). In Perception, the channels are named Ch B8 and Ch B9 (see Figure J.21).

For this example, connect one B-Txx CON2 Speed and wire it to the Ch B9 counter (Pins 13, 14, 15 on the digital input connector).

Note *Perception allows you to view each of the inputs individually as an event channel in addition to seeing the counter result.*

The reset signal is Ev B7_01, the input F1- is Ev B7_02 and the input F1+ is Ev B7_03. If you only need to view the Timer/Counter result and have no interest in the individual signals, do not activate the event channels. This will decrease the size of the final data file by not recording channels that are not needed.

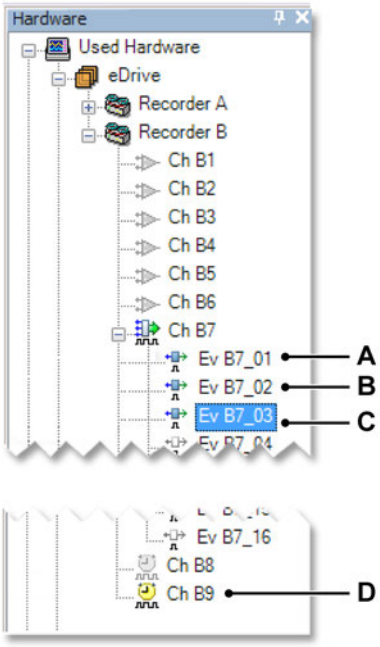


Figure J.21: Channels in Perception

A Reset

B F1-

C F1+

D B-Txx CON2 Speed

To activate Channel 8 or Channel 9 in Perception

1 Change the resolution of Recorder B to **18 bit**

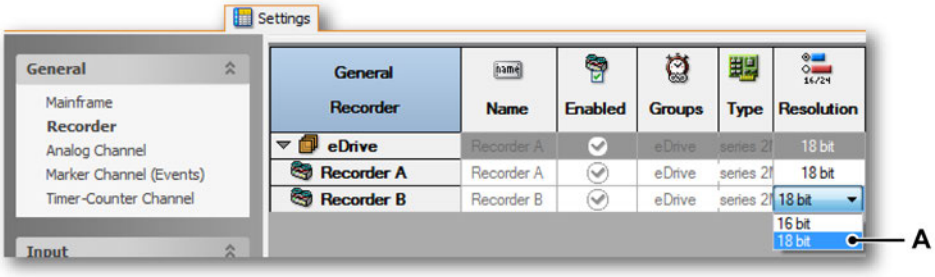


Figure J.22: Activating Channel 8 or Channel 9 in Perception

A Recorder B with 18 bit resolution

2 Configure the B-Txx CON2 in Ch B9 (Perception):

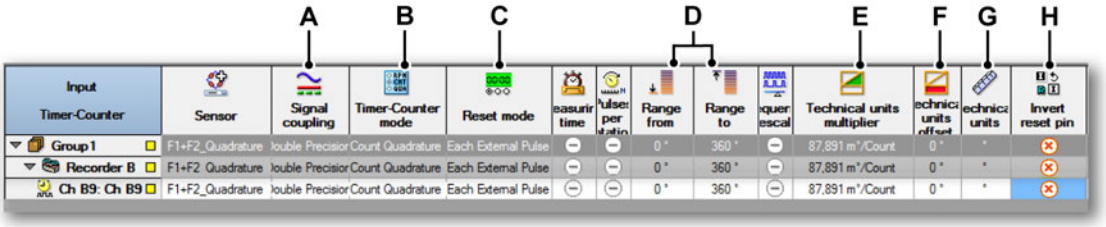


Figure J.23: Configuration of the B-Txx CON2 connector in Perception

A **Signal coupling mode** In quadrature mode, the counter supports three ways of tracking the quadrature states defined by the signal coupling.

- Single precision
- Double precision
- Quad precision

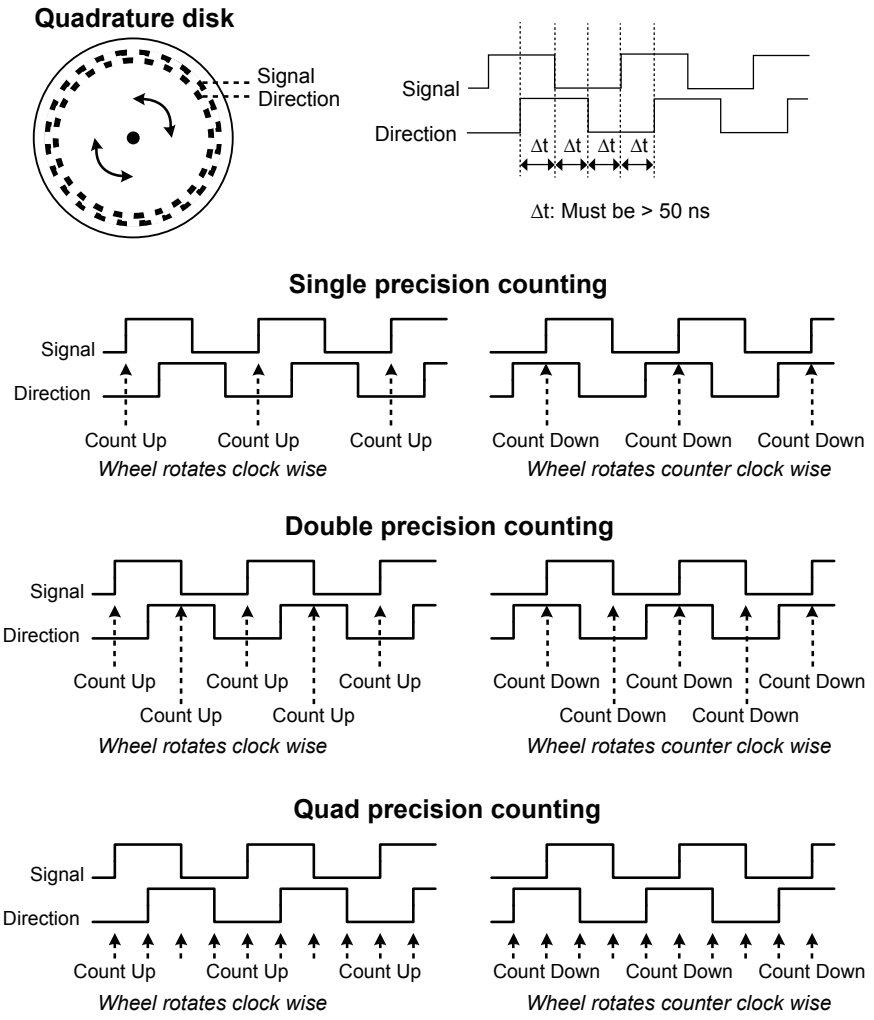


Figure J.24: Signal coupling/precision modes

- In **single precision**, the counter only increments/decrements on the rising edge of the signal input. This is the default traditional quadrature count mode.
- In **double precision**, the counter increments/decrements on both the rising and falling edge of the signal input. As a result, smaller rotations can already be detected. For every full rotation the counter counts double the values compared to the single precision signal coupling mode.
- In **quad precision**, the counter increments/decrements on every rising and falling edge of both the signal and direction input. As a result, even smaller rotations can already be detected. For every full rotation the counter counts quadruple values compared to the single precision signal coupling mode.

Unless other requirements do not allow the quad precision mode to be selected, using this mode is strongly advised due to it higher accuracy.

B **Timer Counter mode:** Count Quadrature -> counters monitor the transition of the four different states the signal can be in.

C **Reset Mode:** Each External Pulse -> resets the counter every time we receive a pulse in Reset input.

D **Range from/to** 0 to 360°

E **Technical units multiplier: 87.891** m°/Count
This setting assumes the use of an encoder with **4096** pulses/rotation
1024 pulses [from encoder] x 4 transitions [quad precision selected].

F **Technical units offset:** 0°

G **Technical units:** ° (degrees)

H **Invert reset pin:** Deactivated* -> A High Level of Reset input is needed to reset the counter to 0.

Note ***** *The counter works ONLY when the reset input is set to Low. After you reset the counter with a High Level, you need to return the reset level to Low to continue the measurement. In other words, your reset signal needs to be a really short impulse in order to minimize the amount of time that the counter is not counting.*

3 Another possibility is to configure the counter channel using the Perception Sensor Database:

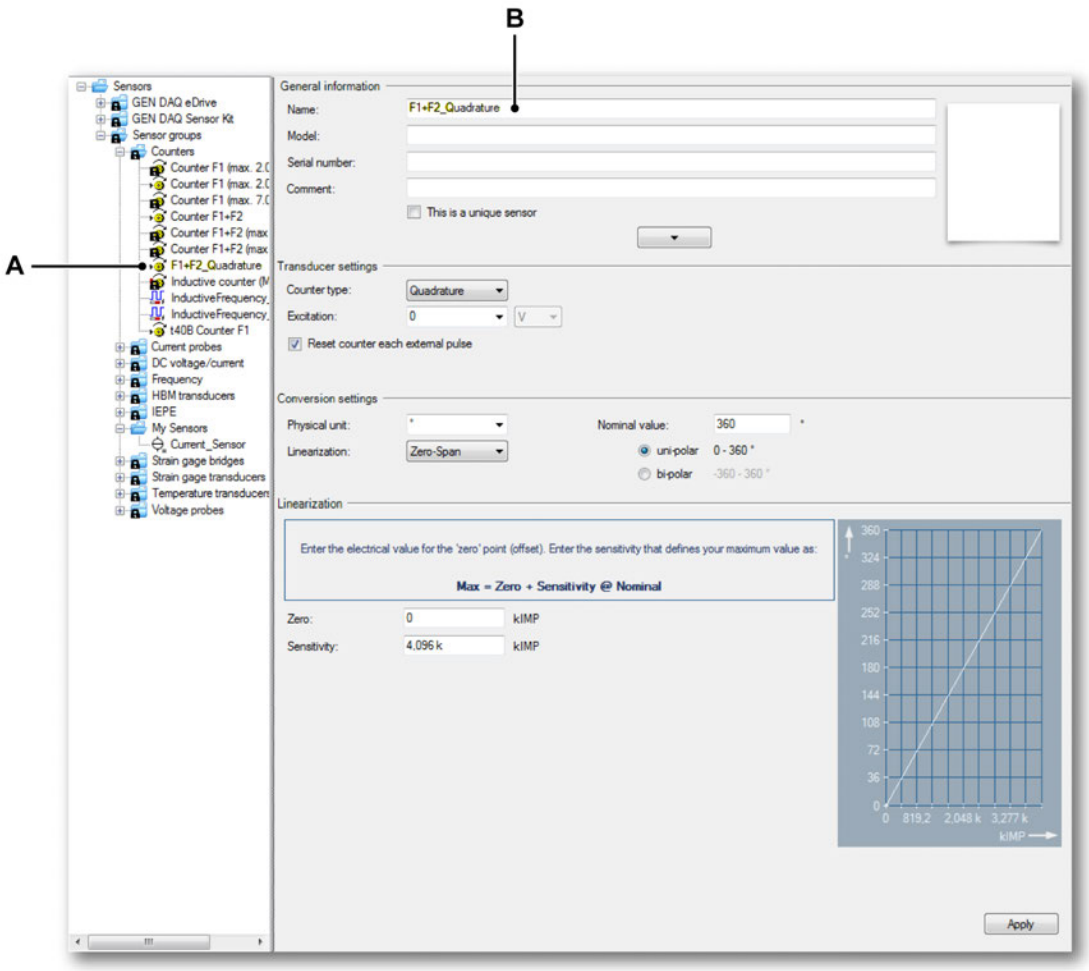


Figure J.25: Perception Sensor Database (Configuring the counters channel)

A Sensor goups/Counters: F1 + F2 Quadrature

B General information/Name: F1 + F2 Quadrature

Assign the sensor **F1+F2_Quadrature** sensor to Channel Ch B9.

Note *Disable the **Invert reset pin** option manually. All other settings are set correctly after the sensor has been selected.*

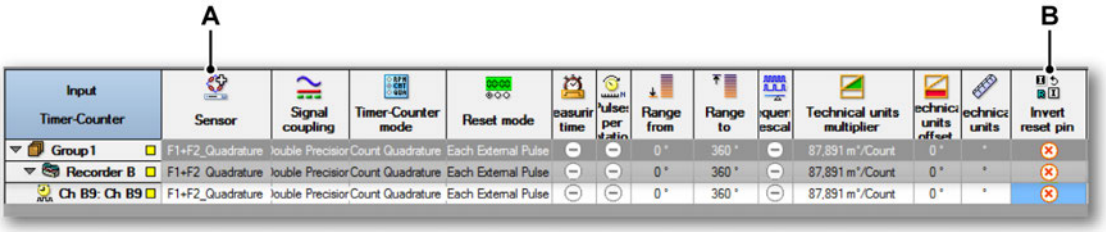


Figure J.26: Configuration of the B-Txx CON2 connector in Perception

A Sensor

B Invert reset pin

The settings of the the frequencies **F1+**, **F1-**, reset and the counter signal on **ChB9** are displayed in the following window (see Figure J.27)

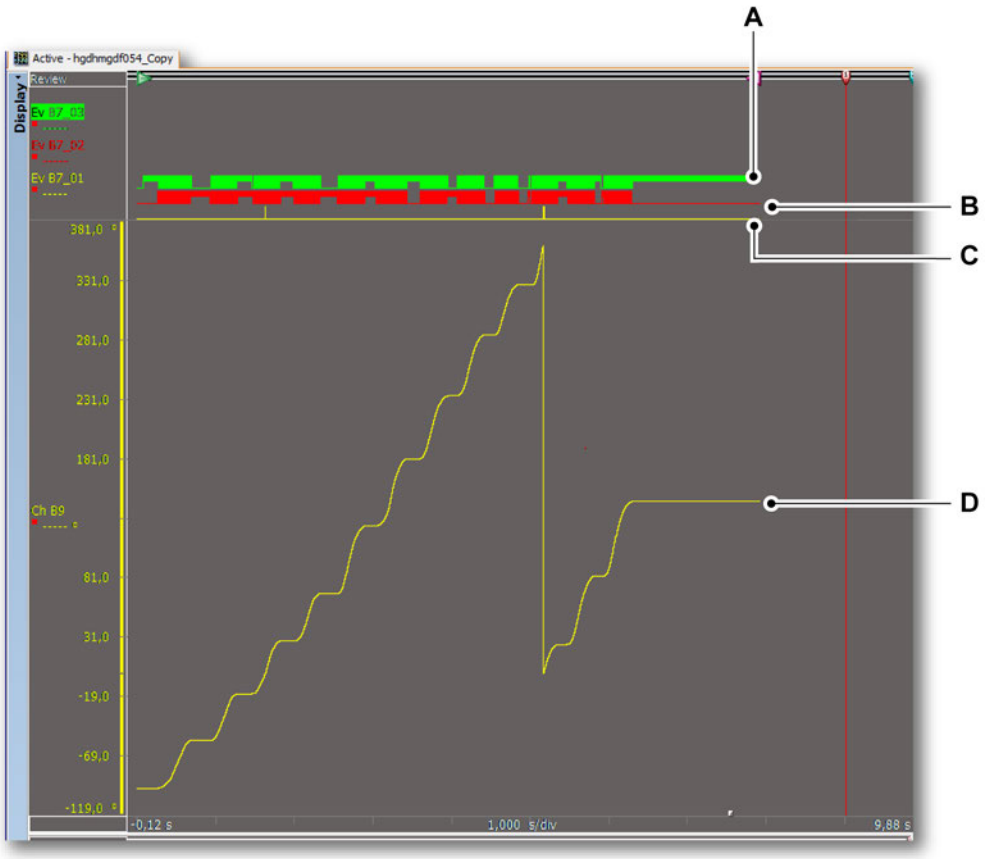


Figure J.27: F1+, F1- , Reset Angular variation (Perception)

A F1+

B F1-

C Reset

D Angular variation

K Network Technology

K.1 10 GB Ethernet Windows settings

To help achieve the highest possible speed rating for the 10 Gbit Ethernet card the following settings can be made to the network adaptor in Windows® 7.

Windows® 10G network adapter settings:

- Interrupt moderation rate: **high**
- Receive side scaling queues: **8**
- Receive buffers: **2048**

Note *The above Windows® settings were tested and chosen using a specific setup of equipment (including the Ethernet Server adaptor x520). These settings may not be the optimal settings for your specific system.*

1 Firstly, on the Windows® 7 desktop navigate to the **Network and Sharing Centre**.

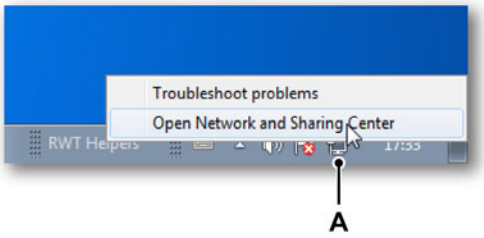


Figure K.1: Windows® 7 Network and Sharing Centre tooltip

A Network icon

Right click the **network icon** in the Windows® system tray and click **Open Network and Sharing Centre**.
Note: This dialog is also available by clicking **Start (Windows orb) > Control Panel > Network and Sharing Centre.**

2 The following dialog will open.

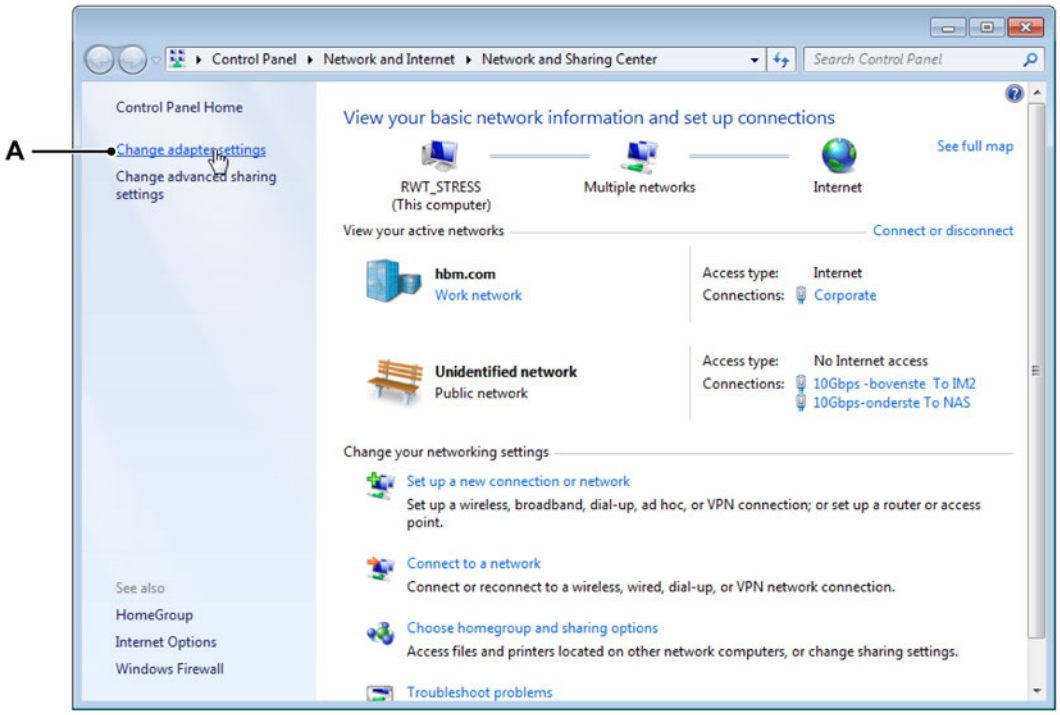


Figure K.2: Windows® 7 Network and Sharing Center

A Change adapter settings

Click **Change adaptor settings**

3 The available adaptors in **Network Connections** should be shown as in the following Figure K.3.

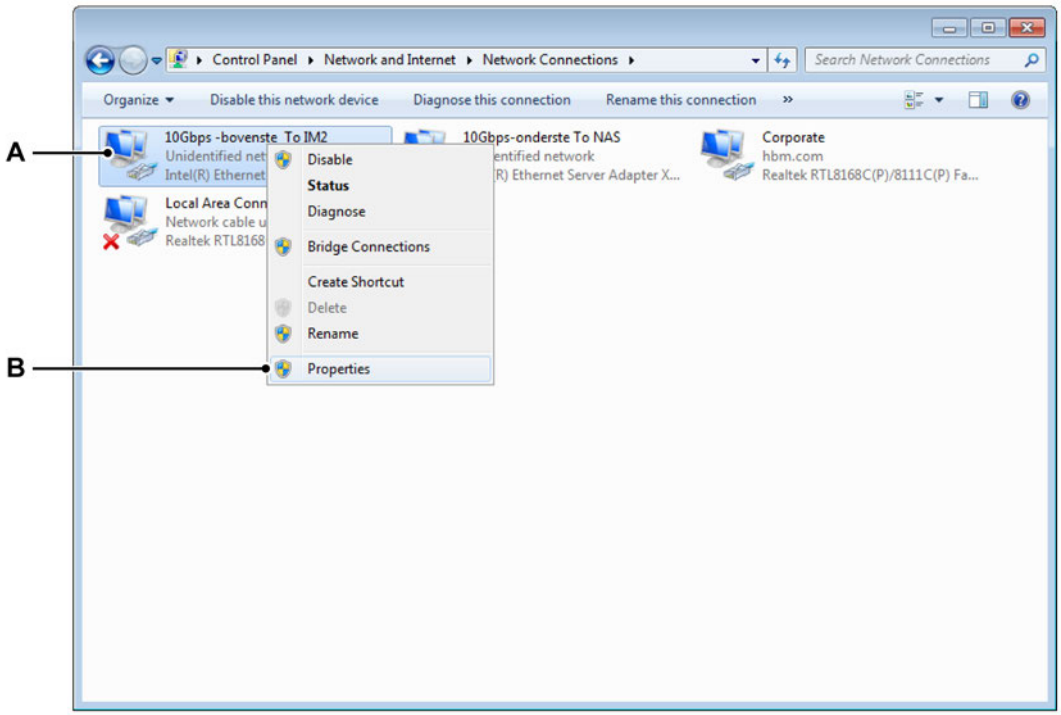


Figure K.3: Network Connections

A Adaptor

B Properties

Right click the 10 Gbit Ethernet adaptor connected to the IM2 module, In the pop-up menu select **Properties.**

4 The following properties dialog will appear.

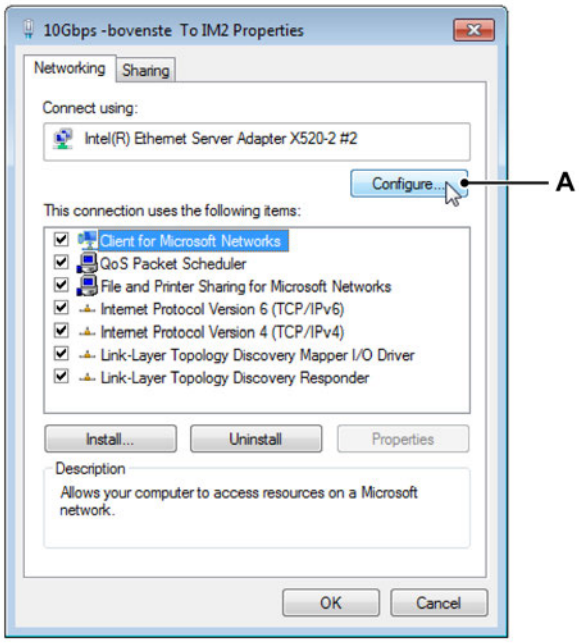


Figure K.4: Networking properties dialog

A Configure

Click **Configure…**

5 The Ethernet Server Adaptor properties dialog for your specific adaptor will appear.

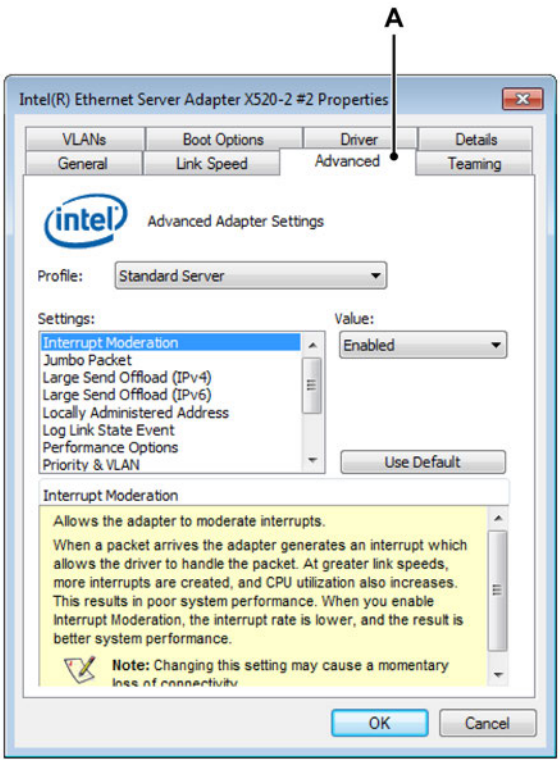


Figure K.5: Ethernet Server Adaptor properties dialog (Part 1)

A Advanced tab

Click the **Advanced** tab.

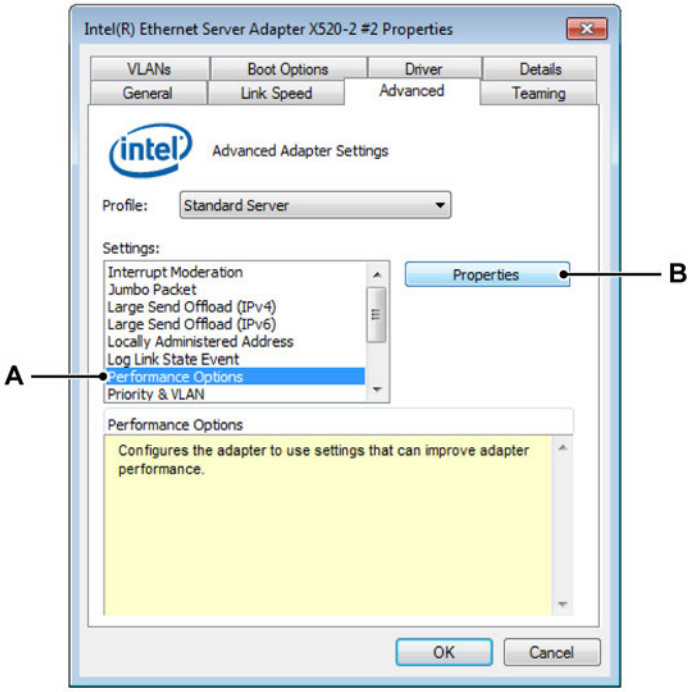


Figure K.6: Ethernet Server Adaptor properties dialog (Part 2)

A Settings/Performance Option

B Properties

Scroll down in the settings menu to **Performance Options** and then click **Properties** on the right hand side.

6 The **Performance Options** properties dialog will appear

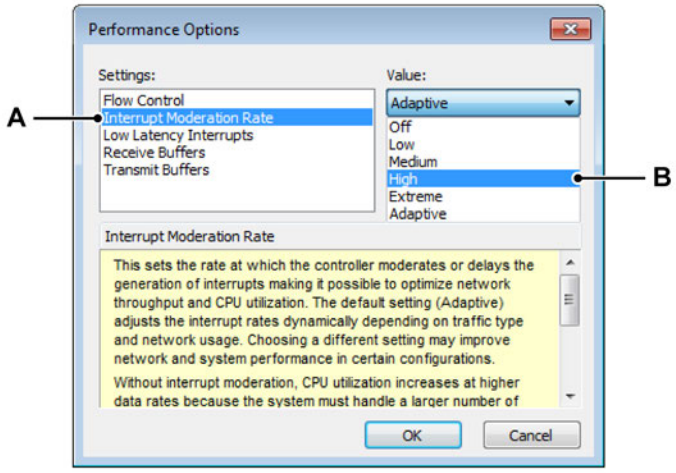


Figure K.7: Performance Options (Part 1)

A Settings/Interrupt Moderation Rate

B Value/High

Select **Interrupt Moderation Rate** and then click **High** in the Value drop down selection box.

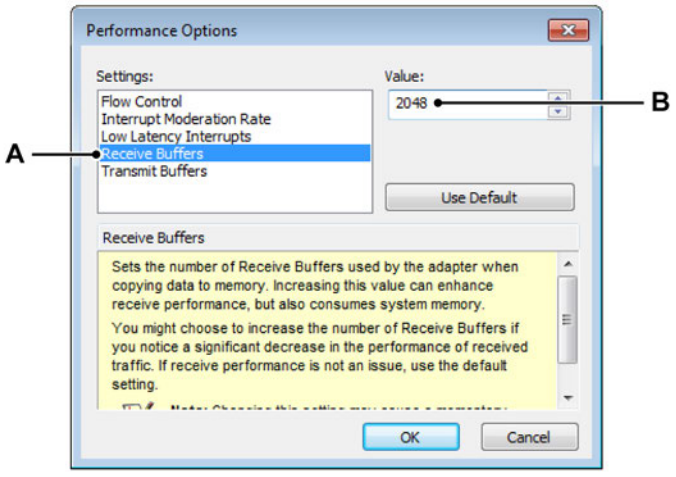


Figure K.8: Performance Options (Part 2)

A Settings/Receive Buffers

B Value/2048

Now click **Receive Buffers** in the settings pane, this should be set to **2048** in the **Value** box.

Click **OK** to return to the previous dialog

7 The Ethernet Server Adaptor properties dialog appears

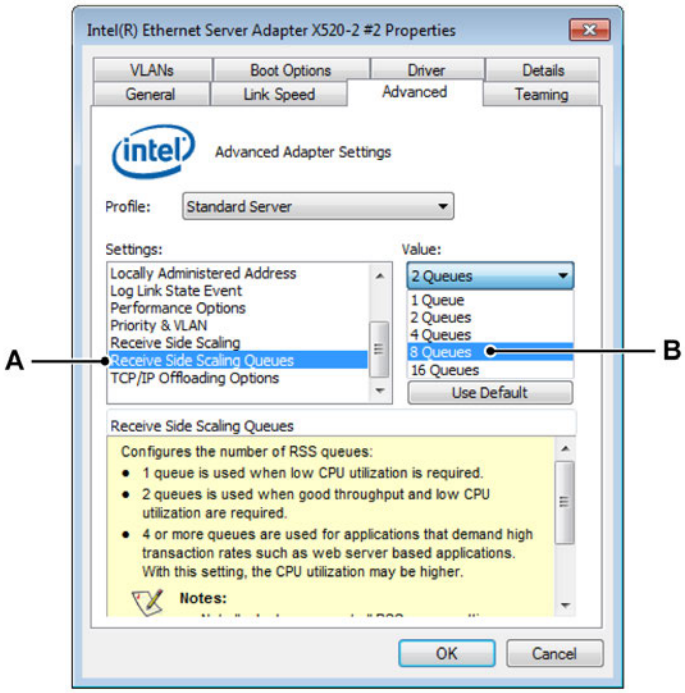


Figure K.9: Ethernet Server Adaptor properties dialog (Part 3)

A Settings/Receive side scaling queues

B Value/8 queues

In the drop down **Value** list select **8 queues** and then click **OK.**

The procedure is now complete.

L Disk Storage Technology

L.1 Most used RAID modes

RAID (Redundant Array of Independent Disks) is a technology that is used to increase the performance and/or reliability of data storage. A RAID system consists of two or more disks working as a single logical unit for the purposes of data redundancy or performance improvement. These disks can be solid state or hard disks. There are different RAID levels, each optimized for a specific situation. Some companies come up with their own unique implementations.

HINT/TIP

Sometimes disks in a RAID system are defined as JBOD, which stands for “Just a Bunch Of Disks”. This means that those disks do not use a specific RAID level and act as stand-alone disks. This is often done for drives that contain swap files or temporary data.

WARNING

RAID is no substitute for back-up!
All RAID levels offer protection from a single drive failure, except RAID 0. For complete security, back-up of the data from a RAID system is always required.

- The back-up will come in handy if two or more drives fail simultaneously because of a power spike.
- It is a safeguard if the storage system is lost/fails all together.
- Back-ups can be kept off-site at a different location in case of a natural disaster or fire destroying your workplace.

The most popular RAID levels are:

- RAID 0 – Striping (see "RAID 0 – Striping" on page 883)
- RAID 1 – Mirroring (see "RAID 1 – Mirroring" on page 884)
- RAID 5 – Striping with distributed parity check (see "RAID 5 – Striping with parity" on page 885)
- RAID 10 – Combining RAID 0 & RAID 1 (see "RAID level 10 – Combining RAID 0 & RAID 1" on page 886)

	RAID 0	RAID 1	RAID 5	RAID 10
Minimum no. of disks required	2	2	3	4
Required no. of disks to extend array	1	N/A	1	2
Maximum volume size	Sum of Disks	One disk size	Sum Of Disks -1	Sum of Disks /2
Redundant storage	0%	100%	1 parity disk/ array	100%
Approximate storage speed	Sum of disks	No. of Disks/2	No. of Disks - 1	No. of Disks/2
Supported loss of disks	0	1	1	1

L.1.1 RAID 0 – Striping

In a **RAID 0** system, storage is split into blocks that are written split across all the drives in the array. Using more disks in one RAID 0 system offers higher storage rates. The performance also depends on the RAID controller used.

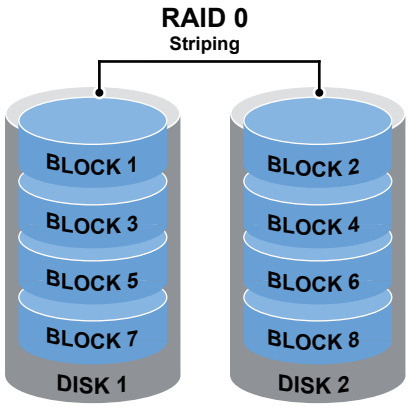


Figure L.1: RAID 0 – Striping

Advantages

- Great performance, both in read and write operations.
- All storage capacity is used; there is no disk overhead.
- Volume size grows with every extra disk added.
- The technology is easy to implement.

Disadvantages

- Not fault-tolerant. If one disk fails, all data is lost.

WARNING

It should not be used on mission-critical systems.

L.1.2 RAID 1 – Mirroring

In a **RAID 1** system, data is stored twice by writing to both a (set of) data disk(s) and a (set of) mirror disk(s). If one disk fails, the controller uses either the data disk or the mirror disk for data recovery and continues operation. You can only use two disks for a RAID 1 array.

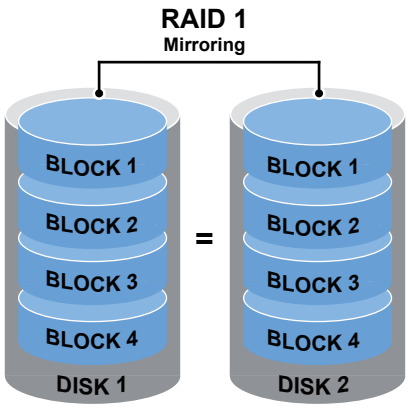


Figure L.2: RAID 1 – Mirroring

Advantages

- Offers excellent read speed and a write speed that is comparable to that of a single disk.
- If a disk fails and is replaced by a new disk, data does not have to be rebuilt; it just has to be copied to the replacement disk.
- RAID 1 is very simple technology.

Disadvantages

- Volume size limited to one disk
- Ineffective storage capacity; only half of the total disk capacity is available.

L.1.3 RAID 5 – Striping with parity

RAID 5 arrays require at least three disks. Data blocks are subdivided (striped) and written to two (or more) drives. Parity for the stored data blocks is calculated and stored on an additional drive. Parity is not stored on a dedicated drive but spread across all the drives in the array. Since parity is used, a stripe set can withstand a single disk failure without losing data. Although RAID 5 can be achieved in software, a hardware controller is recommended to support the parity calculations in hardware. Extra cache memory is often used on these controllers to improve the write performance. RAID 5 is a good all-round system that combines efficient storage with excellent security and decent performance.

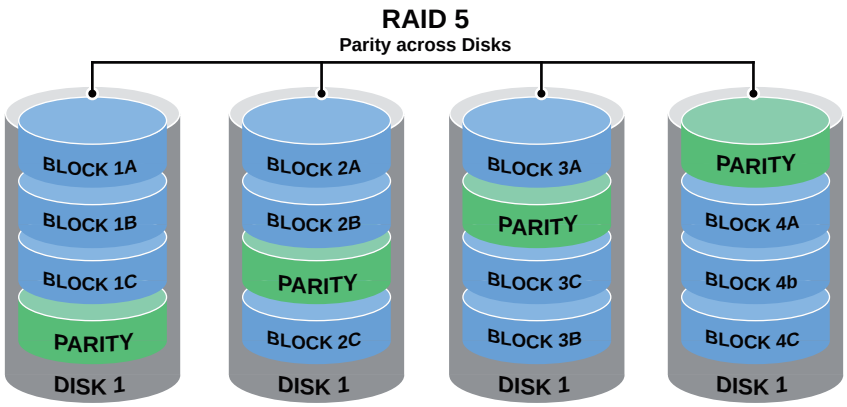


Figure L.3: RAID 5 – Striping with parity

Advantages

- Read data transactions are very fast while write data transaction are somewhat slower (due to the parity that has to be calculated).

Disadvantages

- Disk failures have an effect on throughput, although this is still acceptable.
- Complex technology requiring hardware support to efficiently calculate parity.

L.1.4 RAID level 10 – Combining RAID 0 & RAID 1

RAID 10 combines RAID 0 and RAID 1 in one single system. It provides security by mirroring all data on a secondary set of disks (Disk 2 and 4 in the drawing below) while using striping across each set of disks to speed up data transfers.

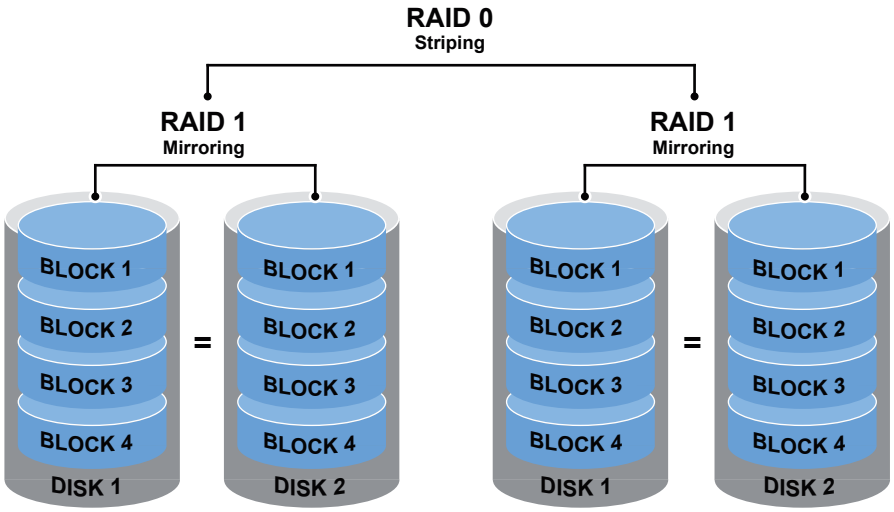


Figure L.4: RAID level 10 – Combining RAID 0 & RAID 1

Advantages

- Great performance, both in read and write operations.
- If a disk fails and is replaced by a new disk, data does not have to be rebuilt; it just has to be copied to the replacement disk.
- The technology is easy to implement. No parity calculations are required.
- Volume size is not limited to one disk.

Disadvantages

- Ineffective storage capacity, only half of the total disk capacity is available.

L.2 Setting up the iSCSI target using Synology® NAS

For further tutorials, please refer to:
www.synology.com/tutorials/tutorials.php

Equipment needed:

- Synology® assistant
- iSCSI NAS
- GEN DAQ system with Ethernet

1. Make sure the network is set up and correctly connected to the NAS storage device.
2. If the Synology® software is not installed yet, please follow the Synology® installation instructions to install the iSCSI setup software.
   Available here: www.synology.com/support/download.php?lang=us
3. Start **Synology® assistant** from the program menu.

Note ***Synology® assistant auto lists connected Synology® devices only.***

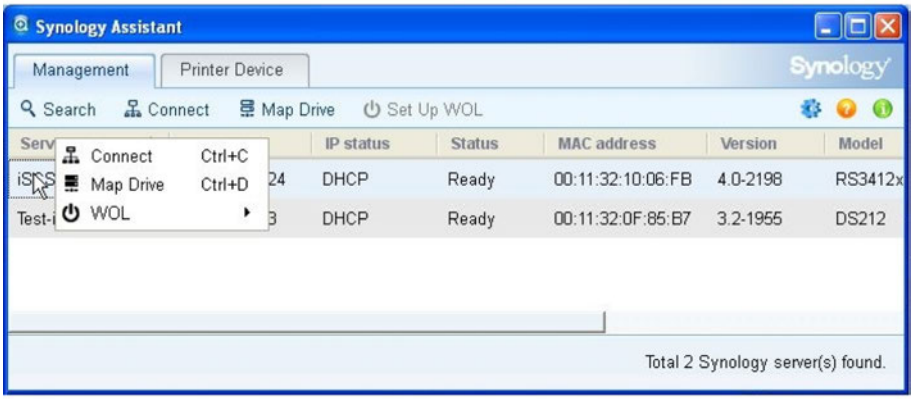


Figure L.5: Synology Assistant

Select or right click an iSCSI device and then click **Connect**.
Your web browser should open to **DSM Synology® RackStation** or **FileStation**. The **IP address** and **Port number** of the Synology® NAS server should now be displayed in your internet browser address bar.

4 A login screen may appear, depending on whether or not the NAS has been set up before. You should not need to log in for the first time when setting up a NAS.

If you see a login screen, you need to log in with the details that were used to set up the NAS the first time it was used. Please refer to the manufacturer's guide if you need more information.

Please refer to the Synology® manual for the start-up procedure and how to create login details.

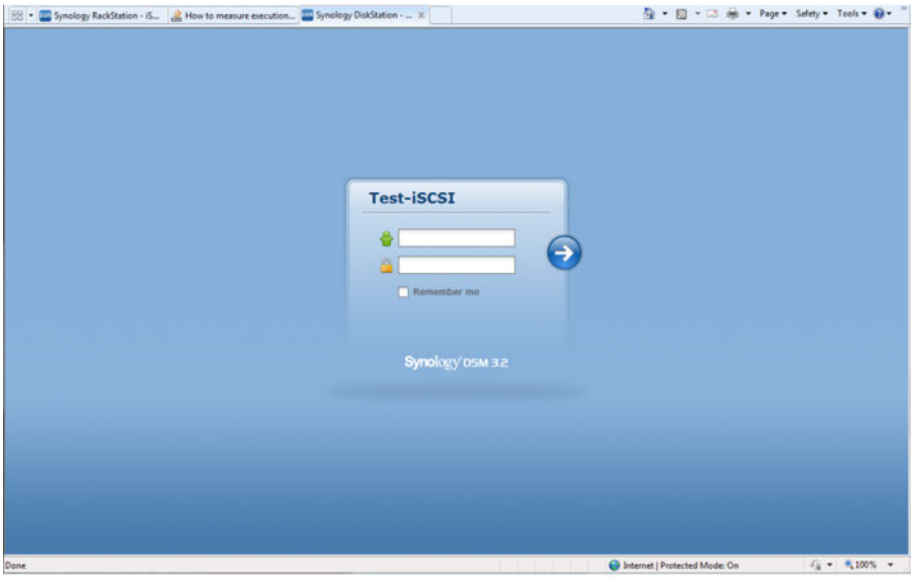


Figure L.6: Login dialog

5 When logged in and on the home screen, click the main-menu icon (A) as shown in Figure L.7.

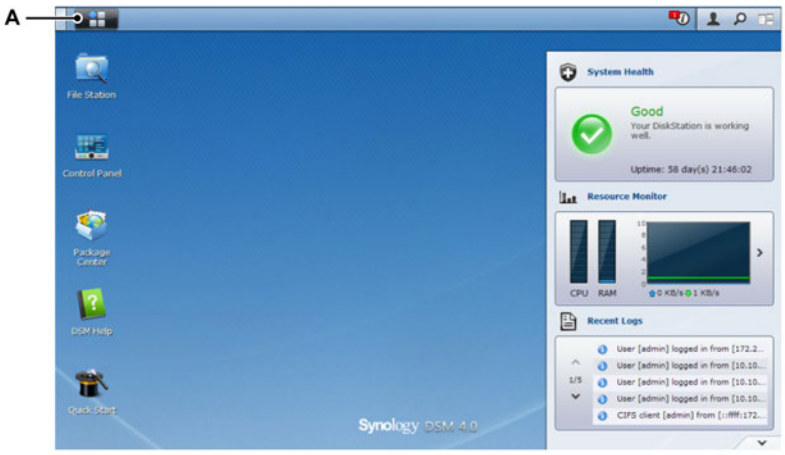


Figure L.7: Home screen

A Main-menu icon

6 A quick launch window will open.

Figure L.8: Quick launch window

A Storage Manager

Click the **Storage Manager** icon.

7 The **Storage Manager** dialog opens.

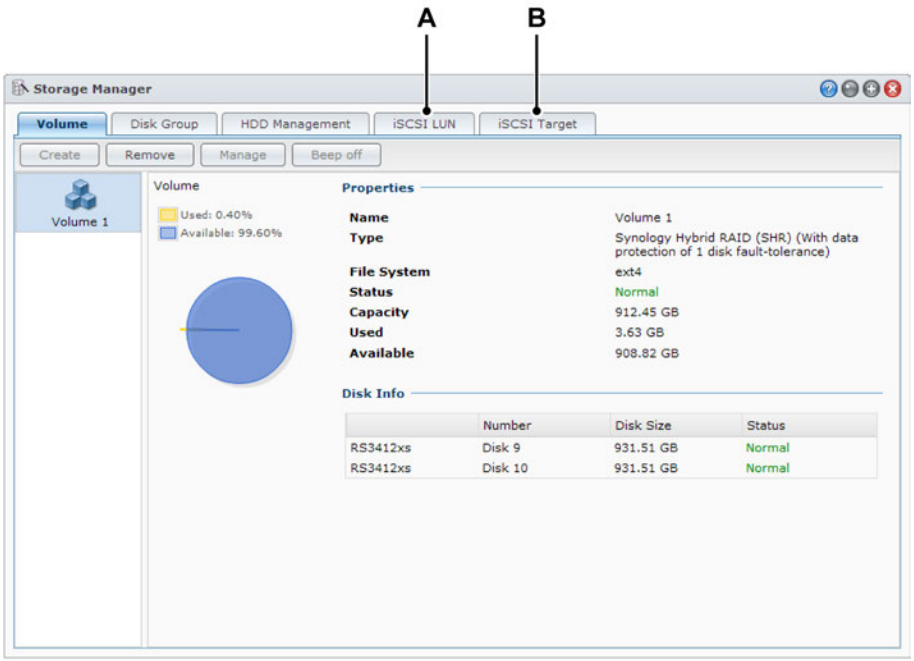


Figure L.9: Storage Manager dialog

A iSCSI LUN

B iSCSI Target

First, set up an **iSCSI Target** or **iSCSI LUN**.
In Perception, this information will be used in the **External Storage Setup: iSCSI Target** dialog box.

The same procedure can be performed by using the **iSCSI LUN** tab, **Create** button.
If you want to create an iSCSI LUN first, please refer to
Figure L.12 "Create a new iSCSI LUN target dialog" on page 895.

8 Click the tab **iSCSI Target:**

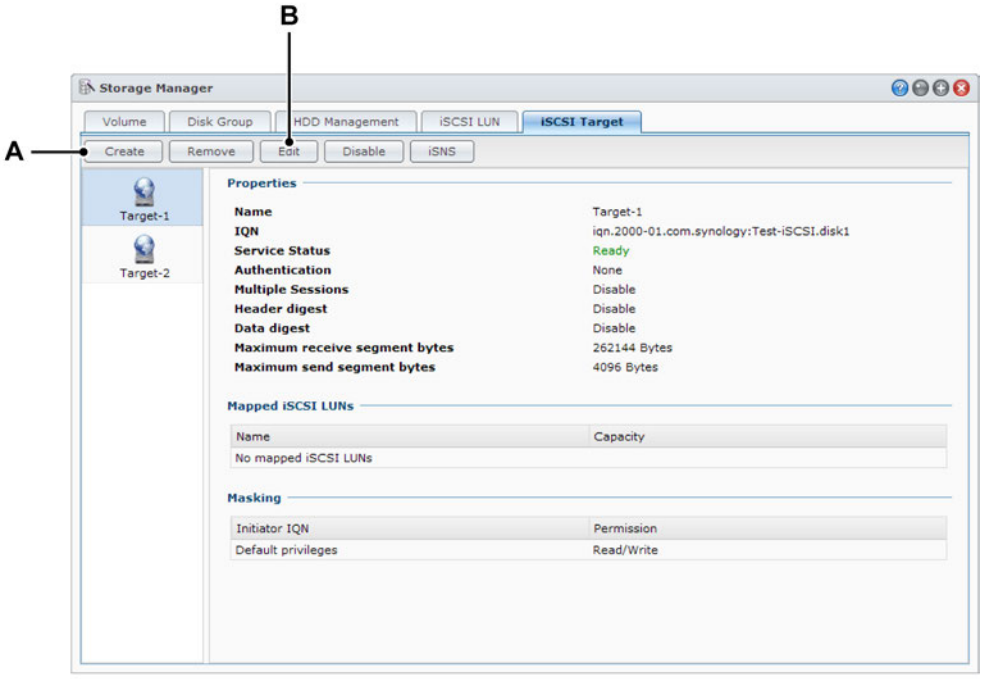


Figure L.10: iSCSI Target window dialog

A Create tab

B Edit tab

This tab shows the available iSCSI Target disks and their details. To create a new iSCSI Target, click **Create**.

9 The following **iSCSI** Creation Wizard dialog appears:

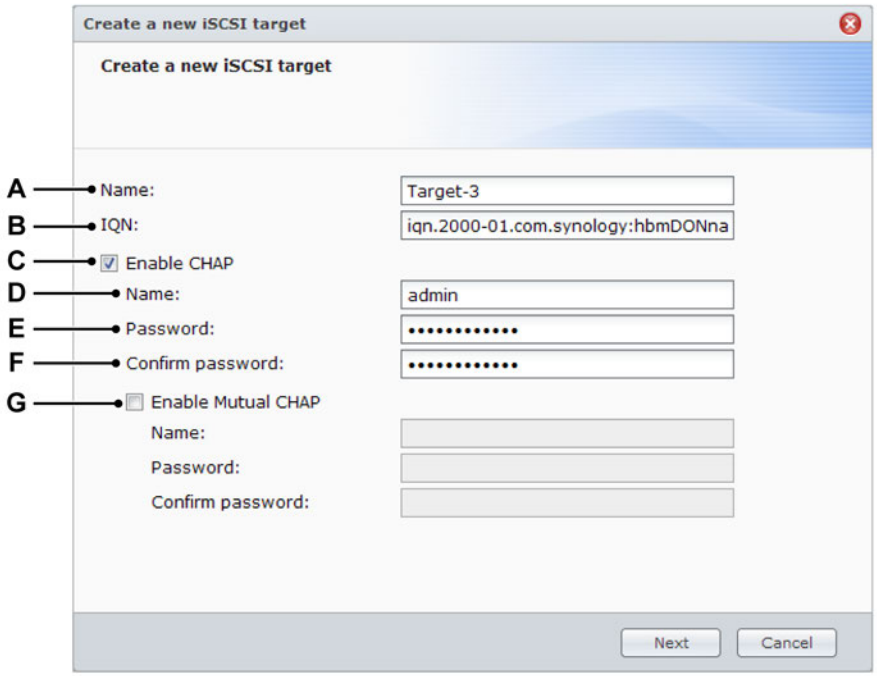


Figure L.11: Create a new iSCSI Target dialog

A Name

B IQN number

C Enable CHAP

D CHAP Name:

E CHAP Password:

F CHAP Confirm Password:

G Enable Mutual CHAP

The dialog in Figure L.11 asks for your **IQN (B)** number and a Target **Name (A)**. **CHAP (C)** password protection can also be set up, this is the same password that will be used in the Perception setup dialog; **External Storage Setup > iSCSI Logon: User name and Password**.

If you need to check the user name of an existing iSCSI Target, click the correct target in the **iSCSI Target tab** (see Figure L.10 **(B)**) and then click **Edit**.

A **Name:** Enter a name for target mapping.
Recommended Format: iqn.yyyy-mm.domain:device.ID

B **IQN:** Enter the actual iSCSI IQN name here.
Recommended Format: iqn.yyyy-mm.domain:device.ID
This IQN name is the same name used in the Perception dialog **External storage setup: iSCSI Target - Target name** (see chapter “Interface/Controller Module” in the GEN series Data Acquisition System” manual.

C **Enable CHAP** If logon Password protection is needed, select this check box.

Note *CHAP is used to authenticate iSCSI Initiators before using the iSCSI Target.*

D **CHAP Name:** Enter a name to be used for login to the iSCSI.

E **CHAP Password:** Enter a password; minimum 12 characters.

F **CHAP Confirm Password:** Re-type the password.

G **Enable Mutual CHAP** will require both the initiator and the target to authenticate each other before communicating.

When done, click **Next**.

10 When setting up an iSCSI Target, you also need to set up an iSCSI LUN as follows.

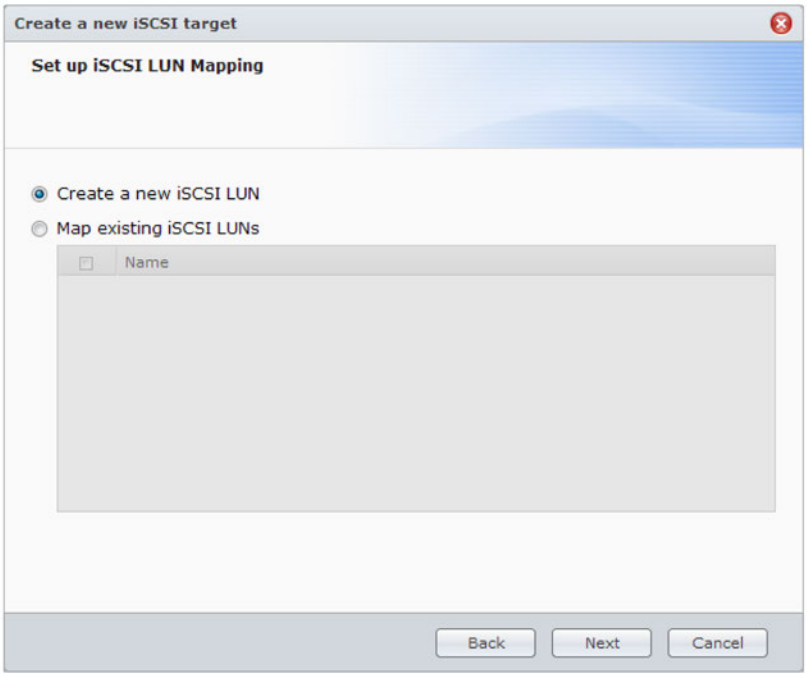


Figure L.12: Create a new iSCSI LUN target dialog

From the **Storage Manager** window, select **Create new iSCSI LUN** when no LUNs are yet available. If LUNs are available, then you may select **Map existing iSCSI LUNs.**

Click the **Next** button.

11 Create a new iSCSI LUN

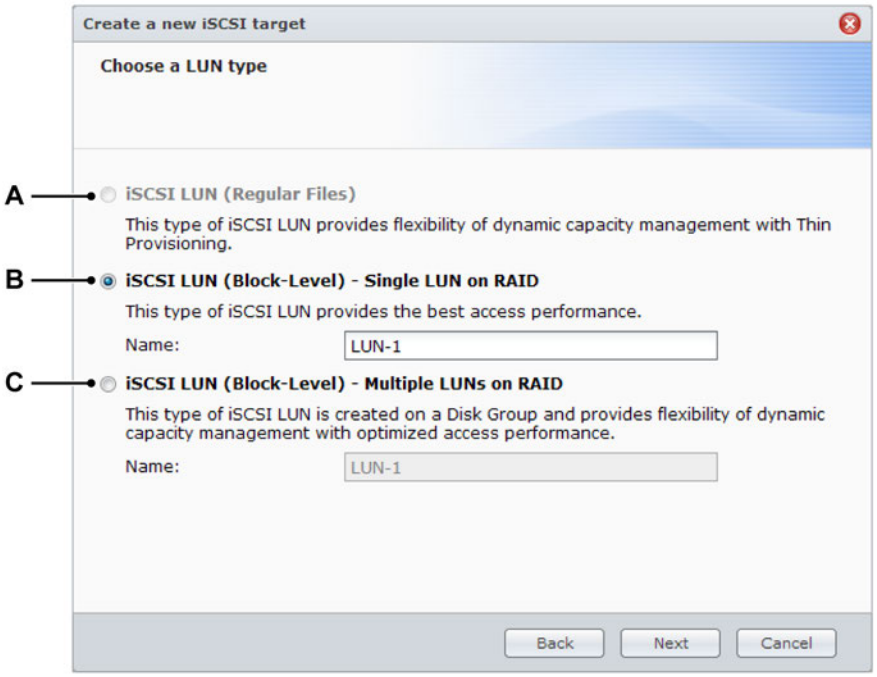


Figure L.13: Create a new iSCSI LUN target - Choose a LUN type dialog

A iSCSI LUN (Regular Files)

B iSCSI LUN (Block-Level) - Single LUN on RAID

C iSCSI (Block-Level) - Multiple LUNs on RAID

Select **iSCSI LUN (Block-level) - Single LUN on RAID (B)**. This mode copies blocks of data exactly as they are and therefore offers the best performance.

For the following options:

- **iSCSI LUN (Regular files) (A)**
- **iSCSI LUN (Block-level) - Multiple LUN on RAID (C)**

Please see the manufacturer's description online:
www.synology.com/tutorials

Click the **Next** button.

12 The **Create a new iSCI target - Choose disks** dialog appears.

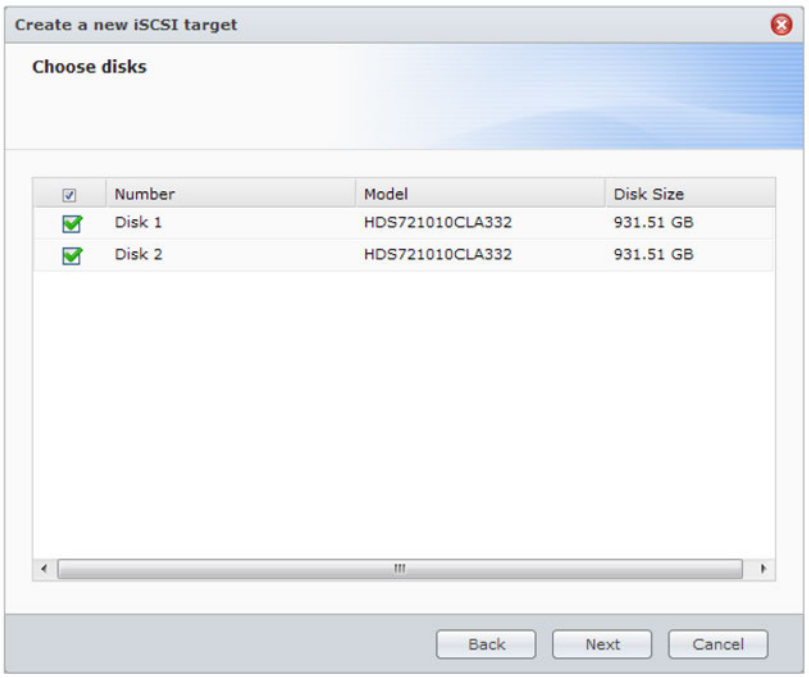


Figure L.14: Create a new iSCSI LUN target - Choose disks dialog

Choose one or more physical discs to use as a LUN target and click **Next**.

13 The **Create a new iSCI target - Choose RAID type** dialog appears.

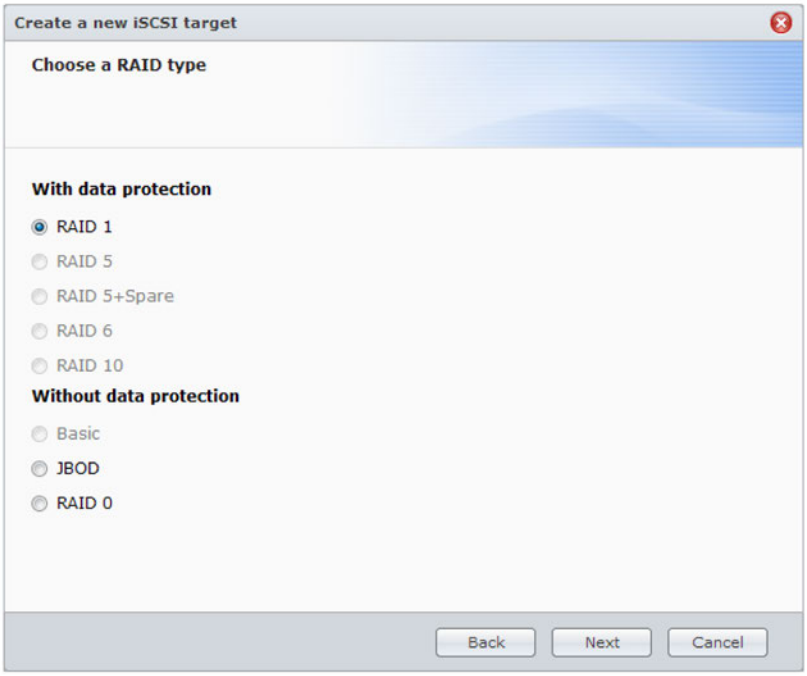


Figure L.15: Create a new iSCSI LUN target - Choose a RAID type

Select the RAID configuration you require.

A number of configurations are possible, depending on the available setup. The user must decide what is best here. Some information is available on the **Synology®** website:
www.forum.synology.com/wiki/index.php

Click the **Next** button.

14 The **Create a new iSCI target - Perform disk check** dialog appears.

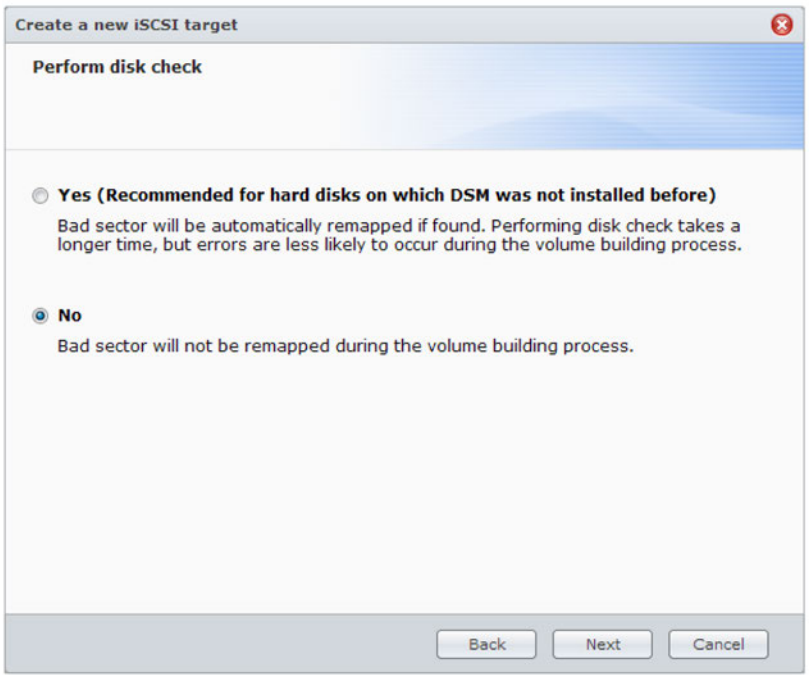


Figure L.16: Create a new iSCSI LUN target - Perform disk check dialog

Follow the on screen dialog and select your preference.
Disk checking will take a long time and depends on the size of the disk being checked.

Click the **Next** button.

15 The **Create a new iSCI target - Confirm Settings** dialog appears.

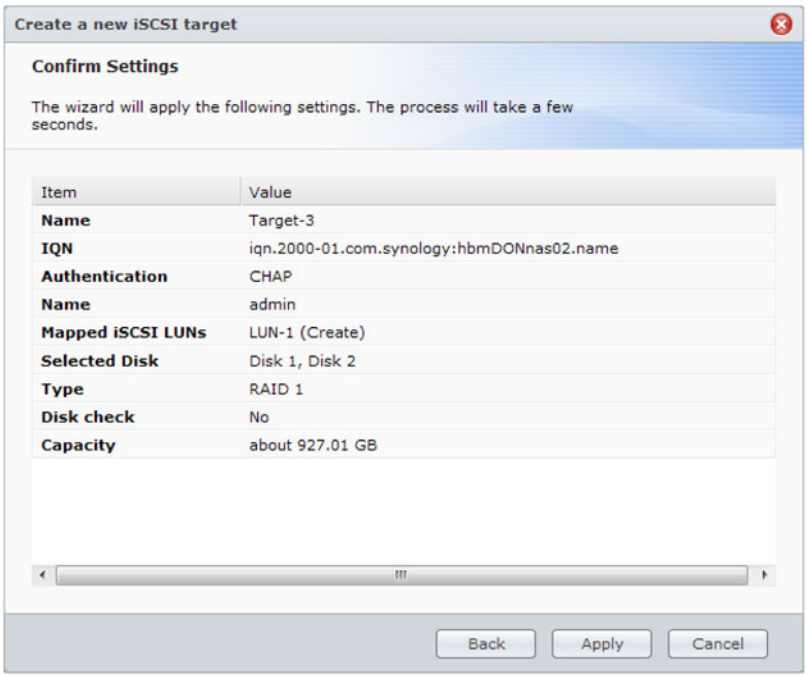


Figure L.17: Create a new iSCSI LUN target - Confirm Settings dialog

A summary of the information used to create the new iSCSI LUN/Target is presented. Make sure the information is correct and then click **Apply**.

When the dialog box closes, a new iSCSI Target/LUN will appear in the iSCSI Target and/or LUN tab of the Sinology® software.

Note *This disk is not formatted and requires formatting to use Perception. When connecting to this disk for the first time, Perception will inform you of the format requirements.*

M BE3200 USB to Optical RS232 convertor

M.1 Re-programming of the USB-RS232 (opt. 650nm) converter to work with BE3200

1 Download the “FT-Prog“ from:
www.ftdichip.com/Support/Utilities.htm
This is required to re-program the internal EEPROM in the converter to support inverted TX/RX lines (required to work with BE3200).

2 Unzip the downloaded ZIP-Archive and run the “FT_Prog“ program. Connect the converter to a free USB connector on your PC.

3 Press **F5** or go to the menu **Devices ▸ Scan and Pharse**. As soon as the USB converter is found, the display should look like this:

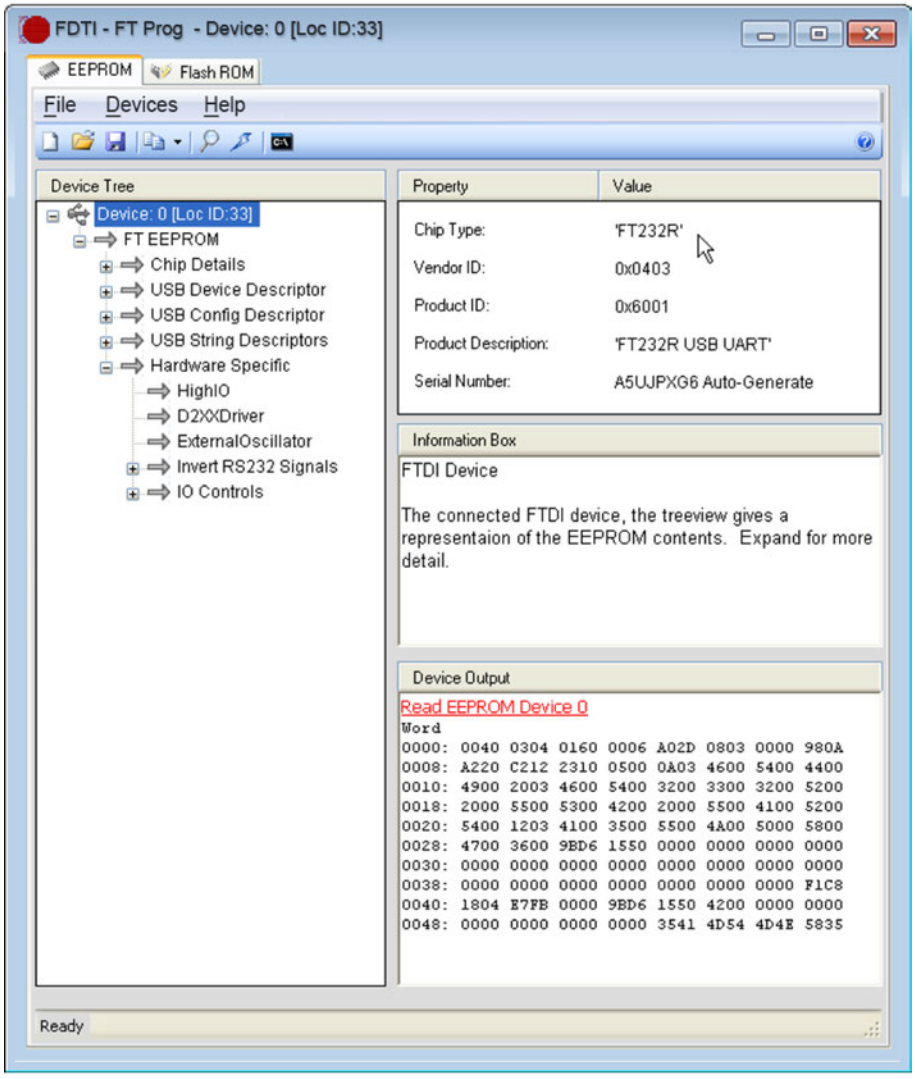


Figure M.1: FTDI - FT Prog (Part1)

4 In **Device Tree** in the left-hand column, expand the **Hardware Specific** node and select the **Invert RS232 Signals** (see Figure M.2).

5 In the **Property** column, select **Invert TXD** and **Invert RXD** check boxes (see Figure M.2):

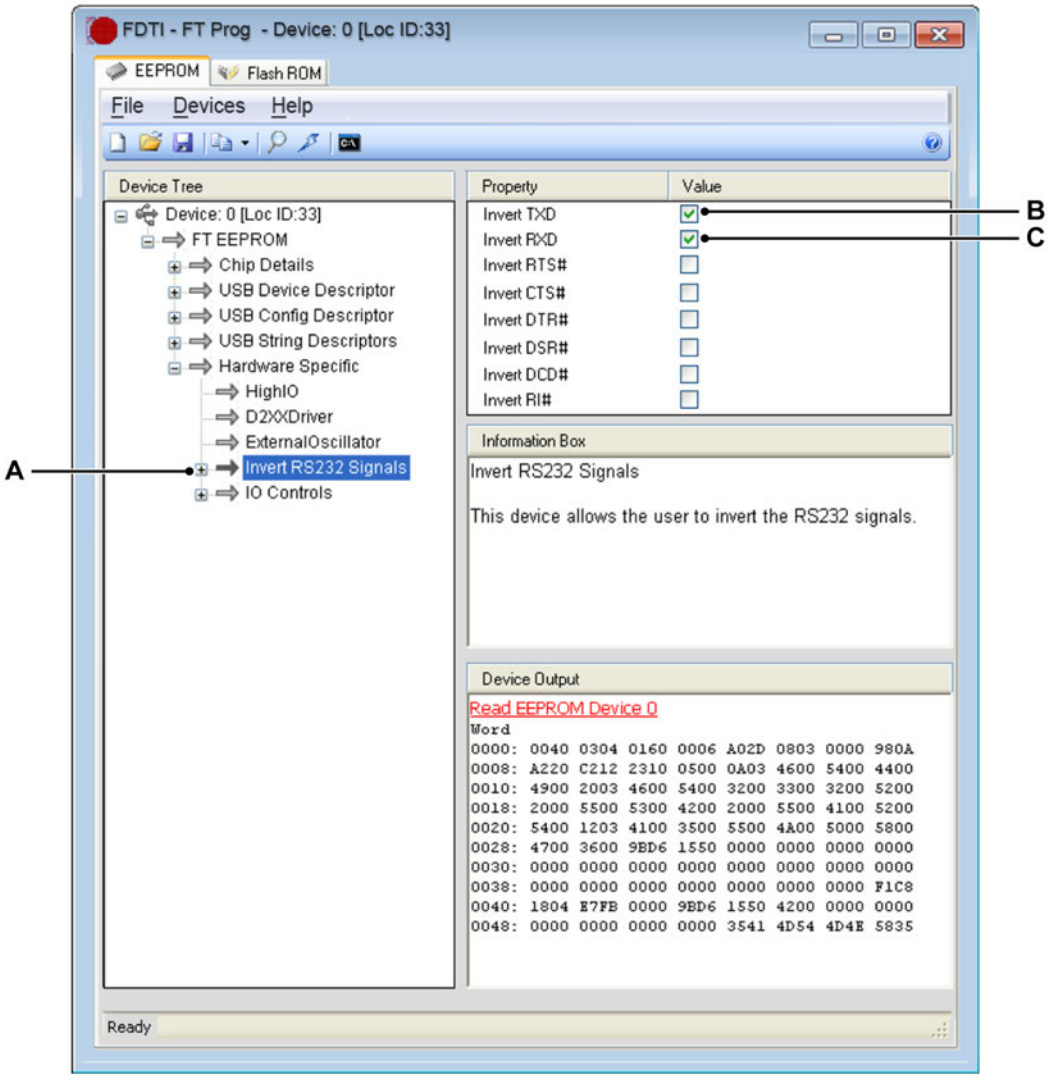


Figure M.2: FTDI - FT Prog (Part2)

A RS232 Signals

B Invert TXD

C Invert RXD

6 Finally: Select from the menu **Devices** ► **Program** to re-program the **EEPROM** on the converter.

N Legacy Information - Input Cards

N.1 GN410 and GN411 Bridge input cards

The GN410 and GN411 bridge input cards are suitable for strain gauges, strain-gauge based force, pressure or torque transducers and piezo-resistive accelerometers. The inputs can also be used as a general purpose low voltage differential amplifier with AC and DC coupling. It provides bipolar DC excitation voltage or current, flexible software-switched completion options and a variety of calibration methods for any type of bridge configuration.

The type of front panel connectors is LEMO 2B. Every channel is equipped with an independent high-gain amplifier, a seven-pole Bessel and Butterworth anti-alias filters, a 16 bit Analog-to-Digital converter operating at up to 1 MS/s, and digital filtering. All channels are sampled at full speed with no multiplexing and almost immeasurable crosstalk. A 200 kS/s model is available for medium speed acquisition requirements.

The bridge amplifiers support quarter-bridge, half-bridge and full-bridge configurations from three to eleven wires. Each channel includes software-switched half-bridge completion resistors, two fixed shunt calibration resistors and one socket for an additional shunt resistor provided by the user. A 350 Ω quarter-bridge completion resistor is supplied for each channel, plus one socket for an additional value supplied by the user. A unique and powerful ability allows the amplifier to measure each input and each excitation individually, which allows for a quick diagnosis of wiring problems. Each channel also features two set-points for trigger or alarm purposes plus hardware detection of open/ shorted excitation leads and amplifier overrange.

N.1.1 Bridge amplifier configuration

Input diagrams and typical connection diagrams for the GN410 and GN411 bridge amplifiers are shown on this and the following pages. For the maximum versatility, the amplifiers allow a wide range of configurations. A minimum of three wires are necessary for a quarter- or half-bridge sensor and four wires for a full bridge. Optional remote sensing of excitation voltage is supported for precision transducer applications, which adds two wires. Remote shunt calibration is possible with the addition of two or three more wires. Finally, both an isolated common and a driven guard are provided for optional shielding.

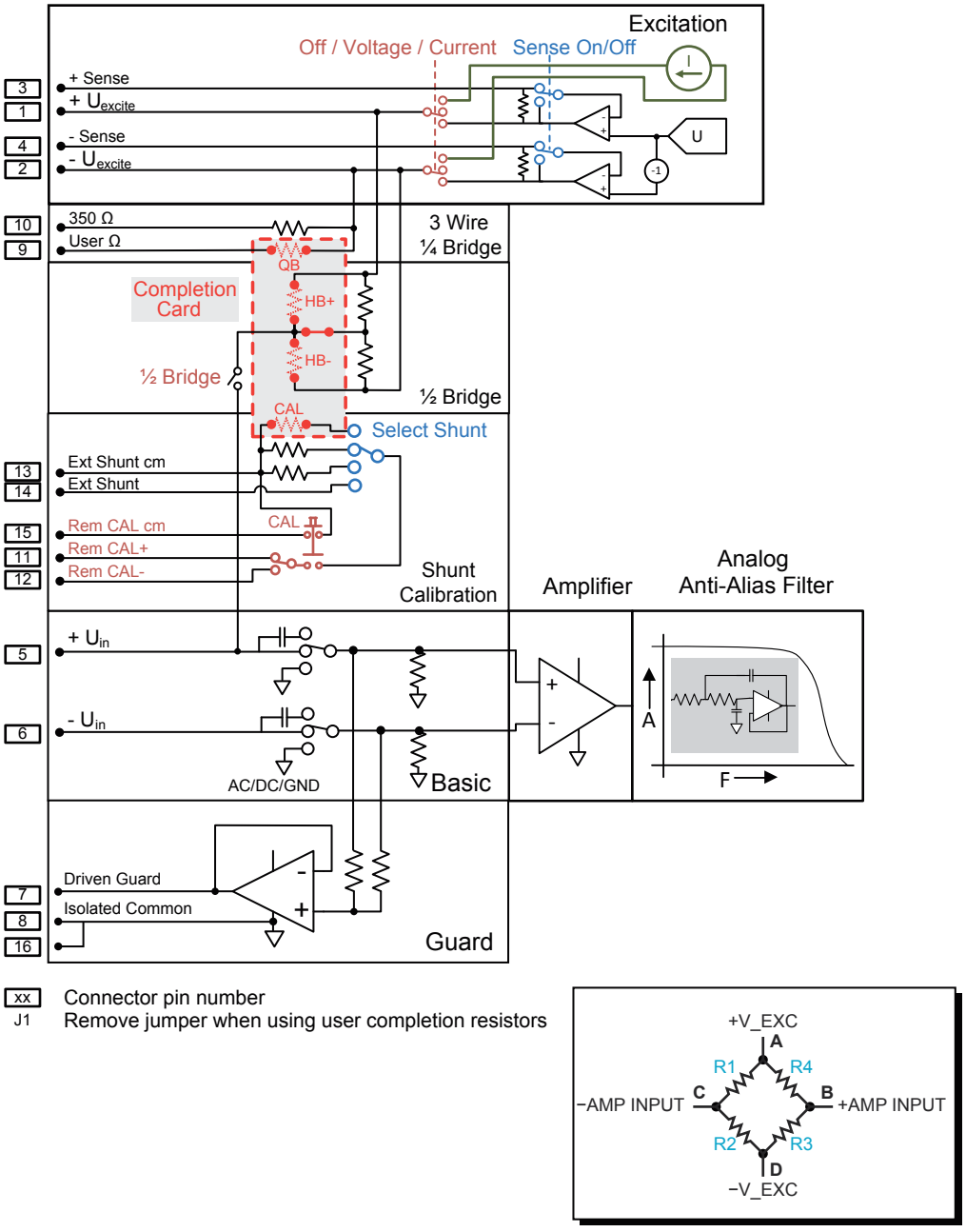


Figure N.1: Bridge amplifier block diagram with pinning

N.1.2 Input connectors

The LEMO 2B316 connector pin-out is compatible with the Liberty data acquisition system. The mating male connector is LEMO P/N FGG2B316CLADxx, where xx is the desired cable collet size or a similar size.

N.1.3 Bridge completion

Each bridge amplifier channel contains a pair of fixed 10 kΩ resistors for half-bridge completion that can be switched in by software control. The user can install two resistors on the removable bridge completion card for another value and/or precision half-bridge completion. If so, a soldered jumper must be removed for correct operation.

Additional pins on the LEMO connector provide a precision 350 Ω resistor, plus an additional value for quarter-bridge completion that has been provided by a user. The user-provided value is located on a removable bridge completion card. The completion sockets are designed for Vishay Micro Measurements S-Type resistors but can be used with other similar types. A diagram of the card layout on one of the following page shows the location of each resistor.

N.1.4 Shunt calibration

Each bridge amplifier channel contains 100 KΩ and 20 KΩ, 0.1% fixed precision resistors that can be switched in by software control. With a gage factor of 2.00, this resistor simulates the following values of deflection for various bridge configurations.

Table N.1: Deflection for various bridge configurations

	100 KΩ			20 KΩ		
BRIDGE	**1000 Ω**	**350 Ω**	**120 Ω**	**1000 Ω**	**350 Ω**	**120 Ω**
mV/V	2.4888	0.873	0.299	12.20	4.337	1.495
µstr full bridge	1244	437	150	6098	2169	748
µstr $^1/_2$ bridge	2488	873	300	12195	4337	1496
µstr $^1/_4$ bridge	4975	1747	600	24390	8674	2991

A convenient plug-in module is provided to install one additional user-supplied shunt resistor on each channel. The diagram below shows the location of the resistors completed by the user. A fourth calibration resistor can be connected to the connector pins externally. Any of the four available shunt cal resistors can be switched in by software control to provide multi-point calibration and linearity verification.

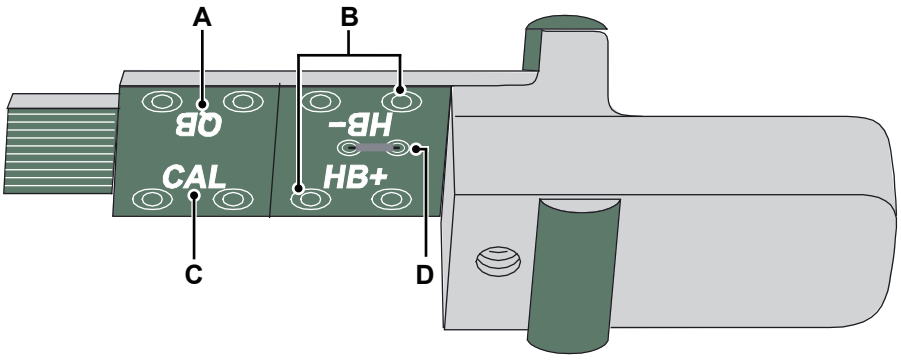


Figure N.2: Shunt calibration completion plug-in module

A User quarter-bridge Completion

B User half-bridge Completion

C User shunt cal

D JUMPER! *Remove when installing a half-bridge completion*

N.1.5 Shielding and driven guard

When long cable runs are required, the excitation leads and signal leads are generally separately twisted and shielded within the cable to minimize the cross-coupling that would otherwise occur.

The high-performance signal conditioners offers the “driven guard” system where the cable shield is connected only to the drive pin of the conditioner. When connected like this, the shield is driven to a potential that is equal to the common-mode voltage of the bridge. The driven shield or guard therefore minimizes the potential difference between the internal conductors and the shield, thereby reducing the amount and levels of partial discharges between them. In all cases, the driven shield is terminated only at the driven guard conditioner terminal. It is strongly advised to have the driven shield surrounded by an outer shield that is terminated to ground preferably at the strain gauge installation site as shown in Figure N.3.

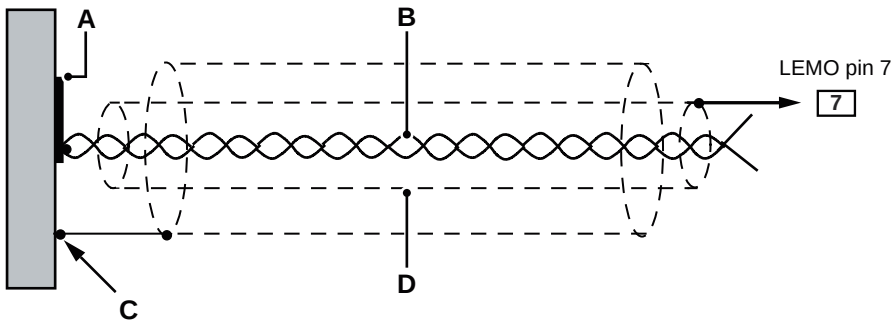


Figure N.3: The driven guard approach to minimize induced noise

A Strain gauges

B Signal conductors

C Outer shield
Terminated near strain gauges - Signal source

D Inner shield
Driven guard at +Vcm

N.1.6 Various bridge configurations

The diagrams below shows possible bridge configurations.

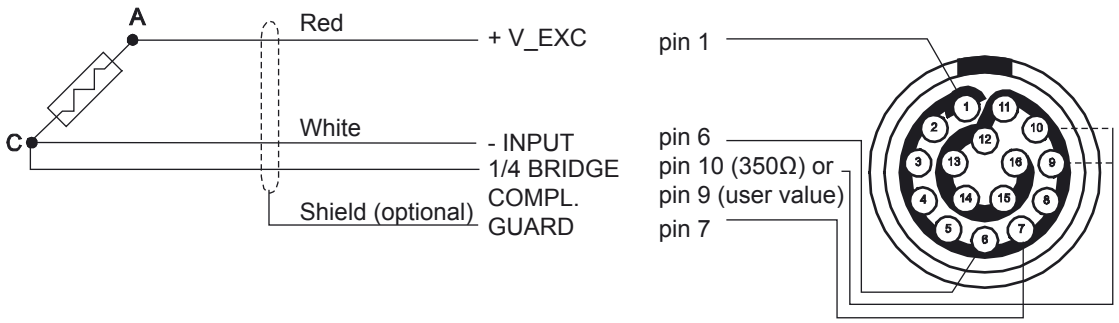


Figure N.4: Three-wire quarter bridge

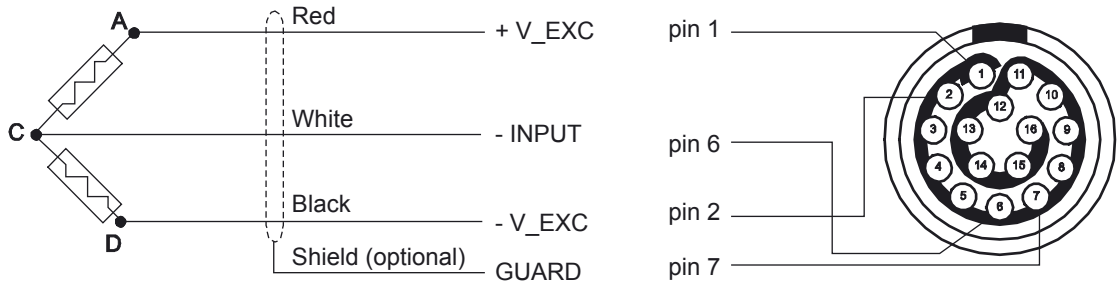


Figure N.5: Half-bridge standard wiring

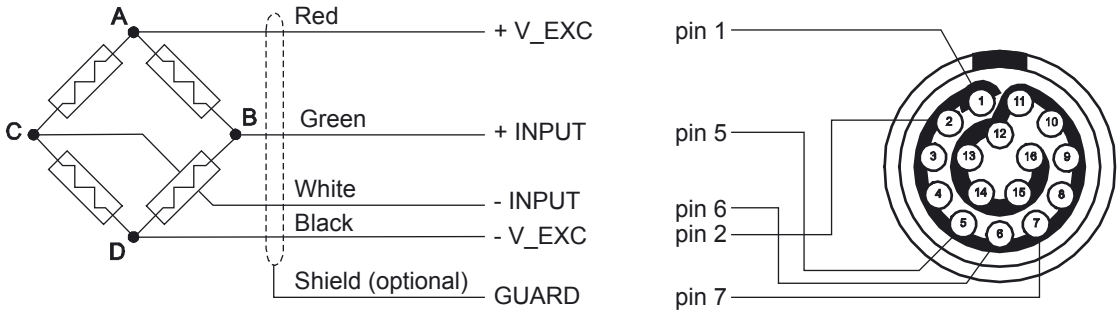


Figure N.6: Full-bridge standard wiring

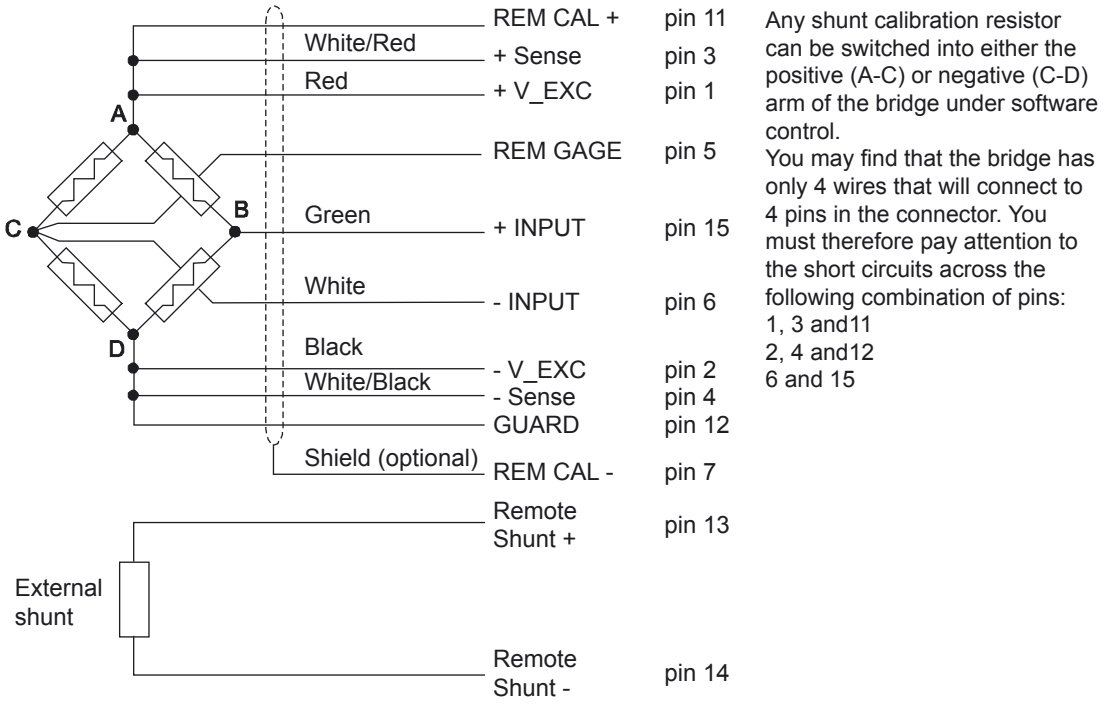


Figure N.7: Full-bridge with remote sensing and remote calibration

N.1.7 Bridge connector reference card

Make copies of this page to record and document your test setups.

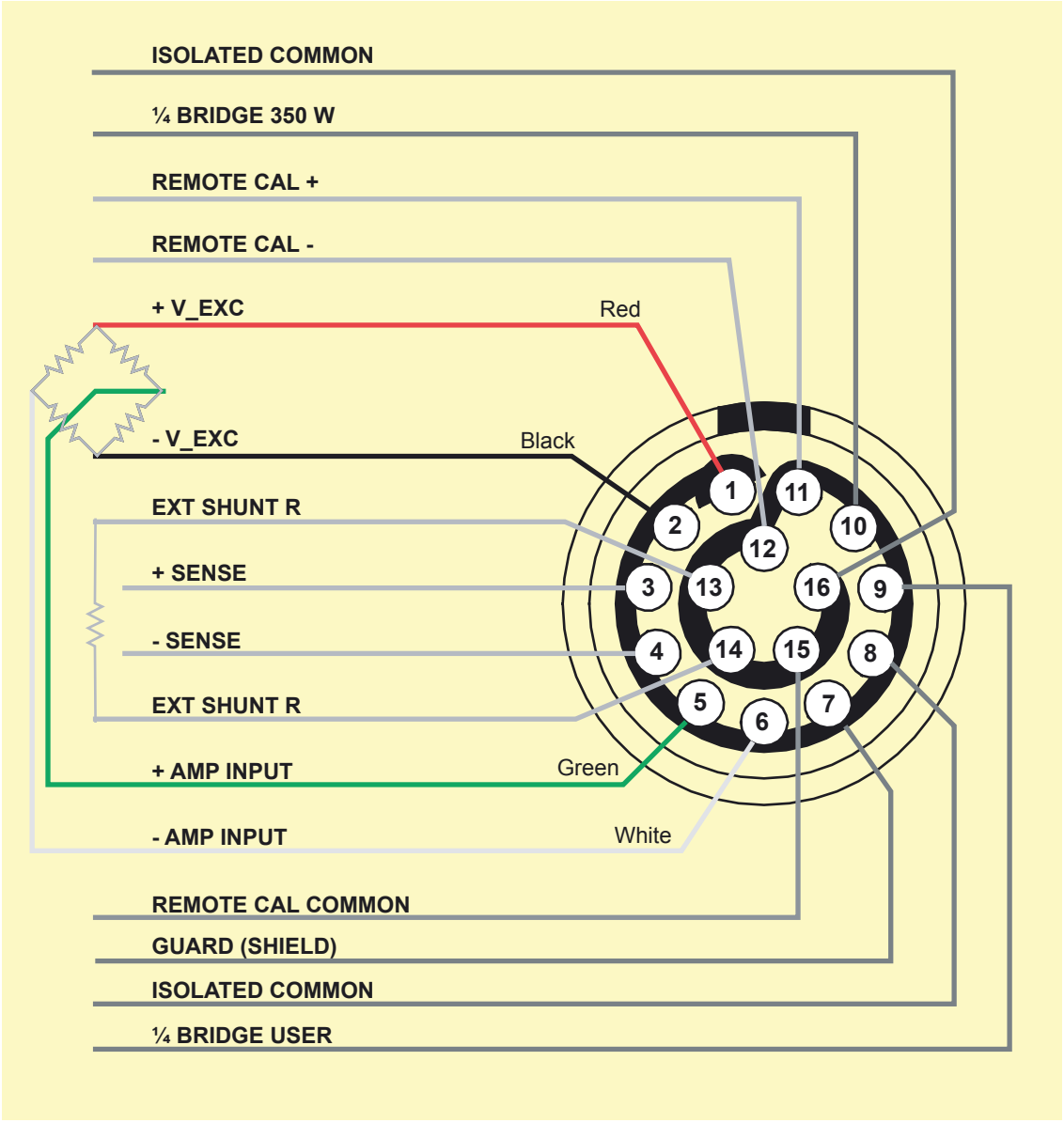


Figure N.8: Reference card: LEMO FGG.2B.316 Connector, solder cup view of male connector

N.1.8 Configuring and using the bridge amplifier

This section describes the procedures required when configuring and using the bridge amplifier for both the hardware as well as the software (Perception).

In the Perception software, a simplified block diagram is used as reference and complementary control.

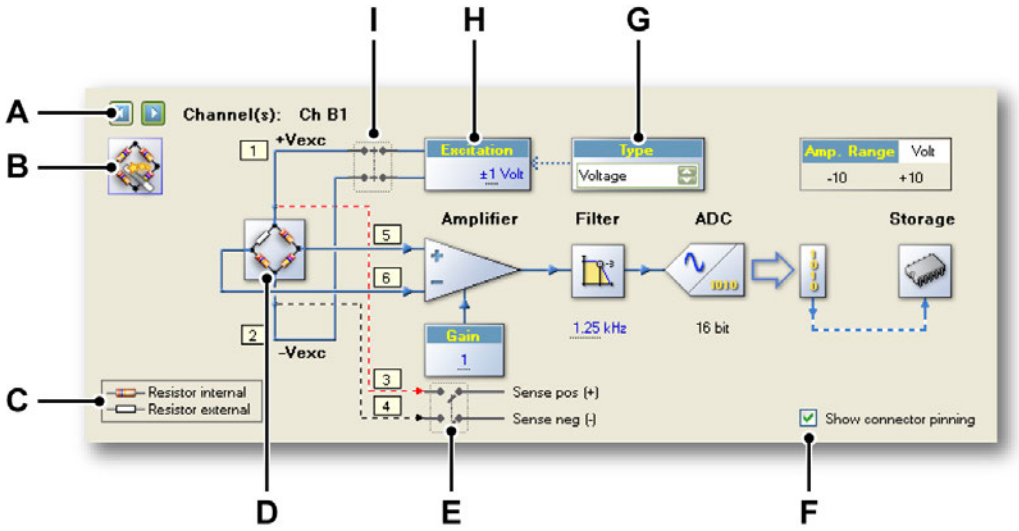


Figure N.9: Perception Bridge Amplifier simplified block diagram

A Channel select

B Start bridge wizard

C Legend

D Bridge representation (click to toggle bridge completion)

E Sense on/off (S1a and S1b in Figure N.1 on page 904)

F Show connector pinning on/off

G Excitation type

H Excitation value

I Excitation on/off (S2a and S2b in Figure N.1 on page 904)

Bridge completion

The Wheatstone bridge used in most strain gauge measurement circuits usually consists of (a) the gages for actively measuring the strains and (b) precision resistors for completing the circuit. In GN410 and GN411, bridge completion can be for full-bridge, half-bridge and quarter-bridge configurations. Completion resistors can be internal (incorporated in the GN410 and GN411) or external (when required).

Bridge completion - full (4/4) bridge
A full bridge type sensor is a sensor that has all four bridge resistors on-board; no completion is required.

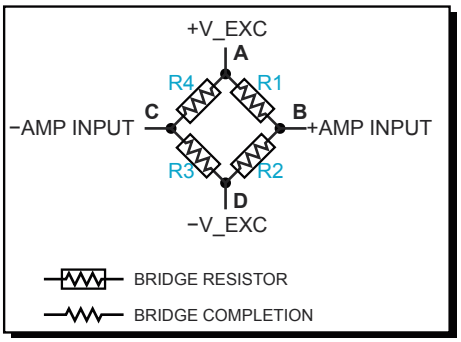


Figure N.10: Full-bridge layout

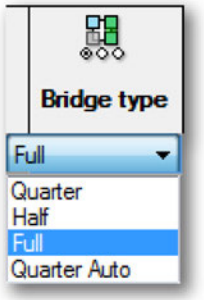
At least four wires are necessary to connect a bridge such as this. Please refer to Figure N.7 for connection details. Inform the Perception software when a full bridge is used.

To select full bridge completion in Perception
To select full bridge completion, proceed as follows:

1 In Perception, go to the **Settings** sheet.
2 In the task pane, select the **Bridge** in the **Input** section.
3 Select one or more channels.

4 Do one of the following:

- In the **Bridge type** column of the spreadsheet style matrix, select the bridge type **Full**.



- In the simplified graphical diagram, click on the bridge icon (**D** in Figure N.9 on page 911) until the full-bridge representation can be seen.

Bridge completion - Half (1/2 or 2/4) bridge
A half-bridge type sensor is a sensor that has two bridge resistors on-board; completion is required.

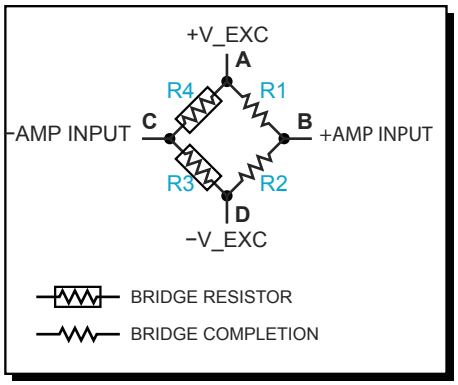


Figure N.11: Half-bridge layout

In this situation, a sensor is used with two (out of four) resistors: R4 and R3. These resistors are placed between A-C and C-D.

Two additional resistors must be provided: R1 and R2. There are two ways of doing this:

1 Use the standard 100 kΩ resistors inside the acquisition card.
2 Provide two resistors.

Nothing needs to be done to the hardware for the first situation.

Two resistors need to be added to the plug-in module in the locations marked HB+ and HB- for the second situation. You will also need to remove the jumper J1. Please refer to Figure N.1 on page 904 for electrical/schematic details and to Figure N.2 on page 906 for mechanical/location details.

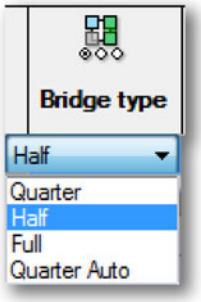
At least three wires are necessary to connect a bridge such as this. Please refer to Figure N.6 for connection details. Inform the Perception software when a half bridge is used.

To select half-bridge completion in Perception
To select half-bridge completion in Perception, proceed as follows:

1 In Perception, go to the **Settings** sheet.
2 In the task pane, select the **Bridge** in the **Input** section.
3 Select one or more channels.

4 Do one of the following:

- In the **Bridge type** column of the spreadsheet style matrix, select the bridge type **Half**.



- In the simplified graphical diagram, click on the bridge icon (**D** in Figure N.9 on page 911) until the half-bridge representation can be seen.

5 Switch S3 in Figure N.1 is closed when half-bridge completion is selected.

Bridge completion - Quarter (1/4) bridge

A quarter-bridge type sensor is a sensor that has a single bridge resistor on-board; completion is required.

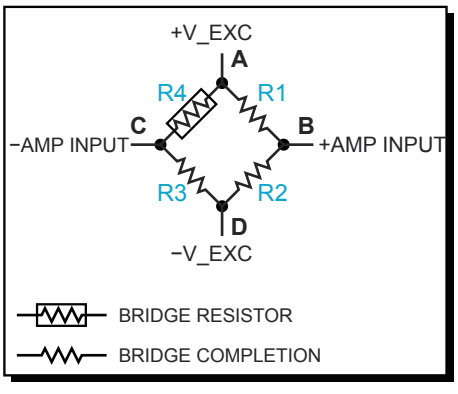


Figure N.12: Quarter-bridge layout

In this situation, a sensor is used with only one resistor, R4. This resistor is placed between A and C.

Three additional resistors must be provided: R1, R2 and R3 to complete the bridge. You do this by using the half-bridge completion as described in the previous section and then adding the additional R3 resistor between C and D. There are two ways of doing this:

1 Use the standard 350 Ω resistor inside the acquisition card.
2 Provide a resistor.

Nothing needs to be done to the hardware for the first situation.

For the second situation, a resistor needs to be added to the plug-in module in the location marked QB. Please refer to Figure N.1 on page 904 for electrical/schematic details and to Figure N.2 on page 906 for mechanical/location details.

Additional wiring needs to be added for the quarter-bridge completion resistor. Depending on the selection made, connect either Pin 10 (350 Ohm) or Pin 9 (user) to the bridge connection marked C in the diagram, or directly to Pin 6 (-amp in) of the connector. Please refer to Figure N.4 for connection details.

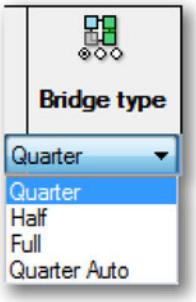
Inform the Perception software when a quarter bridge is used.

To select quarter-bridge completion in Perception
To select half-bridge completion in Perception, proceed as follows:

1 In Perception, go to the **Settings** sheet.
2 In the task pane, select the **Bridge** in the Input section.
3 Select one or more channels.

4 Do one of the following:

- In the **Bridge type** column of the spreadsheet style matrix, select the bridge type **Quarter**.



- In the simplified graphical diagram, click on the bridge icon (**D** in Figure N.9 on page 911) the quarter-bridge representation can be seen.

5 Switch S3 in Figure N.1 on page 904 is closed when quarter-bridge completion is selected.

Excitation

The following options are provided for bridge excitation:

- Switch excitation on and off.
- Select between voltage and current excitation.
- Use sense lines to make sure that the correct voltage is applied to the bridge, even with longer lead wiring.

All selections are made using Perception. However, additional wiring is necessary when using sense lines:

- Add a connection from Pin 3 (+sense) to the bridge connection marked A in Figure N.1 on page 904.
- Add a connection from Pin 4 (-sense) to the bridge connection marked D in Figure N.1 on page 904.

Excitation on/off: Provision for separately switching off the bridge voltage while the remainder of the measuring circuit remains operational. This is an important and useful feature, particularly when measuring dynamic strains. Any output observed when the bridge voltage is switched off must be due to electrical noise, as the output cannot possibly be the result of resistance changes in the measuring circuit when a bridge voltage is not present. The ability to turn off the bridge power is therefore a useful diagnostic tool for establishing whether electrical noise is a problem.

Voltage and current excitation: For the balanced bridge, it does not matter whether the power supply is of the constant-voltage or constant-current variety. In both cases, the output is zero for the resistively balanced state. However, resistive balance circuits may be used with constant current excitation to obtain an initial zero balance of the instrument output when the bridge itself is unbalanced.

Sense lines: Remote sense or, more correctly, remote sensing of excitation voltage, is commonly recommended for use with precision, commercial transducers to prevent leadwire resistance changes (due to changes in either temperature or length) from affecting transducer span, or sensitivity.

Leadwire attenuation presents a potentially significant error source in transducers utilizing a Wheatstone bridge circuit. The leadwires represent a parasitic resistance, and a portion of the excitation voltage intended for the bridge circuit is dropped in the leadwire system, reducing the voltage actually present at the transducer, and effectively reducing the transducer sensitivity.

In Perception
To select the required settings in the Perception software, do the following:

1 In Perception, go to the **Settings** sheet.
2 In the task pane, select the **Bridge** in the **Input** section.
3 Select one or more channels.

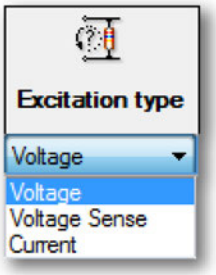
4 To switch the excitation on or off, do one of the following (this opens/closes the switch marked S2a and S2b in Figure N.1):

- Double-click in the correct row(s) of the **Excitation** column in the spreadsheet style matrix.

- In the simplified graphical diagram, click on the excitation switch (**I** in Figure N.9 on page 911).

5 To select an excitation type, do one of the following:

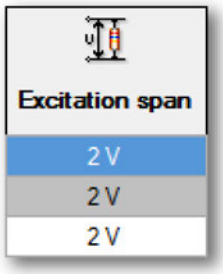
- Select the excitation type in the **Excitation type** column of the spreadsheet style matrix.



- In the simplified graphical diagram, click the **Type** spinner (**G** in Figure N.9 on page 911) the correct selection is shown.

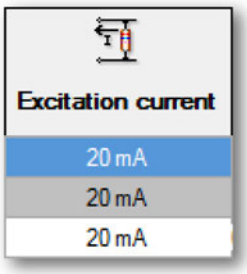
Select one of the following options:

- **Voltage:** Voltage excitation. A voltage is applied between the bridge connection marked A (positive) and the bridge connection marked D (negative). To set the voltage level either:
  - Enter the required voltage in the **Excitation span** column of the spreadsheet style matrix.



  - In the simplified graphical diagram, use the **Excitation** box (**H** in Figure N.9 on page 911) to enter a value.

- **Voltage Sense:** Voltage excitation with sense. Sense inputs are used to monitor the voltage at the sensor connection point. This puts the switch marked S1a and S1b in Figure N.9 on page 911 into the sense position. Use the **Voltage** procedure to set the required voltage. The sense check boxed (marked **E** in Figure N.9 on page 911) can also be used to toggle the sense lines.
- **Current:** Current excitation. A constant current is fed into the bridge. To set the current level, do one of the following:
  - Enter the required current in the **Excitation current** column of the spreadsheet style matrix.



  - In the simplified graphical diagram, use the **Excitation** box (**H** in Figure N.9 on page 911) to enter a value.

Shunt verification - Setup
A shunt resistor can be used to verify the sensitivity of a bridge. Connect a shunt resistor to Resistor R4 (A-C) or Resistor R3 (C-D) of the bridge and activate the shunt within Perception, an output signal that simulates strain (a deflection) is produced. With known resistor and excitation values, the theoretical deflection can be calculated and compared to the measured deflection value.

The following options are provided:

- Select the active bridge arm: A-C or C-D.
- Select between an internal or external shunt resistor.
- When **internal** is selected, then select between:
  - **Factory-installed:** 20 kΩ or 100 kΩ precision resistors.
  - **User installed:** This resistor needs to be added to the plug-in module in the location marked **CAL**. Please refer to Figure N.1 on page 904 for electrical/schematic details and to Figure N.2 on page 906 for mechanical/location details.

Additional wiring when using remote calibration/shunt

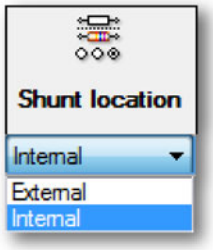
- Connect point A of bridge to Pin 11 (Remote Cal +) of the connector.
- Connect point D of bridge to Pin 12 (Remote Cal -) of the connector.
- Connect point C of bridge to Pin 15 (Remote Cal common) of the connector.
- In addition: when using an external shunt resistor, connect this resistor between Pin 14 (External Shunt A/D) and Pin 13 (External Shunt Common) of the connector.

For an example, please refer to
Figure N.7 "Full-bridge with remote sensing and remote calibration " on page 909.

Perception settings

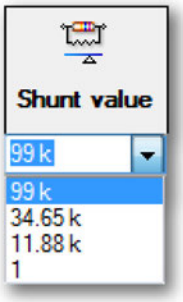
1 Go to the **Settings** sheet.
2 In the task pane, select the **Bridge** in the **Input** section.
3 Select one or more channels.

4 Select between internal or external shunt usage: In the **Internal shunt** column, enable internal to use an **internal** shunt or clear the option to select an **external** resistor. This selection operates switch S7 in Figure N.1.



Depending on the selection:

- When **internal** has been selected, then select the correct value in the **Shunt value** column:



  or type the value of the CAL resistor. This selection operates switch S8 in Figure N.1 on page 904.
- When **external** has been selected, then type the correct value of the external resistor in the **Shunt value** column.

5 Select the bridge arm to operate switch S5 in Figure N.1 on page 904:
- In the sheet, use the **Active gage** column to select between **Positive** (A-C) or **Negative** (C-D).

- In the simplified block diagram, click on the **Remote calibration select** switch (**B** in Figure N.9 on page 911) to switch between the two gages.

Shunt verification - Procedure
Once all the wiring and resistors have been set up correctly, a shunt verification can be done.

Shunt verification preparation

1 In Perception, go to the **Settings** sheet.
2 In the task pane, select the **Bridge** in the **Input** section.
3 Select one or more channels.
4 Switch **Excitation ON**.
5 Select an **Excitation voltage.**
6 In the task pane, select **Shunt Verification** in the **Sensors** section.
7 Select one or more channels.
8 Select between internal or external shunt usage: In the **Internal shunt** column, enable internal to use an **internal** shunt or clear the option to select an **external** resistor. Select the appropriate value setting as described earlier or click on the switch in the diagram (**G** in Figure N.13).
9 Select the bridge arm: Use the **Active gage** column to select between **Positive** (A-C) or **Negative** (C-D) or click on the switch in the diagram (**I** in Figure N.13).

The actual shunt verification is done using the shunt verification dialog.

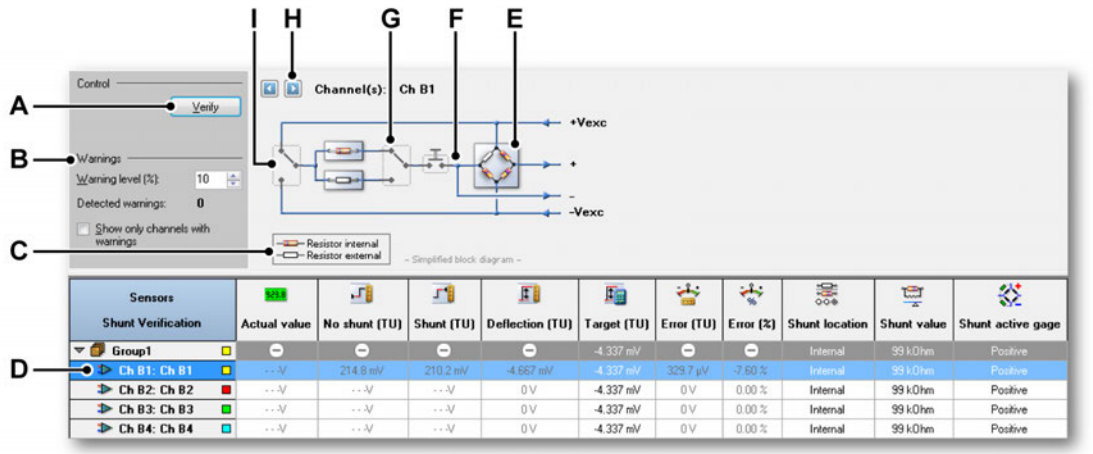


Figure N.13: Shunt verification dialog

A Verify command

B Warning settings

C Legend

D Selected channel

E Bridge representation

F Verify command

G Shunt location selection

H Channel selection

I Shunt active gage selection (S5 in Figure N.1 on page 904)

Shunt verification

1. In Perception, go to the **Settings** sheet.
2. In the task pane, select the **Sensors** in the **Shunt Verification** section.
3. Select one or more channels.
4. Enter a value for the **Warning level** as a percentage.
5. Enter a value as **Target**: The target value is the result of the bridge value, excitation value and shunt value. Tables exist for commonly used values. For an example, please refer to Figure N.8. In Figure N.13 on page 924 the value that corresponds to a 350 Ω bridge, 20 kΩ shunt is used, thereby resulting in a 4.337 mV deflection per volt excitation and a 1 volt excitation.
6. Click **Verify**. This closes S6 in Figure N.1 on page 904 for a short period of time to measure the deflection.

Bridge balance

The bridge circuit is only in balance (has no output when the bridge voltage is applied) when R1 / R2 = R4 / R3. Taking the various resistance tolerances on the strain gauge(s), resistors and lead wires into account, an initial unbalance is invariably present. Adjusting the initial balance so that there is zero output at zero strain is achieved by bridge balancing.

While resistive-balance circuits are widely used in strain gauge instrumentation, GN410 and GN411 use an alternative electronic method of balancing the output to zero, involving measuring the output of the bridge and injecting an equal and opposite voltage. This method permits rapid automatic balancing in multi-channel systems and eliminates the bridge loading errors that can occur in the resistive system when making measurements with precision strain gauge transducers.

HINT/TIP

When doing a bridge balance, the GN410 and GN411 acquisition card measures the input value at the connector of the acquisition card. This means it cannot “see” if a bridge is actually connected or not. No voltage present can mean that the bridge is balanced or that no bridge is connected.

Bridge balancing in Perception is done with the Bridge Balance dialog.

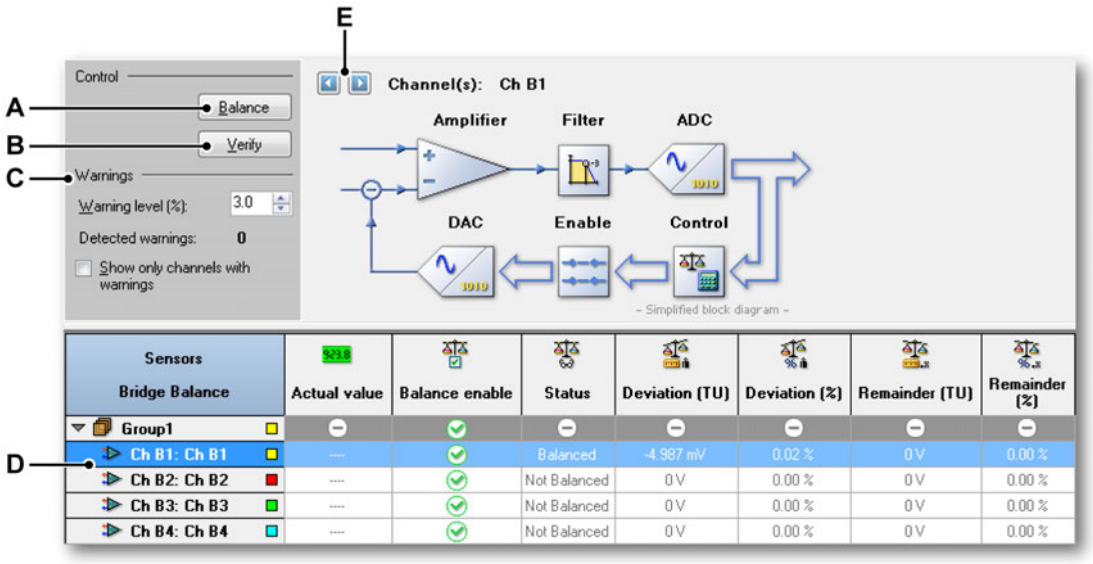


Figure N.14: Bridge Balance dialog

A Balance command

B Verify command

C Warning settings

D Selected channel

E Schematic block diagram of balance circuit

To balance a bridge
To balance a bridge in Perception, do the following:

1. In Perception, go to the **Settings** sheet.
2. In the task pane, select **Bridge Balance** in the **Sensors** section.
3. Use the **Balance Enable** column to enable/disable the balancing of channels.
4. Enter a value for the **Warning level** as a percentage.
5. Select one or more channels.
6. Click the **Balance** command and wait for the results.

N.2 GN440 and GN441 Universal amplifier input cards

This unique, high-end input card with an ultra-fast amplifier serves a variety of needs, from differential and/or isolated measurements to IEPE-based vibration or shunt-based current measurements.

The universal amplifier input card has four input channels. Each channel samples at a maximum speed of 200 kS/s or 1 MS/s with a 16 bit resolution. The bandwidth is 500 kHz and a selection of time or frequency domain optimized filters is available to eliminate noise if needed. The voltage range for a channel can be set from ±10 mV to ±100 V, making the card adaptable to nearly every application. True optical isolation allows for measurements with a common mode voltage of up to 250 V RMS.

The on-board differential input amplifiers eliminate noise picked up in the device under test or the measurement leads. Each amplifier typically offers a high CMRR of 80dB. By switching to "IEPE mode", the amplifiers supports any type of constant current supplied vibration and acceleration sensors. In "Current mode", the built-in shunt can be used to measure up to one ampere in a safe, isolated and fused manner, without the need for external shunt resistors.

N.3 GN412 and GN413 High Speed - Differential input cards

For ultra fast signals, the **25 MS/s** and **100 MS/s** high speed differential input cards are equipped with four channels that sample at incredibly high speeds. With selectable anti-aliasing filtering and a 14 bit (100 MS/s) or 15 bit resolution (25 MS/s), these inputs turn the GEN DAQ systems into an extremely fast transient recorder. Enhanced resolution mode increases the input resolution to 16 bit for both models at lower speeds. The inputs feature a fully differential amplifier that offer a good common mode rejection and enable ground measurements.

N.4 GN401 Optical Fiber Isolated 100 MS/s input card

- **4 transmitters per receiver card**
- Digital fiber optic connection, noise/error and drift free
- Cable length up to 1000 m
- Automatic cable length phase compensation
- 1 isolated, unbalanced differential input per transmitter
- Battery powered transmitter
- **1.8 kV RMS isolation continuous powered transmitter**
- ± 20 mV to ± 100 V input ranges
- Analog/digital anti-alias filters
- 15 or 14 bit resolution
- Metal BNC input on transmitter

The optical fiber isolated system consists of up to four transmitter units (GN110, GN111, GN112 or GN113) connected to the GN401 receiver card built into any GEN series mainframe using a digital fiber optic cable.
By converting the analog signal into a digital signal and transmitting the signal to the receiver card via fiber optic cable, the transmission does not add any drift or error to the measured signal. The automatic cable length compensation phase matches all fiber optic isolated channels to any standard analog input channel. The GN112 and GN113 offer continuous powered isolation at 1.8 kV RMS, while the GN110 and GN111 offer higher isolation options using battery power with a continuous operation time of 30 hours. Optimum anti-alias protection is achieved by the 6-pole analog anti-alias filter combined with a fixed sample rate Analog-to-Digital converter. At lower sample rates the digital anti-alias filters allow for a large range of 8^{th} order Bessel IIR filters with precise phase match and ultra low noise output.
The GN112 and GN113 offer continuous powered isolation at 1.8 kV RMS, while the GN110 and GN111 offer higher isolation options using battery power with an continuous operation time of 30 hours.

N.5 Binary marker cards

N.5.1 GN6470 Binary marker card

The GN6470 binary marker input card is a dedicated binary input option for the GEN series instruments. It enables to record up to 64 binary input channels (marker channels) with up to 1 MS/s per channel. In addition, software control can assign 9 binary input channels to provide 3 channels of counter/timer functionality.

The binary channels can be recorded and reviewed like analog channels in Perception and enable a large number of binary status signals to be recorded together with the analog input channels.

The counter/timer functionality includes:

- 64 bit general purpose up/down counter
- Frequency/RPM counter
- Quadrature/position measurements

The counter/timer functionality uses up to 3 event bits per channel. These event bits also keep their original functionality. For example, a quadrature encoder rotation is recorded, while at the same time the quadrature output signals are recorded separately.

N.5.2 GN4070 Binary marker HV card

The GN4070 binary marker HV card is a combined electrical and optical binary marker input card. It enables to record up to 32 electrical and eight optical binary input channels (marker channels) with up to 1 MS/s per channel. The optical isolated binary makers are specifically suited for the medium/high voltage market. A fiber optic isolated output is provided to present an REC signal that can be used to drive an external instrument. The fiber optic inputs and the fiber optic REC output allow for a tight integration with the BE3200 high-definition test sequencer.

In addition, software control can assign nine binary input channels to provide three channels of counter/timer functionality.

The counter/timer functionality includes:

- 64 bit general purpose up/down counter
- Frequency/RPM counter
- Quadrature/position measurements

The counter/timer functionality uses up to 3 event bits per channel. These event bits also keep their original functionality. For example, a quadrature encoder rotation is recorded, while at the same time the quadrature output signals are recorded separately.

N.5.3 Connector pinning GN6470 and GN4070

The GN6470 binary marker cards come with four 26 pin connectors. The GN4070 replaces the top two connectors with eight optical receivers and one optical transmitter. The following diagram and table provide the pinning information of each 26 pin connector.

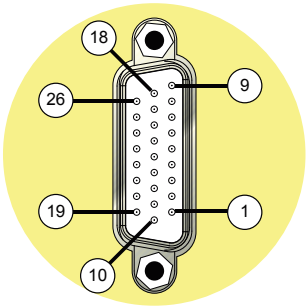


Figure N.15: Binary marker card connector pinning

Table N.2: Event bit (marker) connector pinning

PIN #	EV1-16	EV17-32	EV33-48	EV49-64
1	Event Bit 16	Event Bit 32	Event Bit 48	Event Bit 64
2	Event Bit 15	Event Bit 31	Event Bit 47	Event Bit 63 *
3	Event Bit 14	Event Bit 30	Event Bit 46	Event Bit 62 *
4	Event Bit 13	Event Bit 29	Event Bit 45	Event Bit 61 *
5	Event Bit 12	Event Bit 28	Event Bit 44	Event Bit 60
6	Event Bit 11	Event Bit 27	Event Bit 43	Event Bit 59 *
7	Event Bit 10	Event Bit 26	Event Bit 42	Event Bit 58 *
8	Event Bit 9	Event Bit 25	Event Bit 41	Event Bit 57 *
9	Event Bit 8	Event Bit 24	Event Bit 40	Event Bit 56
10	Event Bit 7	Event Bit 23	Event Bit 39	Event Bit 55 *
11	Event Bit 6	Event Bit 22	Event Bit 38	Event Bit 54 *
12	Event Bit 5	Event Bit 21	Event Bit 37	Event Bit 53 *
13	Event Bit 4	Event Bit 20	Event Bit 36	Event Bit 52
14	Event Bit 3	Event Bit 19	Event Bit 35	Event Bit 51
15	Event Bit 2	Event Bit 18	Event Bit 34	Event Bit 50
16	Event Bit 1	Event Bit 17	Event Bit 33	Event Bit 49
17	Ground	Ground	Ground	Ground
18	Ground	Ground	Ground	Ground
19	Ground	Ground	Ground	Ground
20	Ground	Ground	Ground	Ground

PIN #	EV1-16	EV17-32	EV33-48	EV49-64
21	Ground	Ground	Ground	Ground
22	Ground	Ground	Ground	Ground
23	Ground	Ground	Ground	Ground
24	Ground	Ground	Ground	Ground
25	+5 V	+5 V	+5 V	+5 V
26	+5 V	+5 V	+5 V	+5 V

(*) = Event input combined with counter/timer channel function

N.5.4 GN6470 and GN4070 Input block diagram

The diagram below shows the block schematic representation of the event input circuitry. The actual implementation could deviate slightly from this diagram.

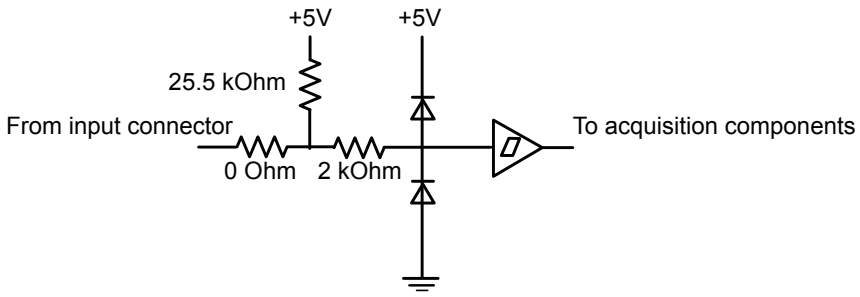


Figure N.16: GN6470/GN4070 binary marker card input circuitry

N.5.5 GN6470 and GN4070 Counter mode pinning

When in counter mode, Event Bits 53 through 63 are used to provide the counter functionality. These bits are located on the bottom connector as follows:

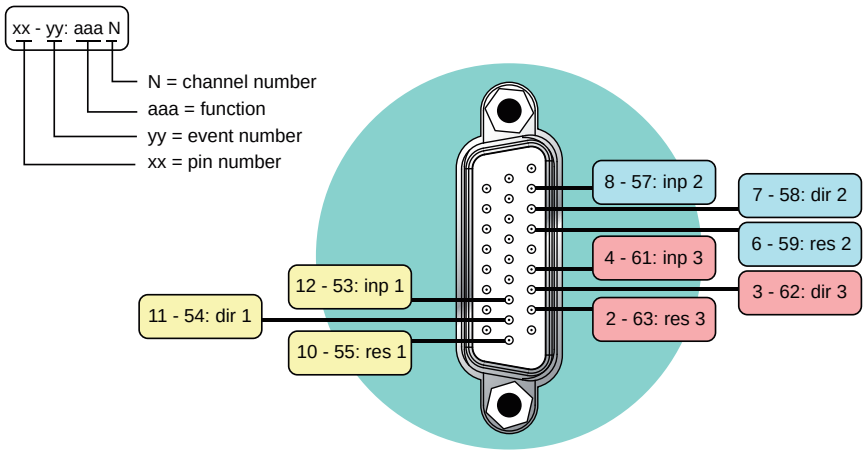


Figure N.17: Counter pinning layout

Table N.3: Counter bit connector pinning

PIN #	EVENT	COUNTER	FUNCTION
12	Event Bit 53	1	Counter input
11	Event Bit 54	1	Direction: increment / decrement
10	Event Bit 55	1	Reset
8	Event Bit 57	2	Counter input
7	Event Bit 58	2	Direction: increment / decrement
6	Event Bit 59	2	Reset
4	Event Bit 61	3	Counter input
3	Event Bit 62	3	Direction: increment / decrement
2	Event Bit 63	3	Reset

In the Perception software, the event bits are combined within one channel and labeled as CH1_1 through CH1_64. The counter/timer channels are referred to as CH2 through CH4.

Counter input The counter input is the actual signal input. The counter value is modified on each rising edge of this signal. The maximum input rate is 10 Mhz.

Direction The direction signal determines whether the counter is incremented (direction = “0”), or decremented (direction = “1”) on each rising edge of the counter input.

Reset The reset signal resets the counter to zero. Software control determines the reset enabling as well as the active level.

Use Perception to select the operation mode of the counter/timer channel.

N.5.6 GN6470 and GN4070 Frequency (RPM) mode pinning

When in frequency mode, Event Bits 53 through 63 are used to provide the frequency measurement functionality. These bits are located on the bottom connector as follows:

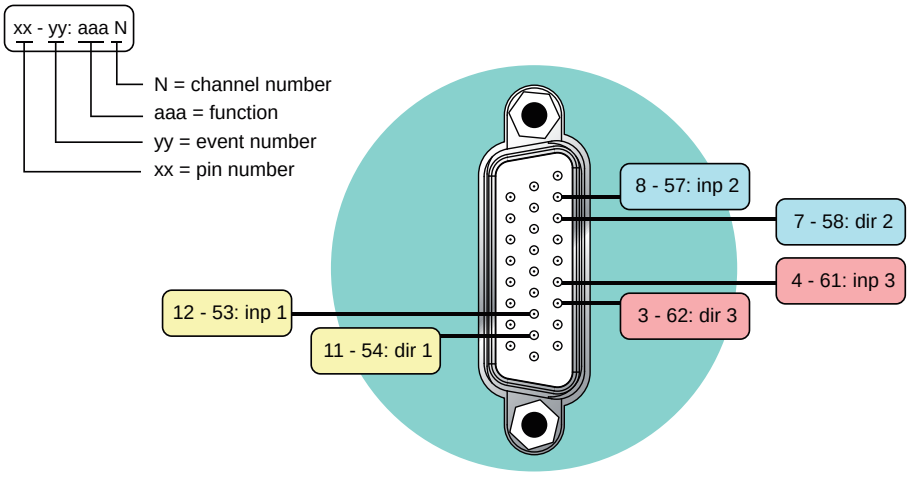


Figure N.18: Frequency measurement pinning layout

Table N.4: Counter bit connector pinning

PIN #	EVENT	FREQ. CH.	FUNCTION
12	Event Bit 53	1	Counter input
11	Event Bit 54	1	Direction: increment / decrement
10	Event Bit 55	–	Not used
8	Event Bit 57	2	Counter input
7	Event Bit 58	2	Direction: increment / decrement
6	Event Bit 59	–	Not used
4	Event Bit 61	3	Counter input
3	Event Bit 62	3	Direction: increment / decrement
2	Event Bit 63	–	Not used

In the Perception software, the event bits are combined within one channel and labeled as CH1_1 through CH1_64. The counter/timer channels are referred to as CH2 through CH4.

For frequency measurements, the counter/timer channels use an additional gate clock to create a time interval (gate time) in which pulses are counted. The minimum gate time is 1 µs and the maximum gate time is 10 s. A long gate time increases the Timer/Counter resolution but comes with slower update rates. Selecting the right gate time is a balance between update rate and required resolution.

Counter input The counter input is the actual signal input. The counter is incremented on each rising edge of this signal. The maximum input frequency is 10 MHz.

Direction The direction signal determines whether the counter is incremented (direction = “0”), or decremented (direction = “1”) on each rising edge of the counter input.

Use Perception to select the operation mode of the counter/timer channel. Perception will also calculate the RPM (Rotations Per Minute) using the measured frequency and additional information like pulses per rotation.

N.5.7 GN6470 and GN4070 Quadrature (position) mode pinning

When in quadrature mode, Event Bits 53 through 63 are used to provide the position measurement capability by measuring the signals as provided by quadrature encoders. These bits are located on the bottom connector as follows:

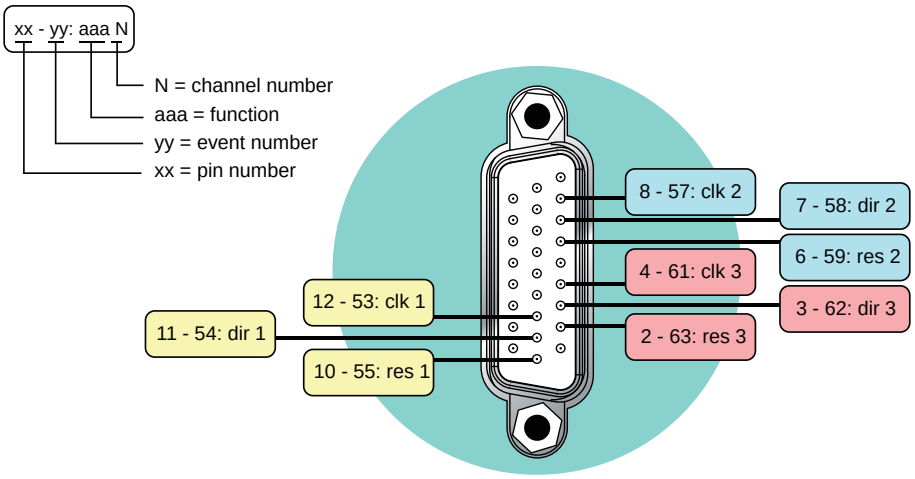


Figure N.19: Quadrature measurement pinning layout

Table N.5: Quadrature measurement bit connector pinning

PIN #	EVENT	QUAD. CH.	FUNCTION
12	Event Bit 53	1	Clock input (A)
11	Event Bit 54	1	Direction input (B)
10	Event Bit 55	1	Reset
8	Event Bit 57	2	Clock input (A)
7	Event Bit 58	2	Direction input (B)
6	Event Bit 59	2	Reset
4	Event Bit 61	3	Clock input (A)
3	Event Bit 62	3	Direction input (B)
2	Event Bit 63	3	Reset

In the Perception software, the event bits are combined within one channel and labeled as CH1_1 through CH1_64. The counter/timer channels are referred to as CH2 through CH4.

Clock input (A) The clock input is the actual signal input. The counter is incremented on each rising edge of this signal if the direction input is low (“0”). The counter is decremented on each rising edge of this signal if the direction input is high (“1”).

Direction input (B) The direction signal determines whether the counter is incremented (direction = “0”), or decremented (direction = “1”) on each rising edge of the counter input.

Reset The reset signal resets the counter to zero. Software control determines the reset enabling and the active level.

Use Perception to select the operation mode of the counter/timer channel.

The most common type of incremental encoder uses two output channels (A and B) to sense position. Using two code tracks with sectors positioned 90 degrees out of phase, the two output channels of the quadrature encoder indicate the position and direction of rotation. For example, if A leads B, the disk is rotating in a clockwise direction. If B leads A, then the disk is rotating in a counter-clockwise direction.

By monitoring both the number of pulses and the relative phase of signals A and B, both the position and direction of rotation can be tracked.

Some quadrature encoders also include a third output channel, called a zero, index or reference signal. The third output channel supplies a single pulse per revolution. This single pulse is used to determine a reference position precisely.

N.5.8 Configure the Timer/Counters in Perception

To activate Channel 8 or Channel 9 in Perception

1 Change the resolution of Recorder B to **18 bit**

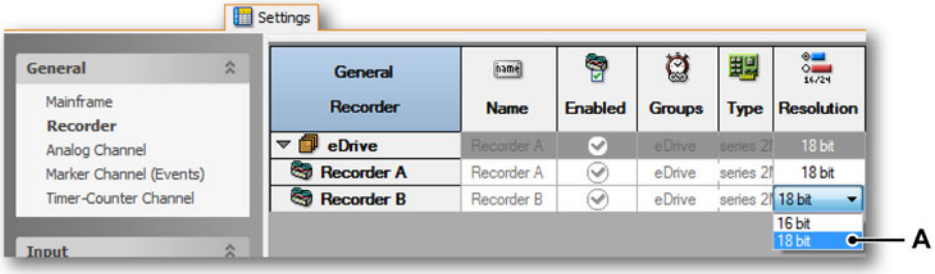


Figure N.20: Activating Channel 8 or Channel 9 in Perception

A Recorder B with 18 bit resolution

2 Configure the Timer/Counter (Perception):

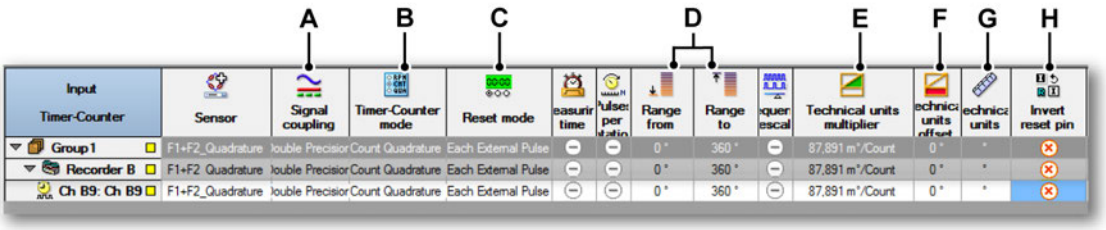


Figure N.21: Configuration of the Timer/Counter connector in Perception

A **Signal coupling mode** In quadrature mode, the counter supports three ways of tracking the quadrature states defined by the signal coupling.

- Single precision
- Double precision
- Quad precision

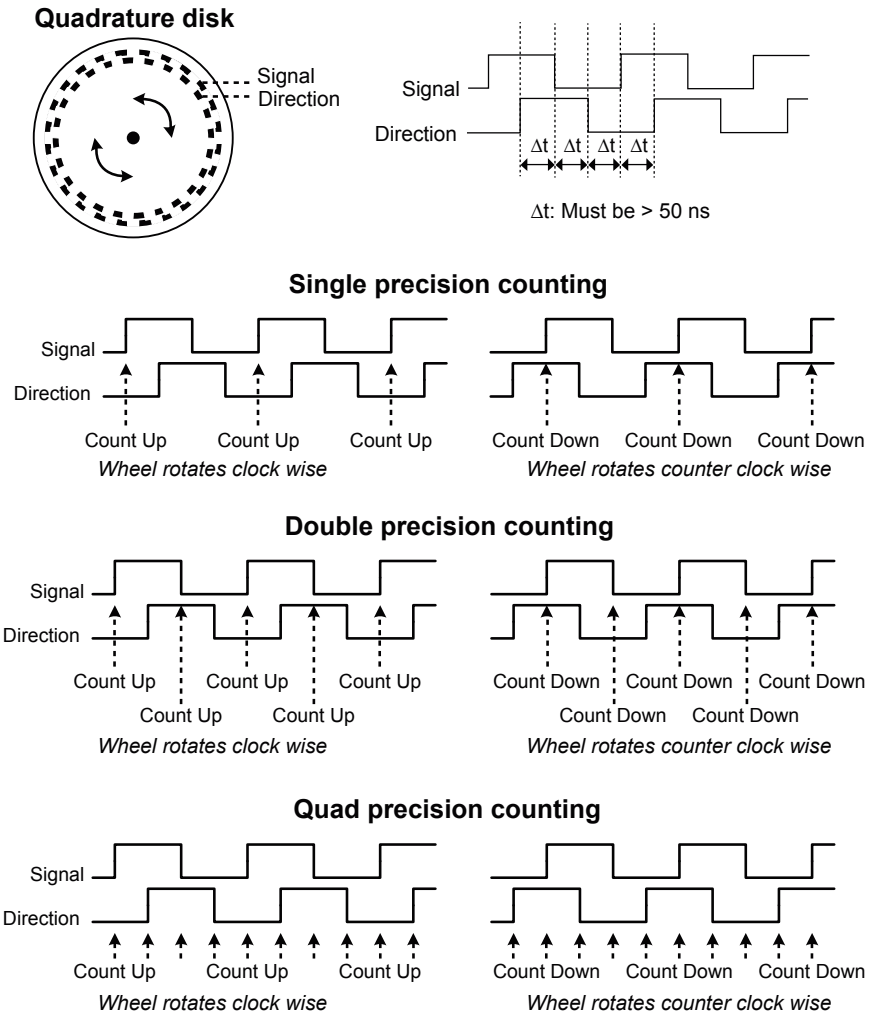


Figure N.22: Signal coupling/precision modes

- In **single precision**, the counter only increments/decrements on the rising edge of the signal input. This is the default traditional quadrature count mode.
- In **double precision**, the counter increments/decrements on both the rising and falling edge of the signal input. As a result, smaller rotations can already be detected. For every full rotation the counter counts double the values compared to the single precision signal coupling mode.
- In **quad precision**, the counter increments/decrements on every rising and falling edge of both the signal and direction input. As a result, even smaller rotations can already be detected. For every full rotation the counter counts quadruple values compared to the single precision signal coupling mode.

Unless other requirements do not allow the quad precision mode to be selected, using this mode is strongly advised due to it higher accuracy.

B **Timer Counter mode:** Count Quadrature -> counters monitor the transition of the four different states the signal can be in.

C **Reset Mode:** Each External Pulse -> resets the counter every time we receive a pulse in Reset input.

D **Range from/to** 0 to 360°

E **Technical units multiplier: 87.891** m°/Count
This setting assumes the use of an encoder with **4096** pulses/rotation
1024 pulses [from encoder] x 4 transitions [quad precision selected].

F **Technical units offset:** 0°

G **Technical units:** ° (degrees)

H **Invert reset pin:** Deactivated* -> A High Level of Reset input is needed to reset the counter to 0.

Note ***** *The counter works ONLY when the reset input is set to Low. After you reset the counter with a High Level, you need to return the reset level to Low to continue the measurement. In other words, your reset signal needs to be a really short impulse in order to minimize the amount of time that the counter is not counting.*

N.5.9 GN4070 Connectors and pinning

The binary marker HV card comes with nine fiber optic connectors (see Figure N.23) and two 26 pin connectors. The lowest fiber optic connector provides the recording status output. The fiber optic input connectors provide the marker (event) channels labeled 1 through 8. The non-isolated marker inputs provide the marker (event) channels labeled 33 through 64.

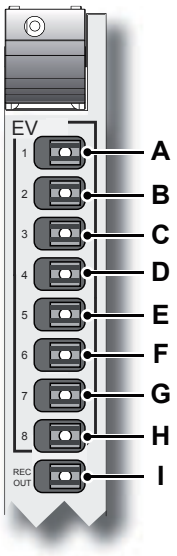


Figure N.23: GN4070 binary marker HV card (detail)

A Event Bit 1

B Event Bit 2

C Event Bit 3

D Event Bit 4

E Event Bit 5

F Event Bit 6

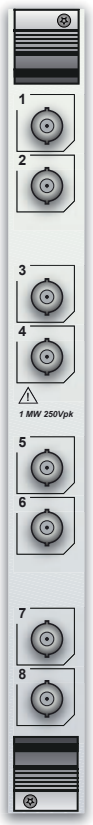
G Event Bit 7

H Event Bit 8

I Recording active output

N.6 Basic amplifier non-isolated input cards

N.6.1 GN810 Basic 200kS/s input card

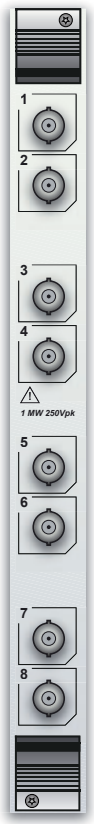


- 8 analog channels
- Single-ended inputs
- ± 1 V to ± 50 V input range
- User selectable digital Bessel and FIR filters
- 200 kS/s sample rate
- 16 bit resolution
- 128 MB memory
- Single metal BNC for each channel

The GEN DAQ Basic 200 kS/s input card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or probes and current clamps.
The basic signal conditioner provides eight channels of single-ended voltage inputs from ± 1 V to ± 50 V Full Scale with full offset and auto-zero capability. Every channel is equipped with an independent full range input amplifier, a seven-pole Bessel and Butterworth anti-alias filter, a 16 bit Analog-to-Digital converter and several selections of digital filtering.
The on-board transient memory size is 64 Mega-Samples (128 Mega-Bytes). The memory is shared among enabled channels. Each channel also features two set-points for trigger or alarm purposes. Extensive acquisition and trigger modes allow for many different ways to capture valuable data, even at the highest sample rates. All channels are synchronously sampled at full speed without multiplexing and almost immeasurable crosstalk. The model uses standard metal BNC connectors, whose shells are connected to ground. The inputs have an impedance of 1 MΩ and are compatible with probes and current clamps.

For more information on the GN810 Basic 200K input card, please refer to "B2632-3.1 en (GEN series GN810)" on page 984.

N.6.2 GN811 Basic 1MS/s input card

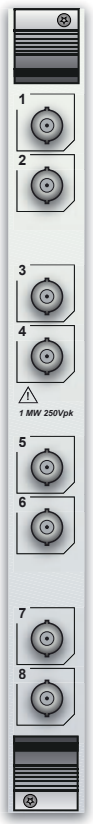


- 8 analog channels
- Single-ended inputs
- ± 1 V to ± 50 V input range
- User selectable digital Bessel and FIR filters
- 1 MS/s sample rate
- 16 bit resolution
- 256 MB memory
- Single metal BNC for each channel

The GEN DAQ Basic 1 MS/s input card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or probes and current clamps.
The basic signal conditioner provides eight channels of single-ended voltage inputs from ± 1 V to ± 50 V Full Scale with full offset and auto-zero capability. Every channel is equipped with an independent full range input amplifier, a seven-pole Bessel and Butterworth anti-alias filter, a 16 bit Analog-to-Digital converter operating at 1 MS/s and several selections of digital filtering.
The on-board transient memory size is 128 Mega-Samples (256 Mega-Bytes). The memory is shared among enabled channels.
Each channel also features two set-points for trigger or alarm purposes. Extensive acquisition and trigger modes allow for many different ways to capture valuable data, even at the highest sample rates. All channels are synchronously sampled at full speed without multiplexing and almost immeasurable crosstalk. The model uses standard metal BNC connectors. The inputs have an impedance of 1 MΩ and are compatible with probes and current clamps.

For more information on the GN811 Basic 1M input card, please refer to "B2640-3.1 en (GEN series GN811)" on page 999.

N.7 GN812 Basic ISO 1MS/s input card



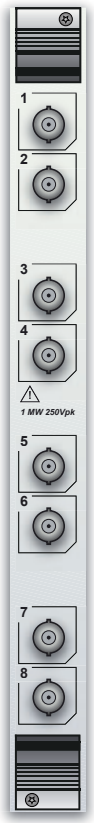
- 8 analog channels
- Unbalanced differential inputs
- ± 1 V to ± 50 V input range
- 250 V DC Isolation
- User selectable digital Bessel and FIR filters
- 1 MS/s sample rate
- 16 bit resolution
- 512 MB memory
- Single isolated BNC for each channel

The GEN DAQ Basic ISO 1 MS/s input card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or isolated probes and current clamps.
The basic signal conditioner provides eight channels of isolated single-ended voltage inputs from ± 1 V to ± 50 V Full Scale with full offset and auto-zero capability. Every channel is equipped with an independent full range input amplifier, a seven-pole and Butterworth anti-alias filter, a 16 bit Analog-to-Digital converter operating at 1 MS/s and several selections of digital filtering.
The on-board transient memory size is 256 Mega-Samples (512 Mega-Bytes). The memory is shared among enabled channels.
Each channel also features two set-points for trigger or alarm purposes. Extensive acquisition and trigger modes allow for many different ways to capture valuable data, even at the highest sample rates. All channels are synchronously sampled at full speed without multiplexing and almost immeasurable crosstalk. The model uses standard isolated BNC connectors, whose shells are connected to isolated ground. The inputs have an impedance of 1 MΩ and are compatible with isolated probes and current clamps.

For more information on the GN812 Basic 1M Isolated input card, please refer to "B2634-3.1 en (GEN series GN812)" on page 1015.

N.8 Basic Extended Isolated amplifier card

N.8.1 GN813 Basic XT ISO 1 MS/s input card

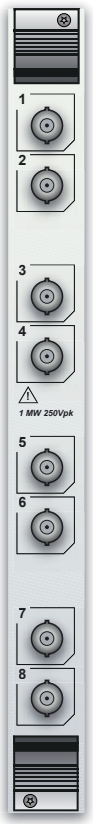


- 8 analog channels
- Unbalanced differential inputs
- ± 2 V to ± 100 V input range
- 250 V DC channel to channel isolation
- User selectable digital Bessel and FIR filters
- 1 MS/s sample rate
- 16 bit resolution
- 512 MB memory
- Single isolated BNC for each channel

The GEN DAQ Basic XT ISO 1 MS/s input card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or isolated probes and current clamps.
The basic signal conditioner provides eight channels of isolated single-ended voltage inputs from ± 2 V to ± 100 V Full Scale with full offset and auto-zero capability. Every channel is equipped with an independent full range input amplifier, a seven-pole Bessel and Butterworth anti-alias filter, a 16 bit Analog-to-Digital converter operating at 1 MS/s and several selections of digital filtering.
The on-board transient memory size is 256 Mega-Samples (512 Mega-Bytes). The memory is shared by enabled channels.
Each channel also features two set-points for trigger or alarm purposes. Extensive acquisition and trigger modes allow for many different ways to capture valuable data, even at the highest sample rates. All channels are synchronously sampled at full speed without multiplexing and almost immeasurable crosstalk. The model uses standard isolated BNC connectors, whose shells are connected to isolated ground. The inputs have an impedance of 1 MΩ and are compatible with isolated probes and current clamps.

For more information on the GN813 Basic XT ISO 1 MS/s input card, please refer to "B2635-4.1 en (GEN series GN813)" on page 1031.

N.8.2 GN814 Basic XT ISO 200kS/s input card



- 8 analog channels
- Unbalanced differential inputs
- ± 2 V to ± 100 V input range
- 250 V DC isolation
- User selectable digital Bessel and FIR filters
- 200 kS/s sample rate
- 16 bit resolution
- 128 MB memory
- Single isolated BNC for each channel

The GEN DAQ Basic XT ISO 200 kS/s input card is a general purpose signal conditioner for use with voltage inputs, externally conditioned signals or isolated probes and current clamps.
The basic signal conditioner provides eight channels of isolated single-ended voltage inputs from ± 2 V to ± 100 V Full Scale with full offset and auto-zero capability. Every channel is equipped with an independent full range input amplifier, a seven-pole Bessel and Butterworth anti-alias filter, a 16 bit Analog-to-Digital converter and several selections of digital filtering.
The on-board transient memory size is 64 Mega-Samples (128 Mega-Bytes). The memory is shared among enabled channels. Each channel also features two set-points for trigger or alarm purposes. Extensive acquisition and trigger modes allow for many different ways to capture valuable data, even at the highest sample rates. All channels are synchronously sampled at full speed without multiplexing and almost immeasurable crosstalk. The model uses standard isolated BNC connectors, whose shells are connected to isolated ground. The inputs have an impedance of 1 MΩ and are compatible with isolated probes and current clamps.

For more information on the GN814 Basic XT ISO 200K input card, please refer to "B2889-5.1 en (GEN series GN814)" on page 1047.

N.8.3 Optional G041 1kV DC probe

The 1kV DC probe is a special front-end extension for the Basic Extended Isolated amplifier cards (1-GN813-2 and 1-GN814-2). It increases the maximum input range by a factor of ten with a maximum input voltage of +/- 1000 V.
The HV probe offers an accuracy of 0.1% (accuracy is typically 0.05%) and can be freely moved in front of any channel within these specification. Using the probe with the Basic Extended Isolated amplifier card operating in wideband, the bandwidth is designed to meet 250 kHz ± 10% (-3 dB)

To accommodate the probes, a 1kV DC probe rack mount housing is available. This uses up a single height unit and holds up to sixteen 1kV DC probes. Each probe comes with a fixed output connection cable with a double isolated coax cable. This connects directly into the Genesis Isolated Basic amplifier.

CAUTION

As the probe rack specifies the maximum voltages per input pin, the 1kV DC and AC probes are not to be mixed in one probe rack.

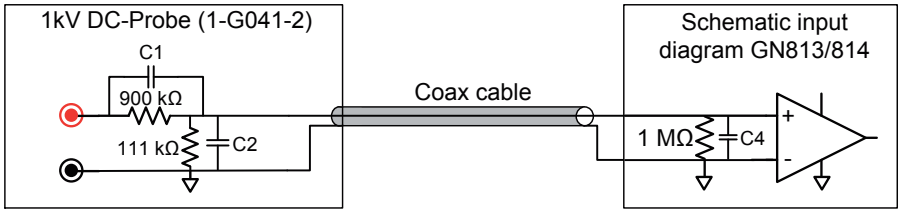


Figure N.24: 1kV DC probe 1-G041-2

The probes have no calibration points. The DC inaccuracy is designed to meet its specifications based in the input resistance of the basic extended isolated amplifiers. The AC bandwidth inaccuracy is designed to meet its specification based on the variance of the capacitive load of the basic extended isolated amplifiers. Calibration of the 1kV DC probes will only check whether tolerances are still met. When deviations occur, the probes must be repaired, as no adjustments can be carried out.

CAUTION

The coaxial cable attached to the 1kv DC probe adds a capacitive load to the output of the probe. Every cm length added or removed changes the capacitive load. By design, the cable length of the 1kV DC probe is fixed and cannot be changed.

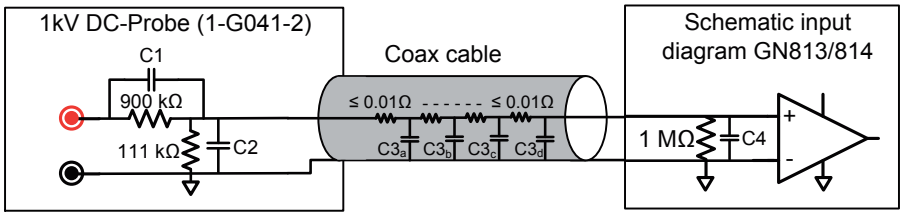


Figure N.25: 1kV DC probe cable capacitance

Specifications	
Number of channels	1 per probe, 16 per probe rack
Input type	Isolated unbalanced differential (isolated single-ended)
Input connectors	2; 4 mm safety banana plugs (red and black)
Input impedance	1 MΩ ± 1%; when using a 1 MΩ output load
Divider ratio	1:10
Inaccuracy	0.1%
Maximum input voltage	
Positive input (red)	1000 V DC
Negative input (black)	250 V DC; As specified by GN813 and GN814 cards
Bandwidth	250 kHz ± 10% (-3 dB)
Coax cable length	Fixed; Several variances as delivered

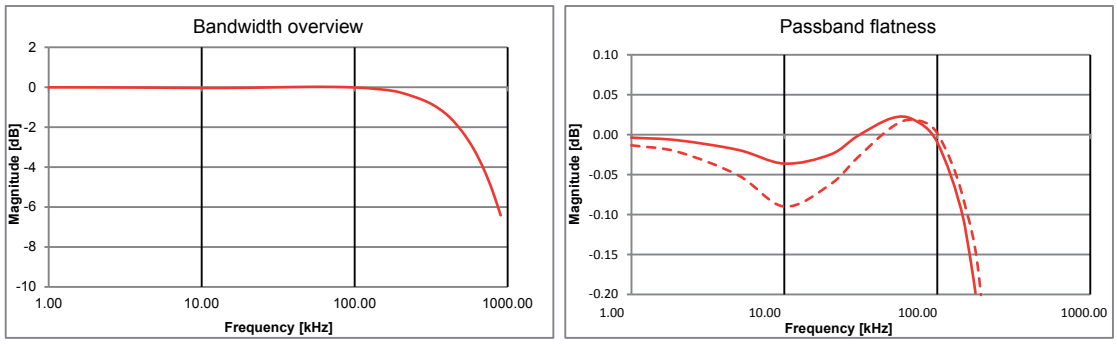


Figure N.26: Typical 1kV DC probe bandwith

N.8.4 Optional G042 1kV AC probe

The 1kV AC probe is a special front-end extension for the Basic Extended Isolated amplifier cards (1-GN813-2 and 1-GN814-2). It decouples any DC voltage component up to ± 1000 V DC from the amplifiers input and allows for high resolution acquisition of the AC portion only of the incoming signal. The AC portion can be as high as 100 V when using the input ranges of the attached acquisition card. Higher resolution can be achieved by selecting the proper measurement range. The high pass AC coupled bandwidth is at 0.8 Hz ± 20%.

To accommodate the probes, a 1kV AC probe rack mount housing is available. This uses up a single height unit and holds up to sixteen 1kV AC probes. Each probe comes with a fixed output connection cable with a double isolated coax cable. This connects directly into the Genesis Isolated Basic amplifier.

CAUTION

As the probe rack specifies the maximum voltages per input pin, the 1kV DC and AC probes are not to be mixed in one probe rack.

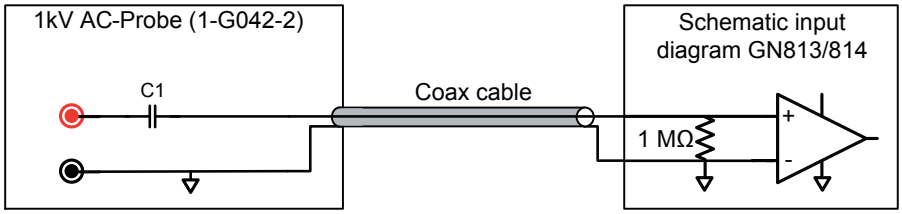


Figure N.27: 1kV DC probe 1-G042-2

The probes have no calibration points. As the probe is fixed AC coupled, no DC inaccuracy is specified. The AC high pass bandwidth inaccuracy is designed to meet its specification based on the input impedance of the basic extended isolated amplifiers. Calibration of the 1kV AC probes only checks whether tolerances are still met. When deviations occur, the probes must be repaired, as no adjustments can be carried out.

CAUTION

Cable length of the 1kV AC probes is not critical for correct operation. However, it is advised not to change the length to prevent possible side effects, such as ringing of step responses due to large impedance mismatches.

Specifications	
Number of channels	1 per probe, 16 per probe rack
Input type	Isolated unbalanced differential (isolated single-ended)
Input connectors	2; 4 mm safety banana plugs (red and black)
Input impedance	1 MΩ ± 1% for AC signal > 1 Hz; when using a 1 MΩ output load
Divider ratio	1:1 for AC signal > 20 Hz
Inaccuracy	AC signal > 100 Hz; As specified by GN813 and GN814 cards
Maximum input voltage	
Positive input (red)	1000 V DC
Negative input (black)	250 V DC; As specified by GN813 and GN814 cards.
AC coupling bandwidth	0.8 Hz ± 20% (-3 dB)
Bandwidth	As specified by GN813 and GN814 cards
Coax cable length	Fixed; Several variances as delivered

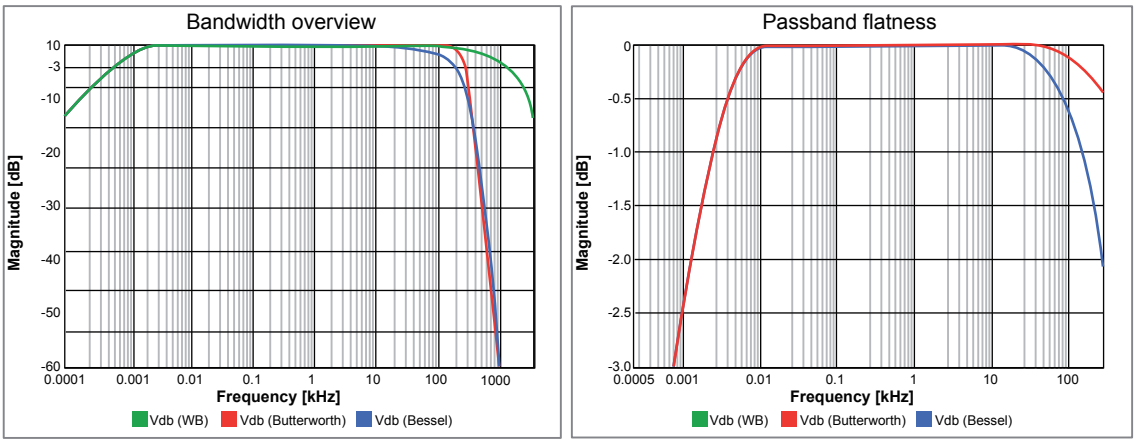


Figure N.28: Typical 1kV AC probe bandwith

Green: GN813/GN814 in wideband

Red: GN813/GN814 using a Butterworth anti-alias filter

Blue: GN813/GN814 using a Bessel anti-alias filter

N.9 High Resolution IEPE and Charge input cards

N.9.1 GN1610 250 kS/s input card

The **GN1610 charge 250 kS/s** input cards are a no-compromise solution for high channel count data acquisition systems.

This card brings:

- A cost-effective solution with 16 channels per card
- High precision with a 24 bit A-to-D convertor for each channel
- Sample rates up to 250 kS/s (both decimal and binary)
- Flexibility; each channel can be individually assigned one of the following signal conditioners:
  - IEPE for accelerometers, microphones, etc.
  - Charge for pressure transducers, piezoelectric accelerometers, etc.
  - Voltage (full differential and single-ended)
- TEDS readout support for IEPE transducers
- Digital event and timer-counter support (on compatible mainframes only)
- 1.8 GB on-board memory

The large number of channels on this single card requires special attention. Therefore, the card is equipped with 50 pin D connectors. To provide easy access to all channels, breakout cables with 19-inch panels for BNC connectors are available as an option.

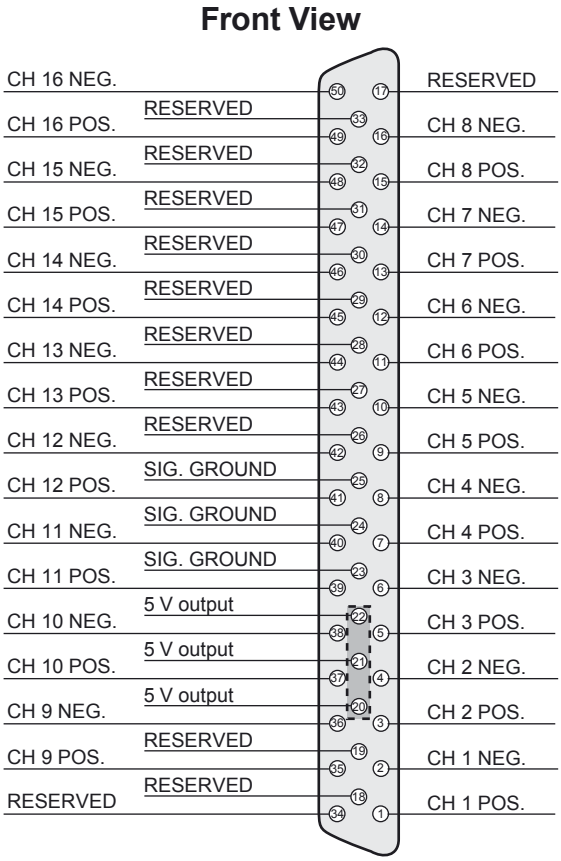


Figure N.29: Pin diagram 16 channel connector

Note *Both positive and negative pins must be connected to avoid erroneous measurement results with noise.*

Note *There are three output pins available on each connector. Each pin's output voltage is 5 V. The maximum current for each pins is 0.1 A. When connecting all three pins 0.3 A can be used.*
Over current protection is add for the maximum 0.3 A using an automatic resettable fuse.

For more information on the 16/32 Channel Accel Card 250 kS/s input card, please refer to "B3240-3.1 en (GEN series GN1610)" on page 1062.

N.9.2 GN1611 basic 20 kS/s input card

The **GN1611 20 kS/s** input card is a no-compromise solution for high-channel-count data acquisition systems.

This card offers:

- A cost-effective solution with 16 channel per card
- High precision with a 16 bit A-to-D convertor for each channel
- Sample rates up to 20 kS/s (both decimal and binary)
- Digital event support (on compatible mainframes only)
- 200 MB on-board memory

The large number of channels on this single card requires special attention. The card is therefore equipped with 50 pin D connectors. To provide easy access to all channels, breakout cables with 19-inch panels for BNC connectors are available as an option.

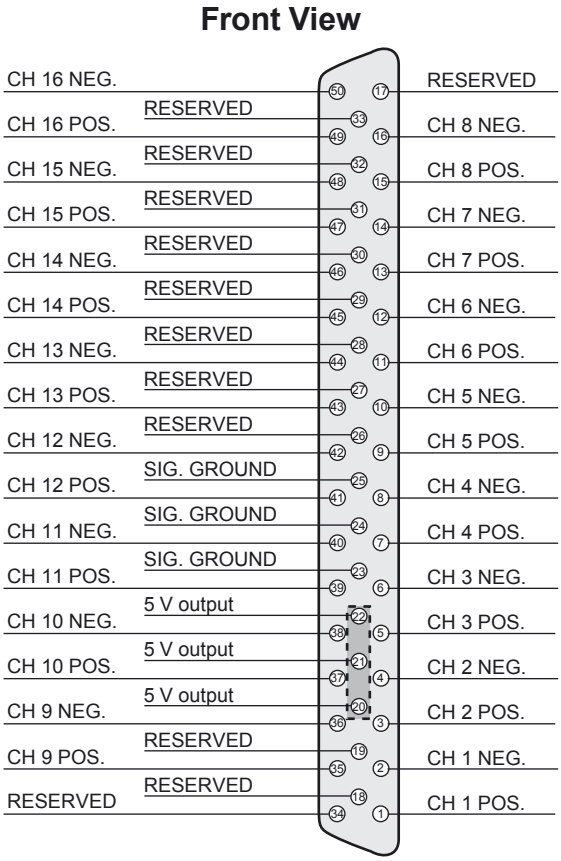


Figure N.30: Pin diagram 16 channel connector

Note *Both positive and negative pins must be connected to avoid erroneous measurement results with noise.*

Note *There are three output pins available on each connector. Each pin's output voltage is 5 V. The maximum current for each pins is 0.1 A. When connecting all three pins 0.3 A can be used.*
Over current protection is add for the maximum 0.3 A using an automatic resettable fuse.

For more information on the 16/32 Channel Basic Card 20 kS/s input card, please refer to "B3264-3.1 en (GEN series GN1611)" on page 1087.

N.10 Master/Slave card (G040)

The GEN series can be operated as a fully synchronized Multi-Mainframe system with multiple mainframes using the Master/Slave card.

With the Master/Slave card you can:

- connect one GEN series “Master” to up to eight “Slaves”
- fully synchronize up to nine mainframes
- record up to 1080 channels with 1 MS/s sampling speed each by using all slots
- or record up to 540 channels with 100 MS/s per channel by using all slots
- use the fiber optic link with up to a 500 m cable between the master and each slave

And the Master/Slave option provides:

- the sampling clock, absolute time info, trigger and start/stop signals between the mainframes, creating a real high channel synchronized system out of the nine mainframes
- a timing accuracy between the mainframes better than 100 ns
- an automatic cable length detection and compensation

Master/Slave card operating modes

The Master/Slave card has three operating modes:

- Master
- Slave
- Stand-alone

In Master mode:

- all connectors function as master output
- the start of recording as well as synchronization signals are transmitted to all connected slaves
- all trigger signals are combined into a global master/slave trigger signal

In Slave mode:

- the top connector is configured as slave input, all other connectors are unused
- all received signals are transferred to a bus for internal distribution
- internal slave trigger signals are transferred to the outside

In Stand-alone mode:

- Stand-alone mode is OFF: the Master/Slave card does not communicate with other Master/Slave cards.

Fiber optic cable
The Master/Slave card has optical I/O (IN/OUT) that connects to other Master/Slave cards.

The fiber optic cable:

- allows up to a 500 m cable between the master and each slave (for more information, please refer to "Calculating maximum fiber cable length" on page 853)
- distributes the sampling clock, absolute time info, trigger and start/stop signals between mainframes, creating a real high channel synchronized system out of the nine mainframes
- enables a timing accuracy between the mainframes less than 100 ns

N.10.1 Master/Slave card operations

The Master/Slave card is easily inserted into the GEN series mainframe and is automatically recognized by the Perception software. A Master/Slave card can be used as a master or slave. One card is required in the master mainframe and one card is required per slave mainframe. Each card has eight LC® connectors for the fiber optic cable.

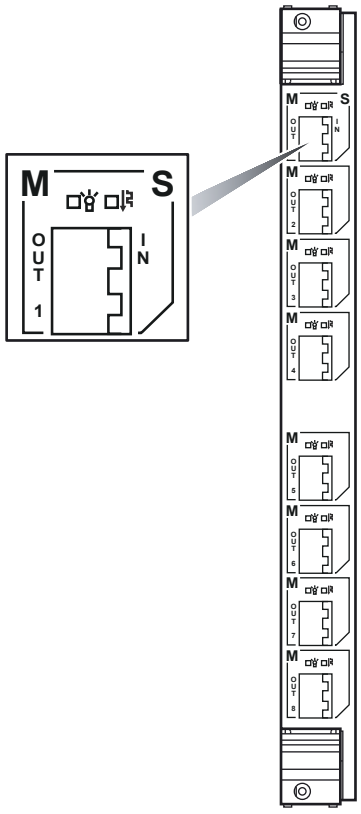


Figure N.31: Master/Slave card

In Master mode, all connectors **M** function as master output (**OUT 1** to **OUT 8**).

In Slave mode, the top connector **S** functions as a slave input (**IN**), all other connectors are unused.

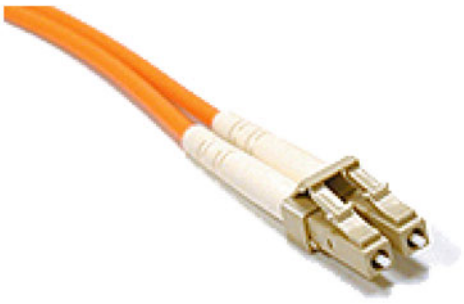


Figure N.32: Example of a duplex LC® connector

LED indicators

On the front panel of the Master/Slave card two LEDs indicate the status of the link.

The icon is used to identify the signal detect function.

The icon is for data/synchronization identification.

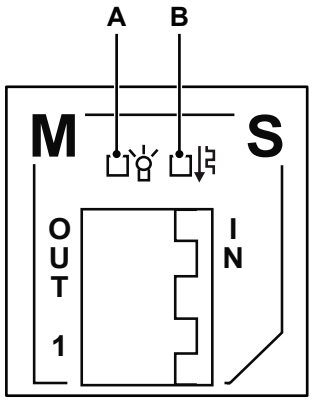


Figure N.33: LED indicators

A icon

B icon

The following table shows the function and possible combinations of the two LEDs.

Table N.6: Master/Slave card front panel LED indicators

FRONT PANEL LED INDICATORS			
Status			**Description**
No Link	off	off	No valid characters detected/ no optical signal detected
Optical signal detection/ initialization	on	off	Alignment characters detected
Receiving data	on	on	Receiving valid data

In the GEN series tower model the Master/Slave card is installed on the left-hand side of the Interface/Controller module.

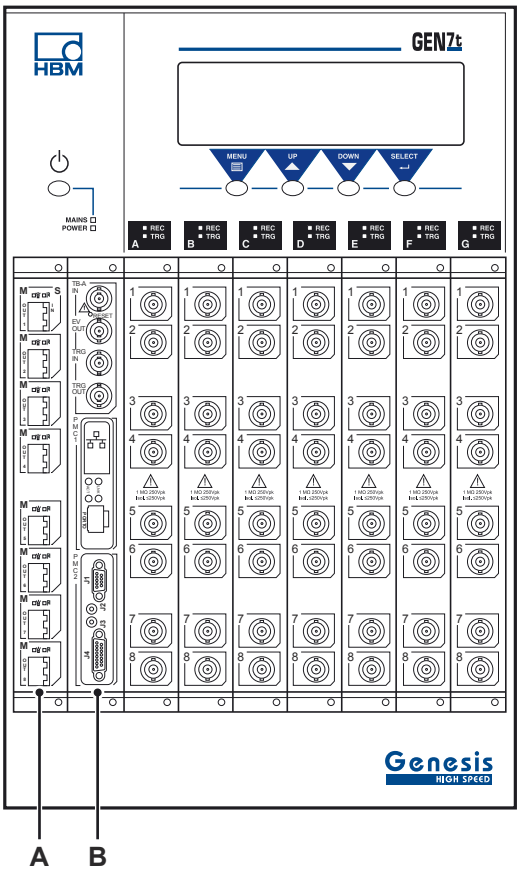


Figure N.34: GEN series tower model with Master/Slave card installed

A Master/Slave card

B Interface/Controller module

In the GEN series 19” rack model the Master/Slave card is installed into Slot **A** on the right-hand side of the Interface/Controller module.

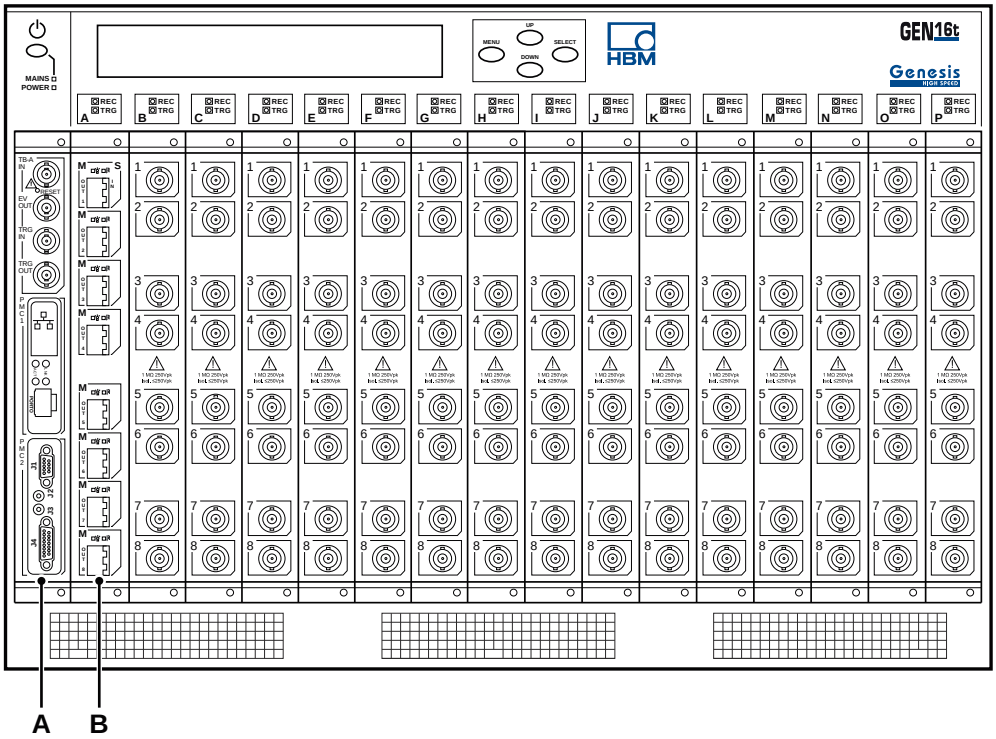


Figure N.35: GEN series 19” rack model with Master/Slave card installed

A Interface/Controller module

B Master/Slave card (Slot A)

Note *With a Master/Slave card installed the GEN series 19” rack model can accommodate up to 15 cards (recorders).*

N.10.2 Installing and removing the Master/Slave card

The Master/Slave card is easily inserted into the GEN series mainframe and is automatically recognized by the Perception software.

The card is removed and installed in the same way as all the acquisition cards.

Note *On the GEN series 19" rack model remove the acquisition card from slot A.*

CAUTION

HBM uses state-of-the-art electronic components in its equipment. These electronic components can be damaged by discharge of static electricity (ESD). Therefore, we must emphasize the importance of ESD preventions when removing or installing cards/modules.

CAUTION

The GEN series Data Acquisition System is factory-calibrated as delivered to the customer. Swapping, replacing or removing of cards/ modules may result in minor deviations to the original calibration. The GEN series system should be tested and if necessary, calibrated, at one-year intervals or after any major event that may affect calibration. When in doubt, consult your local supplier.

LASER SAFETY

CLASS 1 LASER PRODUCT. Avoid exposure to laser radiation. Do not stare into an open aperture, because invisible laser radiation may be emitted from the aperture when a cable is not inserted in the connector port. The system is classified as a Class 1 laser product. The Master/Slave card uses an LC® Optical Tranceiver for communication. It does not emit hazardous light but it is recommended to avoid direct exposure to the beam.

The built-in laser complies with laser product standards set by government agencies for Class 1 laser products:

- In the USA, the Master/Slave card is certified as a Class 1 laser product conforming to the requirements contained in the Department of Health and Human Services (DHHS) regulation CDRH 21 CFR, Chapter I Subchapter J Part 1040.10.
- Outside the USA, the Master/Slave card is certified as a Class 1 laser product conforming to the requirements contained in IEC/EN 60825-1:1994+A1+A2 and IEC/EN 60825-2.

Installing the Master/Slave card

To install the Master/Slave card proceed as follows:

1 Power off the GEN series and remove the power input cable.
2 Ensure that the ejector levers are in the outermost position, tilting away from the card.

3 Slide the card into its guide rails until the ejectors contact the perforated metal strips at top and bottom.

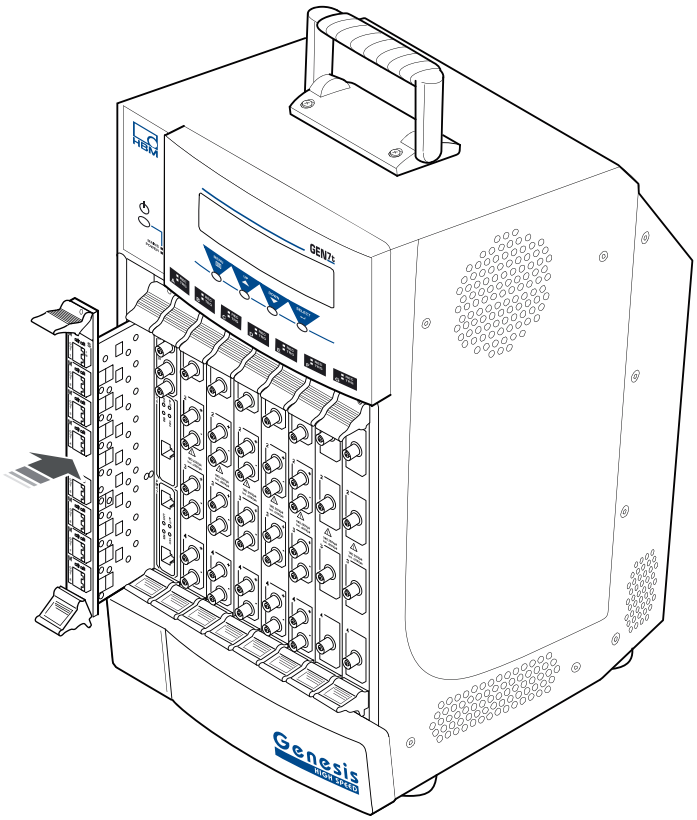


Figure N.36: Slide in the card

4 Press both ejectors inwards to seat the card. They act as levers to gently push the card into its backplane sockets.

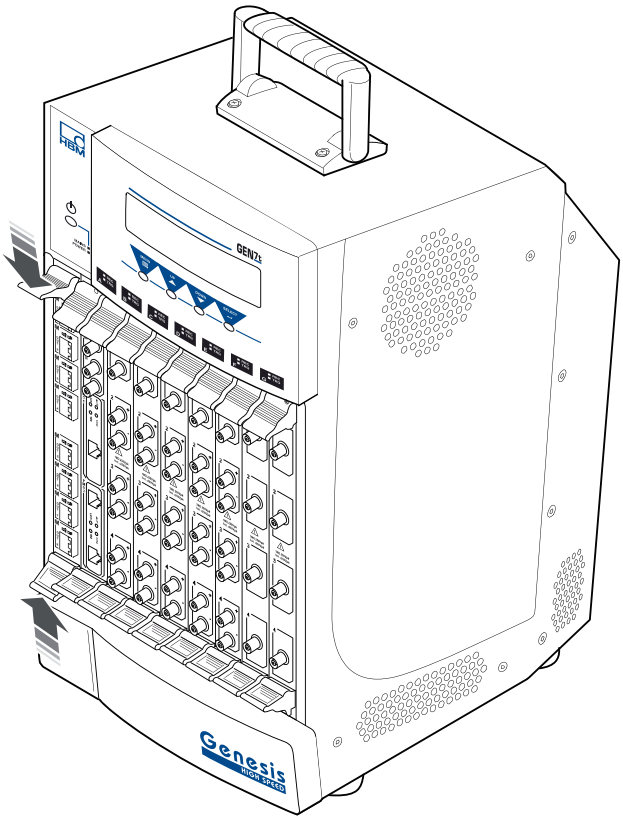


Figure N.37: Press ejectors inwards

5 Fasten the small set screw on both ejectors on the card.

Figure N.38: Ejector set screw

The Master/Slave card is installed.

Removing the Master/Slave card

To remove the Master/Slave card:

1 Power off the GEN series and remove the power input cable.
2 Loosen the small set screw on both ejectors on the card.

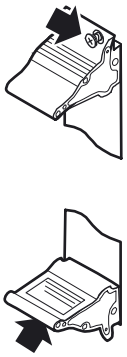


Figure N.39: Ejector set screw

3 Press the inner grey button on each ejector to release the catch.

Figure N.40: Inner grey button on ejector

4 Press both ejectors outwards to release the card. They act as levers to gently pull the card from its backplane sockets.

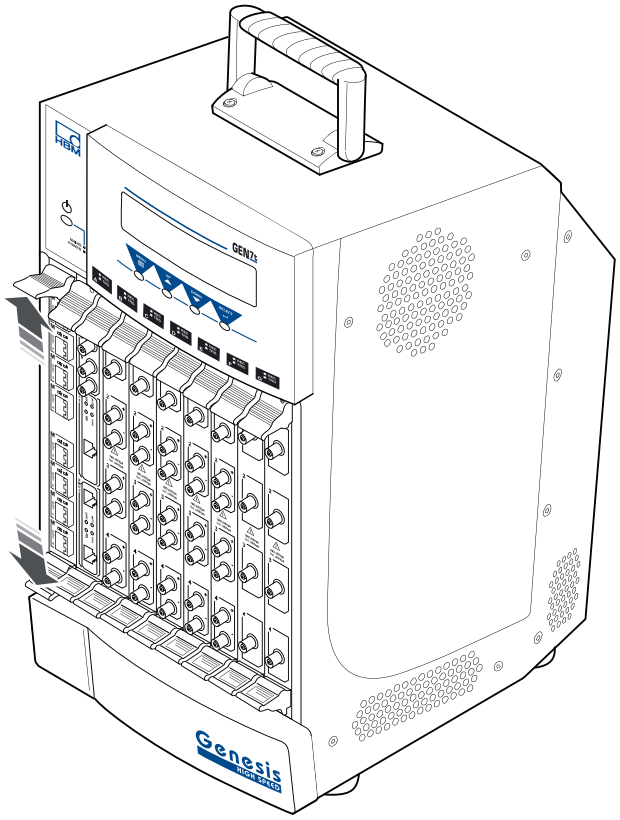


Figure N.41: Press ejectors outwards

5 Slide the card out of the GEN series unit.

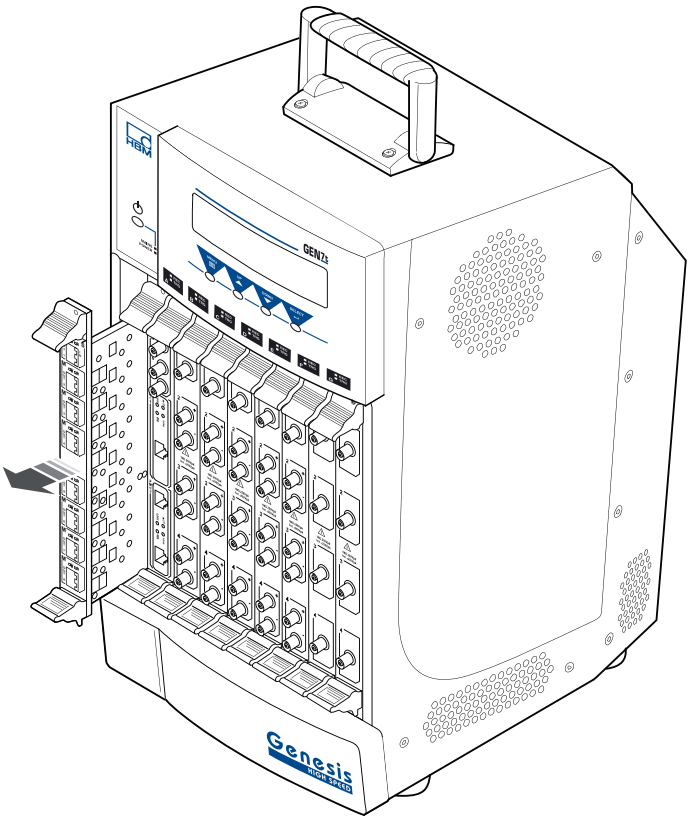


Figure N.42: Remove the card

N.10.3 Connecting the Master/Slave card

With the fiber optic cable, connect the Master/Slave card labelled **M**, **OUT** of the master mainframe to the top connector labelled **M/S IN** of the Master/Slave card of the slave mainframes.

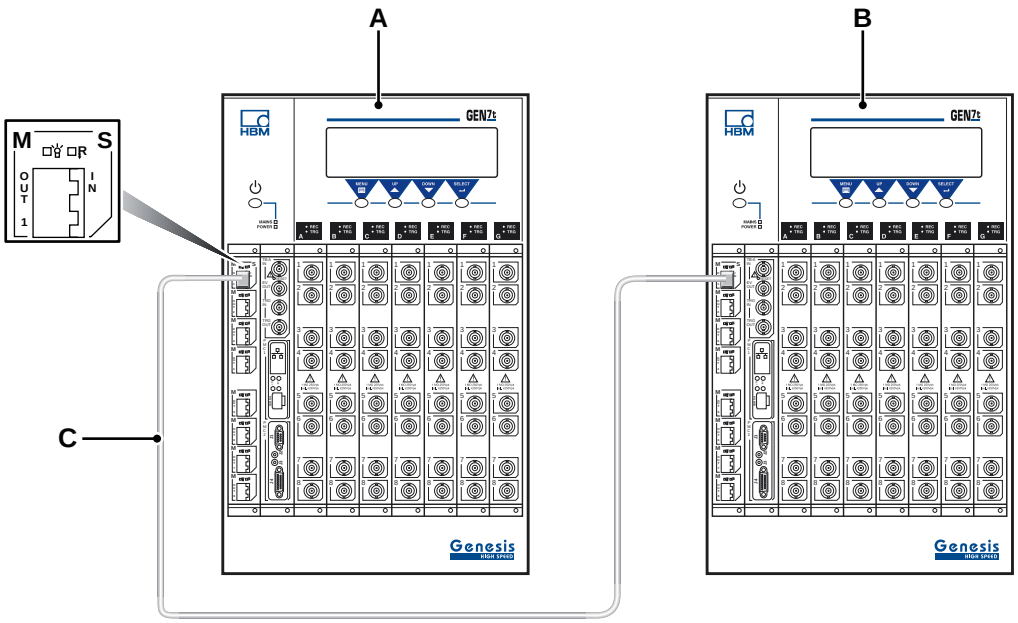


Figure N.43: Connecting the Master/Slave

A Master mainframe (**M**, **OUT**)

B Slave mainframe (**M/S IN**)

C Fiber optic cable

IMPORTANT

Connect the Fiber optic cable of the slave mainframes to the top connector labelled M/S IN of its Master/Slave card.
With a Master/Slave card operating in slave mode only the top connector labelled M/S IN is configured as a slave, all other connectors will not send or receive signals.

N.10.4 Example of a Master/Slave configuration (legacy)

The following diagram shows an example of a Master/Slave configuration with a master driving six slave mainframes.

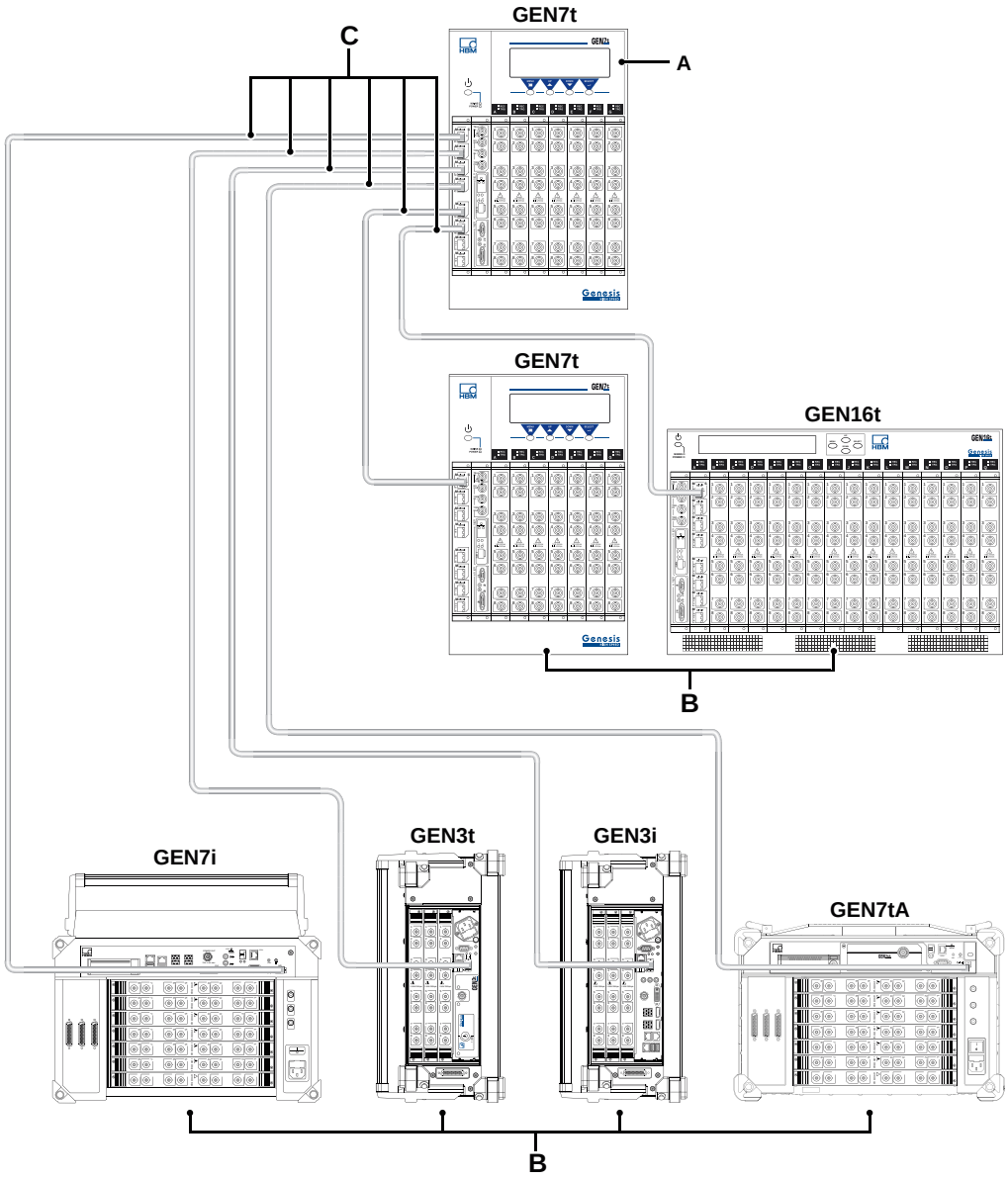


Figure N.44: Master/Slave configuration with six slave mainframes

A Master mainframe

B Slave mainframes

C Fiber optic cable

1 Connect the connector labelled **M/S**, **OUT 1** of the Master mainframe to the top connector labelled **M/S IN** of the first Slave mainframe.

2 Connect the connector labelled **M**, **OUT 2** of the Master mainframe to the top connector labelled **M/S IN** of the second Slave mainframe.

3 Connect the connector labelled **M**, **OUT 3** of the Master mainframe to the Master/Slave synchronization connector of the third Slave mainframe.

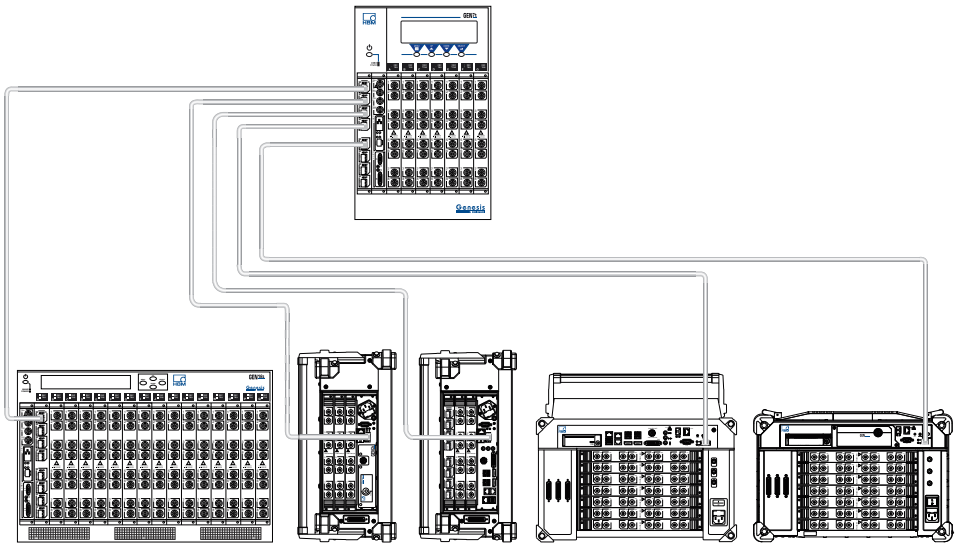
4 Connect the connector labelled **M**, **OUT 4** of the Master mainframe to the Master/Slave synchronization connector of the fourth Slave mainframe.

5 Connect the connector labelled **M**, **OUT 5** of the Master mainframe to the Master/Slave synchronization connector of the fifth Slave mainframe.

6 Connect the connector labelled **M**, **OUT 6** of the Master mainframe to the Master/Slave synchronization connector of the sixth Slave mainframe.

N.10.5 Using legacy and new mainframes in Master/Slave setup

Connect to a group of nine mainframes as Slave. At least one mainframe in this group must use the Master/Slave card option. This mainframe must be Master, as Master/Slave is always a STAR topology. The synchronization works in basic synchronization mode.



N.10.6 Connecting multiple mainframes using the Master/Slave card (legacy)

At the time of this manual's release, the only option to connect between three and nine mainframes together is to use the Master/Slave card option.

IMPORTANT

The optional Master/Slave card is not supported in the GEN3i, GEN3iA, GEN3t, GEN7i, GEN7tA or GEN17tA. Therefore, this setup requires a GEN7t, GEN16t, GEN5i or GEN2i with a Master/Slave card installed as a Master unit.

In this setup, one of the mainframes with a Master/Slave card must be set to Master while the other mainframes must all be set to Slave. This setup automatically uses basic synchronization.

The multiple mainframe Master/Slave setup only works in a star configuration. All Master/Slave fiber optic cables are on one side connected to the Master mainframe while the other side connects to one of the Slave mainframes.

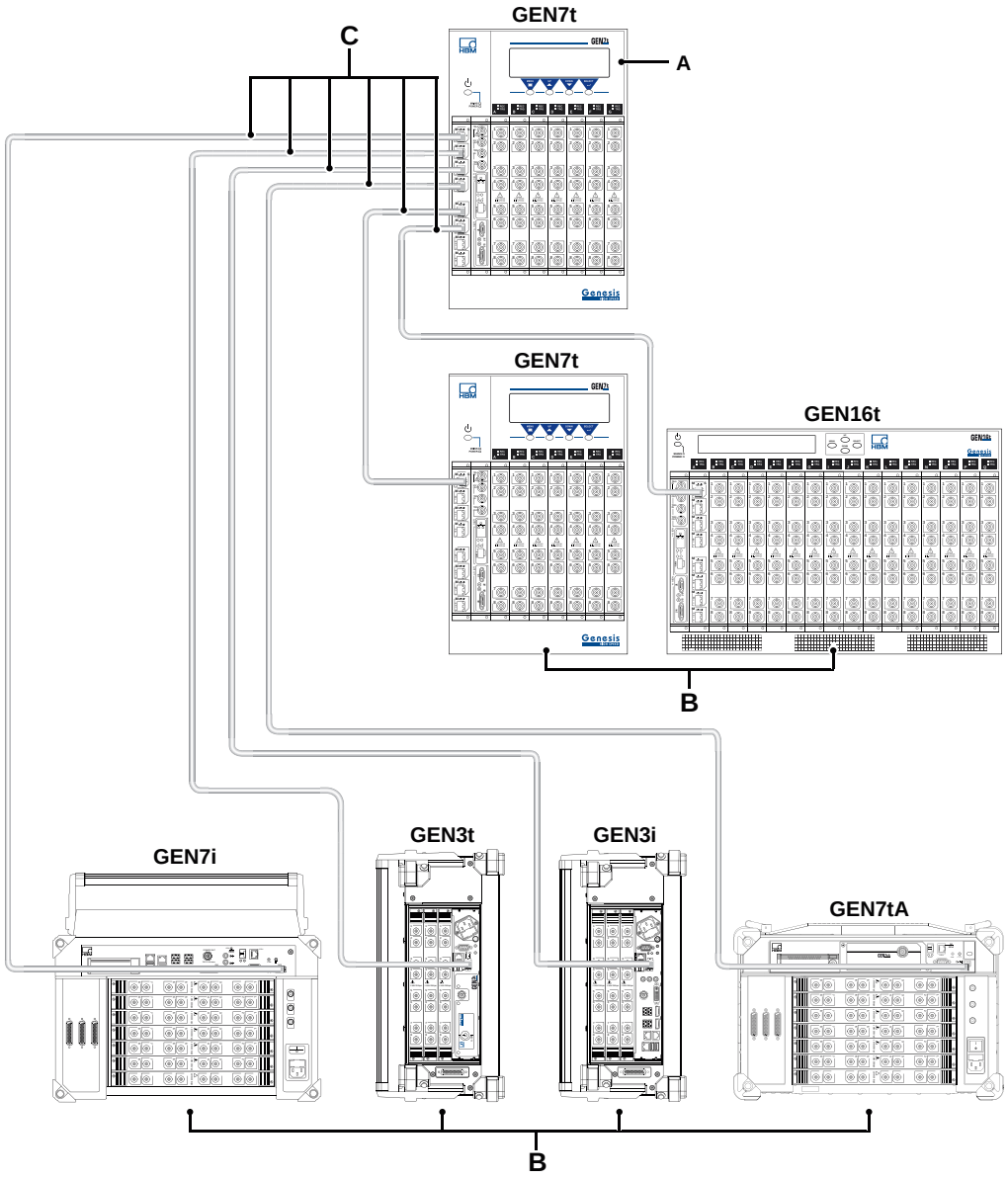


Figure N.45: Master/Slave configuration with six slave mainframes

A Master mainframe

B Slave mainframes

C Fiber optic cable

1. Connect the connector labelled **M/S**, **OUT 1** of the Master mainframe to the top connector labelled **M/S IN** of the first Slave mainframe.
2. Connect the connector labelled **M**, **OUT 2** of the Master mainframe to the top connector labelled **M/S IN** of the second Slave mainframe.

3 Connect the connector labelled **M**, **OUT 3** of the Master mainframe to the Master/Slave synchronization connector of the third Slave mainframe.

4 Connect the connector labelled **M**, **OUT 4** of the Master mainframe to the Master/Slave synchronization connector of the fourth Slave mainframe.

5 Connect the connector labelled **M**, **OUT 5** of the Master mainframe to the Master/Slave synchronization connector of the fifth Slave mainframe.

6 Connect the connector labelled **M**, **OUT 6** of the Master mainframe to the Master/Slave synchronization connector of the sixth Slave mainframe.

N.11 5B Integration card

The Genesis data acquisition system offers a variety of standard input cards to cover the most important physical application requirements. In situations where non-standard or specific requirements are needed, for example LVDT or PT100 signals that need to be conditioned and acquired, the 5B Integration card is used.

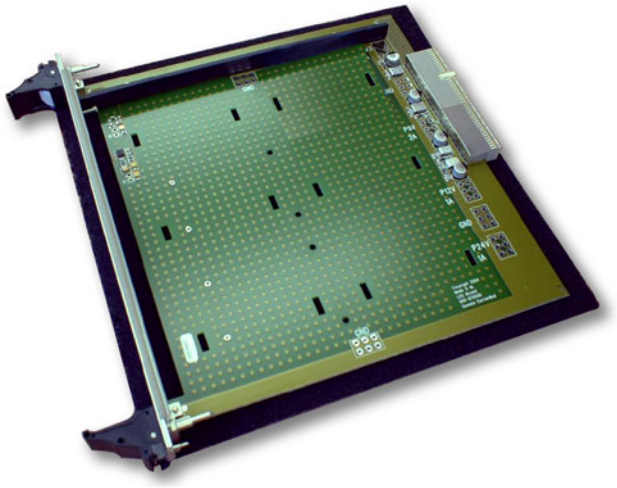


Figure N.46: 5B Integration card

The 5B Integration card can be customized for these kinds of specific requirements using 5B modules that are available from separate vendors and can be directly fixed to the 5B Integration card.

A 5B module

A 5B module offers a small footprint, defined input and output connections, isolation, and good price/performance. A 5B module is a single channel fixed-range amplifier. These modules are the standard for fixed application signal conditioning in the lab and the factory floor.

Figure N.47: 5B module

There are several hundred different types of 5B modules available for nearly each and every physical signal.

5B modules are available for signals like:

- Isolated AC and DC
- True RMS
- Current
- Strain gauge
- Carrier
- All kinds of TCs
- RTDs with 2, 3 or 4 wires
- LVDTs
- f to V converters
- RPM to V converters
- Potentiometers
- 4-20 mA transmitters

Using the 5B Integration card with Genesis series

The 5B Integration card is designed to work seamlessly with the GEN series mainframes. Up to six 5B preamplifier modules can be attached to a card that supplies a range of fused supply voltages to the modules and that has enough front panel space to mount the required input and output connectors.

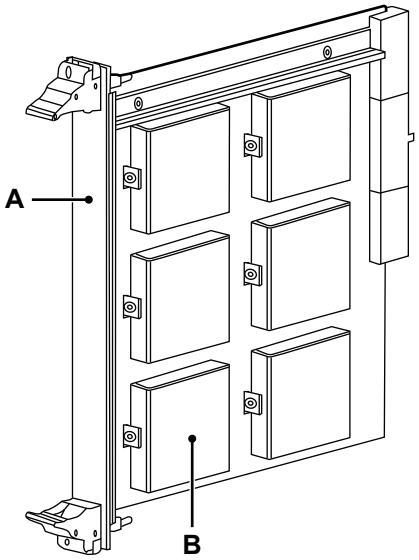


Figure N.48: 5B Integration card design

A The front panel input and output connections and the internal wiring have to be done in accordance with the customer's requirements.

B Up to six 5B modules can be mounted on the 5B Integration card.

After signal conditioning, the signal is then fed into a standard input channel of any Genesis input card using the 5B module.

Customization and ordering

First, check whether there are 5B modules that do the job with respect to their fixed input range and the other limitations available. The output range is very often suitable because the Genesis input cards used with the 5Bs offer a 16 bit resolution. Therefore, the modules normally have a resolution high enough for any range required. Then, select the proper module and define the input connectors needed for the sensor used.

From there, the special card can be “customized” on site by the local service department or through an outside vendor.

The 5B Integration card can be ordered from HBM and the 5B modules from any of the 5B vendors. The designer needs to take care of the cabling, connectors and the specific documentation.

What is included?

When ordering the 5B Integration card, the following components are included:

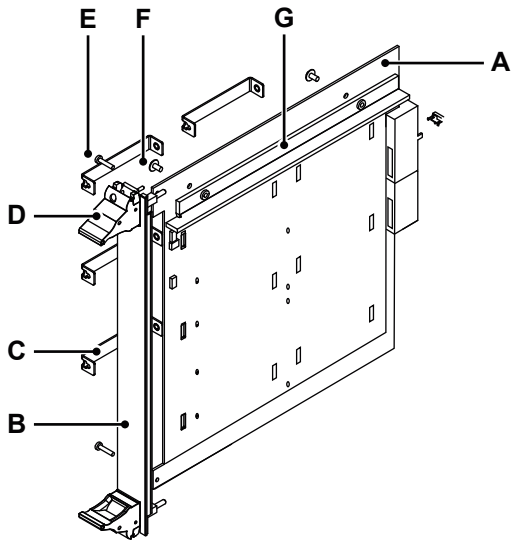


Figure N.49: 5B Integration card components

A Genesis 5B Integration card 1x

B Execution/Genesis blind single with handle 1x

C Bracket/Genesis 5B carrier clamp 6x

D PAN/Genesis blind single with handle 1x

E Screw M2.5x0.45 12Torx 2x

F Screw M3x0.5 6ST 2x

G BRKT/Genesis carrier airflow 1x

How to use the 5B based amplifier with Genesis and Perception
As an example of a working 5B Integration card, we will consider a card with two 5B modules mounted, one being an f to V converter and one being a TC module. These two modules have fixed ranges like 0-10.000 Hz and -200 °C to +600 °C, each module has a 0-5 V output.

Connect the output (preferable BNCs mounted on the 5B Integration card front panel) to two selected Genesis input channels now acting as the “Frequency” and “TC” channels. Set sensitivity to 0-5 Volt (or whatever the 5B modules that are used deliver as Full Scale value) in these channels.
Scale the inputs to 0-10,000 Hz and -200 °C to +600 °C using the TU (technical units) input fields for those channels in Perception.
In order to do this, either calculate the TU multiplier value, or just do a two-point calibration and enter the upper and lower values there.
Save this setup as a hardware setting and start any future measurements from there.

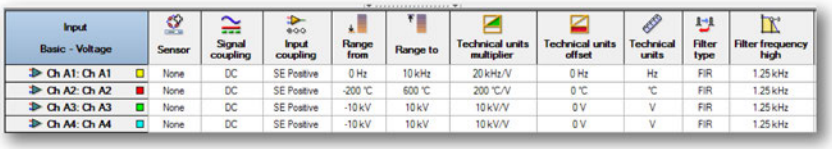
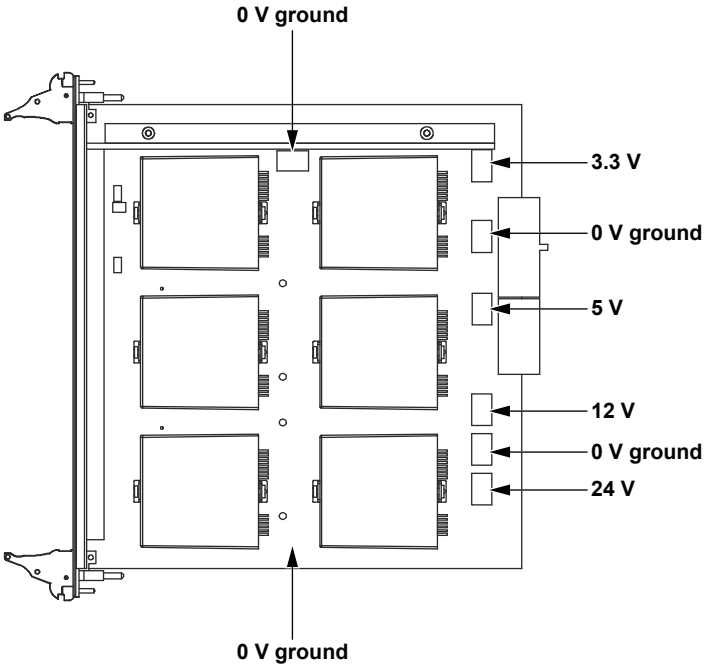


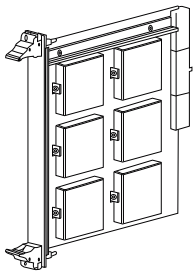
Figure N.50: 5B Integration card setup

CH 1A and CH 2A are scaled to measure frequency and temperature using 5B modules in front of standard input channels.

5B Integration card specifications

General Specifications	
	
5B mounting positions	6 (mounting materials included)
Voltage rails	
3.3 V	Fused @ 2 A with soldering tabs
5 V	Fused @ 2 A with soldering tabs
12 V	Fused @ 1 A with soldering tabs
24 V	Fused @ 1 A with soldering tabs

Note *The card alone does not serve any function and must be combined with 5B series signal conditioners. Proper connectors have to be mounted, internal card wiring (input/ output/power) has to be implemented and additional Genesis input channels have to be used to receive the 5B series output signal. HBM's Basic input cards series (GN810, GN811, GN815 or GN816) are most suited for this task.*
For further help or information on the construction of this card, please contact HBM's project group.

Ordering information		
Article	**Description**	**Order No.**
5B Integration card 	GEN DAQ 5B Integration card - Uses one GEN DAQ slot, holds up to six 5B modules. **Note** *5B modules, I/O Connectors and cabling not included. Basic card required for acquisition.*	1-G028-2

O Legacy Information - Specifications

O.1 B2632-3.1 en (GEN series GN810)

Capabilities Overview	
Model	GN810
Maximum sample rate per channel	200 kS/s
Memory per card	128 MB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16 bit
Isolation	Not supported
Input type	Analog, single-ended
Passive voltage/current probes	Passive, single-ended voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	Not supported
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	Not supported
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

Block Diagram

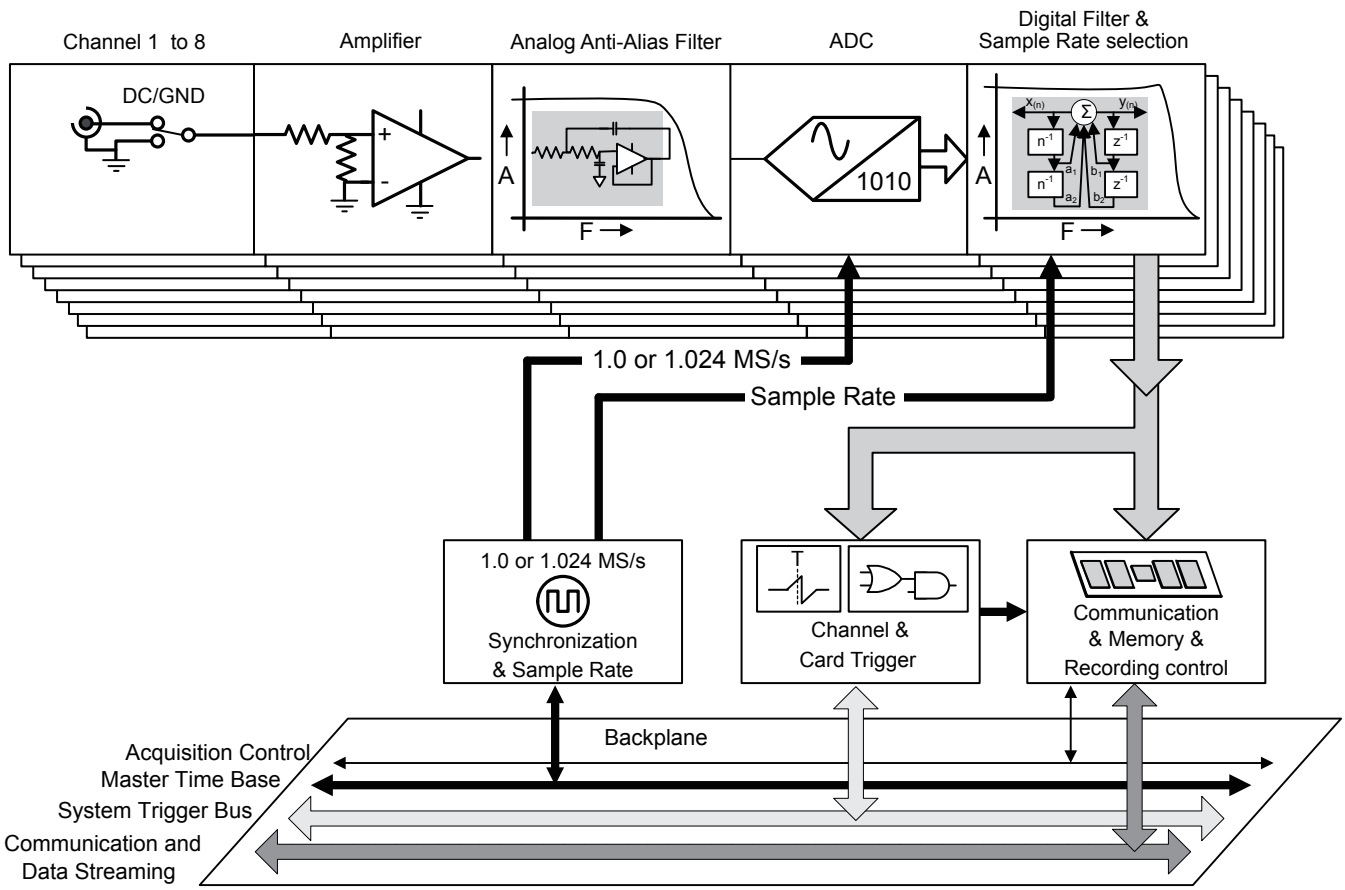


Figure O.1: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	8
Connectors	Metal BNC, 1 per channel
Input type	Analog single-ended
Input coupling	DC, GND
Impedance	1 MΩ ± 1% // 65 pF ± 10%
Ranges	± 1 V, ± 2 V, ± 5.0 V, ± 10 V, ± 20 V, ± 50 V Each fixed range supports a variable gain with 1000 steps (0.1%). Variable gain creates 1000 extra ranges between two fixed ranges.
Offset	± 50% in 1000 steps (0.1%); ± 50 V range has fixed 0% offset
DC Offset error	
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Offset error drift	± 100 ppm/°C (± 180 ppm/°F)
DC Gain error	
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Gain error drift	± 70 ppm/°C (± 130 ppm/°F)
Maximum static error (MSE)	
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
RMS Noise	
Bessel IIR and FIR	0.02% of Full Scale ± 10 µV
Input overload protection	
Maximum voltage	± 250 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 1 µs after 200% overload

Analog to Digital Conversion	
Sample rate per channel	0.1 S/s to 200 kS/s
ADC resolution; one ADC per channel	16 bit
ADC Type	Successive Approximation Register (SAR); TI ADS8401IB
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; when calculating FFTs results in rounded/integer BIN sizes
Maximum binary sample rate	204.8 kS/s
External time base sample rate	0 S/s to 200 kS/s
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ± 30 ppm

Anti-Alias Filters

Using different filter selections (Bessel IIR/FIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

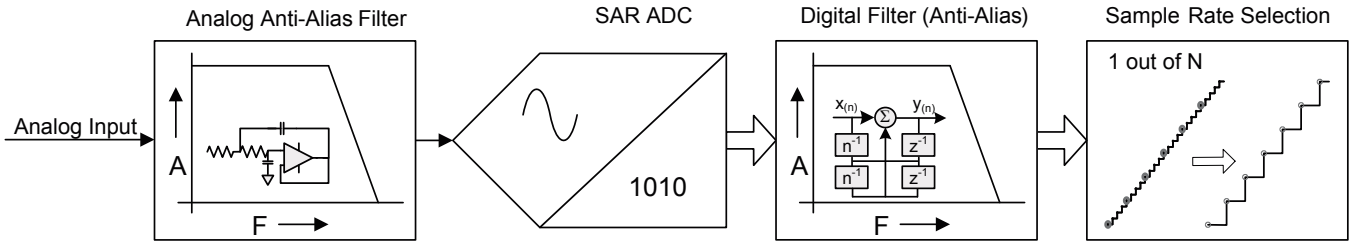
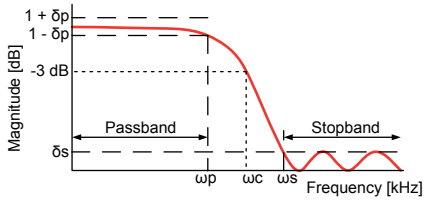


Figure O.2: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Digital Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Digital FIR (Fc @ -0.1 dB)	Standard FIR filter with corner frequency (Fc) defined at -0.1 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Digital FIR (Fc @ -3 dB) Supported by Perception V6.40 and higher	Adapted FIR filter with corner frequency (Fc) calculated as close as possible to -3 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Bessel IIR Filter (Digital Anti-Alias)



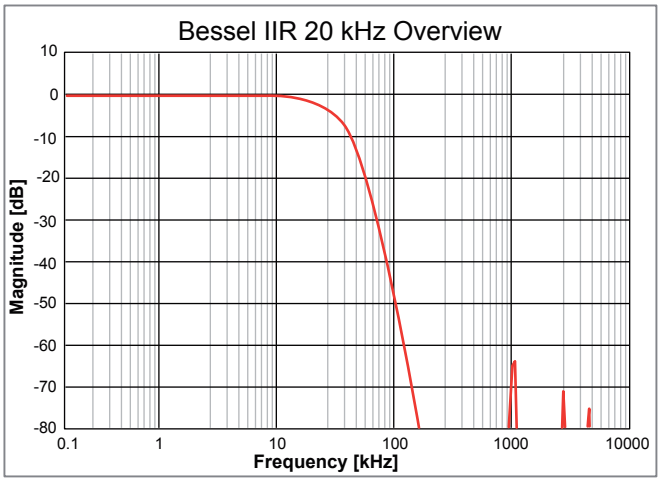
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.3: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-aliasing filter bandwidth	220 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	6-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed
Bessel IIR filter bandwidth (ωc)	Auto tracking the sample rate with the selected Bessel IIR filter; user selection from 0.0125 Hz to 20 kHz
Bessel IIR passband flatness (ωp)(1)	0.1 dB; DC to 3 kHz @ ωc = 20 kHz
Bessel IIR filter stopband attenuation (δs)	60 dB
Bessel IIR filter roll-off	36 dB/Octave



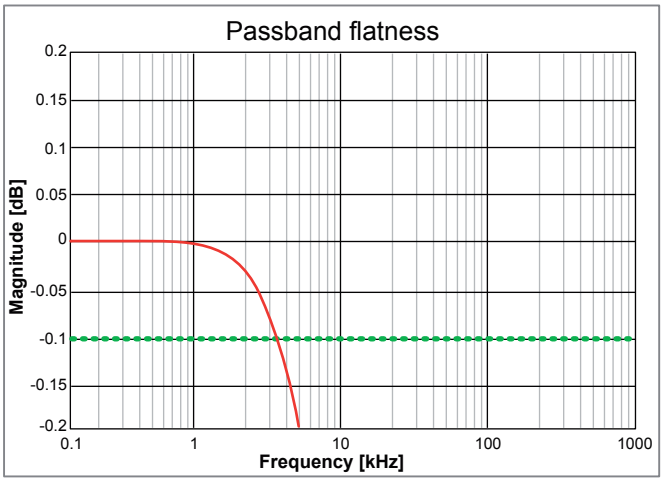
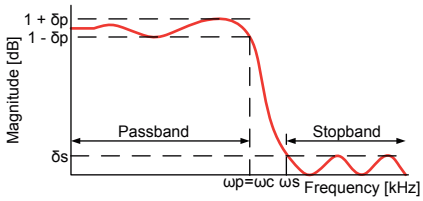


Figure O.4: Representative Bessel IIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -0.1 dB) Filter (Digital Anti-Alias)



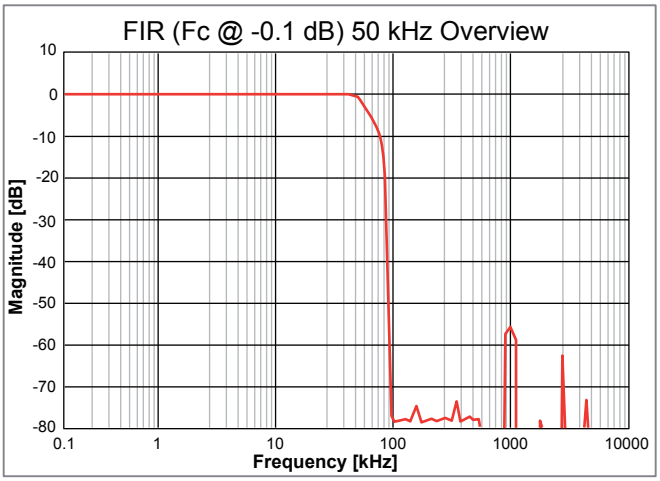
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.5: Digital FIR (Fc @ -0.1 dB) filter

When FIR (Fc @ -0.1 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -0.1 dB) filter.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -0.1 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -0.1 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40
FIR (Fc @ -0.1 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -0.1 dB) filter; user selection from 0.031 Hz to 50 kHz
FIR (Fc @ -0.1 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to filter bandwidth (ωc)
FIR (Fc @ -0.1 dB) filter stopband attenuation (δs)	60 dB
FIR (Fc @ -0.1 dB) filter roll-off	72 dB/Octave



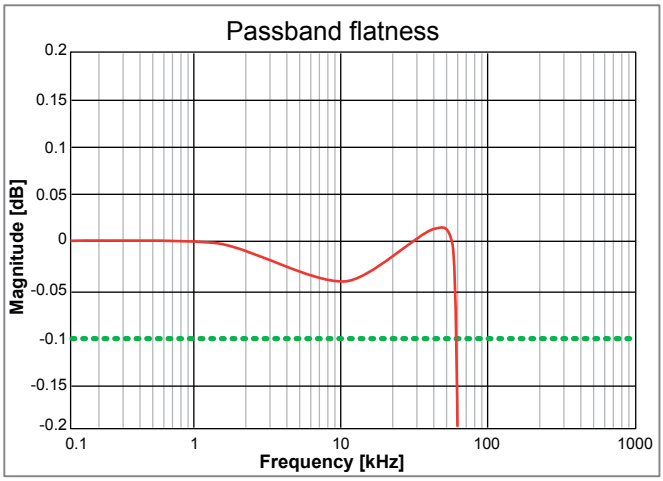
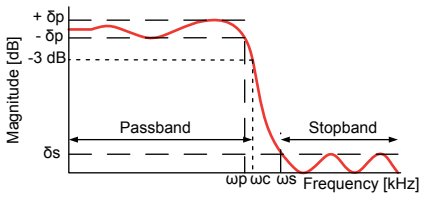


Figure O.6: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -3 dB) Filter (Digital Anti-Alias)



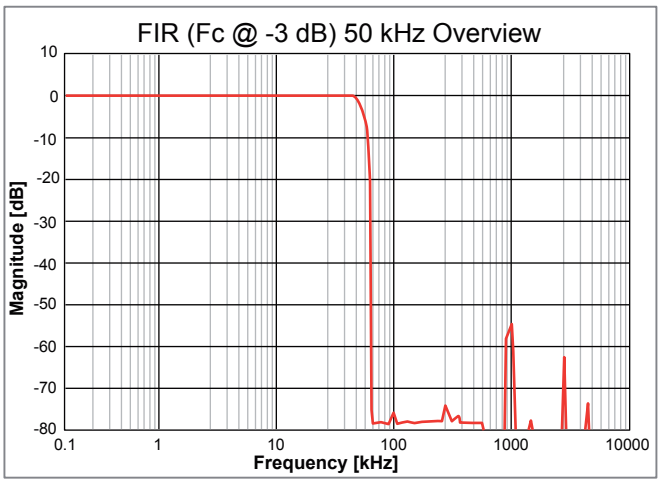
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.7: Digital FIR (Fc @ -3 dB) filter

When FIR (Fc @ -3 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -3 dB) filter. The FIR (Fc @ -3 dB) is an adapted FIR filter. Its ωp is reduced by a factor of ≈1.4 compared to the FIR (Fc @ -0.1 dB) filter. It is supported by Perception V6.40 and higher.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -3 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -3 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40
FIR (Fc @ -3 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -3 dB) filter; user selection from 0.031 Hz to 50 kHz
FIR (Fc @ -3 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to ≈ωc/1.4 (Adapted FIR filter behavior)
FIR (Fc @ -3 dB) filter stopband attenuation (δs)	60 dB
FIR (Fc @ -3 dB) filter roll-off	72 dB/Octave



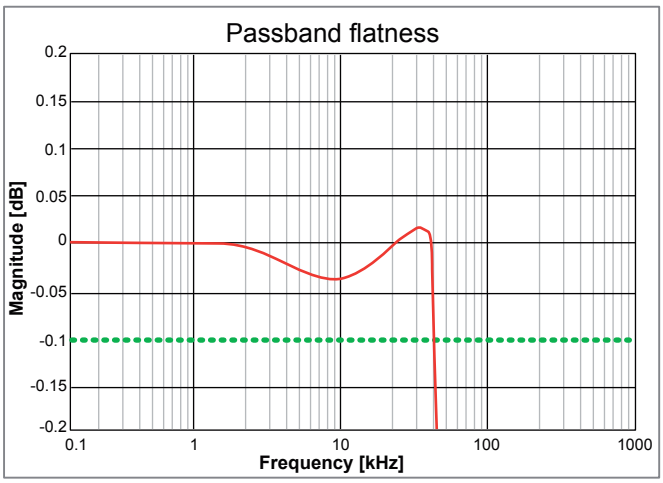


Figure O.8: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Bessel IIR/FIR/etc.) or different filter bandwidths results in phase mismatches between channels.	
Bessel IIR (Fc @ -3 dB), 20 kHz Filter frequency; 10 kHz sine wave	
Channels on card	0.4 deg (0.1 µs)
GN810 Channels within mainframe	0.4 deg (0.1 µs)
FIR (Fc@ -0.1dB) and FIR (Fc @ -3 dB), 50 kHz Filter frequency; 10 kHz sine wave	
Channels on card	0.4 deg (0.1 µs)
GN810 Channels within mainframe	0.4 deg (0.1 µs)
GN810 Channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	128 MB (64 MS)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	16 bits, 2 bytes/sample

Digital Events/Timer/Counter	
Digital event inputs	Not supported
Digital event outputs	Not supported
Timer/Counter	Not supported

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Active edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Delay	± 1 µs + maximum 1 sample period (for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Active level	High/Low/Hold High; selectable per mainframe, identical for all cards
Pulse width	High/Low: 12.8 µs Hold high: Active from first mainframe trigger to end of recording Pulse width created by mainframe
Delay	516 µs ± 1 µs + maximum 1 sample period using decimal time base 504 µs ± 1 µs + maximum 1 sample period using binary time base
Cross channel triggering	
Channels on card	Logical OR; Analog triggers of all channels Logical AND; Qualifiers of all channels
Cards in mainframe	User selectable through system trigger bus Selections: Send/Receive/Transceive (Send & Receive)
System trigger bus	
Connections	3 System trigger busses connecting all cards within mainframe 1 Master/Slave bus connecting all cards within mainframe and connecting all mainframes when using Master/Slave option
Operation	Logical OR of all triggers of all cards Logical AND of all qualifiers of all cards
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; Single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Pulse detect/reject	Disable/Detect/Reject software selectable. Maximum pulse width 65 535 samples
dY/dT conversion	dY: 16 bit (0.0015%) for both levels dT: 1 to 1023 samples. dT setting shared for both levels
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; Two individual levels, OR-ed
Window	Arm/trigger and a disarm level; Trigger on peak level changes in a uni-polar signal
Dual Window	Arm/trigger/disarm per level; Trigger on peak level changes in a bi-polar signal
Sequential	One arm and one trigger level; eliminate false triggering due to noise or hysteresis
Analog channel qualifier modes	
Basic	Above or below level check. Enable/disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/disable trigger with dual level
Trigger hold off	Disable channel trigger for 1 to 65 535 samples after trigger detected Maximum hold off time depends on sample rate

Triggering	
Interval timer	
Modes	Less than, trigger when rate is too low More than, trigger when rate is too high Between, trigger when rate between lower and upper limit Not between, trigger when rate is not between lower and upper limit
Interval timers	Start timer and width Timer
Timer value	1 to 65 535 samples
Event counter	Counts channel trigger events before card trigger is activated 1 to 256 trigger events

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

	Single Sweep Multiple Sweeps Slow-Fast Sweep			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch
Max. sweep memory	60 MS	30 MS	7.5 MS	not used			48 MS	24 MS	6 MS
Max. sweep sample rate	200 kS/s			not used			200 kS/s		
Max. continuous FIFO	not used			60 MS	30 MS	7.5 MS	12 MS	6 MS	1.5 MS
Max. continuous sample rate	not used			200 kS/s			Sweep sample rate / 2 Maximum 50 kS/s		
Max. aggregate continuous streaming rate	not used			0.2 MS/s 0.4 MB/s	0.4 MS/s 0.8 MB/s	1.6 MS/s 3.2 MB/s	0.05 MS/s 0.1 MB/s	0.1 MS/s 0.2 MB/s	0.8 MS/s 1.6 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two or 50 kS/s per channel, whichever is the smallest sample rate
Maximum sample rate switches	400 sample rate switches per second, 200 000 switches maximum, switching stops when sweep ends

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives	
Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

O.2 B2640-3.1 en (GEN series GN811)

Capabilities Overview	
Model	GN811
Maximum sample rate per channel	1 MS/s
Memory per card	256 MB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16 bit
Isolation	Not supported
Input type	Analog, single-ended
Passive voltage/current probes	Passive, single-ended voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	Not supported
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	Not supported
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

Block Diagram

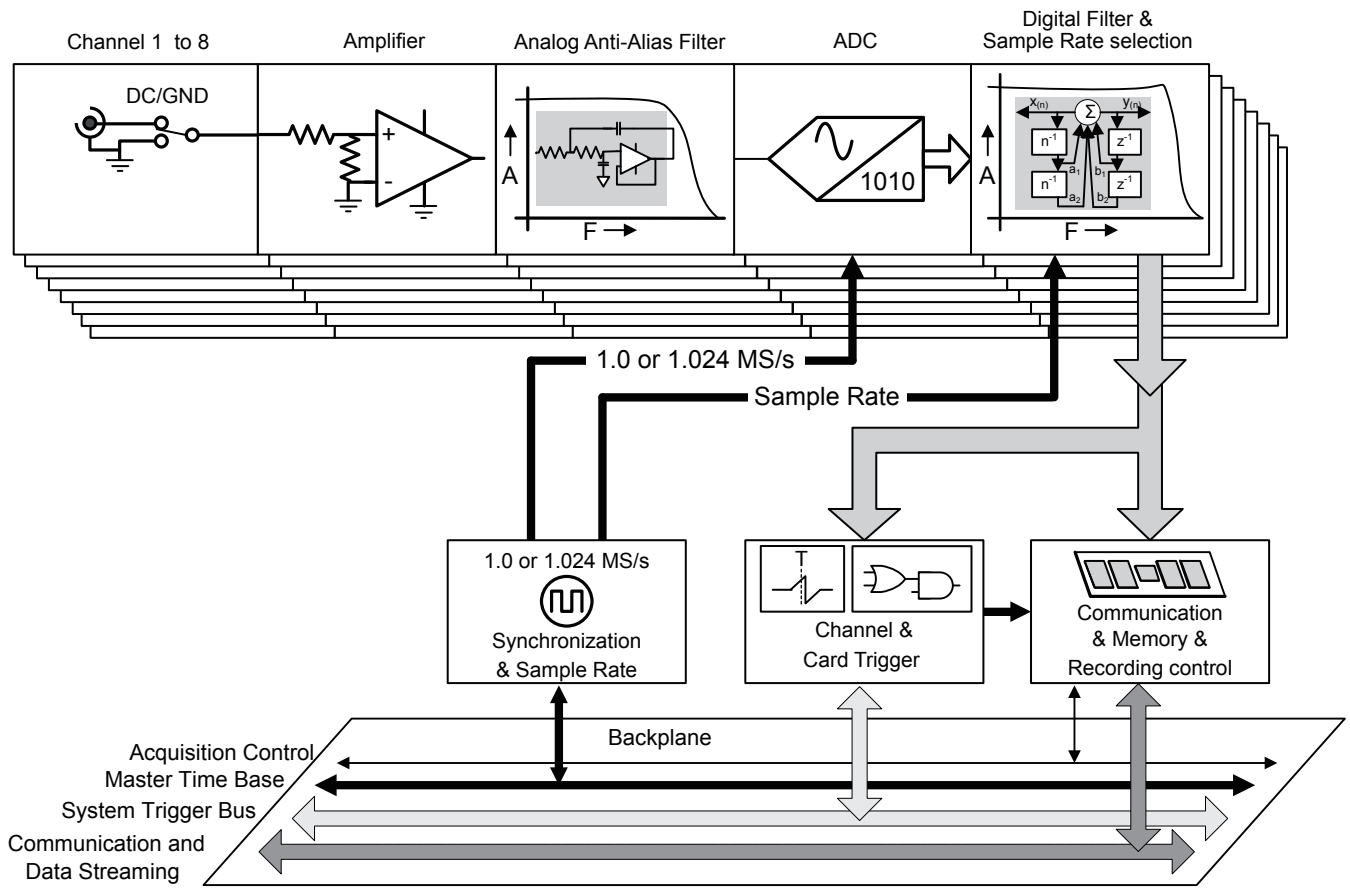


Figure O.9: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	8
Connectors	Metal BNC, 1 per channel
Input type	Analog single-ended
Input coupling	DC, GND
Impedance	1 MΩ ± 1% // 65 pF ± 10%
Ranges	± 1 V, ± 2 V, ± 5.0 V, ± 10 V, ± 20 V, ± 50 V Each fixed range supports a variable gain with 1000 steps (0.1%). Variable gain creates 1000 extra ranges between two fixed ranges.
Offset	± 50% in 1000 steps (0.1%); ± 50 V range has fixed 0% offset
DC Offset error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Offset error drift	± 100 ppm/°C (± 180 ppm/°F)
DC Gain error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Gain error drift	± 70 ppm/°C (± 130 ppm/°F)
Maximum static error (MSE)	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
RMS Noise	
Wideband	0.02% of Full Scale ± 10 µV
Bessel IIR and FIR	0.02% of Full Scale ± 10 µV
Input overload protection	
Maximum voltage	± 250 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 1 µs after 200% overload

Analog to Digital Conversion	
Sample rate per channel	0.1 S/s to 1 MS/s
ADC resolution; one ADC per channel	16 bit
ADC Type	Successive Approximation Register (SAR); TI ADS8401IB
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; when calculating FFTs results in rounded/integer BIN sizes
Maximum binary sample rate	1.024 MS/s
External time base sample rate	0 S/s to 500 kS/s
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ± 30 ppm

Anti-Alias Filters

Using different filter selections (Wideband/Bessel IIR/FIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

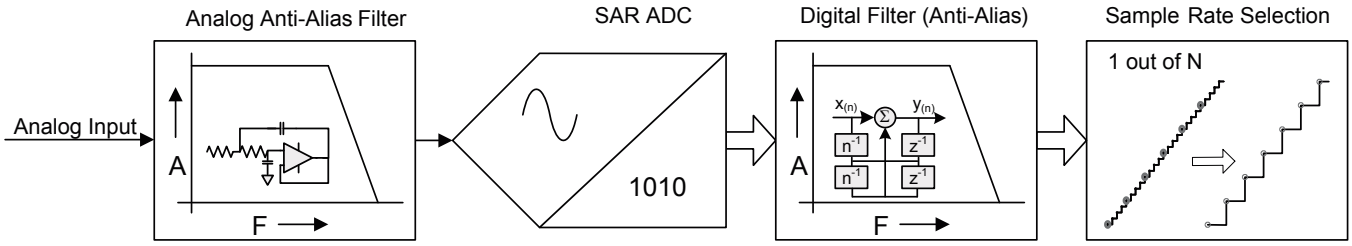


Figure O.10: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Should not be used if working in a frequency domain with recorded data.
Digital Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. Best used for measuring transient signals or sharp edge signals like square waves or step responses.
Digital FIR (Fc @ -0.1 dB)	Standard FIR filter with corner frequency (Fc) defined at -0.1 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Digital FIR (Fc @ -3 dB) Supported by Perception V6.40 and higher	Adapted FIR filter with corner frequency (Fc) calculated as close as possible to -3 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	Between 540 kHz and 690 kHz (-3 dB)
Passband flatness (1)	0.1 dB; DC to 150 kHz

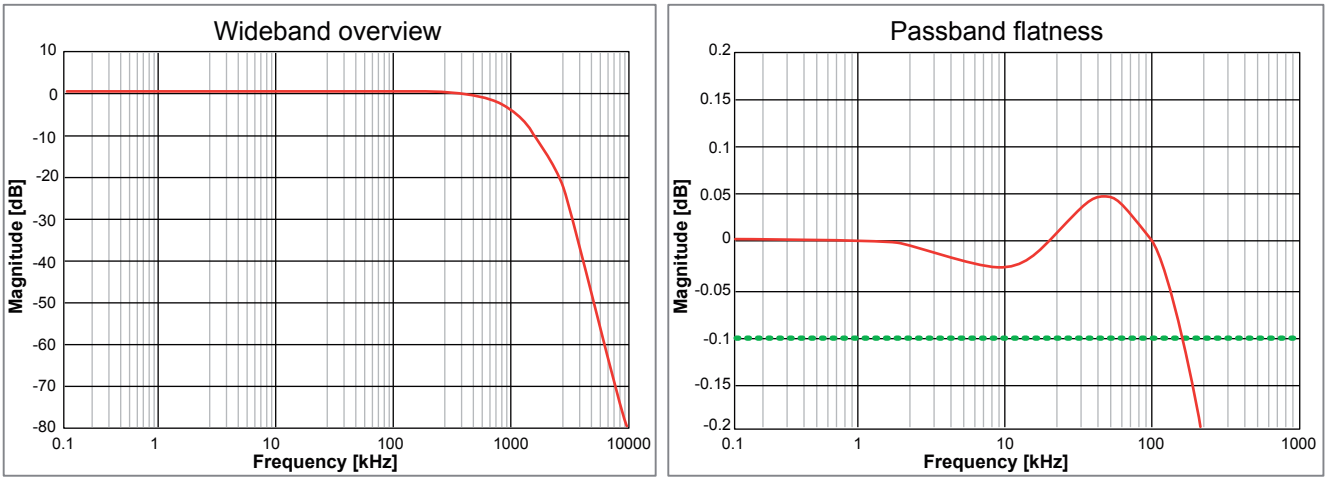
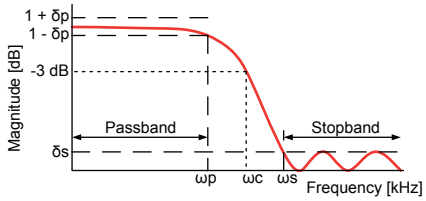


Figure O.11: Representative Wideband examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



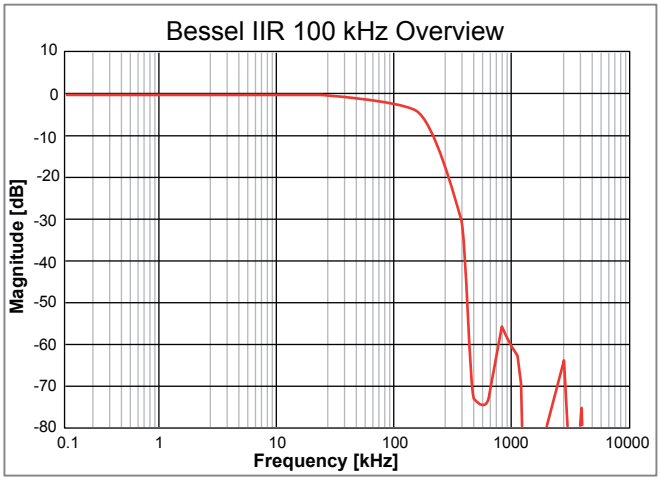
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.12: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-aliasing filter bandwidth	220 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	6-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	Auto tracking the sample rate with the selected Bessel IIR filter; user selection from 0.0125 Hz to 100 kHz
Bessel IIR passband flatness (ωp)(1)	0.1 dB; DC to 20 kHz @ ωc = 100 kHz
Bessel IIR filter stopband attenuation (δs)	60 dB With the Bessel IIR filter bandwidth selection of ωc = 100 kHz, a peak of -55 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
Bessel IIR filter roll-off	36 dB/Octave



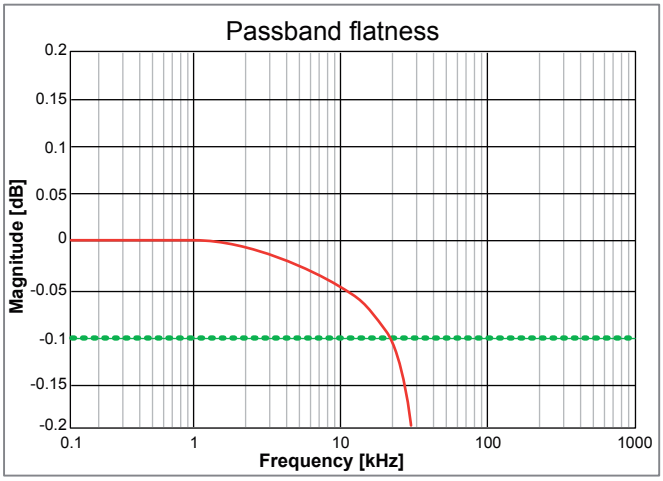
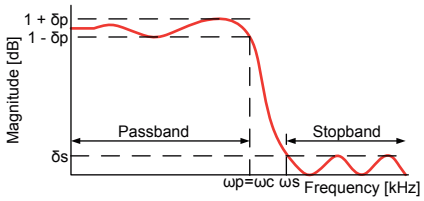


Figure O.13: Representative Bessel IIR examples

(1) Measured using Fluke 5700 calibrator, DC normalized

FIR (Fc @ -0.1 dB) Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.14: Digital FIR (Fc @ -0.1 dB) filter

When FIR (Fc @ -0.1 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -0.1 dB) filter.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -0.1 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -0.1 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 Divided by 40 not available for 1 MS/s & 500 kS/s sample rate The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
FIR (Fc @ -0.1 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -0.1 dB) filter; user selection from 0.031 Hz to 250 kHz
FIR (Fc @ -0.1 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to filter bandwidth (ωc) 0.1 dB; DC to 125 kHz; FIR (Fc @ -0.1 dB) filter bandwidth selection of ωc = 250 kHz, limited by the 370 kHz analog anti-alias filter amplitude response. All other bandwidth selections are not affected.
FIR (Fc @ -0.1 dB) filter stopband attenuation (δs)	60 dB With the FIR (Fc @ -0.1 dB) filter bandwidth selection of ωc = 250 kHz, a peak of -35 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
FIR (Fc @ -0.1 dB) filter roll-off	72 dB/Octave

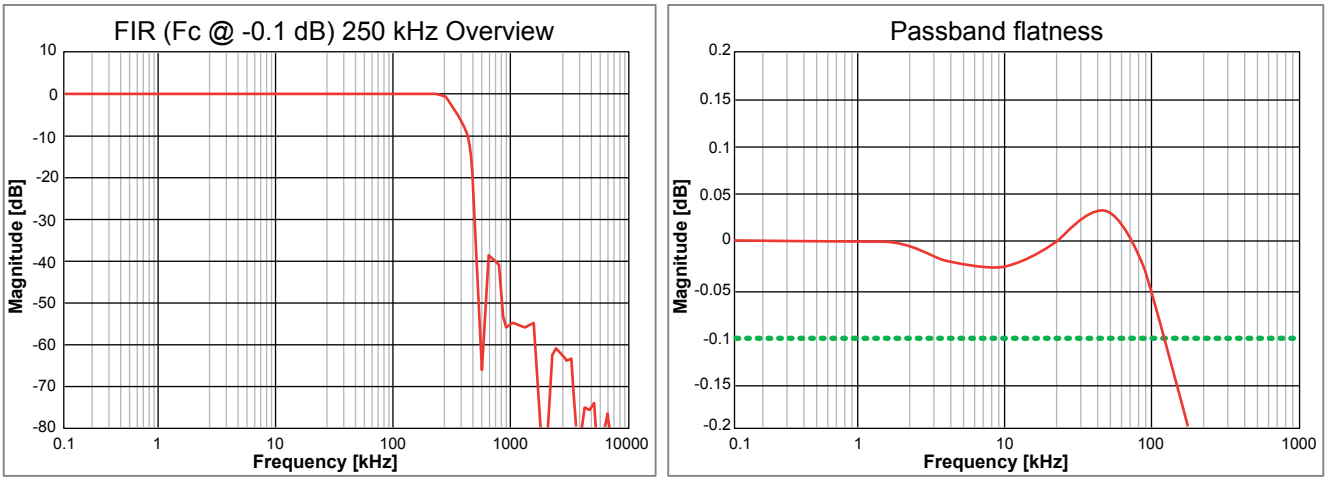
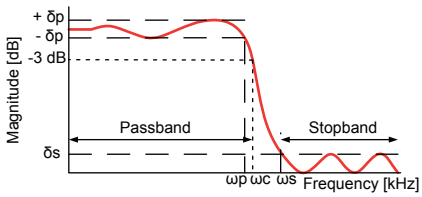


Figure O.15: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -3 dB) Filter (Digital Anti-Alias)



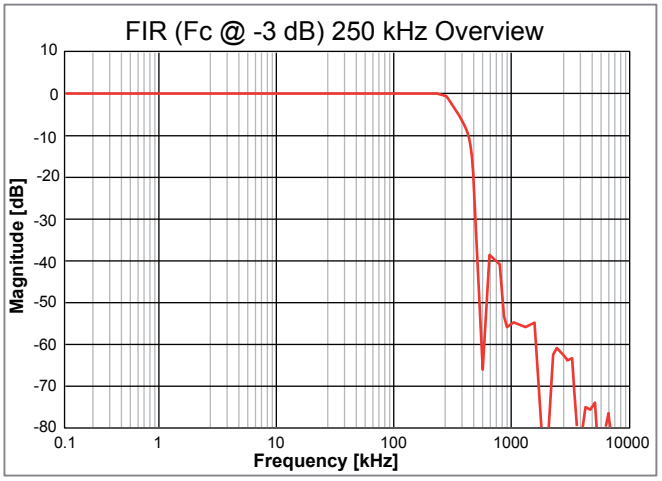
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.16: Digital FIR (Fc @ -3 dB) filter

When FIR (Fc @ -3 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -3 dB) filter. The FIR (Fc @ -3 dB) is an adapted FIR filter. Its ωp is reduced by a factor of ≈1.4 compared to the FIR (Fc @ -0.1 dB) filter. It is supported by Perception V6.40 and higher.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -3 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -3 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 Divided by 40 not available for 1 MS/s & 500 kS/s sample rate The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
FIR (Fc @ -3 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -3 dB) filter, user selection from 0.031 Hz to 250 kHz
FIR (Fc @ -3 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to ≈ωc/1.4 (Adapted FIR filter behavior) 0.1 dB; DC to 125 kHz; FIR (Fc @ -3 dB) filter bandwidth selection of ωc = 250 kHz, limited by the 370 kHz analog anti-alias filter amplitude response. All other bandwidth selections are not affected.
FIR (Fc @ -3 dB) filter stopband attenuation (δs)	60 dB With the FIR (Fc @ -3 dB) filter bandwidth selection of ωc = 250 kHz, a peak of -35 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
FIR (Fc @ -3 dB) filter roll-off	72 dB/Octave



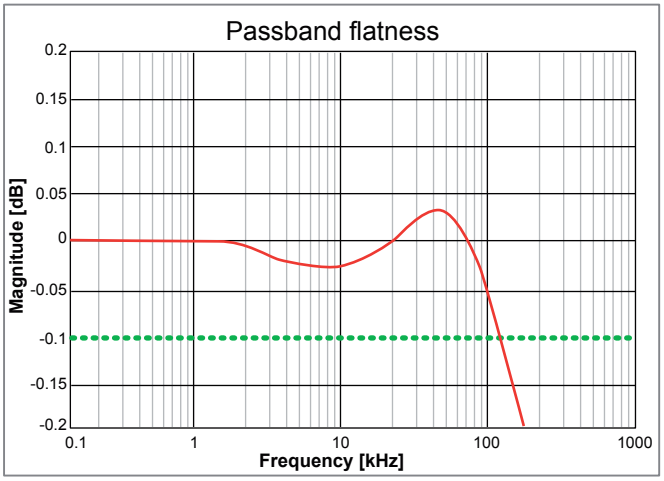


Figure O.17: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/FIR/etc.) or different filter bandwidths results in phase mismatches between channels.	
Wideband	100 kHz Sine
Channels on card	0.7 deg (0.02 µs)
GN811 Channels within mainframe	0.7 deg (0.02 µs)
Bessel IIR (Fc @ -3 dB), 100 kHz Filter frequency	
Channels on card	0.7 deg (0.02 µs)
GN811 Channels within mainframe	0.7 deg (0.02 µs)
FIR (Fc@ -0.1dB) and FIR (Fc @ -3 dB), 250 kHz Filter frequency	
Channels on card	0.7 deg (0.02 µs)
GN811 Channels within mainframe	0.7 deg (0.02 µs)
GN811 Channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	256 MB (128 MS)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	16 bits, 2 bytes/sample

Digital Events/Timer/Counter	
Digital event inputs	Not supported
Digital event outputs	Not supported
Timer/Counter	Not supported

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Active edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Delay	± 1 µs + maximum 1 sample period (for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Active level	High/Low/Hold High; selectable per mainframe, identical for all cards
Pulse width	High/Low: 12.8 µs Hold high: Active from first mainframe trigger to end of recording Pulse width created by mainframe
Delay	516 µs ± 1 µs + maximum 1 sample period using decimal time base 504 µs ± 1 µs + maximum 1 sample period using binary time base
Cross channel triggering	
Channels on card	Logical OR; Analog triggers of all channels Logical AND; Qualifiers of all channels
Cards in mainframe	User selectable through system trigger bus Selections: Send/Receive/Transceive (Send & Receive)
System trigger bus	
Connections	3 System trigger busses connecting all cards within mainframe 1 Master/Slave bus connecting all cards within mainframe and connecting all mainframes when using Master/Slave option
Operation	Logical OR of all triggers of all cards Logical AND of all qualifiers of all cards
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; Single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Pulse detect/reject	Disable/Detect/Reject software selectable. Maximum pulse width 65 535 samples
dY/dT conversion	dY: 16 bit (0.0015%) for both levels dT: 1 to 1023 samples. dT setting shared for both levels
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; Two individual levels, OR-ed
Window	Arm/trigger and a disarm level; Trigger on peak level changes in a uni-polar signal
Dual Window	Arm/trigger/disarm per level; Trigger on peak level changes in a bi-polar signal
Sequential	One arm and one trigger level; eliminate false triggering due to noise or hysteresis
Analog channel qualifier modes	
Basic	Above or below level check. Enable/disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/disable trigger with dual level
Trigger hold off	Disable channel trigger for 1 to 65 535 samples after trigger detected Maximum hold off time depends on sample rate

Triggering	
Interval timer	
Modes	Less than, trigger when rate is too low More than, trigger when rate is too high Between, trigger when rate between lower and upper limit Not between, trigger when rate is not between lower and upper limit
Interval timers	Start timer and width Timer
Timer value	1 to 65 535 samples
Event counter	Counts channel trigger events before card trigger is activated 1 to 256 trigger events

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

	Single Sweep Multiple Sweeps Slow-Fast Sweep			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch
Max. sweep memory	124 MS	62 MS	15.5 MS	not used			99 MS	50 MS	12 MS
Max. sweep sample rate	1 MS/s			not used			1 MS/s		
Max. continuous FIFO	not used			124 MS	62 MS	15.5 MS	24 MS	12 MS	3 MS
Max. continuous sample rate	not used			1 MS/s			Sweep sample rate / 2 Maximum 50 kS/s		
Max. aggregate continuous streaming rate	not used			1 MS/s 2 MB/s	2 MS/s 4 MB/s	8 MS/s 16 MB/s	0.05 MS/s 0.1 MB/s	0.1 MS/s 0.2 MB/s	0.8 MS/s 1.6 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two or 50 kS/s per channel, whichever is the smallest sample rate
Maximum sample rate switches	400 sample rate switches per second, 200 000 switches maximum, switching stops when sweep ends

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives	
Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

O.3 B2634-3.1 en (GEN series GN812)

Capabilities Overview	
Model	GN812
Maximum sample rate per channel	1 MS/s
Memory per card	512 MB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16 bit
Isolation	Yes; channel to channel and channel to chassis
Input type	Analog, isolated, single-ended, unbalanced differential (1)
Passive voltage/current probes	Passive, single-ended, isolated voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	Not supported
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	Not supported
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

(1) An unbalanced differential input can be used to isolated, single-ended and differential measurements.

Block Diagram

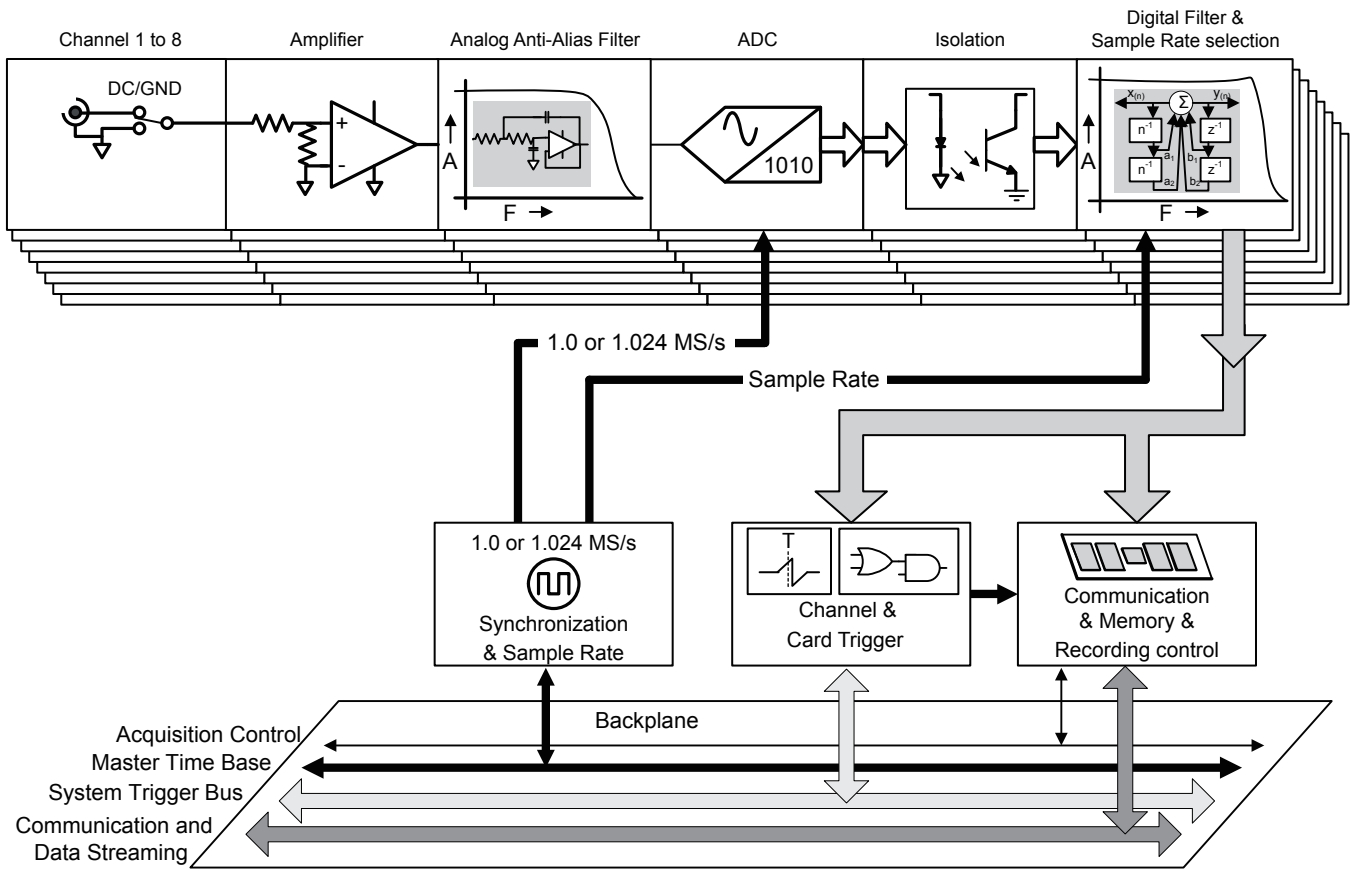


Figure O.18: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	8
Connectors	Fully isolated BNC (Plastic), 1 per channel
Input type	Analog, isolated, single-ended, unbalanced differential
Input coupling	DC, GND
Impedance	1 MΩ ± 1% // 65 pF ± 10%
Ranges	± 1 V, ± 2 V, ± 5.0 V, ± 10 V, ± 20 V, ± 50 V Each fixed range supports a variable gain with 1000 steps (0.1%). Variable gain creates 1000 extra ranges between two fixed ranges.
Offset	± 50% in 1000 steps (0.1%); ± 50 V range has fixed 0% offset
DC Offset error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Offset error drift	± 100 ppm/°C (± 180 ppm/°F)
DC Gain error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Gain error drift	± 70 ppm/°C (± 130 ppm/°F)
Maximum static error (MSE)	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
RMS Noise	
Wideband	0.02% of Full Scale ± 10 µV
Bessel IIR and FIR	0.02% of Full Scale ± 10 µV
Common mode	
Rejection Ratio (CMRR)	> 72 dB @ 80 Hz
Voltage	250 V DC
Input overload protection	
Maximum voltage	± 250 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 1 µs after 200% overload

Isolation	
Channel to chassis	± 250 V DC
Channel to channel	± 500 V DC
Nondestructive to chassis (earth)	± 250 V DC

Analog to Digital Conversion	
Sample rate per channel	0.1 S/s to 1 MS/s
ADC resolution; one ADC per channel	16 bit
ADC Type	Successive Approximation Register (SAR); TI ADS8401IB
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; when calculating FFTs results in rounded/integer BIN sizes
Maximum binary sample rate	1.024 MS/s
External time base sample rate	0 S/s to 500 kS/s
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ± 30 ppm

Anti-Alias Filters

Using different filter selections (Wideband/Bessel IIR/FIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

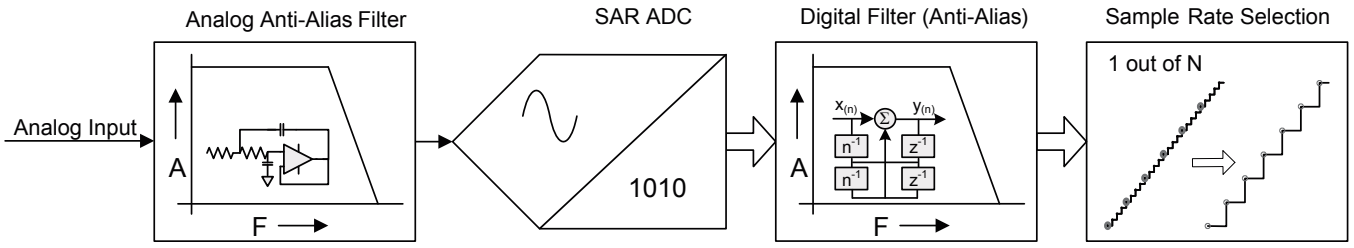


Figure O.19: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Should not be used if working in a frequency domain with recorded data.
Digital Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. Best used for measuring transient signals or sharp edge signals like square waves or step responses.
Digital FIR (Fc @ -0.1 dB)	Standard FIR filter with corner frequency (Fc) defined at -0.1 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Digital FIR (Fc @ -3 dB) Supported by Perception V6.40 and higher	Adapted FIR filter with corner frequency (Fc) calculated as close as possible to -3 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	Between 540 kHz and 690 kHz (-3 dB)
Passband flatness (1)	0.1 dB; DC to 150 kHz

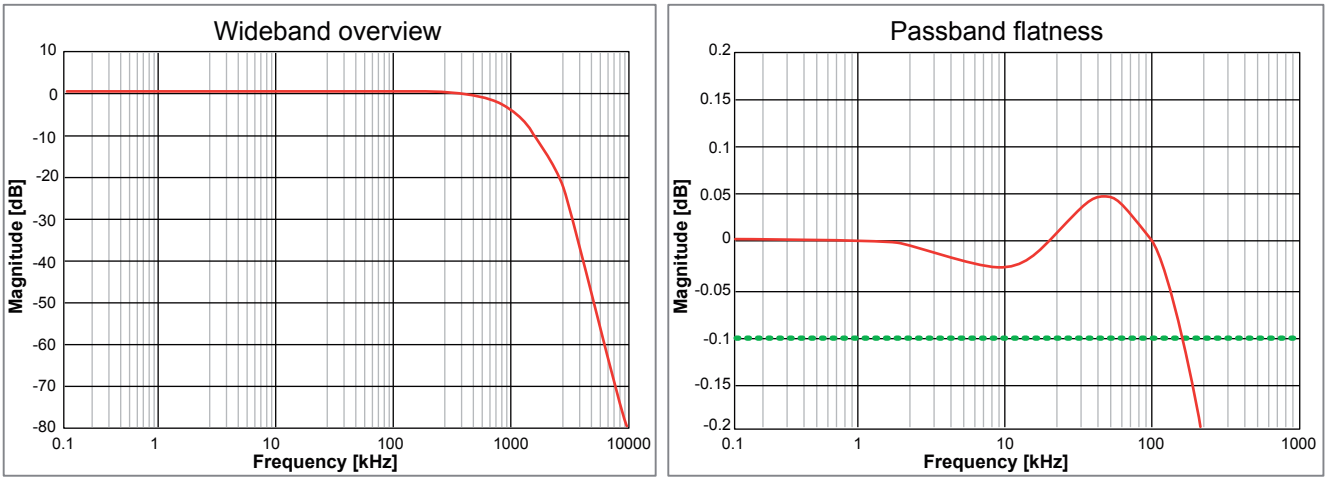
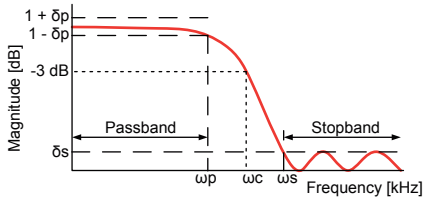


Figure O.20: Representative Wideband examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



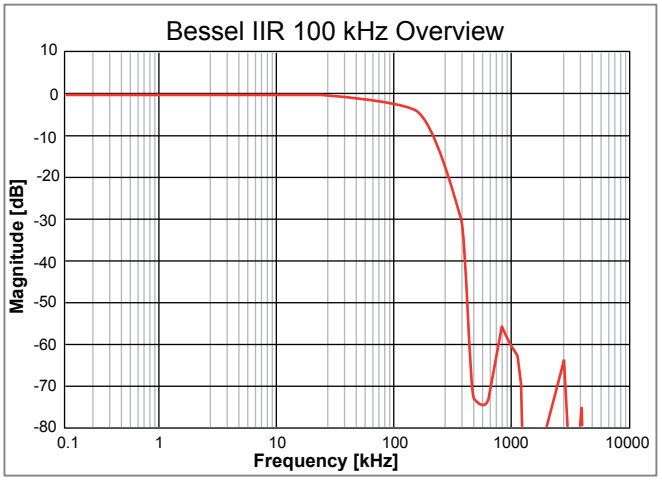
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.21: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-aliasing filter bandwidth	220 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	6-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	Auto tracking the sample rate with the selected Bessel IIR filter; user selection from 0.0125 Hz to 100 kHz
Bessel IIR passband flatness (ωp)(1)	0.1 dB; DC to 20 kHz @ ωc = 100 kHz
Bessel IIR filter stopband attenuation (δs)	60 dB With the Bessel IIR filter bandwidth selection of ωc = 100 kHz, a peak of -55 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
Bessel IIR filter roll-off	36 dB/Octave



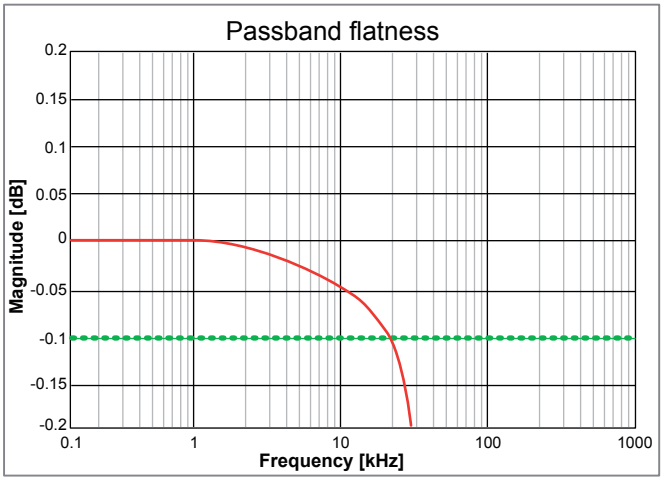
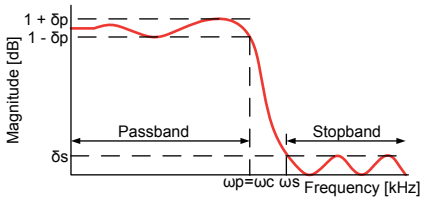


Figure O.22: Representative Bessel IIR examples

(1) Measured using Fluke 5700 calibrator, DC normalized

FIR (Fc @ -0.1 dB) Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.23: Digital FIR (Fc @ -0.1 dB) filter

When FIR (Fc @ -0.1 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -0.1 dB) filter.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -0.1 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -0.1 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 Divided by 40 not available for 1 MS/s & 500 kS/s sample rate The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
FIR (Fc @ -0.1 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -0.1 dB) filter; user selection from 0.031 Hz to 250 kHz
FIR (Fc @ -0.1 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to filter bandwidth (ωc) 0.1 dB; DC to 125 kHz; FIR (Fc @ -0.1 dB) filter bandwidth selection of ωc = 250 kHz, limited by the 370 kHz analog anti-alias filter amplitude response. All other bandwidth selections are not affected.
FIR (Fc @ -0.1 dB) filter stopband attenuation (δs)	60 dB With the FIR (Fc @ -0.1 dB) filter bandwidth selection of ωc = 250 kHz, a peak of -35 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
FIR (Fc @ -0.1 dB) filter roll-off	72 dB/Octave

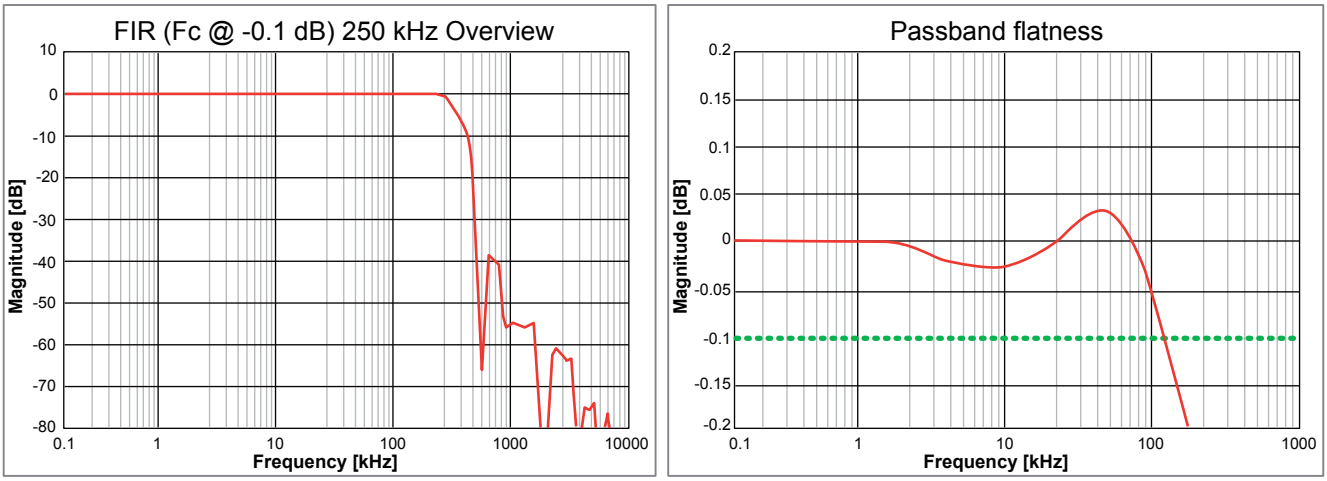
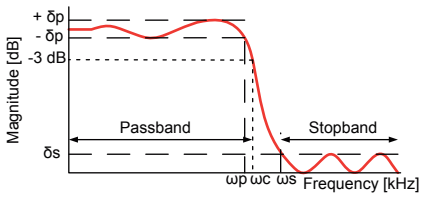


Figure O.24: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -3 dB) Filter (Digital Anti-Alias)



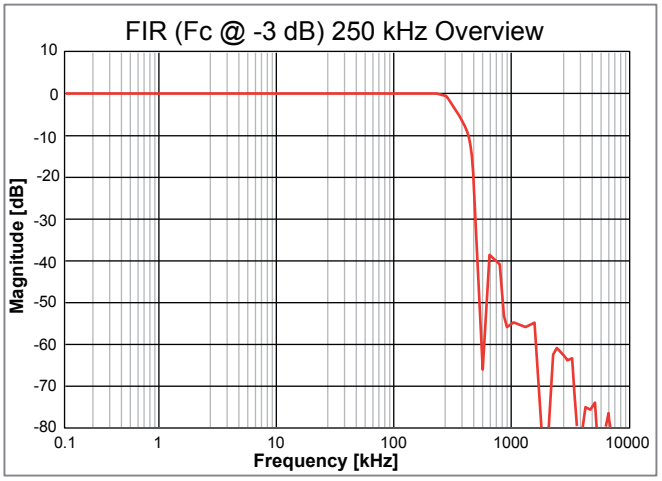
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.25: Digital FIR (Fc @ -3 dB) filter

When FIR (Fc @ -3 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -3 dB) filter. The FIR (Fc @ -3 dB) is an adapted FIR filter. Its ωp is reduced by a factor of ≈1.4 compared to the FIR (Fc @ -0.1 dB) filter. It is supported by Perception V6.40 and higher.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -3 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -3 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 Divided by 40 not available for 1 MS/s & 500 kS/s sample rate The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
FIR (Fc @ -3 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -3 dB) filter, user selection from 0.031 Hz to 250 kHz
FIR (Fc @ -3 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to ≈ωc/1.4 (Adapted FIR filter behavior) 0.1 dB; DC to 125 kHz; FIR (Fc @ -3 dB) filter bandwidth selection of ωc = 250 kHz, limited by the 370 kHz analog anti-alias filter amplitude response. All other bandwidth selections are not affected.
FIR (Fc @ -3 dB) filter stopband attenuation (δs)	60 dB With the FIR (Fc @ -3 dB) filter bandwidth selection of ωc = 250 kHz, a peak of -35 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
FIR (Fc @ -3 dB) filter roll-off	72 dB/Octave



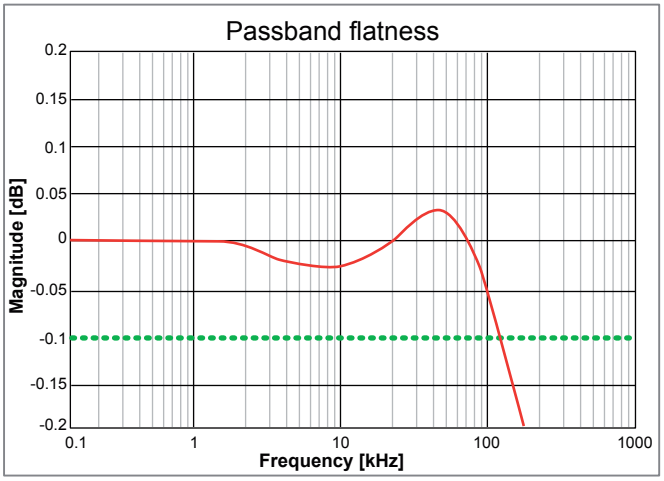


Figure O.26: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/FIR/etc.) or different filter bandwidths results in phase mismatches between channels.	
Wideband	100 kHz Sine
Channels on card	0.7 deg (0.02 µs)
GN812 Channels within mainframe	0.7 deg (0.02 µs)
Bessel IIR (Fc @ -3 dB), 100 kHz Filter frequency	
Channels on card	0.7 deg (0.02 µs)
GN812 Channels within mainframe	0.7 deg (0.02 µs)
FIR (Fc@ -0.1dB) and FIR (Fc @ -3 dB), 250 kHz Filter frequency	
Channels on card	0.7 deg (0.02 µs)
GN812 Channels within mainframe	0.7 deg (0.02 µs)
GN812 Channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	512 MB (256 MS)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	16 bits, 2 bytes/sample

Digital Events/Timer/Counter	
Digital event inputs	Not supported
Digital event outputs	Not supported
Timer/Counter	Not supported

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Active edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Delay	± 1 µs + maximum 1 sample period (for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Active level	High/Low/Hold High; selectable per mainframe, identical for all cards
Pulse width	High/Low: 12.8 µs Hold high: Active from first mainframe trigger to end of recording Pulse width created by mainframe
Delay	516 µs ± 1 µs + maximum 1 sample period using decimal time base 504 µs ± 1 µs + maximum 1 sample period using binary time base
Cross channel triggering	
Channels on card	Logical OR; Analog triggers of all channels Logical AND; Qualifiers of all channels
Cards in mainframe	User selectable through system trigger bus Selections: Send/Receive/Transceive (Send & Receive)
System trigger bus	
Connections	3 System trigger busses connecting all cards within mainframe 1 Master/Slave bus connecting all cards within mainframe and connecting all mainframes when using Master/Slave option
Operation	Logical OR of all triggers of all cards Logical AND of all qualifiers of all cards
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; Single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Pulse detect/reject	Disable/Detect/Reject software selectable. Maximum pulse width 65 535 samples
dY/dT conversion	dY: 16 bit (0.0015%) for both levels dT: 1 to 1023 samples. dT setting shared for both levels
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; Two individual levels, OR-ed
Window	Arm/trigger and a disarm level; Trigger on peak level changes in a uni-polar signal
Dual Window	Arm/trigger/disarm per level; Trigger on peak level changes in a bi-polar signal
Sequential	One arm and one trigger level; eliminate false triggering due to noise or hysteresis
Analog channel qualifier modes	
Basic	Above or below level check. Enable/disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/disable trigger with dual level
Trigger hold off	Disable channel trigger for 1 to 65 535 samples after trigger detected Maximum hold off time depends on sample rate

Triggering	
Interval timer	
Modes	Less than, trigger when rate is too low More than, trigger when rate is too high Between, trigger when rate between lower and upper limit Not between, trigger when rate is not between lower and upper limit
Interval timers	Start timer and width Timer
Timer value	1 to 65 535 samples
Event counter	Counts channel trigger events before card trigger is activated 1 to 256 trigger events

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

	Single Sweep Multiple Sweeps Slow-Fast Sweep			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch
Max. sweep memory	252 MS	126 MS	31.5 MS	not used			200 MS	100 MS	25 MS
Max. sweep sample rate	1 MS/s			not used			1 MS/s		
Max. continuous FIFO	not used			252 MS	126 MS	31.5 MS	50 MS	25 MS	6 MS
Max. continuous sample rate	not used			1 MS/s			Sweep sample rate / 2 Maximum 50 kS/s		
Max. aggregate continuous streaming rate	not used			1 MS/s 2 MB/s	2 MS/s 4 MB/s	8 MS/s 16 MB/s	0.05 MS/s 0.1 MB/s	0.1 MS/s 0.2 MB/s	0.8 MS/s 1.6 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two or 50 kS/s per channel, whichever is the smallest sample rate
Maximum sample rate switches	400 sample rate switches per second, 200 000 switches maximum, switching stops when sweep ends

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

O.4 B2635-4.1 en (GEN series GN813)

Capabilities Overview	
Model	GN813
Maximum sample rate per channel	1 MS/s
Memory per card	512 MB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16 bit
Isolation	Yes; channel to channel and channel to chassis
Input type	Analog, isolated, single-ended, unbalanced differential (1)
Passive voltage/current probes	Passive, single-ended, isolated voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	Not supported
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	Not supported
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

(1) An unbalanced differential input can be used to isolated, single-ended and differential measurements.

Block Diagram

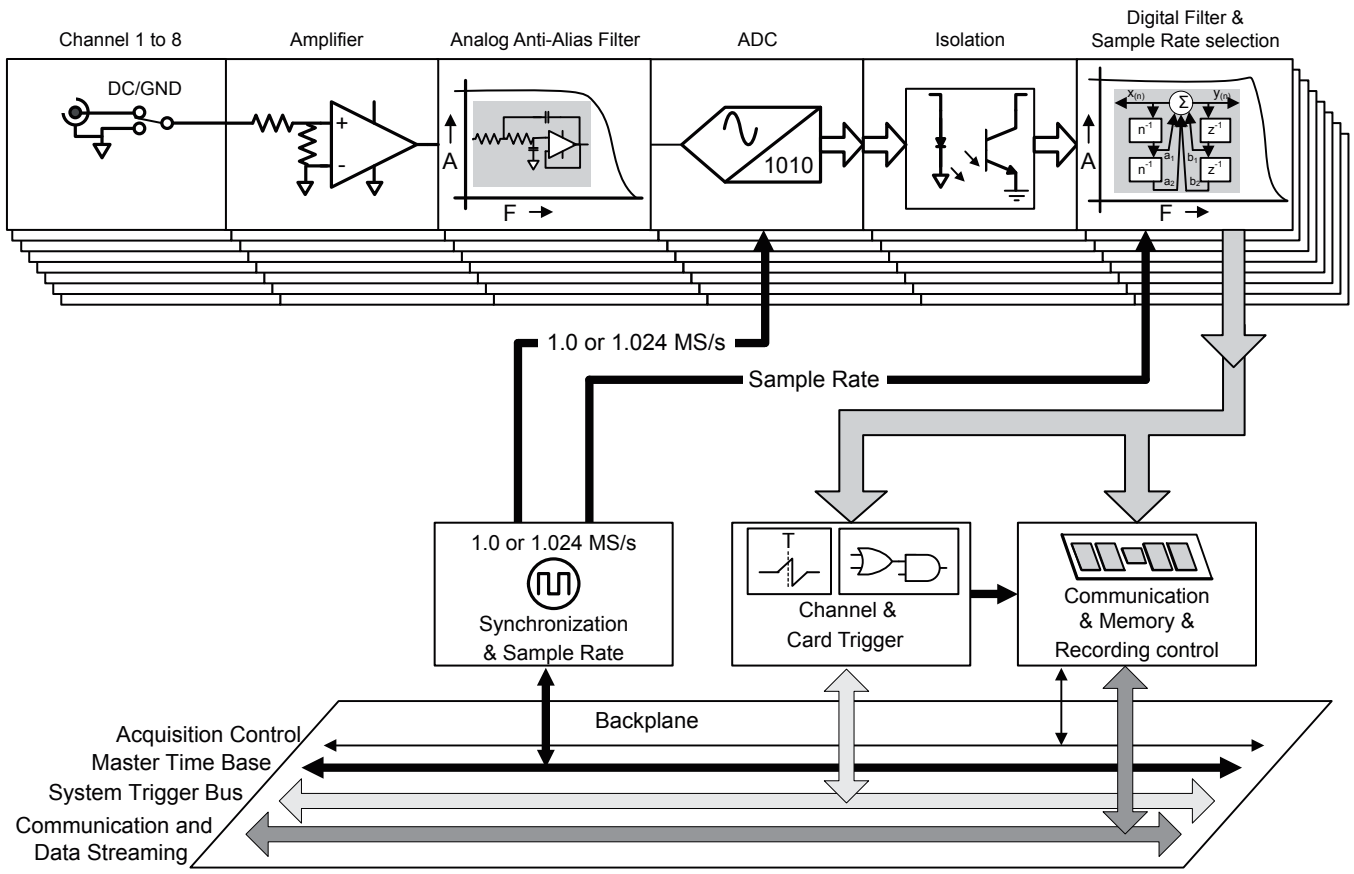


Figure O.27: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	8
Connectors	Fully isolated BNC (Plastic), 1 per channel
Input type	Analog, isolated, single-ended, unbalanced differential
Input coupling	DC, GND
Impedance	1 MΩ ± 1% // 55 pF ± 10%
Ranges	± 2.0 V, ± 4.0 V, ± 10.0 V, ± 20 V, ± 40 V, ± 100 V Each fixed range supports a variable gain with 1000 steps (0.1%). Variable gain creates 1000 extra ranges between two fixed ranges.
Offset	± 50% in 1000 steps (0.1%); ± 100 V range has fixed 0% offset
DC Offset error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Offset error drift	± 100 ppm/°C (± 180 ppm/°F)
DC Gain error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Gain error drift	± 70 ppm/°C (± 130 ppm/°F)
Maximum static error (MSE)	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
RMS Noise	
Wideband	0.02% of Full Scale ± 10 µV
Bessel IIR and FIR	0.02% of Full Scale ± 10 µV
Common mode	
Rejection Ratio (CMRR)	> 72 dB @ 80 Hz
Voltage	250 V DC
Input overload protection	
Maximum voltage	± 250 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 1 µs after 200% overload

Isolation	
Channel to chassis	± 250 V DC
Channel to channel	± 500 V DC
Nondestructive to chassis (earth)	± 250 V DC

Analog to Digital Conversion	
Sample rate per channel	0.1 S/s to 1 MS/s
ADC resolution; one ADC per channel	16 bit
ADC Type	Successive Approximation Register (SAR); TI ADS8401IB
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; when calculating FFTs results in rounded/integer BIN sizes
Maximum binary sample rate	1.024 MS/s
External time base sample rate	0 S/s to 500 kS/s
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ± 30 ppm

Anti-Alias Filters

Using different filter selections (Wideband/Bessel IIR/FIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

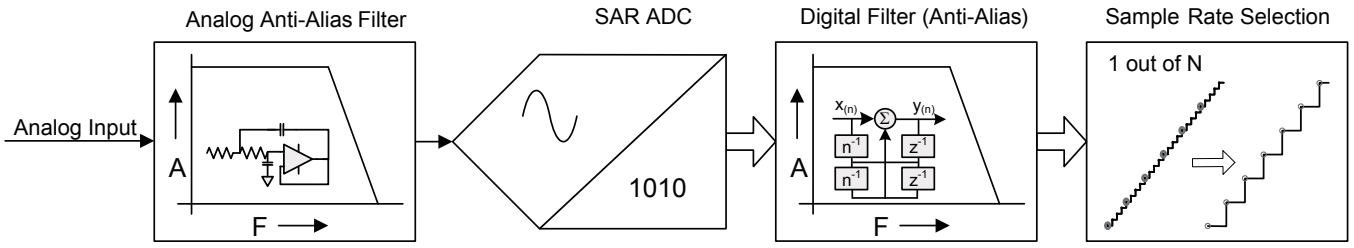


Figure O.28: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Wideband	When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected. Should not be used if working in a frequency domain with recorded data.
Digital Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. Best used for measuring transient signals or sharp edge signals like square waves or step responses.
Digital FIR (Fc @ -0.1 dB)	Standard FIR filter with corner frequency (Fc) defined at -0.1 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Digital FIR (Fc @ -3 dB) Supported by Perception V6.40 and higher	Adapted FIR filter with corner frequency (Fc) calculated as close as possible to -3 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Wideband (No Anti-Alias Protection)

When wideband is selected, there is neither an analog anti-alias filter nor any digital filter in the signal path. Therefore, there is no anti-alias protection when wideband is selected.

Wideband bandwidth	Between 540 kHz and 690 kHz (-3 dB)
Passband flatness (1)	0.1 dB; DC to 150 kHz

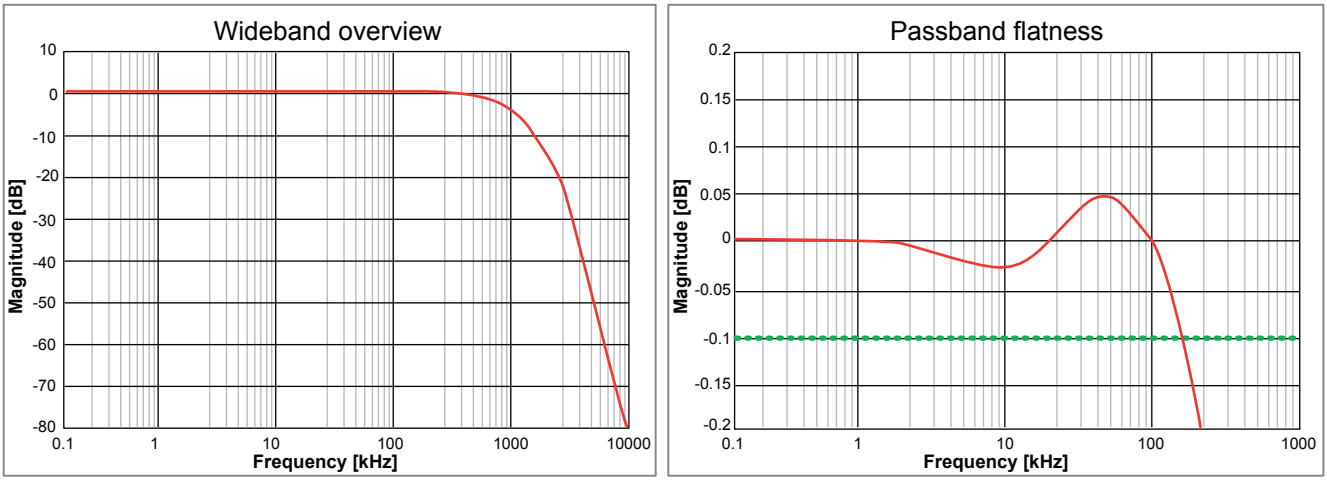
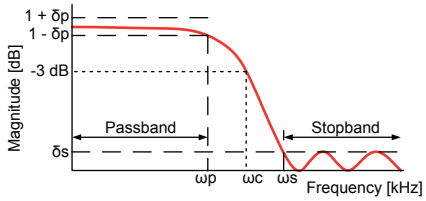


Figure O.29: Representative Wideband examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



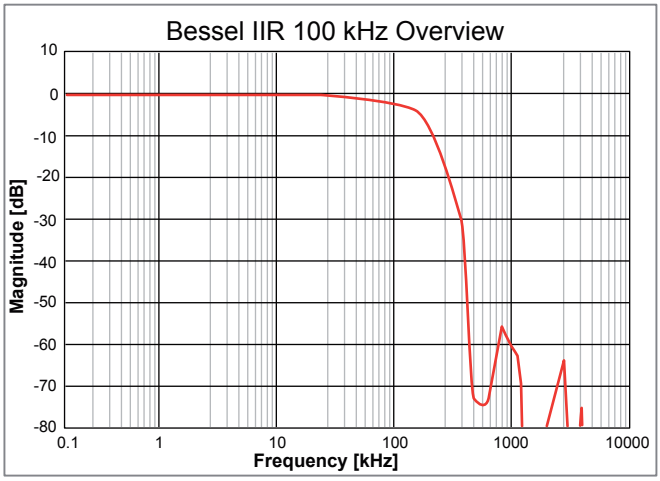
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.30: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-aliasing filter bandwidth	220 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	6-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
Bessel IIR filter bandwidth (ωc)	Auto tracking the sample rate with the selected Bessel IIR filter; user selection from 0.0125 Hz to 100 kHz
Bessel IIR passband flatness (ωp)(1)	0.1 dB; DC to 20 kHz @ ωc = 100 kHz
Bessel IIR filter stopband attenuation (δs)	60 dB With the Bessel IIR filter bandwidth selection of ωc = 100 kHz, a peak of -55 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
Bessel IIR filter roll-off	36 dB/Octave



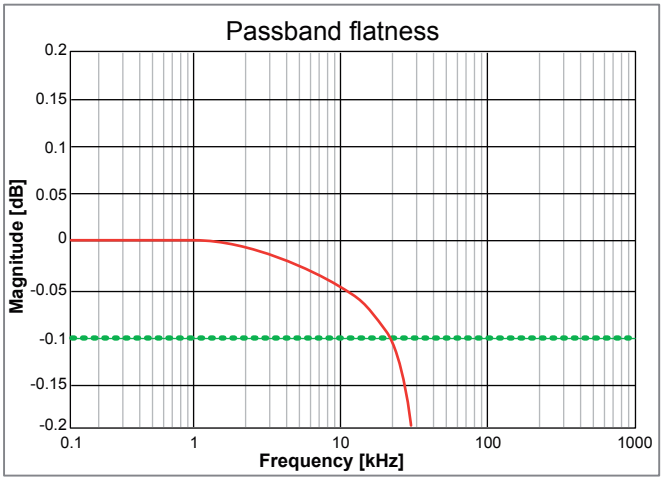
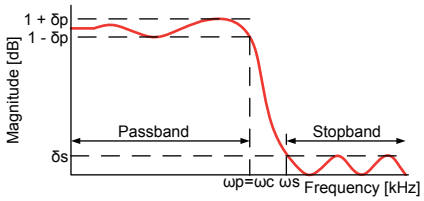


Figure O.31: Representative Bessel IIR examples

(1) Measured using Fluke 5700 calibrator, DC normalized

FIR (Fc @ -0.1 dB) Filter (Digital Anti-Alias)



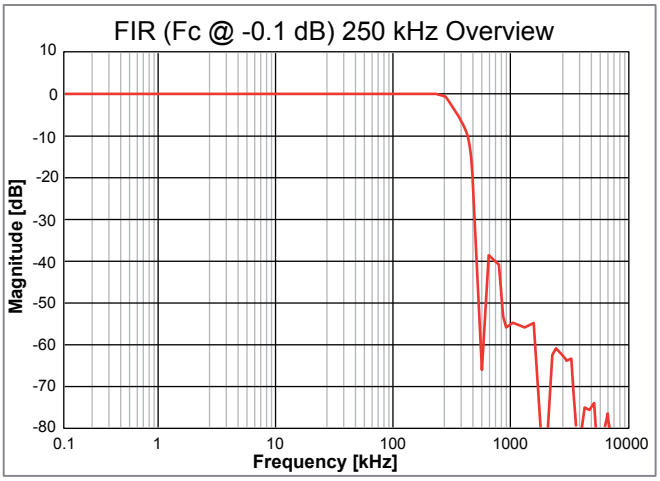
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.32: Digital FIR (Fc @ -0.1 dB) filter

When FIR (Fc @ -0.1 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -0.1 dB) filter.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -0.1 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -0.1 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 Divided by 40 not available for 1 MS/s & 500 kS/s sample rate The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
FIR (Fc @ -0.1 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -0.1 dB) filter; user selection from 0.031 Hz to 250 kHz
FIR (Fc @ -0.1 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to filter bandwidth (ωc) 0.1 dB; DC to 125 kHz; FIR (Fc @ -0.1 dB) filter bandwidth selection of ωc = 250 kHz, limited by the 370 kHz analog anti-alias filter amplitude response. All other bandwidth selections are not affected.
FIR (Fc @ -0.1 dB) filter stopband attenuation (δs)	60 dB With the FIR (Fc @ -0.1 dB) filter bandwidth selection of ωc = 250 kHz, a peak of -35 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
FIR (Fc @ -0.1 dB) filter roll-off	72 dB/Octave



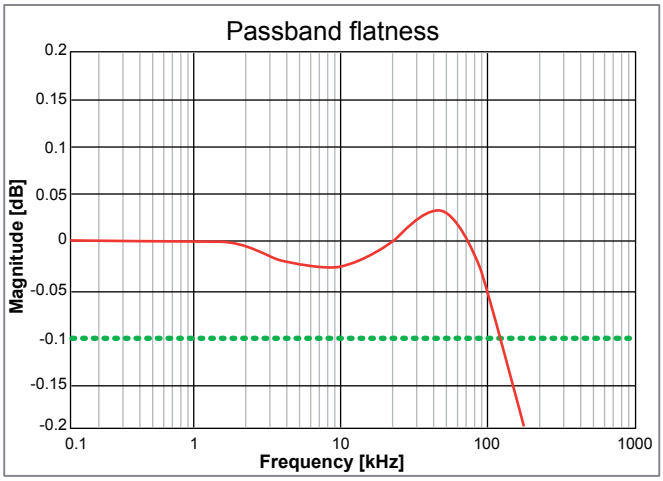
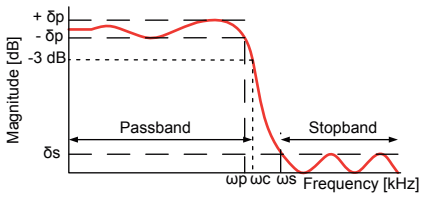


Figure O.33: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -3 dB) Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.34: Digital FIR (Fc @ -3 dB) filter

When FIR (Fc @ -3 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -3 dB) filter. The FIR (Fc @ -3 dB) is an adapted FIR filter. Its ωp is reduced by a factor of ≈1.4 compared to the FIR (Fc @ -0.1 dB) filter. It is supported by Perception V6.40 and higher.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -3 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -3 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40 Divided by 40 not available for 1 MS/s & 500 kS/s sample rate The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed.
FIR (Fc @ -3 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -3 dB) filter, user selection from 0.031 Hz to 250 kHz
FIR (Fc @ -3 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to ≈ωc/1.4 (Adapted FIR filter behavior) 0.1 dB; DC to 125 kHz; FIR (Fc @ -3 dB) filter bandwidth selection of ωc = 250 kHz, limited by the 370 kHz analog anti-alias filter amplitude response. All other bandwidth selections are not affected.
FIR (Fc @ -3 dB) filter stopband attenuation (δs)	60 dB With the FIR (Fc @ -3 dB) filter bandwidth selection of ωc = 250 kHz, a peak of -35 dB occurs between 500 kHz and 1 MHz due to limited analog anti-alias filter amplitude reduction. At lower bandwidth selections, the digital filter reduces this peak to -60 dB.
FIR (Fc @ -3 dB) filter roll-off	72 dB/Octave

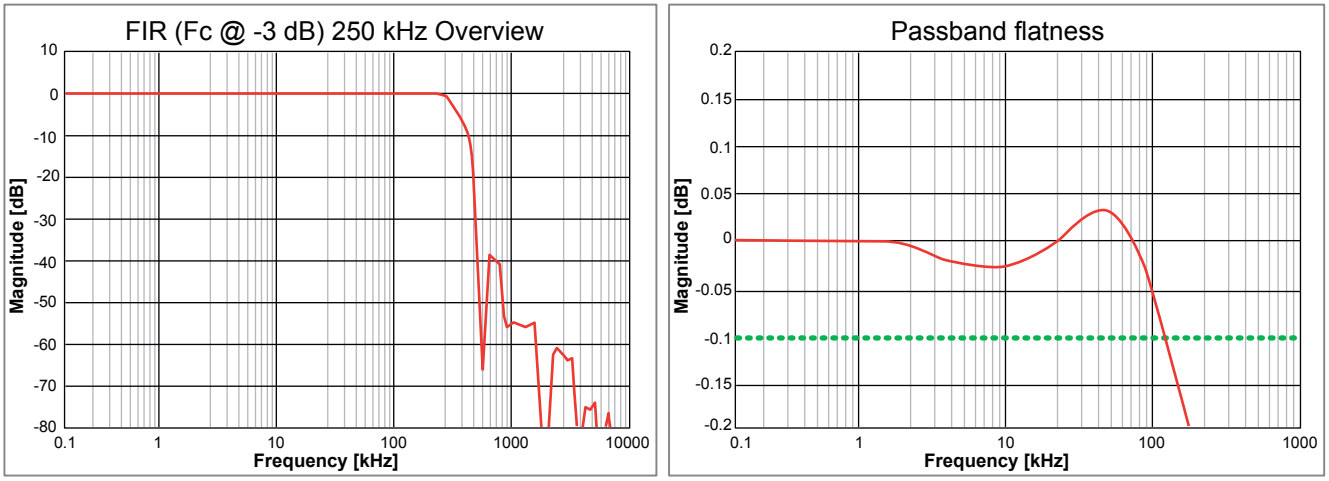


Figure O.35: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/FIR/etc.) or different filter bandwidths results in phase mismatches between channels.	
Wideband	100 kHz Sine
Channels on card	0.7 deg (0.02 µs)
GN813 Channels within mainframe	0.7 deg (0.02 µs)
Bessel IIR (Fc @ -3 dB), 100 kHz Filter frequency	
Channels on card	0.7 deg (0.02 µs)
GN813 Channels within mainframe	0.7 deg (0.02 µs)
FIR (Fc@ -0.1dB) and FIR (Fc @ -3 dB), 250 kHz Filter frequency	
Channels on card	0.7 deg (0.02 µs)
GN813 Channels within mainframe	0.7 deg (0.02 µs)
GN813 Channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave , PTP)

On-board Memory	
Per card	512 MB (256 MS)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	16 bits, 2 bytes/sample

Digital Events/Timer/Counter	
Digital event inputs	Not supported
Digital event outputs	Not supported
Timer/Counter	Not supported

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Active edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Delay	± 1 µs + maximum 1 sample period (for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Active level	High/Low/Hold High; selectable per mainframe, identical for all cards
Pulse width	High/Low: 12.8 µs Hold high: Active from first mainframe trigger to end of recording Pulse width created by mainframe
Delay	516 µs ± 1 µs + maximum 1 sample period using decimal time base 504 µs ± 1 µs + maximum 1 sample period using binary time base
Cross channel triggering	
Channels on card	Logical OR; Analog triggers of all channels Logical AND; Qualifiers of all channels
Cards in mainframe	User selectable through system trigger bus Selections: Send/Receive/Transceive (Send & Receive)
System trigger bus	
Connections	3 System trigger busses connecting all cards within mainframe 1 Master/Slave bus connecting all cards within mainframe and connecting all mainframes when using Master/Slave option
Operation	Logical OR of all triggers of all cards Logical AND of all qualifiers of all cards
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; Single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Pulse detect/reject	Disable/Detect/Reject software selectable. Maximum pulse width 65 535 samples
dY/dT conversion	dY: 16 bit (0.0015%) for both levels dT: 1 to 1023 samples. dT setting shared for both levels
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; Two individual levels, OR-ed
Window	Arm/trigger and a disarm level; Trigger on peak level changes in a uni-polar signal
Dual Window	Arm/trigger/disarm per level; Trigger on peak level changes in a bi-polar signal
Sequential	One arm and one trigger level; eliminate false triggering due to noise or hysteresis
Analog channel qualifier modes	
Basic	Above or below level check. Enable/disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/disable trigger with dual level
Trigger hold off	Disable channel trigger for 1 to 65 535 samples after trigger detected Maximum hold off time depends on sample rate

Triggering	
Interval timer	
Modes	Less than, trigger when rate is too low More than, trigger when rate is too high Between, trigger when rate between lower and upper limit Not between, trigger when rate is not between lower and upper limit
Interval timers	Start timer and width Timer
Timer value	1 to 65 535 samples
Event counter	Counts channel trigger events before card trigger is activated 1 to 256 trigger events

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

	Single Sweep Multiple Sweeps Slow-Fast Sweep			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch
Max. sweep memory	252 MS	126 MS	31.5 MS	not used			200 MS	100 MS	25 MS
Max. sweep sample rate	1 MS/s			not used			1 MS/s		
Max. continuous FIFO	not used			252 MS	126 MS	31.5 MS	50 MS	25 MS	6 MS
Max. continuous sample rate	not used			1 MS/s			Sweep sample rate / 2 Maximum 50 kS/s		
Max. aggregate continuous streaming rate	not used			1 MS/s 2 MB/s	2 MS/s 4 MB/s	8 MS/s 16 MB/s	0.05 MS/s 0.1 MB/s	0.1 MS/s 0.2 MB/s	0.8 MS/s 1.6 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two or 50 kS/s per channel, whichever is the smallest sample rate
Maximum sample rate switches	400 sample rate switches per second, 200 000 switches maximum, switching stops when sweep ends

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU	
Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

O.5 B2889-5.1 en (GEN series GN814)

Capabilities Overview	
Model	GN814
Maximum sample rate per channel	200 kS/s
Memory per card	128 MB
Analog channels	8
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16 bit
Isolation	Yes; channel to channel and channel to chassis
Input type	Analog, isolated, single-ended, unbalanced differential (1)
Passive voltage/current probes	Passive, single-ended, isolated voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	Not supported
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	Not supported
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

(1) An unbalanced differential input can be used to isolated, single-ended and differential measurements.

Block Diagram

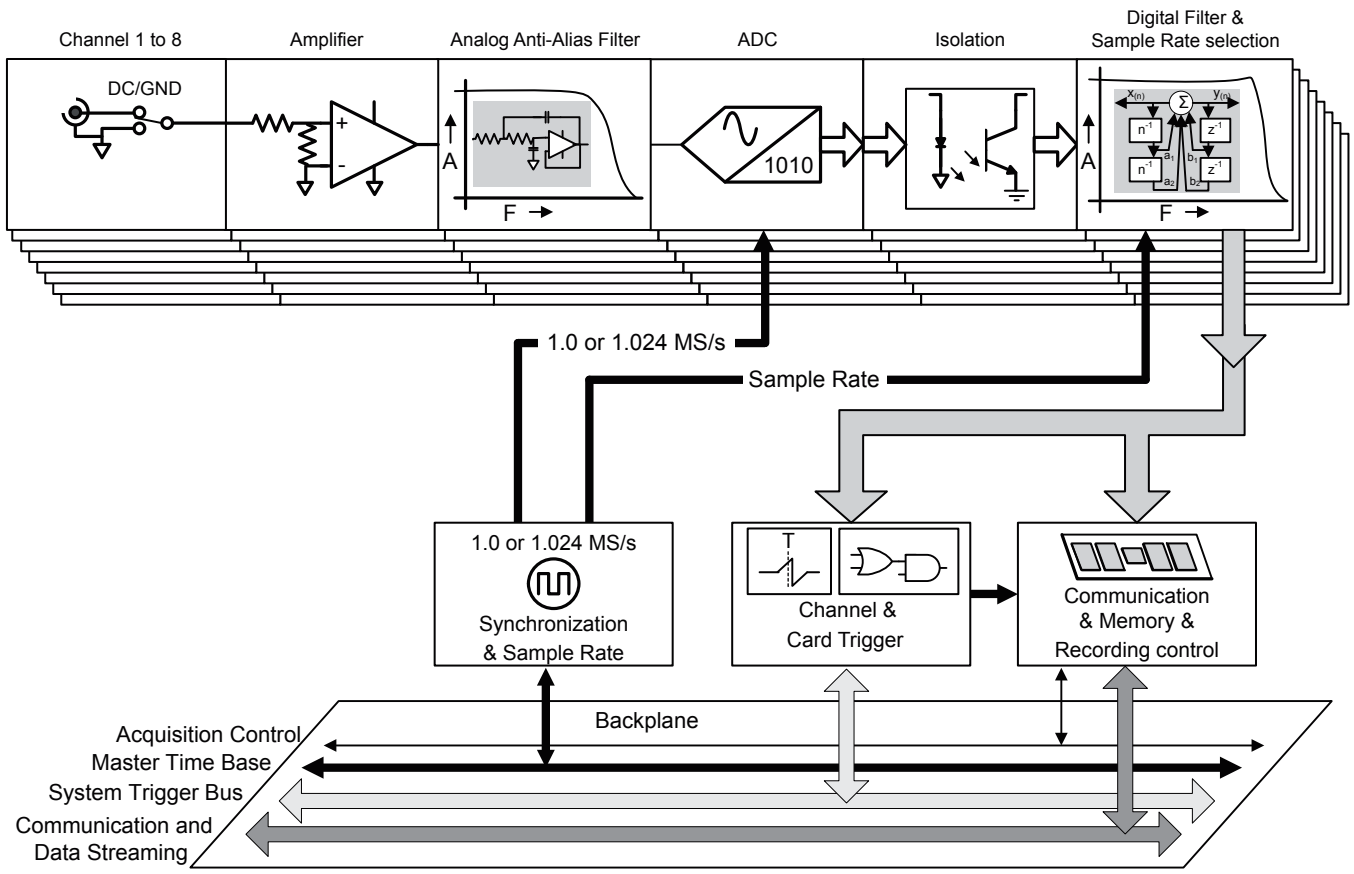


Figure O.36: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	8
Connectors	Fully isolated BNC (Plastic), 1 per channel
Input type	Analog, isolated, single-ended, unbalanced differential
Input coupling	DC, GND
Impedance	1 MΩ ± 1% // 55 pF ± 10%
Ranges	± 2.0 V, ± 4.0 V, ± 10.0 V, ± 20 V, ± 40 V, ± 100 V Each fixed range supports a variable gain with 1000 steps (0.1%). Variable gain creates 1000 extra ranges between two fixed ranges.
Offset	± 50% in 1000 steps (0.1%); ± 100 V range has fixed 0% offset
DC Offset error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Offset error drift	± 100 ppm/°C (± 180 ppm/°F)
DC Gain error	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
Gain error drift	± 70 ppm/°C (± 130 ppm/°F)
Maximum static error (MSE)	
Wideband	0.1% of Full Scale ± 2 mV
Bessel IIR and FIR	0.1% of Full Scale ± 10 µV
RMS Noise	
Wideband	0.02% of Full Scale ± 10 µV
Bessel IIR and FIR	0.02% of Full Scale ± 10 µV
Common mode	
Rejection Ratio (CMRR)	> 72 dB @ 80 Hz
Voltage	250 V DC
Input overload protection	
Maximum voltage	± 250 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 1 µs after 200% overload

Isolation	
Channel to chassis	± 250 V DC
Channel to channel	± 500 V DC
Nondestructive to chassis (earth)	± 250 V DC

Analog to Digital Conversion	
Sample rate per channel	0.1 S/s to 200 kS/s
ADC resolution; one ADC per channel	16 bit
ADC Type	Successive Approximation Register (SAR); TI ADS8401IB
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; when calculating FFTs results in rounded/integer BIN sizes
Maximum binary sample rate	204.8 kS/s
External time base sample rate	0 S/s to 200 kS/s
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ± 30 ppm

Anti-Alias Filters

Using different filter selections (Bessel IIR/FIR/etc.) or different filter bandwidths can result in phase mismatches between channels.

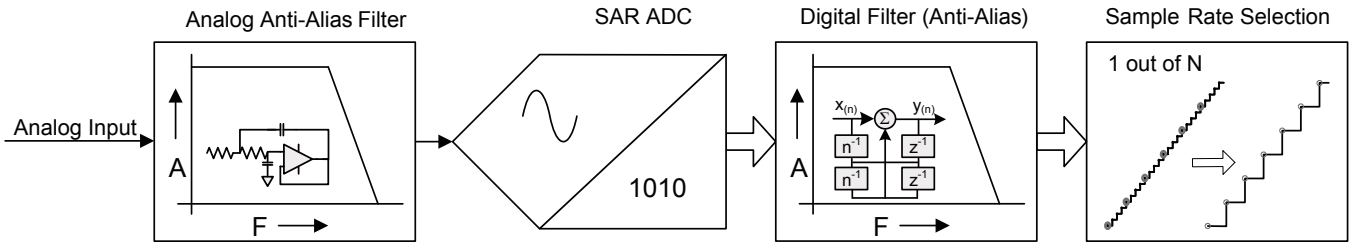
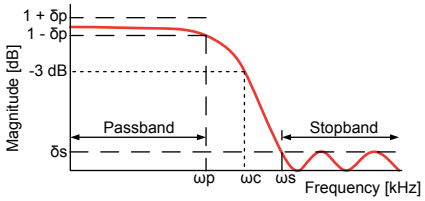


Figure O.37: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter in front of the Analog to Digital Converter (ADC). The ADC always samples at a fixed sample rate. The fixed sample rate of the ADC avoids the need for different analog anti-alias filter frequencies.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Digital Bessel IIR (Fc @ -3 dB)	When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter to prevent aliasing at lower sample rates. Bessel filters are typically used when looking at signals in the time domain. They are best used for measuring transient signals or sharp edge signals like square waves or step responses.
Digital FIR (Fc @ -0.1 dB)	Standard FIR filter with corner frequency (Fc) defined at -0.1 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.
Digital FIR (Fc @ -3 dB) Supported by Perception V6.40 and higher	Adapted FIR filter with corner frequency (Fc) calculated as close as possible to -3 dB. When FIR filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR filter to prevent aliasing at lower sample rates. This filter is best used when working in the frequency domain. When working in the time domain, this filter is best used for signals that are (close to) sine waves.

Bessel IIR Filter (Digital Anti-Alias)



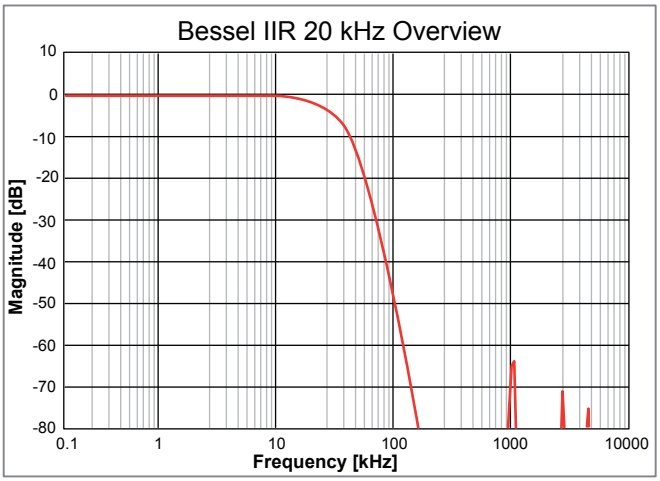
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.38: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of an analog Bessel anti-alias filter and a digital Bessel IIR filter.

Analog anti-aliasing filter bandwidth	220 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Bessel, optimal step response
Bessel IIR filter characteristic	6-pole Bessel style IIR
Bessel IIR filter user selection	Auto tracking for sample rate divided by: 10, 20, 40, 100 The user selects a division factor from the current sample rate; software then adjusts the filter when the sample rate is changed
Bessel IIR filter bandwidth (ωc)	Auto tracking the sample rate with the selected Bessel IIR filter; user selection from 0.0125 Hz to 20 kHz
Bessel IIR passband flatness (ωp)(1)	0.1 dB; DC to 3 kHz @ ωc = 20 kHz
Bessel IIR filter stopband attenuation (δs)	60 dB
Bessel IIR filter roll-off	36 dB/Octave



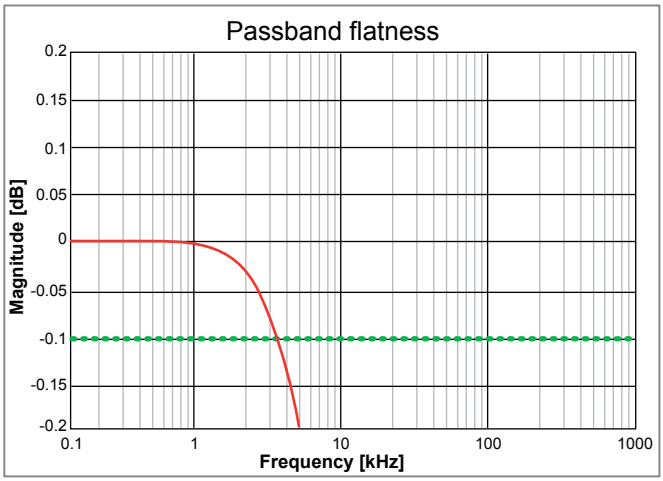
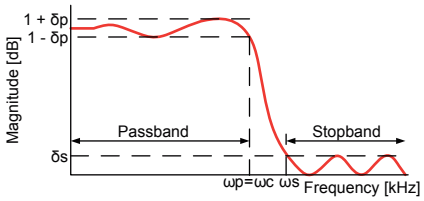


Figure O.39: Representative Bessel IIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -0.1 dB) Filter (Digital Anti-Alias)



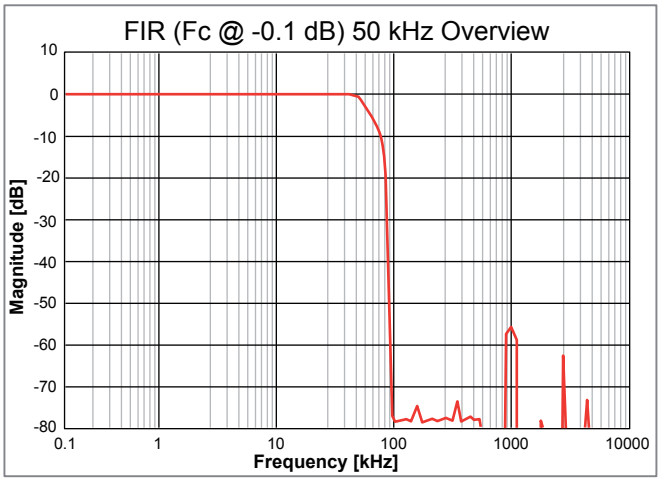
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.40: Digital FIR (Fc @ -0.1 dB) filter

When FIR (Fc @ -0.1 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -0.1 dB) filter.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -0.1 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -0.1 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40
FIR (Fc @ -0.1 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -0.1 dB) filter; user selection from 0.031 Hz to 50 kHz
FIR (Fc @ -0.1 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to filter bandwidth (ωc)
FIR (Fc @ -0.1 dB) filter stopband attenuation (δs)	60 dB
FIR (Fc @ -0.1 dB) filter roll-off	72 dB/Octave



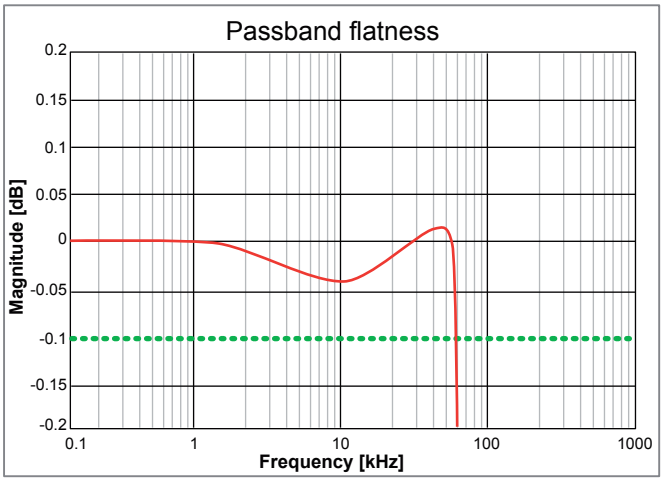
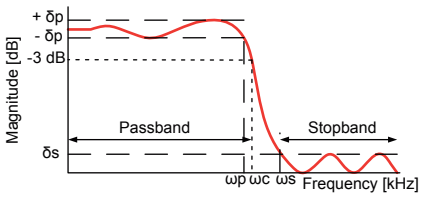


Figure O.41: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

FIR (Fc @ -3 dB) Filter (Digital Anti-Alias)



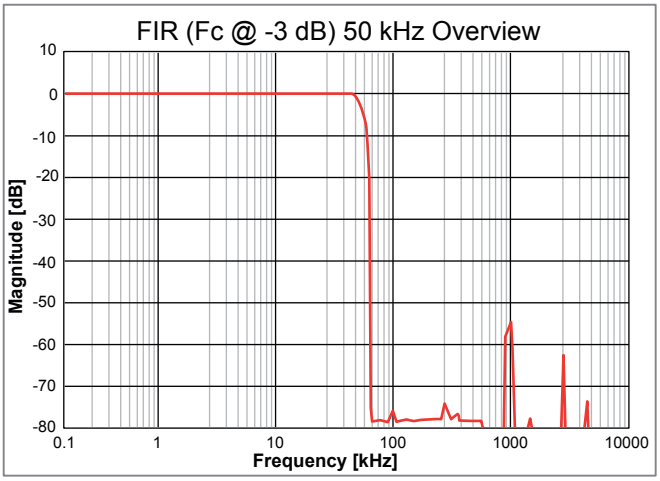
δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.42: Digital FIR (Fc @ -3 dB) filter

When FIR (Fc @ -3 dB) filter is selected, this is always a combination of an analog Butterworth anti-alias filter and a digital FIR (Fc @ -3 dB) filter. The FIR (Fc @ -3 dB) is an adapted FIR filter. Its ωp is reduced by a factor of ≈1.4 compared to the FIR (Fc @ -0.1 dB) filter. It is supported by Perception V6.40 and higher.

Analog anti-aliasing filter bandwidth	370 kHz ± 20 kHz (-3 dB)
Analog anti-aliasing filter characteristic	7-pole Butterworth, extended passband response
FIR (Fc @ -3 dB) filter characteristic	12-pole FIR; FIR is a purely digital characteristic. Its closest analog resemblance is to an Elliptic filter. However, FIR has both overshoot and pre-shoot on the step response. This means that the ringing on the signal starts before the step input is started and that the ringing continues after the step input is complete.
FIR (Fc @ -3 dB) filter user selection	Auto tracking for sample rate divided by: 4, 10, 20, 40
FIR (Fc @ -3 dB) filter bandwidth (ωc)	Auto tracking the sample rate with the selected FIR (Fc @ -3 dB) filter; user selection from 0.031 Hz to 50 kHz
FIR (Fc @ -3 dB) filter passband flatness (ωp) (1)	0.1 dB; DC to ≈ωc/1.4 (Adapted FIR filter behavior)
FIR (Fc @ -3 dB) filter stopband attenuation (δs)	60 dB
FIR (Fc @ -3 dB) filter roll-off	72 dB/Octave



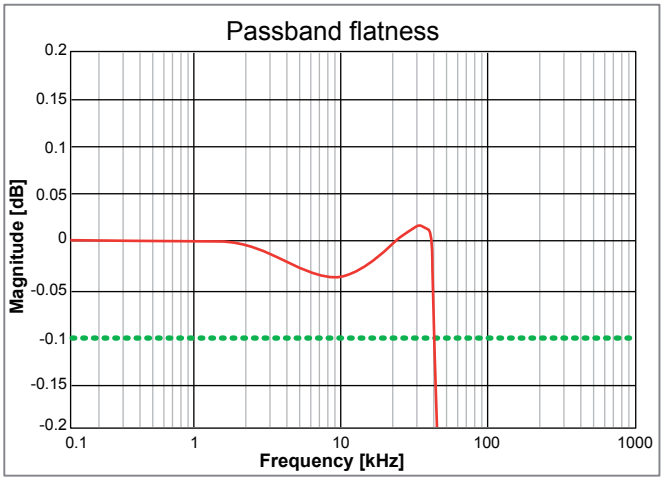


Figure O.43: Representative FIR examples

(1) Measured using a Fluke 5700 calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Bessel IIR/FIR/etc.) or different filter bandwidths results in phase mismatches between channels.	
Bessel IIR (Fc @ -3 dB), 20 kHz Filter frequency; 10 kHz sine wave	
Channels on card	0.4 deg (0.1 µs)
GN814 Channels within mainframe	0.4 deg (0.1 µs)
FIR (Fc@ -0.1dB) and FIR (Fc @ -3 dB), 50 kHz Filter frequency; 10 kHz sine wave	
Channels on card	0.4 deg (0.1 µs)
GN814 Channels within mainframe	0.4 deg (0.1 µs)
GN814 Channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	128 MB (64 MS)
Organization	Automatic distribution amongst enabled channels
Memory diagnostics	Automatic memory test when system is powered on but not recording
Storage sample size	16 bits, 2 bytes/sample

Digital Events/Timer/Counter	
Digital event inputs	Not supported
Digital event outputs	Not supported
Timer/Counter	Not supported

Triggering	
Channel trigger/qualifier	1 per channel; fully independent per channel, software selectable either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Maximum trigger rate	400 triggers per second
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Active edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Delay	± 1 µs + maximum 1 sample period (for decimal and binary time base)
Send to External Trigger Out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Active level	High/Low/Hold High; selectable per mainframe, identical for all cards
Pulse width	High/Low: 12.8 µs Hold high: Active from first mainframe trigger to end of recording Pulse width created by mainframe
Delay	516 µs ± 1 µs + maximum 1 sample period using decimal time base 504 µs ± 1 µs + maximum 1 sample period using binary time base
Cross channel triggering	
Channels on card	Logical OR; Analog triggers of all channels Logical AND; Qualifiers of all channels
Cards in mainframe	User selectable through system trigger bus Selections: Send/Receive/Transceive (Send & Receive)
System trigger bus	
Connections	3 System trigger busses connecting all cards within mainframe 1 Master/Slave bus connecting all cards within mainframe and connecting all mainframes when using Master/Slave option
Operation	Logical OR of all triggers of all cards Logical AND of all qualifiers of all cards
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; Single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Pulse detect/reject	Disable/Detect/Reject software selectable. Maximum pulse width 65 535 samples
dY/dT conversion	dY: 16 bit (0.0015%) for both levels dT: 1 to 1023 samples. dT setting shared for both levels
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; Two individual levels, OR-ed
Window	Arm/trigger and a disarm level; Trigger on peak level changes in a uni-polar signal
Dual Window	Arm/trigger/disarm per level; Trigger on peak level changes in a bi-polar signal
Sequential	One arm and one trigger level; eliminate false triggering due to noise or hysteresis
Analog channel qualifier modes	
Basic	Above or below level check. Enable/disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/disable trigger with dual level
Trigger hold off	Disable channel trigger for 1 to 65 535 samples after trigger detected Maximum hold off time depends on sample rate

Triggering	
Interval timer	
Modes	Less than, trigger when rate is too low More than, trigger when rate is too high Between, trigger when rate between lower and upper limit Not between, trigger when rate is not between lower and upper limit
Interval timers	Start timer and width Timer
Timer value	1 to 65 535 samples
Event counter	Counts channel trigger events before card trigger is activated 1 to 256 trigger events

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

	Single Sweep Multiple Sweeps Slow-Fast Sweep			Continuous			Dual Rate		
	Enabled channels			Enabled channels			Enabled channels		
	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch	1 Ch	2 Ch	8 Ch
Max. sweep memory	60 MS	30 MS	7.5 MS	not used			48 MS	24 MS	6 MS
Max. sweep sample rate	200 kS/s			not used			200 kS/s		
Max. continuous FIFO	not used			60 MS	30 MS	7.5 MS	12 MS	6 MS	1.5 MS
Max. continuous sample rate	not used			200 kS/s			Sweep sample rate / 2 Maximum 50 kS/s		
Max. aggregate continuous streaming rate	not used			0.2 MS/s 0.4 MB/s	0.4 MS/s 0.8 MB/s	1.6 MS/s 3.2 MB/s	0.05 MS/s 0.1 MB/s	0.1 MS/s 0.2 MB/s	0.8 MS/s 1.6 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two or 50 kS/s per channel, whichever is the smallest sample rate
Maximum sample rate switches	400 sample rate switches per second, 200 000 switches maximum, switching stops when sweep ends

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

O.6 B3240-3.1 en (GEN series GN1610)

Capabilities Overview	
Model	GN1610/GN3210
Maximum sample rate per channel	250 kS/s
Memory per card	2 GB
Analog channels	16/32
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16/24 bit
Isolation	Not supported
Input type	Analog balanced differential
Passive voltage/current probes	Passive, single-ended voltage probes Passive, differential matched voltage probes
Sensors	IEPE and charge
TEDS	Class 1, IEPE sensors
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	16 digital events and 2 Timer/Counter channels
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

Block diagram

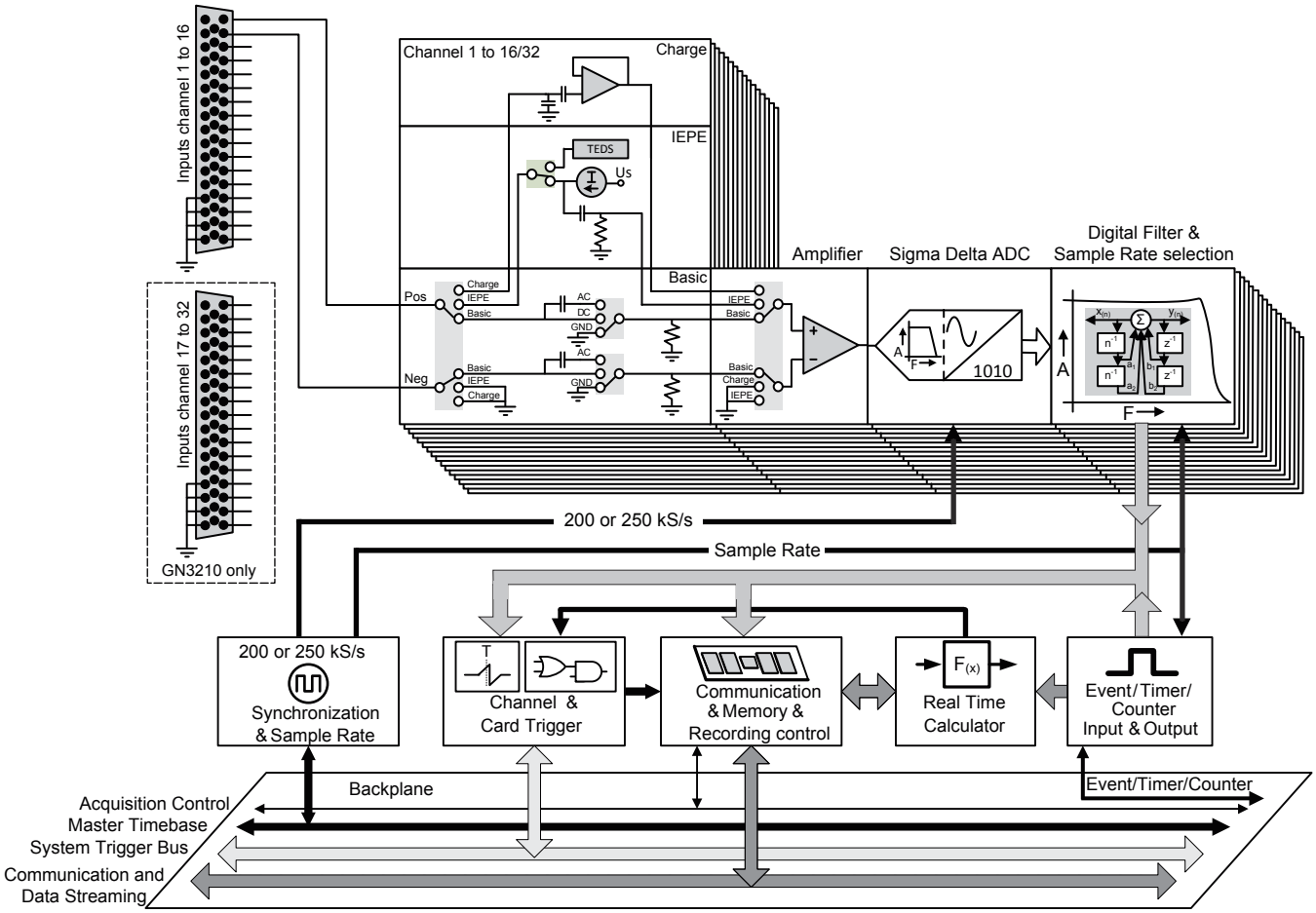


Figure O.44: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	16
Connectors	D-Sub (DD-50) connector
Input type	Analog isolated balanced differential
Input coupling	Differential, single-ended (positive or negative)
Signal input coupling	
Coupling modes	AC, DC, GND
AC coupling frequency	1.6 Hz ± 10%; - 3 dB

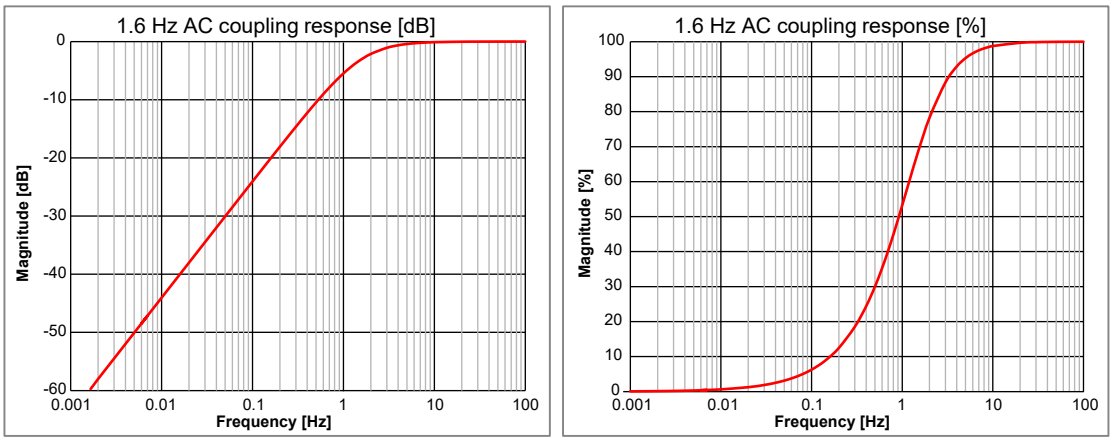


Figure O.45: Representative AC coupling response

Impedance	2 x 1 MΩ ± 0.5% // 75 pF ± 15%
Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Offset	± 50% in 1000 steps (0.1%); ± 20 V range has fixed 0% offset
DC Offset error	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV
Offset error drift	±(10 ppm + 2 µV)/°C (±(6 ppm + 1.5 µV)/°F)
DC Gain error	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
Gain error drift	± 10 ppm/°C (± 6 ppm/°F)
Maximum static error (MSE)	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
RMS Noise (50 Ω terminated)	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV

Analog Input Section

Common mode (referred to system ground)		
Ranges	Less than ± 2 V	Larger than or equal to ± 2 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	2 V RMS	33 V RMS

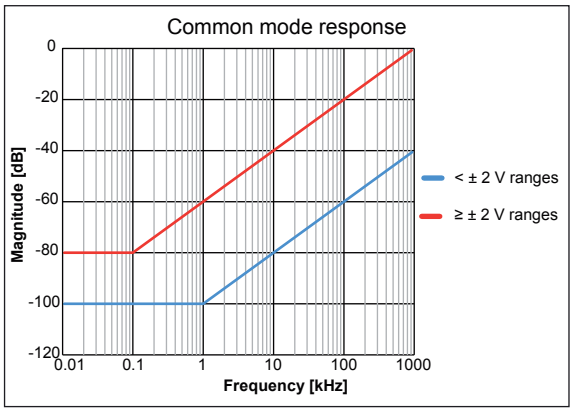


Figure O.46: Representative common mode response

Input overload protection	
Over voltage impedance change	The activation of the over voltage protection system will result in a reduced input impedance. The over voltage protection will not be active as long as the input voltage is less than 200% of the selected input range or 50 V DC whichever is the smallest value.
Maximum nondestructive voltage	± 50 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

Input Ranges When Using Passive Voltage Probes

Detailed probe specifications can be found at the end of this datasheet

Single-ended	**Added voltage ranges**
G901 (10:1 divider)	± 100 V, ± 200 V
G902 (10:1 divider)	± 100 V, ± 200 V
G903 (100:1 divider)	± 100 V, ± 200 V, ± 500 V, ± 1 kV
G904 (100:1 divider)	± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV
G906 (1000:1 divider)	± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV, ± 5 kV, ± 10 kV (± 20 kV @ Dc to 60 Hz)
Differential matched	**Added voltage ranges**
G907 (10:1 divider)	± 100 V, ± 200 V

Input Ranges When Using Current Clamps

Detailed probe specifications can be found at the end of this datasheet

Clamp type	**Added current ranges**
G912 (AC/DC)	± 30 mA to ± 30 A DC ± 30 mA to ± 20 A RMS
G913 (AC)	± 100 mA to ± 1000 A RMS
G914 (xx)	± xxx mA to ± xxx A RMS

IEPE Sensor	
In IEPE mode the negative input of each channel is internally grounded. Best measurement results can be obtained if the negative input pin of each channel is used for the coaxial ground/shield. The return current then flows straight to the channel ground and not to the common card ground.	
Input ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Over voltage protection	- 1 V to 22 V DC
IEPE gain error	0.1% of Full Scale ± 300 µV
IEPE gain error drift	± 10 ppm/°C (± 6 ppm/°F)
IEPE compliance voltage	≥ 22 V
Excitation current	2, 4, 6, 8 mA, software selectable
Excitation current accuracy	± 5%
Coupling time constant	1.5 s
Lower bandwidth	-3 dB @ 0.11 Hz
Maximum cable length	100 m (RG-58)
Wire diagnostics	Open and shorted IEPE wiring detected (Requires Perception V7.00 or higher)
TEDS support	Class 1, including software selectable auto detect the presence of an attached sensor

Charge Amplifier	
In charge mode the negative input of each channel is internally grounded. Best measurement results can be obtained if the negative input pin of each channel is used for the coaxial ground/shield. The return current then flows straight to the channel ground and not to the common card ground.	
Input ranges	± 10 pC, ± 20 pC, ± 50 pC, ± 100 pC, ± 200 pC, ± 0.5 nC, ± 1 nC, ± 2 nC
Over voltage protection	± 20 V DC
Charge gain error	± 2% of Full Scale
Charge gain error drift	± 30 ppm/°C (± 17 ppm/°F)
-3 dB high pass bandwidth limit	1 Hz
-3 dB low pass bandwidth limit	33 kHz ± 10% when a 650 pF source capacity is used 106 kHz ± 10% when a 250 pF source capacity is used
TEDS support	No

Analog to Digital Conversion	
Sample rate; per channel	1 S/s to 250 kS/s
ADC resolution; one ADC per channel	24 bit
ADC type	Sigma Delta (Σ-Δ) ADC; Analog Devices AD7764BRUZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; produces rounded BIN values when calculating FFT's
Maximum binary sample rate	256 kS/s
External time base frequency	0 S/s to 25 kS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ±30 ppm.

Anti-Alias Filters

Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths can lead to phase mismatches between channels.

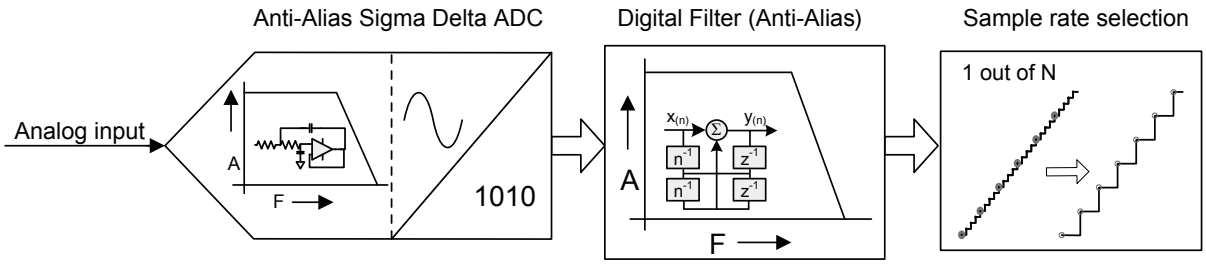


Figure O.47: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter integrated inside the Sigma Delta Analog to Digital Converter (ADC) always sampling at a fixed sample rate. This setup avoids the need for other analog anti-alias filters.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Sigma Delta Wideband	When Sigma Delta wideband is selected the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) is always in the signal path. Therefore, the anti-alias protection is always active when Sigma Delta wideband is selected.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Bessel IIR filter. Bessel filters are typically used when looking at signals in the time domain. Best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Butterworth IIR filter. Best used when working in the frequency domain. When working in the time domain this filter is best used for signals that are (close to) sine waves.
Elliptic IIR	When Elliptic IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter. Best used when working in the frequency domain. When working in the time domain this filter is best used for signals that are (close to) sine waves.
Elliptic Bandpass IIR	When Elliptic Bandpass IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic Bandpass IIR filter. Best used when working in the frequency domain. When working in the time domain this filter is best used for signals that are (close to) sine waves.

Sigma Delta Wideband (Analog Anti-Alias)

When Sigma Delta wideband is selected there is always the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) in the signal path. Therefore there is always anti-alias protection when wideband is selected. Care must be taken as this filter introduces slight overshoots on square wave or pulse response signals. Signals of sine wave type will not be effected.

Wideband

Characteristic	Sigma delta, optimal frequency response
-3 dB Bandwidth	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
0.1 dB passband flatness(1)	DC to 20 kHz

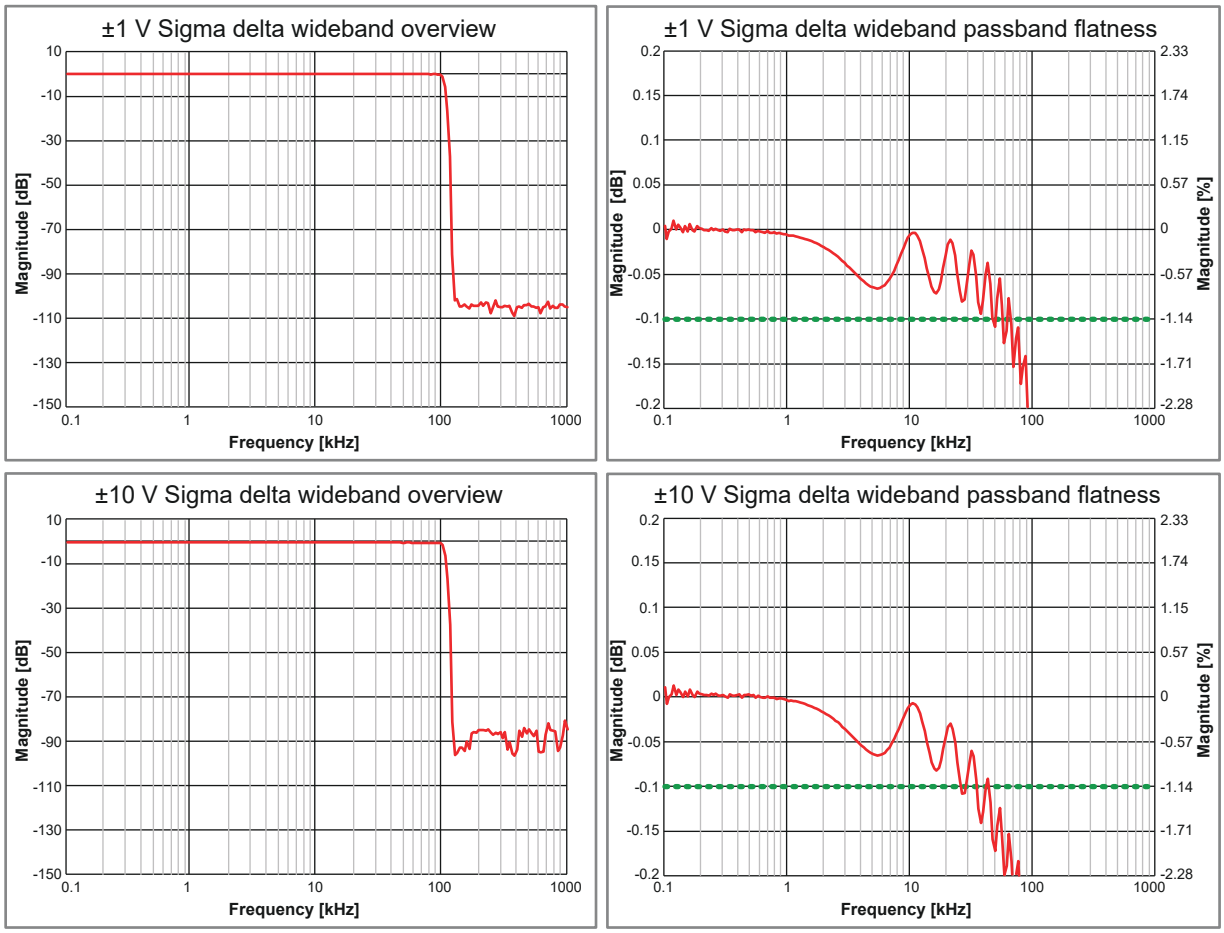
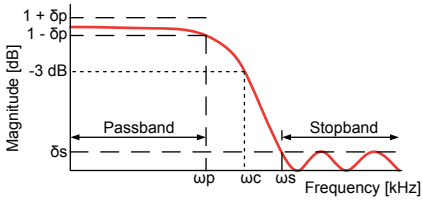


Figure O.48: Representative Sigma Delta Wideband examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.49: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Bessel IIR filter

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth (ωlc)	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Bessel IIR Filter	
Characteristic	12-pole Bessel style IIR 8-pole Bessel style IIR filter frequencies ωc = 25 kHz and ωc = 12.5 kHz
User selection	Auto tracking to sample rate divided by: 10, 20, 40, 100 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	User selectable from 40 Hz to 25 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/10
Stopband attenuation (δs)	80 dB
Roll-off	72 dB/octave for 12-pole filters; 48 dB/octave for 8-pole filters

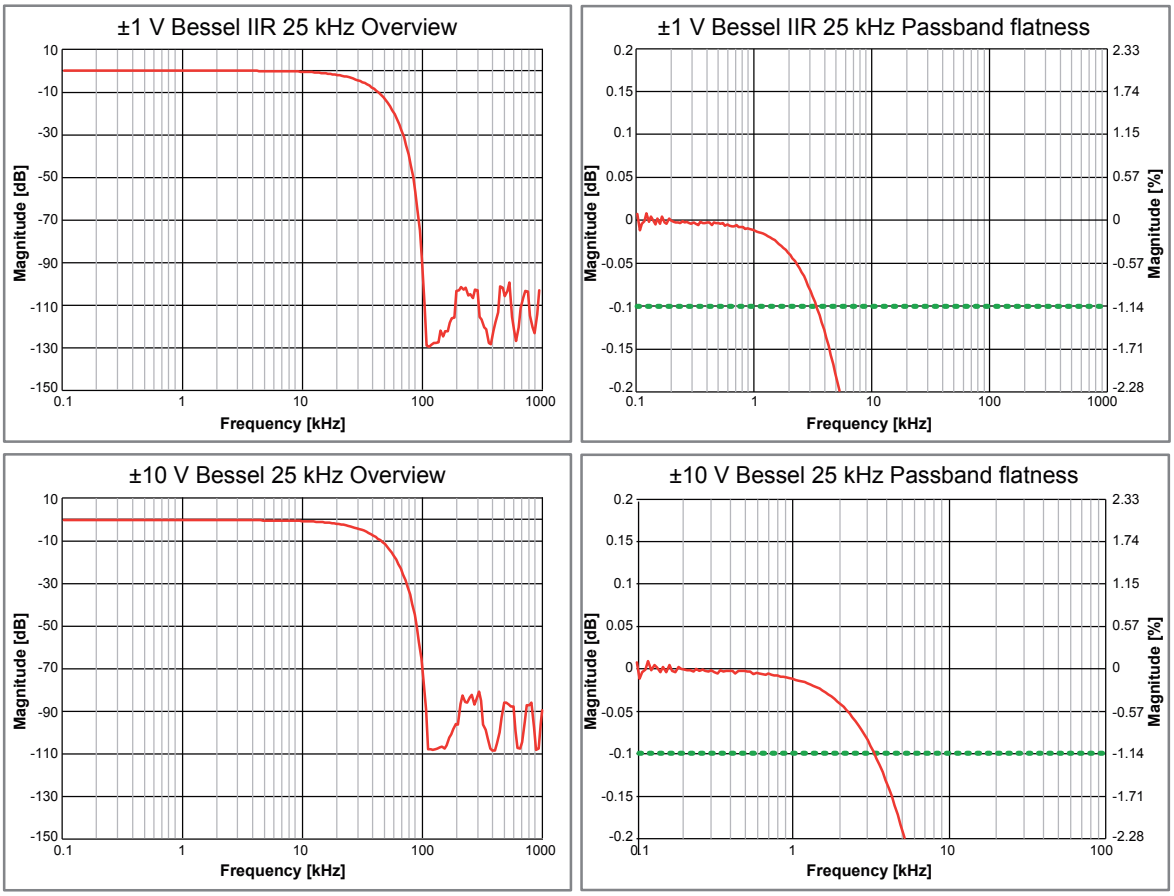
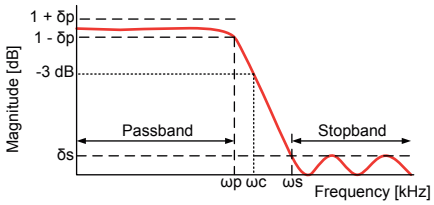


Figure O.50: Representative Bessel IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.51: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Butterworth IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth (ωlc)	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Butterworth IIR Filter	
Characteristic	12-pole Butterworth style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed.
Bandwidth (ωc)	User selectable from 100 Hz to 62.5 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/2 or maximum 10 kHz
Stopband attenuation (δs)	80 dB
Filter roll-off	72 dB/octave

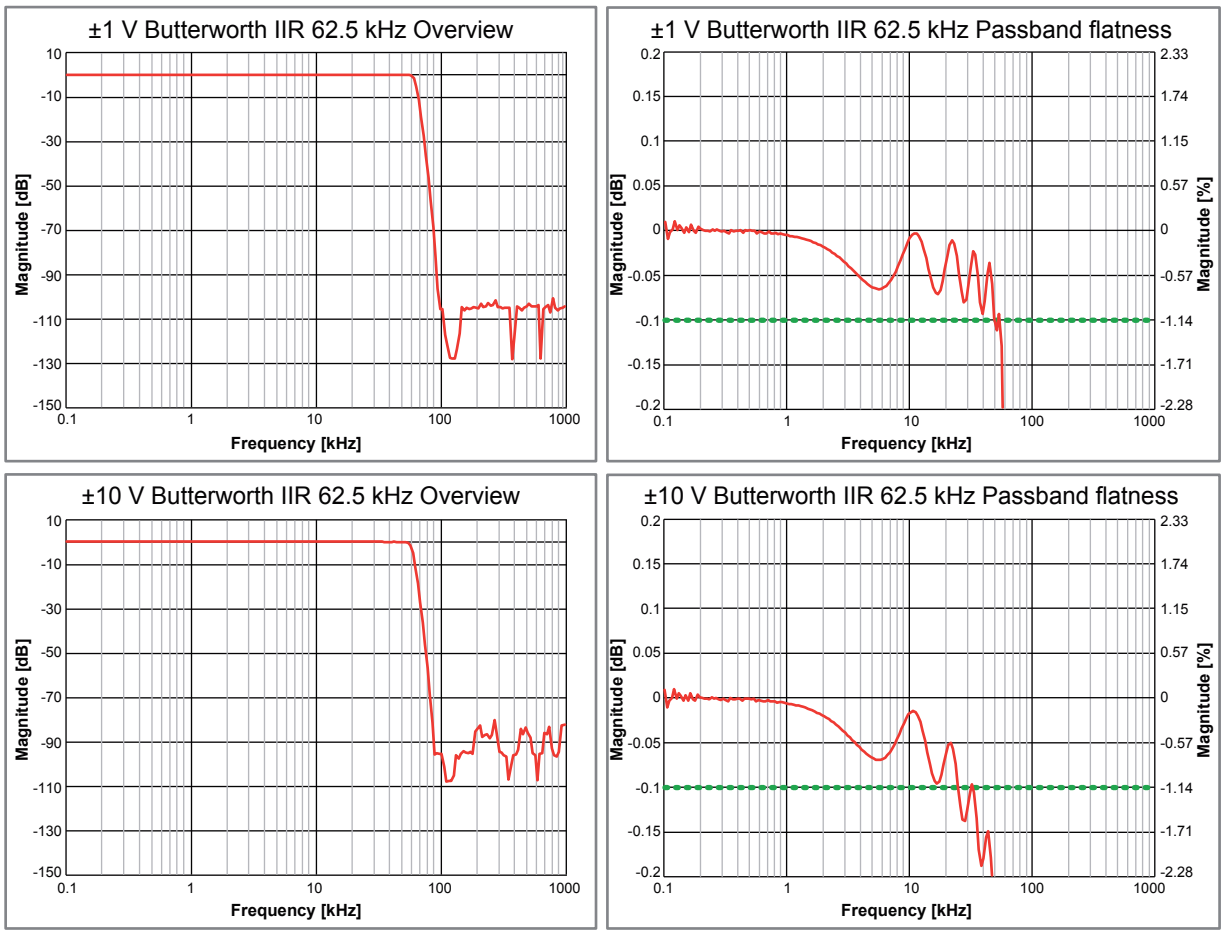
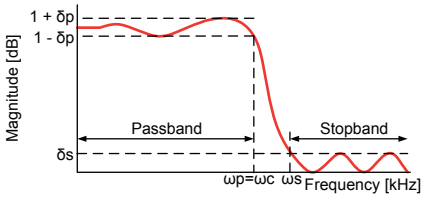


Figure O.52: Representative Butterworth IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.53: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth (ωlc)	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Elliptic IIR Filter	
Characteristic	11th order Elliptic style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	100 Hz to 62.5 kHz
Stopband frequency (ωs)	Approximately 1.25 * ωc
0.1 dB passband flatness (ωp)(1)	DC to ωc/1.5 or maximum 10 kHz
Stopband attenuation (δs)	80 dB

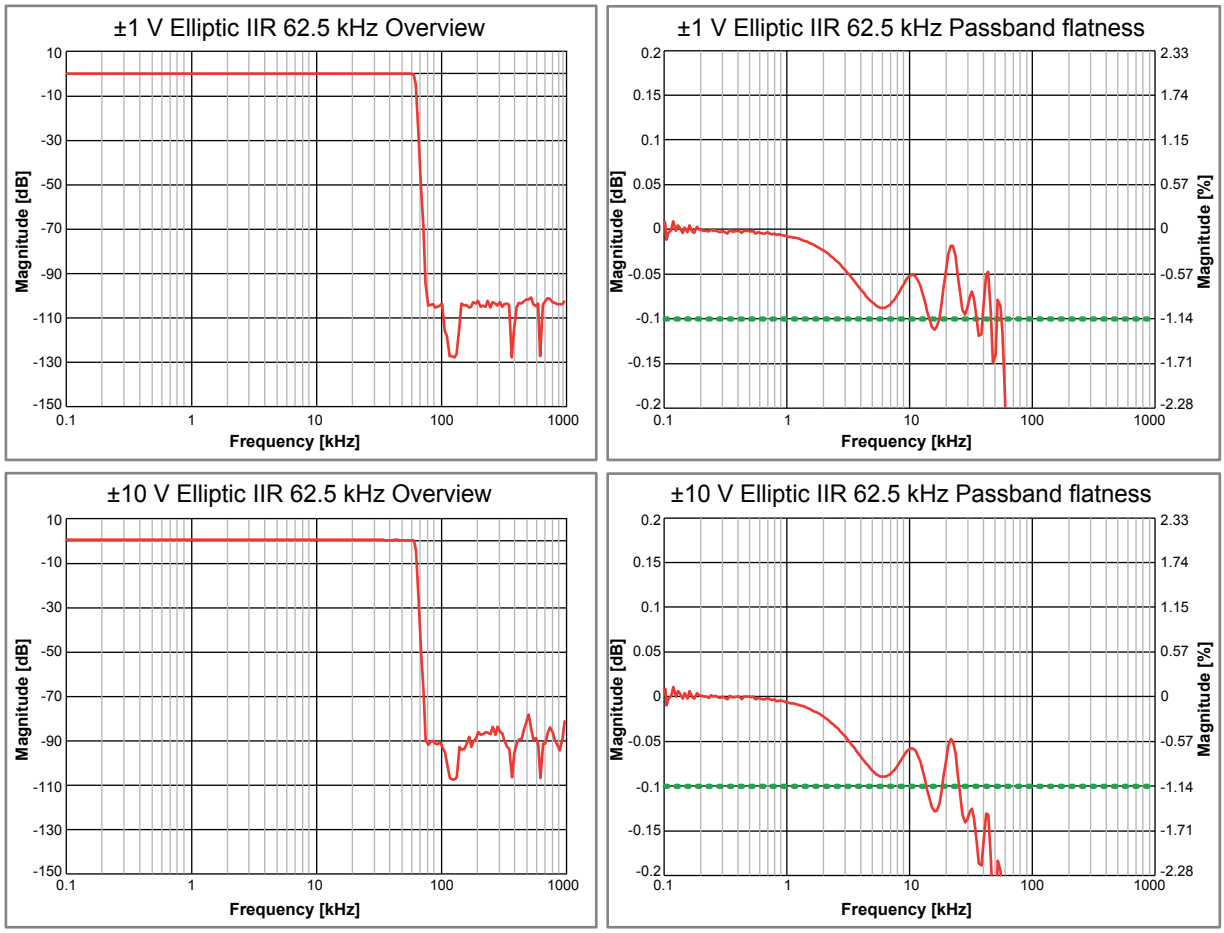
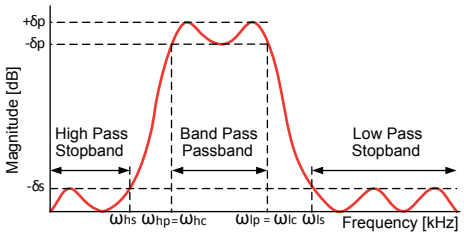


Figure O.54: Representative Elliptic IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Elliptic IIR Bandpass Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.55: Digital Elliptic IIR Bandpass Filter

When Elliptic IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
-3 dB low pass bandwidth (ωlc)	100 kHz ± 5 kHz for sample rates 250 kS/s and 125 kS/s 80 kHz ± 5 kHz for all other sample rates
Elliptic IIR bandpass filter	
Characteristic	14th order Elliptic style IIR
User selection	Two fixed high pass frequencies to be combined with four fixed low pass frequencies
High pass bandwidth (ωhc)	40 Hz and 100 Hz
High pass stopband frequency (ωhs)	Approximately ωhc / 2.5
Low pass bandwidth (ωlc)	2 kHz, 20 kHz, 40 kHz and 50 kHz
Low pass stopband frequency (ωs)	Approximately 1.5 to 2.5 * ωc
0.1 dB passband flatness (ωp)(1)	ωhc to ωlc or maximum 10 kHz
Stopband attenuation (δs)	80 dB

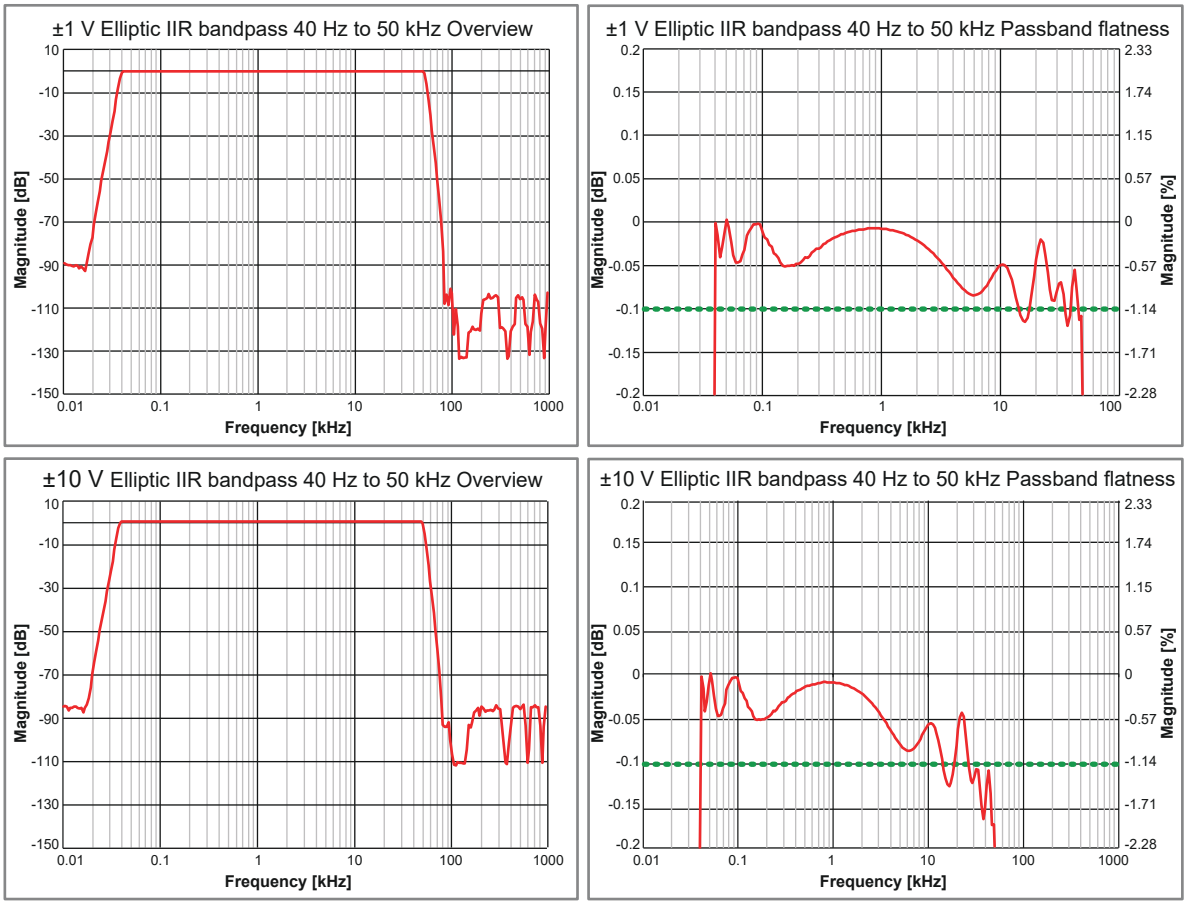


Figure O.56: Representative Elliptic IIR bandpass examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths will lead to phase mismatches between channels.	
Wideband	10 kHz Sine wave
Channels on card	0.5 deg (14 ns)
GN1610 Channels within mainframe	0.5 deg (14 ns)
Bessel IIR, Filter frequency 200 kHz @ 2 MS/s	
Channels on card	0.5 deg (14 ns)
GN1610 Channels within mainframe	0.5 deg (14 ns)
Butterworth IIR, Filter frequency 200 kHz @ 2 MS/s	
Channels on card	0.5 deg (14 ns)
GN1610 Channels within mainframe	0.5 deg (14 ns)
Elliptic IIR, Filter frequency 200 kHz @ 2 MS/s	
Channels on card	0.5 deg (14 ns)
GN1610 Channels within mainframe	0.5 deg (14 ns)
GN1610 channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	2 GB (1 GSample @ 16 Bits Storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered and not recording
Storage sample size	16 bits, 2 bytes/sample 24 bits, 4 bytes/sample (required for Timer/Counter usage)

Digital Event/Timer/Counter[1]	
The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.	
Digital input events	16 per card
Levels	TTL input level, user programmable invert level
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs
Overvoltage protection	± 30 V DC continuously
Minimum pulse width	100 ns
Maximum frequency	5 MHz
Digital output events	2 per card
Levels	TTL output levels, short circuit protected
Output event 1	User selectable: Trigger, Alarm, set High or Low
Output event 2	User selectable: Recording active, set High or Low
Digital output event user selections	
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay
Alarm	High when alarm condition is activated, low when not activated (alarm conditions of this card only) 200 µs ± 1 µs ± 1 sample period alarm event delay
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation
Timer/Counter	2 per card; only available in 32 bit storage mode
Levels	TTL input levels
Inputs	All pins are shared with digital event inputs
Timer-Counter modes	Uni- and bi-directional count Bi-directional quadrature count Uni- and bi-directional frequency/RPM measurement

(1) Only if supported by mainframe

Timer/Counter Mode Uni- and Bi-directional Count

Counter mode is typically used for tracking movement of device under test. When possible use the quadrature modes as these are less sensitive to counting errors.

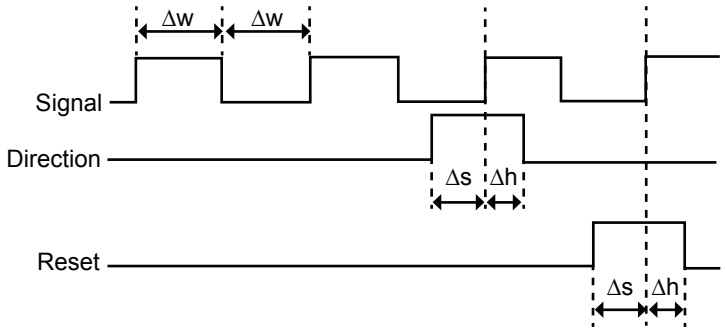


Figure O.57: Uni- and Bi-directional count timing

Inputs	3 pins: signal, reset and direction (only used in bi-directional count)
Maximum input frequency	5 MHz
Minimum pulse width (Δw)	100 ns
Counter range	0 to 2^{31}; uni-directional count -2^{31} to $+2^{31} - 1$; bi-directional count
Gate measuring time	Sample period (1 / sample rate) to 50 s Can be selected by user to control update rate independent of sample rate
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.
Direction input	
Input Level sensitivity	Only used when in bi-directional count Low: increment counter High: decrement counter
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Timer/Counter Mode Bi-directional Quadrature Count

Typically used for tracking rotating/moving devices using a decoder with two signals that are always 90 degree phase shifted. E.g. allow for direct interfacing to HBM torque and speed transducers.

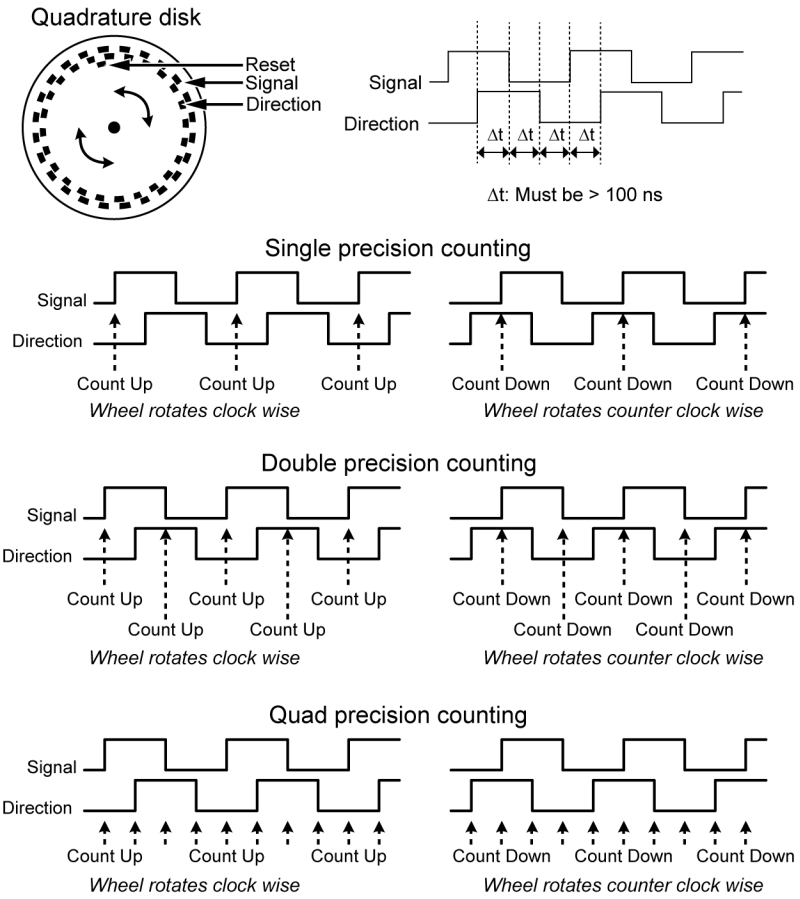


Figure O.58: Bi-directional quadrature count modes

Inputs	3 pins: signal, direction and reset
Maximum input frequency	2 MHz
Minimum pulse width	200 ns (2 * Δt)
Minimum setup time	100 ns (Δt)
Minimum hold time	100 ns (Δt)
Accuracy	Single, dual or quad precision
Counter range	-2^{31} to $+2^{31} - 1$
Reset input	
Level sensitivity	User selectable invert level
Minimum setup time prior to signal edge (Δt)	100 ns
Minimum hold time after signal edge (Δt)	100 ns
Reset options	
Manual	Upon user request by software command
Start recording	Count value set to 0 at Start of recording
First reset pulse	After the recording is started, the first reset pulse sets the counter value to 0. The next reset pulses are ignored.
Each reset pulse	On each external reset pulse, the counter value is reset to 0.

Timer/Counter Mode: Uni- and Bi-directional Frequency/RPM Measurement

Used to measure any kind of frequency like engine RPM, or active sensors with proportional frequency output signal.

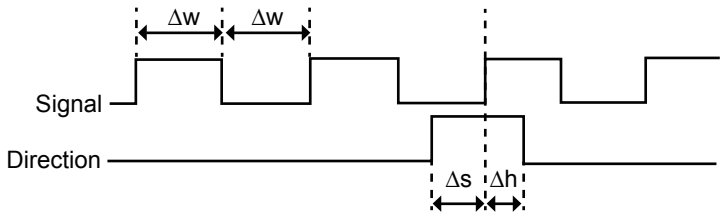


Figure O.59: Uni- and Bi-directional count timing

Inputs	2 pins: signal, direction
Maximum input frequency	5 MHz
Minimum pulse width (Δw)	100 ns
Accuracy	0.1%, when using a gate measuring time of 40 µs or more. With lower gate measuring times, the real-time calculators or Perception formula database can be used to enlarge the measuring time and improve the accuracy more dynamically e.g. based on measured cycles.
Gate measuring time	Sample period (1 / sample rate) to 50 s Can be selected by user to control update rate independent of sample rate
Direction input	
Level sensitivity	Only used when in bi-directional frequency/RPM mode Low: Positive frequency/RPM, e.g. left rotations High: Negative frequency/RPM, e.g. right rotations
Minimum setup time prior to signal edge (Δs)	100 ns
Minimum hold time after signal edge (Δh)	100 ns

Triggering	
Channel trigger/qualifier	1 fully independent per channel either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Trigger rate	400 triggers per second
Delayed trigger	Maximum 1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger in edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger in delay	± 1 µs + maximum 1 sample period (Identical for decimal and binary time base)
Send to external trigger out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; see mainframe datasheet for details
Trigger out delay	Selectable (180 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (176 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516(504) µs for decimal (binary) time base, to be compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Channels on card	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Cards in mainframe	User selectable through system trigger bus Selections: Send/Receive/Transceive (Send & Receive)
System trigger bus	
Connections	3 System trigger busses connecting all cards within mainframe 1 Master/Slave bus connecting all cards within mainframe and connecting all mainframes using Master/Slave option
Operation	Logical OR of all triggers of all cards Logical AND of all qualifiers of all cards
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger (1)	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

(1) Only if supported by mainframe

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators (Perception V6.70 and higher)

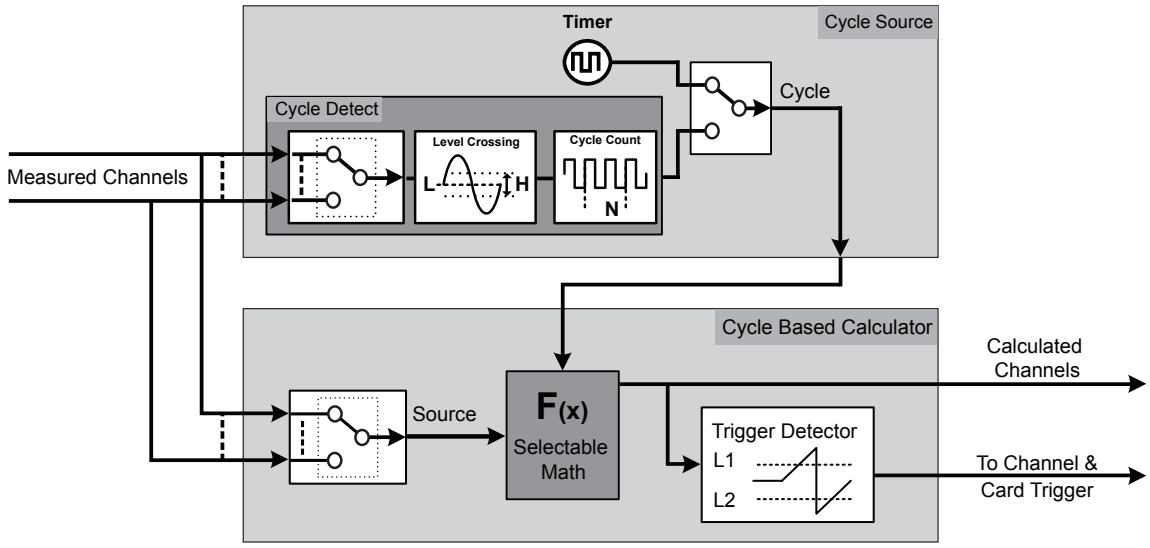


Figure O.60: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased.
Cycle based calculator	
Number of calculators	32; at sample rates 200 kS/s or lower. At higher sample rates, the number of calculators is reduced to match the available DSP power.
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software.
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and MeanOfMultiplication
Timer/Counter channel calculations	Frequency (to enable triggering). RPM of Angle.
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period.
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level.
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms.

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Acquisition Modes	
Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

Recording Mode Details (16 Bit storage)

	Single Sweep Multiple Sweeps Slow-Fast Sweep		**Continuous**		**Dual Rate**	
	Enabled Channels		Enabled Channels		Enabled Channels	
	1 Ch	16 Ch	1 Ch	16 Ch	1 Ch	16 Ch
Max. sweep memory	1000 MS	62.5 MS	not used		800 MS	50 MS
Max. sweep sample rate	250 kS/s		not used		250 kS/s	
Max. continuous FIFO	not used		1000 MS	62 MS	200 MS	12.5 MS
Max. continuous sample rate	not used		250 kS/s		Sweep Sample Rate / 2	
Max. aggregate continuous streaming rate	not used		0.25 MS/s 0.5 MB/s	4.0 MS/s 8.0 MB/s	0.25 MS/s 0.5 MB/s	4.0 MS/s 8.0 MB/s

Recording Mode Details (24 Bit storage)

	Single Sweep		**Continuous**		**Dual Rate**	
	Enabled Channels		Enabled Channels		Enabled Channels	
	1 Ch	16 Ch	1 Ch	16 Ch	1 Ch	16 Ch
Max. sweep memory	500 MS	31 MS	not used		400 MS	25 MS
Max. sweep sample rate	250 kS/s		not used		250 kS/s	
Max. continuous FIFO	not used		500 MS	31 MS	100 MS	6 MS
Max. continuous sample rate	not used		250 kS/s		Sweep Sample Rate / 2	
Max. aggregate continuous streaming rate	not used		0.2 MS/s 1.0 MB/s	8.0 MS/s 16.0 MB/s	0.2 MS/s 1.0 MB/s	8.0 MS/s 16.0 MB/s

Single Sweep	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of Sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two
Maximum fast sample rate switches	20, sample rate switching always stops when sweep ends
Minimum time between sample rate switches	2.5 ms

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Connector Pin Assignment

Connector type	tbd
Mating connector type	tbd
Output voltage	5 V ± 20%
Output current	0.3 A maximum (all output pins internally connected)

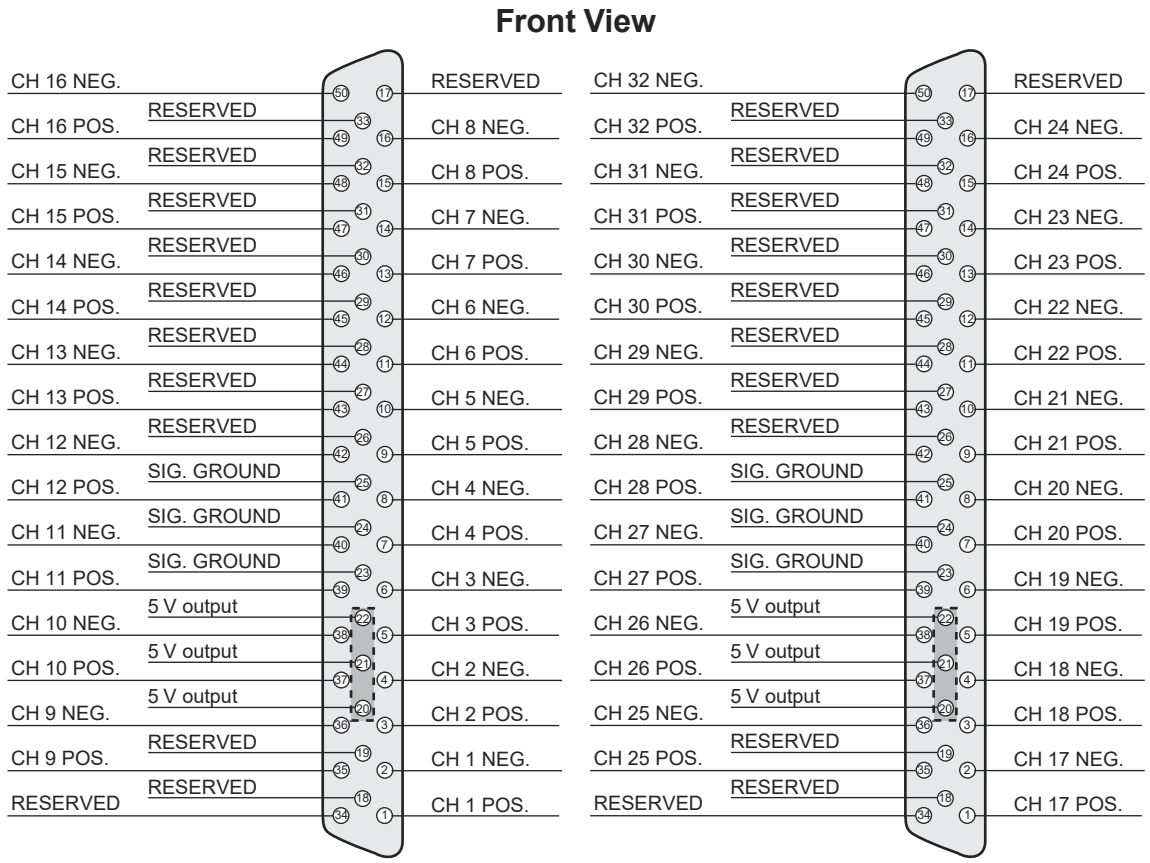


Figure O.61: Input connector pin diagram (Front view)

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives	
Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

O.7 B3264-3.1 en (GEN series GN1611)

Capabilities Overview	
Model	GN1611
Maximum sample rate per channel	20 kS/s
Memory per card	200 MB
Analog channels	32
Anti-alias filters	Fixed bandwidth analog AA-filter combined with sample rate tracking digital AA-filter
ADC resolution	16/24 bit
Isolation	Not supported
Input type	Analog balanced differential
Passive voltage/current probes	Passive, single-ended voltage probes Passive, differential matched voltage probes
Sensors	Not supported
TEDS	Not supported
Real-time cycle based calculators	32; Cycle and Timer based calculations with triggering on calculated results
Real-time formula database calculators (option)	Not supported
EtherCat® output	Not supported
Digital Event/Timer/Counter	16 digital events
Standard data streaming (up to 200 MB/s)	Supported
Fast data streaming (up to 1 GB/s)	Not supported
Slot width	1

Block diagram

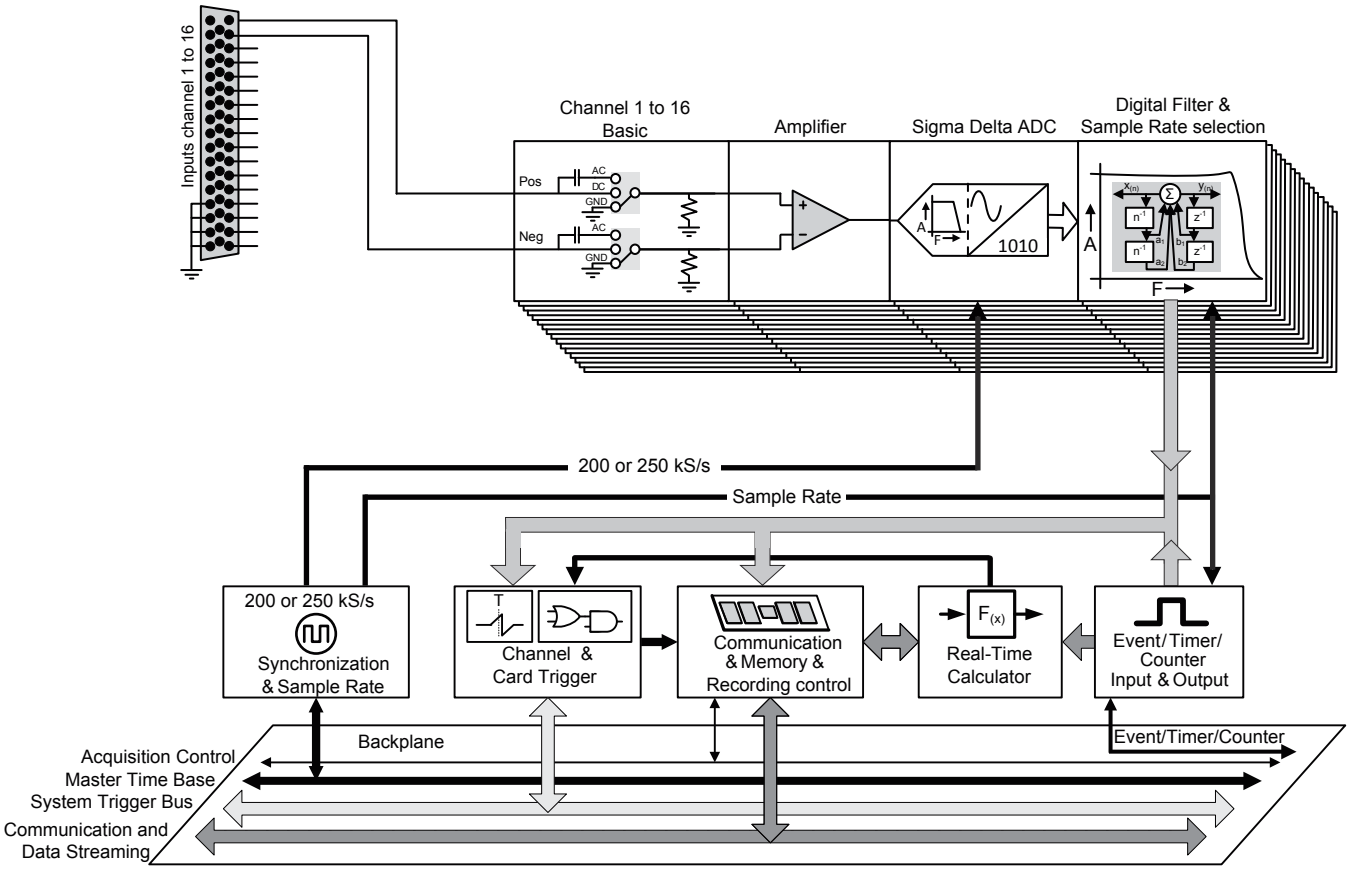


Figure O.62: Block diagram

Note *The specifications listed are valid for cards that have been calibrated and are used in the same mainframe and slots as they were at the time of calibration. When the card is removed from its original location and placed in another slot and/or mainframe, the Offset error, Gain error and MSE specifications are expected to increase (up to double the original specification) due to thermal differences within the configurations. All specifications are defined at 23 °C ± 2 °C, unless specified differently.*

Analog Input Section	
Channels	16
Connectors	D-Sub (DD-50) connector
Input type	Analog isolated balanced differential
Input coupling	Differential, single-ended (positive or negative)
Signal input coupling	
Coupling modes	AC, DC, GND
AC coupling frequency	1.6 Hz ± 10%; - 3 dB

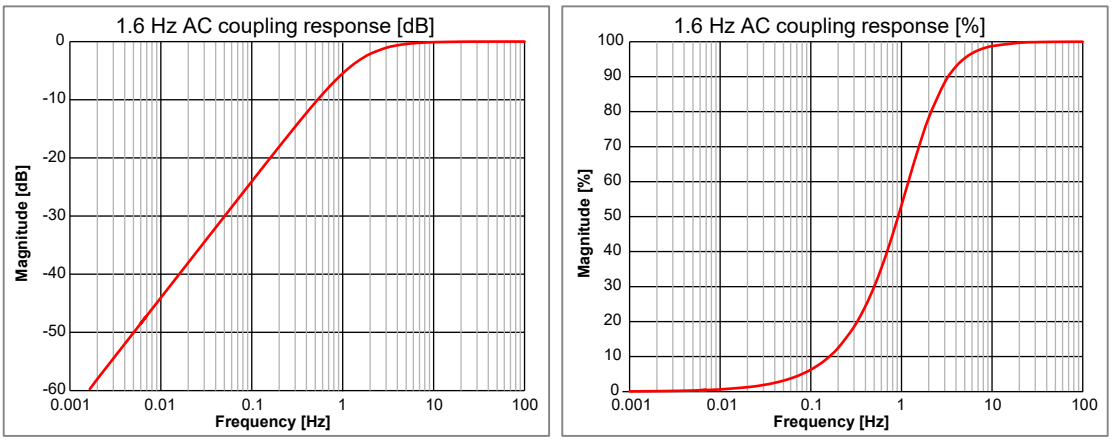


Figure O.63: Representative AC coupling response

Impedance	2 x 1 MΩ ± 0.5% // 75 pF ± 15%
Ranges	± 10 mV, ± 20 mV, ± 50 mV, ± 0.1 V, ± 0.2 V, ± 0.5 V, ± 1 V, ± 2 V, ± 5 V, ± 10 V, ± 20 V
Offset	± 50% in 1000 steps (0.1%); ± 20 V range has fixed 0% offset
DC Offset error	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV
Offset error drift	±(10 ppm + 2 µV)/°C (±(6 ppm + 1.5 µV)/°F)
DC Gain error	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
Gain error drift	± 10 ppm/°C (± 6 ppm/°F)
Maximum static error (MSE)	
Wideband	0.015% of Full Scale ± 25 µV
All IIR filters	0.015% of Full Scale ± 25 µV
RMS Noise (50 Ω terminated)	
Wideband	0.01% of Full Scale ± 25 µV
All IIR filters	0.01% of Full Scale ± 25 µV

Analog Input Section

Common mode (referred to system ground)		
Ranges	Less than ± 2 V	Larger than or equal to ± 2 V
Rejection (CMR)	> 80 dB @ 80 Hz (100 dB typical)	> 60 dB @ 80 Hz (80 dB typical)
Maximum common mode voltage	2 V RMS	33 V RMS

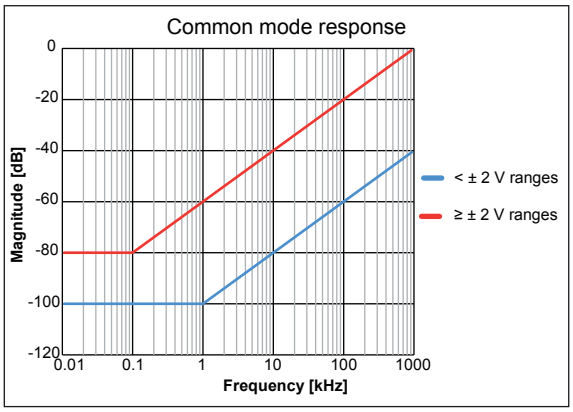


Figure O.64: Representative common mode response

Input overload protection	
Over voltage impedance change	The activation of the over voltage protection system will result in a reduced input impedance. The over voltage protection will not be active as long as the input voltage is less than 200% of the selected input range or 50 V DC whichever is the smallest value.
Maximum nondestructive voltage	± 50 V DC
Overload recovery time	Restored to 0.1% accuracy in less than 5 µs after 200% overload

Input Ranges When Using Passive Voltage Probes

Detailed probe specifications can be found at the end of this datasheet

Single-ended	**Added voltage ranges**
G901 (10:1 divider)	± 50 V, ± 100 V, ± 200 V
G902 (10:1 divider)	± 50 V, ± 100 V, ± 200 V
G903 (100:1 divider)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV
G904 (100:1 divider)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV
G906 (1000:1 divider)	± 50 V, ± 100 V, ± 200 V, ± 500 V, ± 1 kV, ± 2 kV, ± 5 kV, ± 10 kV (± 20 kV @ Dc to 60 Hz)
Differential matched	**Added voltage ranges**
G907 (10:1 divider)	± 50 V, ± 100 V, ± 200 V

Input Ranges When Using Current Clamps

Detailed probe specifications can be found at the end of this datasheet

Clamp type	**Added current ranges**
G912 (AC/DC)	± 30 mA to ± 30 A DC ± 30 mA to ± 20 A RMS
G913 (AC)	± 100 mA to ± 1000 A RMS
G914 (AC)	± 50 mA to ± 20 A RMS

Analog to Digital Conversion	
Sample rate; per channel	1 S/s to 20 kS/s
ADC resolution; one ADC per channel	24 bit, only 16 bit recorded
ADC type	Sigma Delta (Σ-Δ) ADC; Analog Devices AD7764BRUZ
Time base accuracy	Defined by mainframe: ± 3.5 ppm (1); aging after 10 years ± 10 ppm
Binary sample rate	Supported; produces rounded BIN values when calculating FFT's
Maximum binary sample rate	20.48 kS/s
External time base frequency	0 S/s to 20 kS/s
External time base frequency divider	Divide external clock by 1 to 2^{20}
External time base level	TTL
External time base minimum pulse width	200 ns

(1) Mainframes using Interface/Controller modules shipped before 2012: ±30 ppm.

Anti-Alias Filters

Using different filter selections (Wideband/Bessel IIR/Butterworth IIR) or different filter bandwidths can lead to phase mismatches between channels.

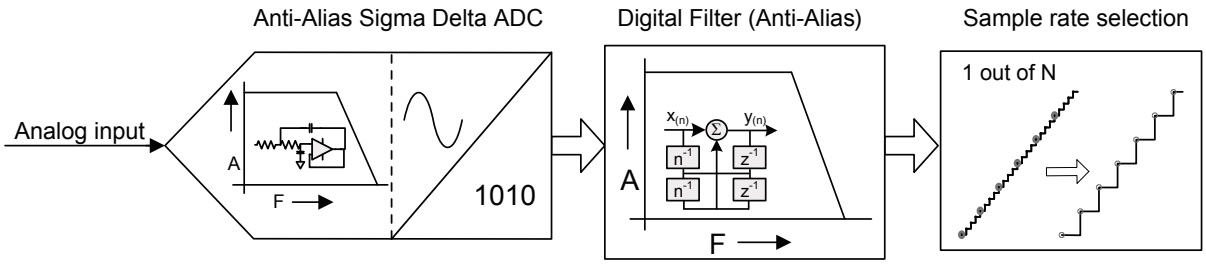


Figure O.65: Combined analog and digital anti-alias filter block diagram

Anti-aliasing is prevented by a steep, fixed frequency analog anti-alias filter integrated inside the Sigma Delta Analog to Digital Converter (ADC) always sampling at a fixed sample rate. This setup avoids the need for other analog anti-alias filters.
Directly behind the ADC, the high precision digital filter is used as anti-alias protection before the digital downsampling to the desired user sample rate is performed. The digital filter is programmed to a fraction of the user sample rate and automatically tracks any user sample rate selection. Compared to analog anti-alias filters, the programmable digital filter offers additional benefits like higher order filter with steep roll-off, a larger selection of filter characteristics, noise-free digital output and no additional phase shifts between channels that use the same filter settings.

Sigma Delta Wideband	When Sigma Delta wideband is selected the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) is always in the signal path. Therefore, the anti-alias protection is always active when Sigma Delta wideband is selected.
Bessel IIR	When Bessel IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Bessel IIR filter. Bessel filters are typically used when looking at signals in the time domain. Best used for measuring transient signals or sharp edge signals like square waves or step responses.
Butterworth IIR	When Butterworth IIR filter is selected, this is always a combination of the built-in anti-alias filter of the Sigma Delta ADC and a digital Butterworth IIR filter. Best used when working in the frequency domain. When working in the time domain this filter is best used for signals that are (close to) sine waves.

Sigma Delta Wideband (Analog Anti-Alias)

When Sigma Delta wideband is selected there is always the built-in anti-alias filter of the Sigma Delta ADC (no digital filter) in the signal path. Therefore there is always anti-alias protection when wideband is selected. Care must be taken as this filter introduces slight overshoots on square wave or pulse response signals. Signals of sine wave type will not be effected.

Wideband

Characteristic	Sigma delta, optimal frequency response
-3 dB Bandwidth	80 kHz ± 5 kHz
0.1 dB passband flatness(1)	DC to 20 kHz

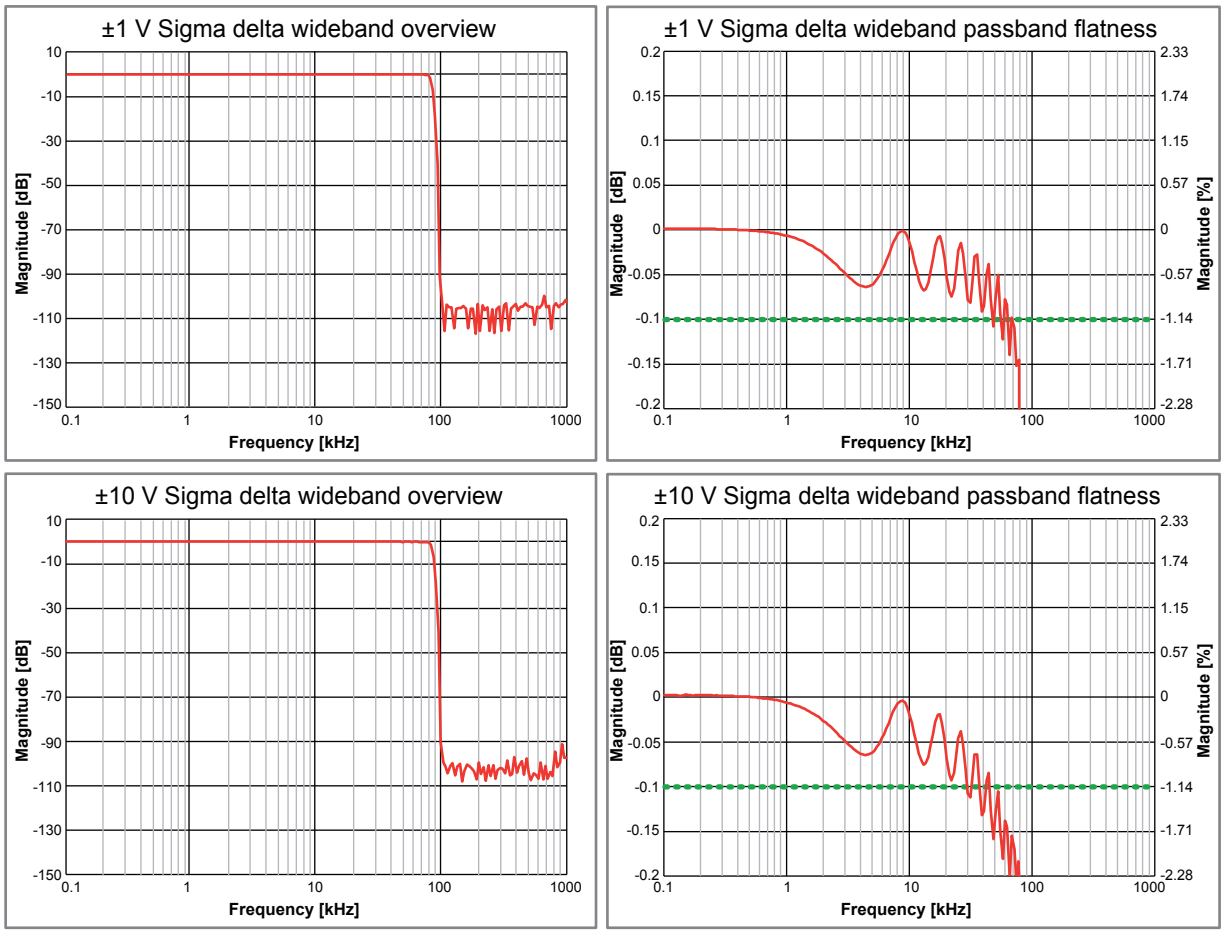
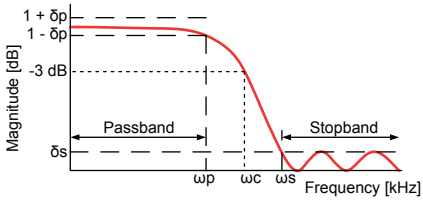


Figure O.66: Representative Wideband examples

(1) Measured using a Fluke 5700A calibrator, DC normalized

Bessel IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.67: Digital Bessel IIR Filter

When Bessel IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Bessel IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
Low pass -3 dB bandwidth	80 kHz ± 5 kHz
Bessel IIR Filter	
Characteristic	12-pole Bessel style IIR
User selection	Auto tracking to sample rate divided by: 10, 20, 40, 100 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	User selectable from 40 Hz to 2 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/10
Stopband attenuation (δs)	80 dB
Roll-off	72 dB/octave for 12-pole filters

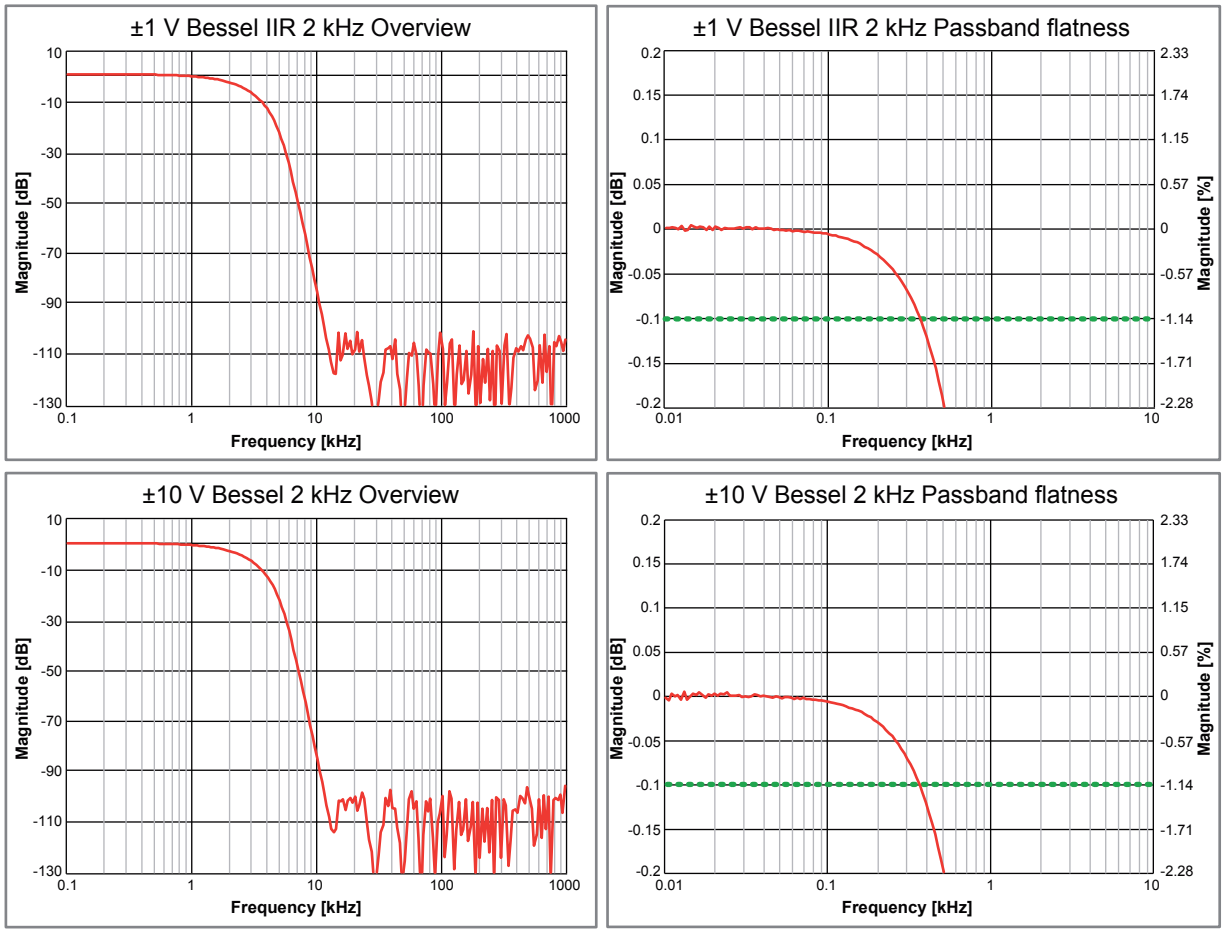
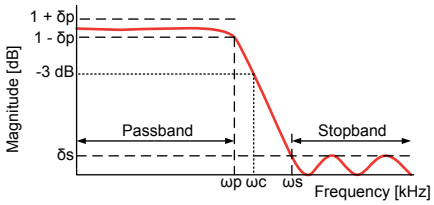


Figure O.68: Representative Bessel IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Butterworth IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.69: Digital Butterworth IIR Filter

When Butterworth IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Butterworth IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
Low pass bandwidth	80 kHz ± 5 kHz (-3 dB)
Butterworth IIR Filter	
Characteristic	12-pole Butterworth style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed.
Bandwidth (ωc)	User selectable from 100 Hz to 5 kHz
0.1 dB passband flatness (ωp)(1)	DC to ωc/2
Stopband attenuation (δs)	80 dB
Filter roll-off	72 dB/octave

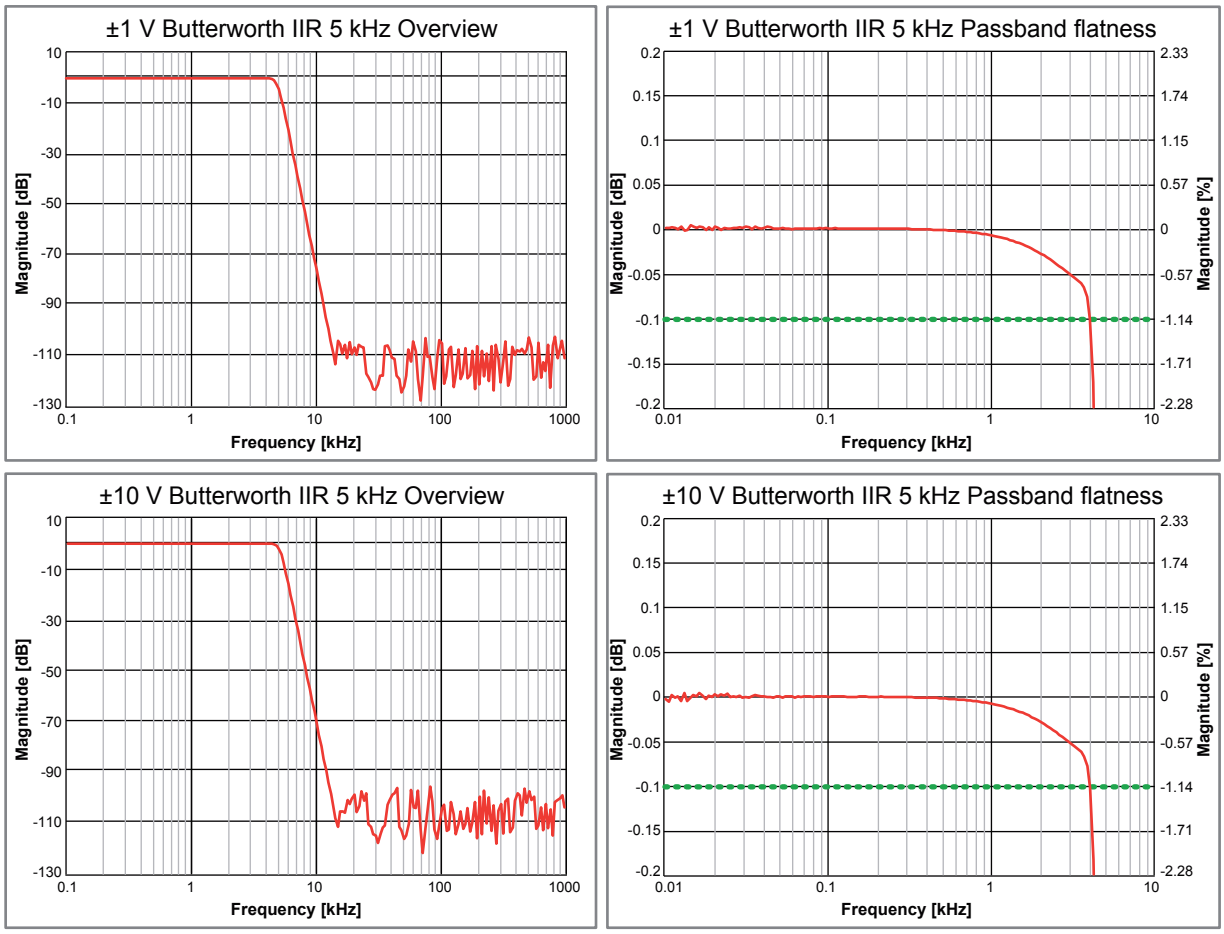
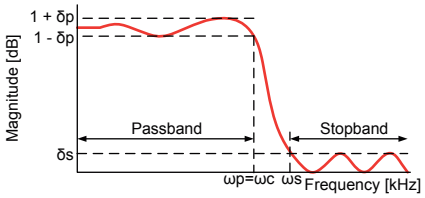


Figure O.70: Representative Butterworth IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Elliptic IIR Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.71: Digital Elliptic IIR Filter

When Elliptic IIR filter is selected, this is always a combination of the anti-alias filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog anti-alias filter	
Characteristic	Sigma delta, optimal frequency response
Low pass bandwidth	80 kHz ± 5 kHz (-3 dB)
Elliptic IIR Filter	
Characteristic	11th order Elliptic style IIR
User selection	Auto tracking to sample rate divided by: 4, 10, 20, 40 User selects divide factor from current sample rate, software then adjusts filter when sample rate is changed
Bandwidth (ωc)	100 Hz to 5 kHz
Stopband frequency (ωs)	Approximately 1.25 * ωc
Passband flatness (ωp)(1)	0.1 dB; DC to ωc/1.5
Stopband attenuation (δs)	80 dB

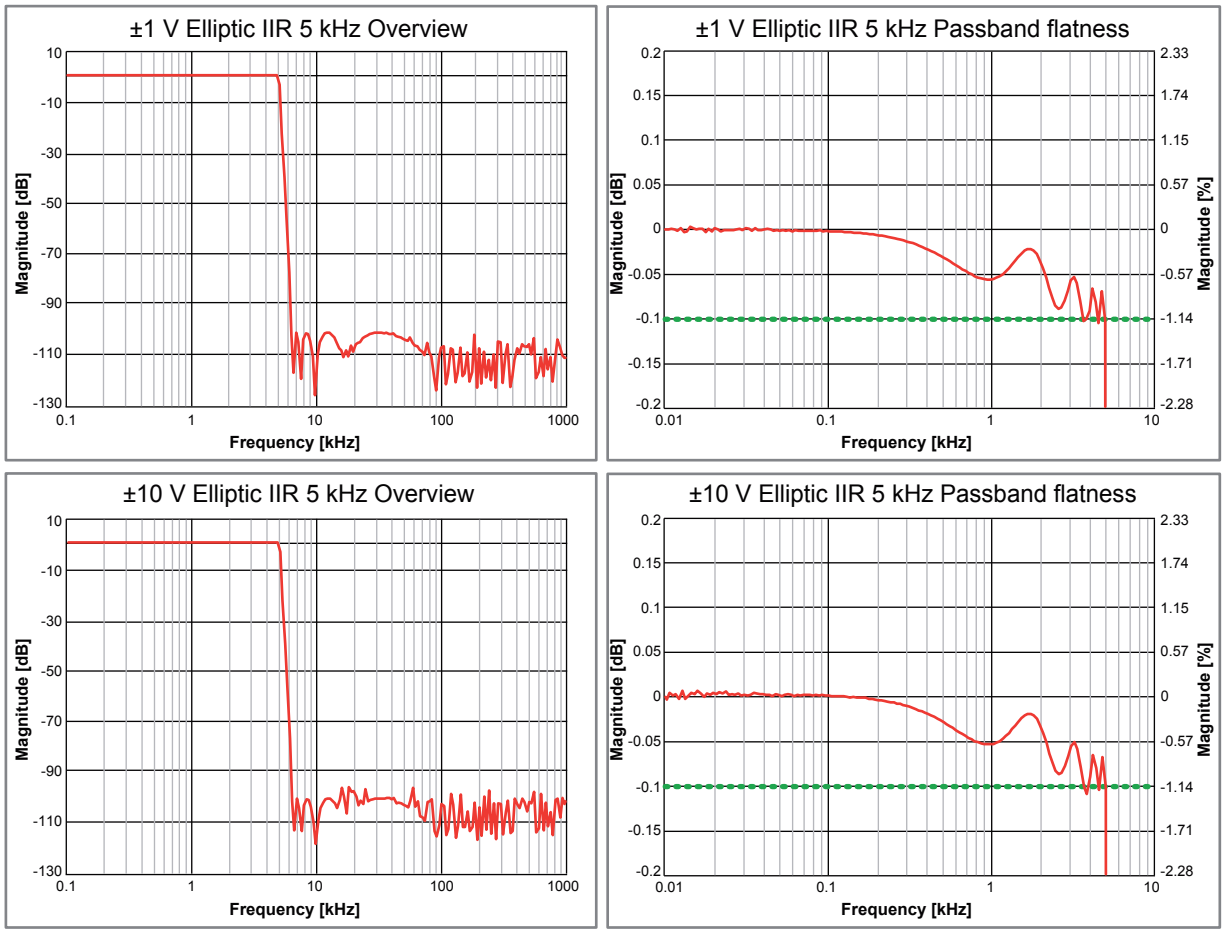
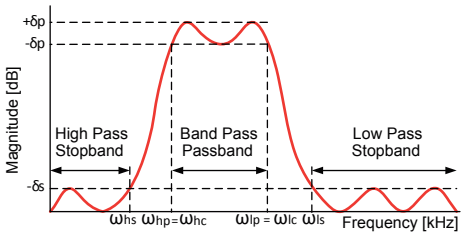


Figure O.72: Representative Elliptic IIR examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Elliptic IIR Bandpass Filter (Digital Anti-Alias)



δp: Passband ripple
δs: Stopband attenuation

ωp: Passband frequency
ωc: Corner frequency
ωs: Stopband frequency

Figure O.73: Digital Elliptic IIR Bandpass Filter

When Elliptic IIR filter is selected, this is always a combination of the filter built-in the Sigma Delta ADC and a digital Elliptic IIR filter.

Analog filter	
Characteristic	Sigma delta, optimal frequency response
Low pass bandwidth (ωlc)	80 kHz ± 5 kHz (-3 dB)
Elliptic IIR bandpass filter	
Characteristic	14th order Elliptic style IIR
User selection	2 Fixed high pass frequencies to be combined with 4 fixed low pass frequencies
High pass bandwidth (ωhc)	40 Hz and 100 Hz
High pass stopband frequency (ωhs)	Approximately ωhc / 2.5
Low pass bandwidth (ωlc)	2 kHz, 20 kHz, 40 kHz and 50 kHz
Low pass stopband frequency (ωs)	Approximately 1.5 to 2.5 * ωc
Passband flatness (ωp)(1)	0.1 dB; ωhc to ωlc or maximum 10 kHz
Stopband attenuation (δs)	80 dB

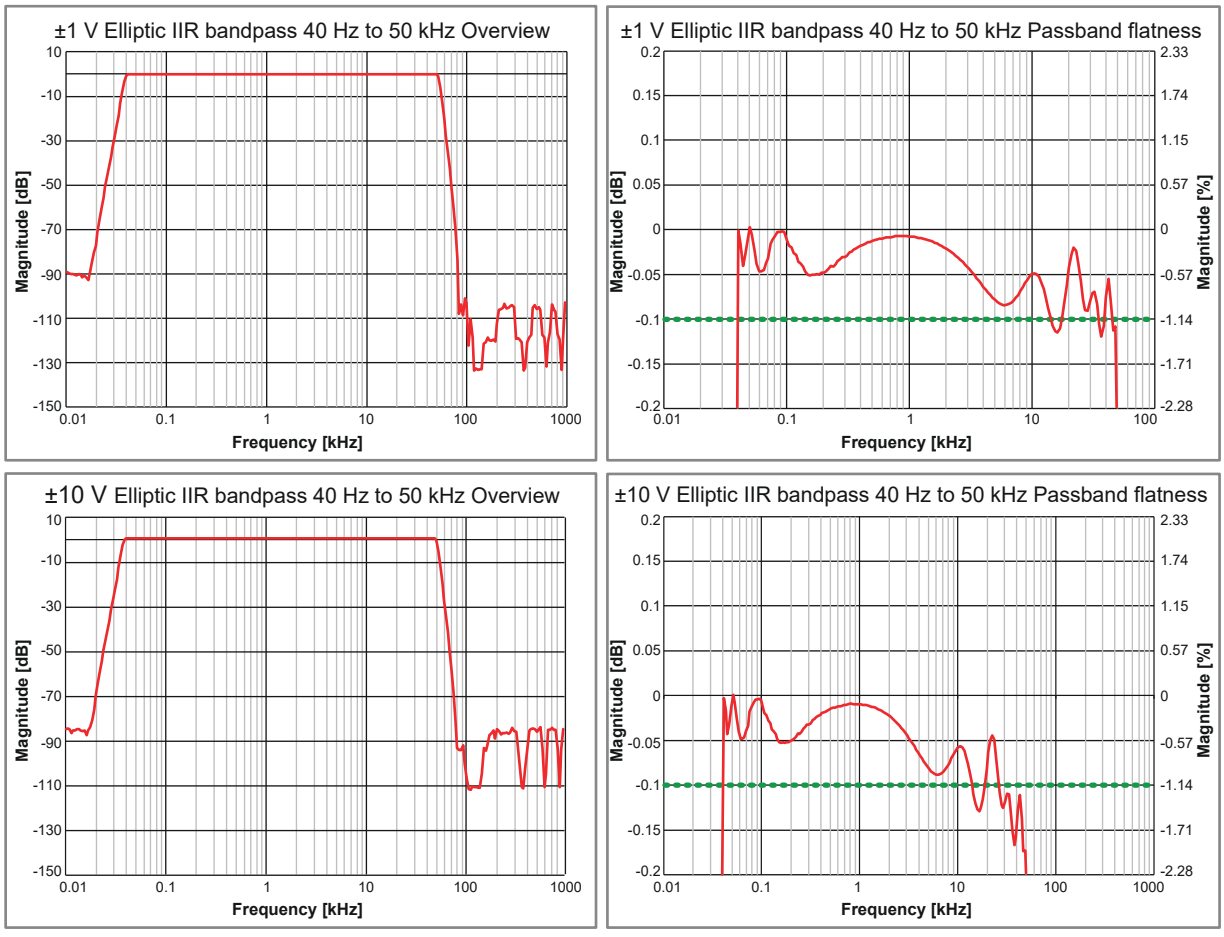


Figure O.74: Representative Elliptic IIR bandpass examples

(1) Measured using Fluke 5700A calibrator, DC normalized

Channel to Channel Phase Match	
Using different filter selections (Wideband/Bessel IIR/Butterworth IIR/etc.) or different filter bandwidths will lead to phase mismatches between channels.	
Wideband	1 kHz Sine wave
Channels on card	0.01 deg (30 ns)
GN1611 Channels within mainframe	0.01 deg (30 ns)
Bessel IIR, Filter frequency 2 kHz @ 20 kS/s	
Channels on card	0.01 deg (30 ns)
GN1611 Channels within mainframe	0.01 deg (30 ns)
Butterworth IIR, Filter frequency 5 kHz @ 20 kS/s	
Channels on card	0.01 deg (30 ns)
GN1611 Channels within mainframe	0.01 deg (30 ns)
Elliptic IIR, Filter frequency 5 kHz @ 20 kS/s	
Channels on card	0.01 deg (30 ns)
GN1611Channels within mainframe	0.01 deg (30 ns)
GN1611 channels across mainframes	Defined by synchronization method used (None, IRIG, GPS, Master/Slave, PTP)

On-board Memory	
Per card	200 MByte (100 MSample @ 16 Bits Storage)
Organization	Automatically distributed amongst channels enabled for storage or real-time calculations
Memory diagnostics	Automatic memory test when system is powered and not recording
Storage sample size	16 bits, 2 bytes/sample 24 bits, 4 bytes/sample (required for Timer/Counter usage)

Digital Event/Timer/Counter[1]	
The Digital Event/Timer/Counter input connector is located on the mainframe. For exact layout and pinning see mainframe data sheet.	
Digital input events	16 per card
Levels	TTL input level, user programmable invert level
Inputs	1 pin per input, some pins are shared with Timer/Counter inputs
Overvoltage protection	± 30 V DC continuously
Minimum pulse width	100 ns
Maximum frequency	5 MHz
Digital output events	2 per card
Levels	TTL output levels, short circuit protected
Output event 1	User selectable: Trigger, Alarm, set High or Low
Output event 2	User selectable: Recording active, set High or Low
Digital output event user selections	
Trigger	1 high pulse per trigger (on every channel trigger of this card only) 12.8 µs minimum pulse width 200 µs ± 1 µs ± 1 sample period pulse delay
Alarm	High when alarm condition is activated, low when not activated (alarm conditions of this card only) 200 µs ± 1 µs ± 1 sample period alarm event delay
Recording active	High when recording, low when in idle or pause mode Recording active output delay of 450 ns
Set High or Low	Output set High or Low; can be controlled by Custom Software Interface (CSI) extensions; delay depends on specific software implementation
Timer/Counter	2 per card; only available in 32 bit storage mode
Levels	TTL input levels
Inputs	All pins are shared with digital event inputs
Timer-Counter modes	Uni- and bi-directional count Bi-directional quadrature count Angle Uni- and bi-directional frequency/RPM measurement
External start	Rising/Falling edge selected by user starts a new recording
External stop	Rising/Falling edge selected by the user stops the recording

(1) Only if supported by mainframe

Triggering	
Channel trigger/qualifier	1 fully independent per channel either trigger or qualifier
Pre- and post-trigger length	0 to full memory
Trigger rate	400 triggers per second
Delayed trigger	Maximum 1000 seconds after a trigger occurred
Manual trigger (Software)	Supported
External Trigger In	
Selection per card	User selectable On/Off
Trigger in edge	Rising/Falling mainframe selectable, identical for all cards
Minimum pulse width	500 ns
Trigger in delay	± 1 µs + maximum 1 sample period (Identical for decimal and binary time base)
Send to external trigger out	User can select to forward External Trigger In to the External Trigger Out BNC
External Trigger Out	
Selection per card	User selectable On/Off
Trigger out level	High/Low/Hold High; mainframe selectable, identical for all cards
Trigger out pulse width	High/Low: 12.8 µs Hold High: Active from first mainframe trigger to end of recording Pulse width created by mainframe; see mainframe datasheet for details
Trigger out delay	Selectable (180 µs to 516 µs) ± 1 µs + maximum 1 sample period using decimal time base Selectable (176 µs to 504 µs) ± 1 µs + maximum 1 sample period using binary time base Default 516(504) µs for decimal (binary) time base, to be compatible with standard behavior. Minimum selectable delay is the smallest delay available for all acquisition cards used within the mainframe
Cross channel triggering	
Measurement channels	Logical OR of triggers from all measured signals Logical AND of qualifiers from all measured signals
Calculated channels	Logical OR of triggers from all calculated signals (RTC and RT-FDB) Logical AND of qualifiers from all calculated signals (RTC and RT-FDB)
Analog channel trigger levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%); for each level
Direction	Rising/Falling; single direction control for both levels based on selected mode
Hysteresis	0.1 to 100% of Full Scale; defines the trigger sensitivity
Analog channel trigger modes	
Basic	POS or NEG crossing; single level
Dual level	One POS and one NEG crossing; two individual levels, logical OR
Analog channel qualifier modes	
Basic	Above or below level check. Enable/Disable trigger with single level
Dual (level)	Outside or within bounds check. Enable/Disable trigger with dual level
Event channel trigger (1)	
Event channels	Individual event trigger per event channel
Levels	Trigger on rising edge or trigger on falling edge
Qualifiers	Active High or Active Low for every event channel

(1) Only if supported by mainframe

Alarm Output	
Selection per card	User selectable On/Off
Alarm modes	Basic or Dual
Basic	Above or below level check
Dual (level)	Outside or within bounds check
Alarm levels	
Levels	Maximum 2 level detectors
Resolution	16 bit (0.0015%) for each level
Alarm output	Active during valid alarm condition, output supported through mainframe
Alarm output delay	515 µs ± 1 µs + maximum 1 sample period using decimal time base 503 µs ± 1 µs + maximum 1 sample period using binary time base

Real-time Statstream®

Patent Number : 7,868,886
Real-time extraction of basic signal parameters.
Supports real-time live scrolling and scoping waveform displays as well as real-time meters while recording.
During recording reviews, it enhances speed for displaying and zooming extremely large recordings and it reduces the calculation time for statistical values on large data sets.

Analog channels	Real-time extraction of Maximum, Minimum, Mean, Peak to Peak, Standard Deviation and RMS values
Event/Timer/Counter channels	Real-time extraction of Maximum, Minimum and Peak to Peak values

Real-Time Cycle Based Calculators (Perception V6.70 and higher)

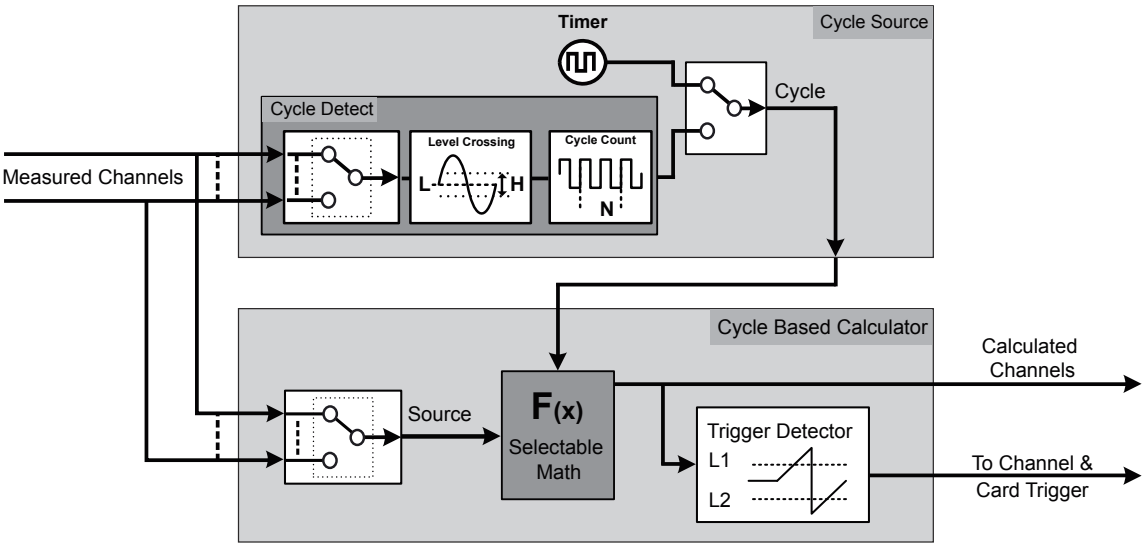


Figure O.75: Real-time cycle based calculators

Cycle Source	Determines the periodic real-time calculation speed by either setting a timer or using a real-time cycle detect
Cycle Source: Timer	
Timer duration	1.0 ms (1 kHz) to 60 s (0.0167 Hz)
Cycle Source: Cycle detect	
Level crossing	Real-time monitors one input channel using a signal level, hysteresis and direction to determine the cyclic nature of the signal
Cycle count	Sets the counted number of cycles used for periodic calculation output
Cycle period(1)	Maximum Cycle period that can be detected: 0.25 s (4 Hz) Minimum Cycle period that can be detected: 0.91 ms (1.1 kHz) Calculations are stopped when the Cycle period exceeds its maximum Cycle period (0.25 s). Cycle count is temporarily increased when Cycle period becomes shorter than minimum Cycle period (0.91 ms). Time event notifications in the channel data indicate when the Cycle period has been exceeded or when the automatic Cycle count is increased.
Cycle based calculator	
Number of calculators	32
DSP load	Each calculator can perform 1 calculation. Not every calculation uses the same DSP power. Selecting a calculation with the highest computation power could result in a reduction in the total number of calculators. Different combinations require different computation power. The effects of selected combinations is reflected in Perception software.
Cycle Source calculations	Cycle and Frequency
Analog channel calculations	RMS, Minimum, Maximum, Mean, Peak-to-Peak, Area, Energy and MeanOfMultiplication
Timer/Counter channel calculations	Frequency (to enable triggering). RPM of Angle.
Cycle	Square wave signal, 50% duty cycle. Represent Cycle Source; rising edge indicates start of new calculation period.
Frequency	Detected cycle interval is converted to a frequency (1/cycle time of input signal)
Trigger detector	
Number of detectors	32; One per real-time calculator
Trigger level	Defined by the user for each detector. Generates trigger when the calculated signal crosses the level.
Trigger output delay	Triggers are delayed by 100 ms on calculated signals. The trigger time is corrected internally so that the sweep triggering is correct. An additional pre-trigger length of 100 ms is added to enable the trigger time correction. This reduces the maximum sweep length by 100 ms.

(1) Cycle period range depends on signal wave shape and hysteresis setting. Specified for Sine wave with 25% Full Scale hysteresis.

Acquisition Modes

Single sweep	Triggered acquisition to on-board memory without sample rate limitations; for single transients or intermittent phenomena. No aggregate sample rate limitations.
Multiple sweeps	Triggered acquisition to on-board memory without sample rate limitations; for repetitive transients or intermittent phenomena. No aggregate sample rate limitations.
Slow-Fast Sweep	Identical to single sweep acquisition with additional support for fast sample rate switches during the post-trigger segment of the slow rate single sweep settings. No aggregate sample rate limitations.
Continuous	Direct storage to PC or mainframe controlled hard disk without file size limitations; triggered or un-triggered; for long duration recorder type applications. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.
Dual	Combination of Multiple sweeps and Continuous; recorder type streaming to hard disk with simultaneously triggered sweeps in on-board memory. Aggregate sample rate limitations depend on Ethernet speed, PC used and data storage media used.

Recording Mode Details

Recording Mode Details (16 Bit storage)

	Single Sweep Multiple Sweeps Slow-Fast Sweep		**Continuous**		**Dual Rate**	
	Enabled Channels		Enabled Channels		Enabled Channels	
	1 Ch	16 Ch	1 Ch	16 Ch	1 Ch	16 Ch
Max. sweep memory	100 MS	5.7 MS	not used		80 MS	4.5 MS
Max. sweep sample rate	20 kS/s		not used		250 kS/s	
Max. continuous FIFO	not used		100 MS	5.7 MS	20 MS	0.9 MS
Max. continuous sample rate	not used		20 kS/s		Sweep Sample Rate / 2	
Max. aggregate continuous streaming rate	not used		0.02 MS/s 0.04 MB/s	0.32 MS/s 0.64 MB/s	0.02 MS/s 0.04 MB/s	0.32 MS/s 0.64 MB/s

Single Sweep

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps

Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweep stretch rate is 1 sweep stretch per 2.5 ms.

Multiple Sweeps	
Sweep storage	Sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the total number of selected channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet.
Exceeding sweep storage rate	Trigger event markers are stored in a recording. No sweep data is stored. New sweep data is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.

Slow-Fast Sweep	
Maximum number of Sweeps	1 per recording
Maximum slow sample rate	Fast sample rate divided by two
Maximum fast sample rate switches	20, sample rate switching always stops when sweep ends
Minimum time between sample rate switches	2.5 ms

Continuous	
Continuous modes supported	Standard, Circular recording, Specified time and Stop on trigger
Standard	User starts and stops recording. Recording is stopped when the storage media is full
Circular recording	User specified recording history on storage media. All recorded data is stored on the storage media as quickly as possible. As soon as the selected history time is reached, older recorded data is overwritten. Recording can be stopped by the user or any system trigger.
Specified time	Recording is stopped after the time specified or when the storage media is full
Stop on trigger	Recording is stopped after any system trigger or when the storage media is full
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet
Exceeding aggregate streaming rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to a storage medium. When internal memory is completely empty again, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Dual	
Dual Sweep Specification	
Pre-trigger segment	0% to 100% of selected sweep length If trigger occurs before the pre-trigger segment is recorded, the pre-trigger segment is truncated to recorded data only.
Delayed trigger	Maximum 1000 seconds after a trigger occurred. The sweep is recorded immediately after a delayed trigger time with 100% post-trigger after this time point.
Maximum number of sweeps	200 000 per recording
Maximum sweep rate	400 sweeps per second
Sweep re-arm time	Zero re-arm time, sweep rate limited to 1 sweep per 2.5 ms
Sweep stretch	User selectable On/Off When enabled, any new trigger event occurring in the post-trigger segment of the sweep restarts the post-trigger length. If, upon the detection of a new trigger, the extended post-trigger does not fit within the sweep memory, sweep stretch does not happen. The maximum sweepstretch rate is 1 sweep stretch per 2.5 ms.
Sweep storage	In dual mode, the storage of the continuous data is prioritized above the storage of the sweep data. If enough storage rate is available, the sweep storage is started immediately after the trigger for this sweep has been detected. Sweep memory becomes available for reuse as soon as storage of the entire sweep for all enabled channels of this card has been completed. Sweeps are stored one by one, starting with the first recorded sweep.
Sweep storage rate	Determined by the continuous sample rate, total number of channels and mainframes, mainframe type, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to mainframe datasheet.
Exceeding sweep storage rate	Continuous recorded data is not stopped, trigger event markers are stored in recording and no new sweep data is stored. A new sweep is recorded as soon as enough internal memory is available to capture a full sweep when a trigger occurs.
Dual Continuous Specifications	
Continuous FIFO memory	Used by enabled channels to optimize the continuous streaming rate
Maximum recording time	Until storage media filled or user selected time or unlimited when using circular recording
Maximum aggregate streaming rate per mainframe	Determined by mainframe, Ethernet speed, PC storage medium and other PC parameters. For details, please refer to the mainframe datasheet. When the average aggregate streaming rate is exceeded, the sweep storage speed is automatically reduced to increase the aggregate streaming rate until the sweep storage is stopped completely.
Exceeding aggregate storage rate	When a streaming rate higher than the aggregate streaming rate of the system is selected, the continuous memory acts as a FIFO. As soon as this FIFO fills up, the recording is suspended (no data is recorded temporarily). During this period, the internal FIFO memory is transferred to the storage medium. When the internal memory (Continuous and Sweep memory) is completely empty, the recording is automatically resumed. User notifications are added to the recording file for post recording identification of storage overrun.

Connector Pin Assignment	
Connector type	POSITRONIC HDC50F5R8N0X/AA
Mating connector type	Harting part number 9670505615 (Metal shell 61030010019, cable clamp 61030000145, blanking piece 61030000041)
Output voltage	5 V ± 20%
Output current	0.3 A maximum (all output pins internally connected)

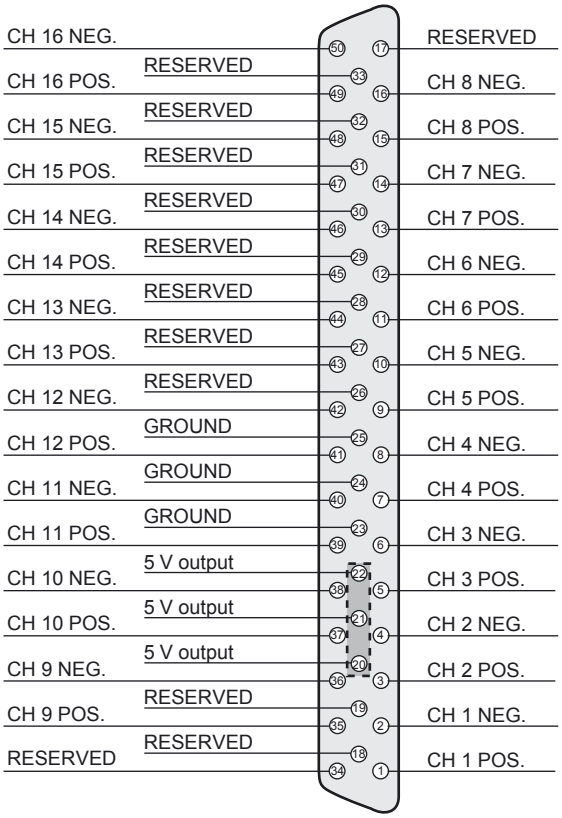


Figure O.76: Input connector pin diagram (Front view)

Environmental Specifications	
Temperature Range	
Operational	0 °C to +40 °C (+32 °F to +104 °F)
Non-operational (Storage)	-25 °C to +70 °C (-13 °F to +158 °F)
Thermal protection	Automatic thermal shutdown at 85 °C (+185 °F) internal temperature User warning notifications at 75 °C (+167 °F) (Supported by Perception V6.30 or higher)
Relative humidity	0% to 80%; non-condensing; operational
Protection class	IP20
Altitude	Maximum 2000 m (6562 ft) above sea level; operational
Shock: IEC 60068-2-27	
Operational	Half-sine 10 g/11 ms; 3-axis, 1000 shocks in positive and negative direction
Non-operational	Half-sine 25 g/6 ms; 3-axis, 3 shocks in positive and negative direction
Vibration: IEC 60068-2-34	
Operational	1 g RMS, ½ h; 3-axis, random 5 to 500 Hz
Non-operational	2 g RMS, 1 h; 3-axis, random 5 to 500 Hz
Operational Environmental Tests	
Cold test IEC 60068-2-1 Test Ad	-5 °C (+23 °F) for 2 hours
Dry heat test IEC 60068-2-2 Test Bd	+40 °C (+104 °F) for 2 hours
Damp heat test IEC 60068-2-3 Test Ca	+40 °C (+104 °F), humidity >93% RH for 4 days
Non-Operational (Storage) Environmental Tests	
Cold test IEC 60068-2-1 Test Ab	-25 °C (-13 °F) for 72 hours
Dry heat test IEC 60068-2-2 Test Bb	+70 °C (+158 °F) humidity < 50% RH for 96 hours
Change of temperature test IEC 60068-2-14 Test Na	-25 °C to +70 °C (-13 °F to +158 °F) 5 cycles, rate 2 to 3 minutes, dwell time 3 hours
Damp heat cyclic test IEC 60068-2-30 Test Db variant 1	+25 °C/+40 °C (+77 °F/+104 °F), humidity > 95/90% RH 6 cycles, cycle duration 24 hours

Harmonized Standards for CE Compliance, According to the Following Directives

Low Voltage Directive (LVD): 2014/35/EU
ElectroMagnetic Compatibility Directive (EMC): 2014/30/EU

Electrical Safety	
EN 61010-1 (2010)	Safety requirements for electrical equipment for measurement, control, and laboratory use - General requirements
EN 61010-2-030 (2010)	Particular requirements for testing and measuring circuits
Electromagnetic Compatibility	
EN 61326-1 (2013)	Electrical equipment for measurement, control and laboratory use - EMC requirements - Part 1: General requirements
Emission	
EN 55011	Industrial, scientific and medical equipment - Radio-frequency disturbance characteristics - Limits and methods of measurement Conducted disturbance: class B; Radiated disturbance: class A
EN 61000-3-2	Limits for harmonic current emissions: class D
EN 61000-3-3	Limitation of voltage changes, voltage fluctuations and flicker in public low voltage supply systems
Immunity	
EN 61000-4-2	Electrostatic discharge immunity test (ESD); contact discharge ± 4 kV/air discharge ± 8 kV: performance criteria B
EN 61000-4-3	Radiated, radio-frequency, electromagnetic field immunity test; 80 to 2700 MHz using 10 V/m, 1000 Hz AM: performance criteria A
EN 61000-4-4	Electrical fast transient/burst immunity test Mains ± 2 kV using coupling network. Channel ± 2 kV using capacitive clamp: performance criteria B
EN 61000-4-5	Surge immunity test Mains ± 0.5 kV/± 1 kV Line-Line and ± 0.5 kV/± 1 kV/± 2 kV Line-earth Channel ± 0.5 kV/± 1 kV using coupling network: performance criteria B

Harmonized Standards for CE Compliance, According to the Following Directives Low Voltage Directive (LVD): 2014/35/EU Electromagnetic Compatibility Directive (EMC): 2014/30/EU	
EN 61000-4-6	Immunity to conducted disturbances, induced by radio-frequency fields 0.15 to 80 MHz, 1000 Hz AM; 10 V RMS @ mains, 3 V RMS @ channel, both using clamp: performance criteria A
EN 61000-4-11	Voltage dips, short interruptions and voltage variations immunity tests Dips: performance criteria A; Interruptions: performance criteria C

P RoHS Compliance Overview

P.1 GEN DAQ mainframes - Restriction of Hazardous Substances Directive (RoHS) status

Mainframe	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-GEN7T-2	*1-GEN7T-2*	*2003*	*2015*	*N.A.*	*No*
1-GEN16T-2	*1-GEN16T-2*	*2004*	*2016*	*N.A.*	*No*
1-GEN5I-2	*1-GEN5I-2*	*2008*	*2012*	*N.A.*	*No*
1-GEN2I-2	*1-GEN2I-2*	*2010*	*2012*	*N.A.*	*No*
1-GEN2TB	1-GEN2TB	2018		Yes	Yes
1-GEN3I	1-GEN3I	2013		Yes	Yes
1-GEN3T	1-GEN3T	2014		Yes	Yes
1-GEN7I	1-GEN7I	2014		Yes	Yes
1-GEN7TA	1-GEN7TA	2015		Yes	Yes
1-GEN17TA	1-GEN17TA	2016		Yes	Yes

Note *Grey columns are end-of-life cards.*
N.A. Regulation doesn't apply to GEN series equipment.

Mainframe Accessories	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-G001-2	IRIG card	2004		N.A.	No
1-G002-2	IRIG/GPS card	2004		N.A.	No
1-G008-2	*GEN7t carring case*	*2003*	*2015*	*Yes*	*Unknown*
1-G010-2	*GEN5i Removable system hard disk drive*	*2008*	*2014*	*Yes*	*Unknown*
1-G014-2	*GEN5i Internal system Solid State Drive*	*2008*	*2014*	*Yes*	*Unknown*
1-G015-2	*GEN5i Removable data Solid State Drive*	*2008*	*2014*	*Yes*	*Unknown*
1-G016-2	*GEN5i Removable system Solid State Drive*	*2008*	*2014*	*Yes*	*Unknown*
1-G028-2	*5B Integration card*	*2008*	*2017*	*Yes*	*Yes*
1-G035-2	*GEN5i Removable data hard disk drive*	*2008*	*2014*	*Yes*	*Unknown*
1-G036-2	*GEN5i Carrying bag*	*2008*	*2014*	*Yes*	*Unknown*
1-G037-2	*GEN5i Shipping case*	*2008*	*2014*	*Yes*	*Unknown*
1-G038-2	*GEN5i 19" Rack mount kit*	*2008*	*2014*	*Yes*	*Unknown*
1-G040-2	*Master/Slave card*	*2005*	*2017*	*N.A.*	*No*
1-G053	GEN2i/GEN3i 19" Rack mount kit	2010		Yes	Yes
1-G054	GEN2i/GEN3i/GEN3t Shipping case	2010		Yes	Yes
1-G060-2	*IM2 Upgrade kit*	*2012*	*2016*	*Yes*	*Unknown*
1-G061-2	*IM2 Solid State Drive*	*2012*	*2016*	*Yes*	*Unknown*
1-G062	1 Gbit Optical Network SFP module 850 nm	2013		Yes	Yes
1-G063	1 Gbit Optical Network SFP module 1310 nm	2013		Yes	Yes
1-G064	10 Gbit Ethernet card, optical	2013		Yes	Yes
1-G065	10 Gbit Optical Network SFP+ module 850 nm	2013		Yes	Yes
1-G066	10 Gbit Optical Network SFP+ module 1310 nm	2013		Yes	Yes

Mainframe Accessories	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-G070A	Torque/RPM adapter	2015		Yes	Yes
1-G072	230 Volt RMS Isolated Digital Event adapter	2015		Yes	Yes
1-G073	GEN3t Solid State Drive	2015		Yes	Yes
1-G074	GEN7i Removable system Solid State Drive	2015		Yes	Yes
1-G075	GEN7i Removable data Solid State Drive	2015		Yes	Yes
1-G076	GEN7i 19" Rack mount kit	2015		Yes	Yes
1-G078	GEN7i/GEN7tA Air filter	2015		Yes	Yes
1-G079	GEN7tA, GEN17t Removable data Solid State Drive	2015		Yes	Yes
1-G081	Option carrier card	2015		Yes	Yes
1-G082	EtherCAT® card	2015		Yes	Yes
1-G083	Master output card	2015		Yes	Yes
1-G084	10 Gbit Ethernet card, electrical	2015		Yes	Yes
1-G085	GEN17tA Air filter	2016		Yes	Yes
1-G093	GEN2tB 19 inch rack mount kit	2018		Yes	Yes
1-G094	GEN2tB External AC-DC Power Supply	2018		Yes	Yes
1-G095	GEN2tB Air filter	2018		Yes	Yes
1-G096	GEN2tB M2 SSD, Local Storage	2018		Yes	Yes
1-G098	GEN2tB Shipping case	2018		Yes	Yes
1-G504	PC USB carrier - US	2008		Yes	Yes
1-G505	PC USB carrier - UK	2008		Yes	Yes
1-G506	PC USB carrier - EU	2008		Yes	Yes

Note *Grey columns are end-of-life cards.*
N.A. Regulation doesn't apply to GEN series equipment.

P.2 GEN DAQ acquisition cards - Restriction of Hazardous Substances Directive (RoHS) status

Acquistion card	Input card	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-GN810-2	*Basic 200 kS/s*	*2003*	*2014*	*N.A.*	*No*
1-GN811-2	*Basic 1 MS/s*	*2003*	*2014*	*N.A.*	*No*
1-GN812-2	*Basic ISO 1 MS/s*	*2004*	*2014*	*N.A.*	*No*
1-GN813-2	*Basic XT ISO 1 MS/s*	*2004*	*2014*	*N.A.*	*No*
1-GN814-2	*Basic XT ISO 200 kS/s*	*2004*	*2014*	*N.A.*	*No*
1-GN440-2	*Differential/IEPE/Current ISO 200 kS/s*	*2004*	*2017*	*N.A.*	*No*
1-GN441-2	*Differential/IEPE/Current ISO 2 MS/s*	*2004*	*2017*	*N.A.*	*No*
1-GN4070-2	*Optical Event Marker 1 MS/s*	*2005*	*2017*	*N.A.*	*No*
1-GN410-2	*Bridge ISO 200 kS/s*	*2005*	*2017*	*N.A.*	*No*
1-GN411-2	*Bridge ISO 1 MS/s*	*2005*	*2017*	*N.A.*	*No*
1-GN6470-2	*Event Marker 1 MS/s*	*2005*	*2017*	*N.A.*	*No*
1-GN401-2	*Optical Fiber Isolated MM 100 MS/s receiver*	*2006*	*2017*	*N.A.*	*No*
1–GN1202B	*Multi Mode Optical Fiber*	2018		Yes	Yes
1-GN402-2	*Optical Fiber Isolated SM 100 MS/s receiver*	*2006*	*2017*	*N.A.*	*No*
1-GN412-2	*Differential 100 MS/s*	*2006*	*2017*	*N.A.*	*No*
1-GN413-2	*Differential 25 MS/s*	*2006*	*2017*	*N.A.*	*No*
1-GN1610	*Basic/IEPE/Charge 250 kS/s 16 chn*	*2011*	*2015*	*Yes*	*Yes*
1-GN1611-2	*Basic/IEPE/Charge 20 kS/s 16 chn*	*2011*	*2015*	*Yes*	*Yes*
1-GN3210	Basic/IEPE/Charge 250 kS/s	2011		Yes	Yes
1-GN3211	Basic/IEPE/Charge 20 kS/s	2011		Yes	Yes
1-GN610-2	*Isolated 1 kV 2 MS/s*	*2012*	*2017*	*Yes*	*Yes*
1-GN611-2	*Isolated 1 kV 200 kS/s*	*2012*	*2017*	*Yes*	*Yes*
1-GN815	Basic/IEPE ISO 2 MS/s	2014		Yes	Yes
1-GN816	Basic/IEPE ISO 200 kS/s	2014		Yes	Yes
1-GN610B	Isolated 1kV 2 MS/s	2015		Yes	Yes
1-GN611B	Isolated 1 kV 200 kS/s	2015		Yes	Yes
1-GN8101B	Single-ended	2018		Yes	Yes
1-GN8102B	Single-ended	2018		Yes	Yes
1-GN8103B	Single-ended	2018		Yes	Yes

Note *Grey columns are end-of-life cards.*
N.A. Regulation doesn't apply to GEN series equipment.

Optical fiber transmitter	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-GN110	Battery optical fiber isolated MM 100 MS/s transmitter	2006		Yes	No
1-GN111	Battery optical fiber isolated MM 25 MS/s transmitter	2006		Yes	No
1-GN112	1.8 kV optical fiber isolated MM 100 MS/s transmitter	2006		Yes	No
1-GN113	1.8 kV optical fiber isolated MM 25 MS/s transmitter	2006		Yes	No
1-GN114	Optical fiber isolated SM 100 MS/s transmitter for system integration	2008		Yes	No

Card Accessories	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-G021-2	Bridge Completion pack	2005		Yes	Yes
1-G069-2	16 pin LEMO connect pack	2005		Yes	Yes
1-G033-2	*10 bay Li-ion battery charger*	*2006*		*Yes*	*Unknown*
1-G034	Li-ion SM202 battery	2006		Yes	Yes
1-G109	2 bay Li-ion battery charger	2006		Yes	Unknown
1-G301	Li-ion SM202 battery with carrier	2006		Yes	Yes
1-G030-2	*2 GB memory upgrade GN401/GN402/GN412*	*2008*	*2017*	*Yes*	*Yes*
1-G030	GN1202B	2018		Yes	Yes
1-KAB282-1.5	Isolated black&red 4 mm banana cable	2010		Yes	Yes
1-G055-2	16 channel single-ended break out panel	2011		Yes	Yes
1-G056	16 channel differential break out panel	2011		Yes	Yes
1-G058	32 channel single-ended break out panel	2011		Yes	Yes
1-KAB171-1	16 channel single-ended break out cable	2011		Yes	Yes
1-KAB172-1	16 channel differential break out cable	2011		Yes	Yes
1-G067	Isolated BNC to banana adapter	2012		Yes	Yes
1-G068	Isolated 600 V CAT II Artificial star adapter	2012		Yes	Yes
1-KAB290-xx	Isolated 600 V CAT II shielded test leads	2012		Yes	Yes
1-G045	2 kV impulse attenuator	2013		Yes	Yes

Note *Grey columns are end-of-life cards.*

XT probes	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-G019-2	*1 kV DC probe rack*	*2006*	*2014*	*Yes*	*Unknown*
1-G020-2	*1 kV AC probe rack*	*2006*	*2014*	*Yes*	*Unknown*
1-G041-2	*1kV DC probe*	*2006*	*2014*	*Yes*	*Unknown*
1-G042-2	*1kV AC probe rack*	*2006*	*2014*	*Yes*	*Unknown*

Note *Grey columns are end-of-life cards.*

P.3 GEN DAQ optical cables - Restriction of Hazardous Substances Directive (RoHS) status

Optical cable	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-KAB277-xx	Fiber cable standard MM LC-SCRJ	2006		Yes	Yes
1-KAB278-xx	Fiber cable heavy duty MM LC-SCRJ	2006		Yes	Yes
1-KAB279-xx	Fiber cable heavy duty MM SCRJ-SCRJ	2006		Yes	Yes
1-KAB280-xx	Fiber cable standard MM LC-LC	2006		Yes	Yes
1-KAB281-xx	Fiber cable standard MM LC-LC	2006		Yes	Yes
1-KAB288-xx	Fiber cable standard SM LC-LC	2006		Yes	Yes
1-KAB289-xx	Fiber cable heavy duty SM LC-LC	2006		Yes	Yes

Note *“xx”: Different cable lengths are available when “xx” is used in part number.*

P.4 GEN DAQ probes - Restriction of Hazardous Substances Directive (RoHS) status

Probe	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-G025	Passive, DIFF matched probe, 200:1, 20 MHz, 100-140 pF, 3 m	2010		Yes	Unknown
1-G026-2	Passive, DIFF matched probe, 10:1, 200 MHZ, 105-140 pF, 3 m	2010		Yes	Unknown
1-G027-2	Passive, SE probe 10:1, 50 MHz, 100-140 pF, 3 m	2010		Yes	Unknown
1-G057	Passive, SE isolated probe, 100:1 , 50 MHz, 30-70 pF, 1.2 m	2010		Yes	Unknown
1-G901	Passive, SE probe 10:1, 200 MHz, 7-75 pF, 1.2 m	2010		Yes	Unknown
1-G902	Passive, SE probe 10:1, 200 MHz, 7-75 pF, 3 m	2010		Yes	Unknown
1-G903	Passive, SE isolated probe, 100:1, 400 MHz, 7-45 pF, 1.2 m	2010		Yes	Unknown
1-G904	Passive, SE isolated probe, 100:1, 300 MHz, 10-50 pF, 2 m	2010		Yes	Unknown
1-G906	Passive, SE isolated probe, 1000:1, 100 MHz, 10-50 pF, 3 m	2010		Yes	Unknown
1-G907	Passive, DIFF matched isolated probe, 10:1, 100 MHz, 35-70 pF, 3 m	2010		Yes	Unknown
1-G909	Active, DIFF isolated probe, 20:1 & 200:1, 25 Mhz, 1 m	2010		Yes	Unknown
1-G910	G901/G902 probe tip adapters	2010		Yes	Unknown
1-G911	G901/G902 probe accessoires	2010		Yes	Unknown
1-G915	Passive, DIFF matched isolated probe, 10:1, 200 MHz, 9 MΩ	2010		Yes	Unknown

P.5 GEN DAQ current clamps - Restriction of Hazardous Substances Directive (RoHS) status

Current clamp	Description	Introduction year	End-of-life year	RoHS 1 (2002/95/EC)	RoHS 2 (2011/65/EU)
1-G912	AC/DC current clamp i30s	2010		Yes	Unknown
1-G913	AC current clamp SR661	2010		Yes	Unknown
1-G914	AC current clamp M1V20-2	2010		Yes	Unknown

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