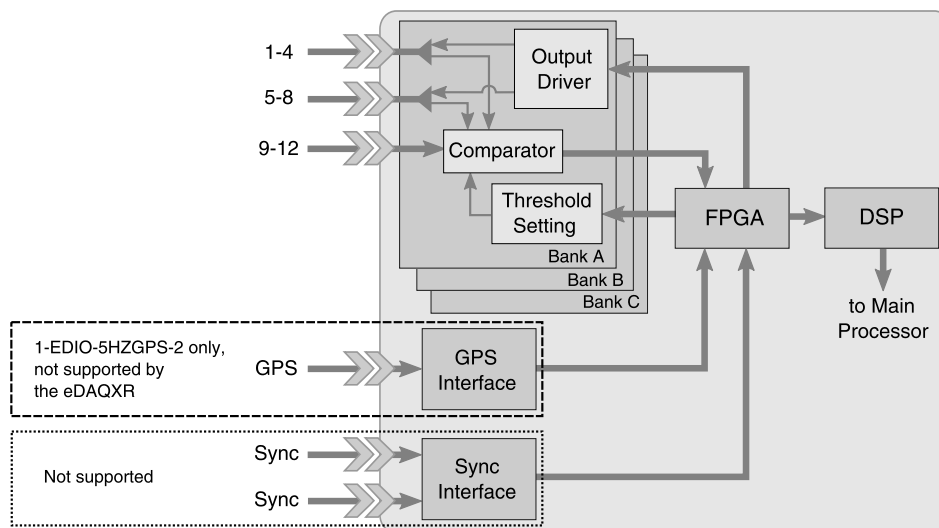# SOMAT XR

EDIO

eDAQ Digital Input/Output Layer

Special Features

– 24 digital inputs/outputs, 12 wide-range inputs, 18 configurable pulse counters and up to two independent vehicle bus module interfaces
– Optional GPS communications port designed to work with SoMat GPS devices
– Use of the GPS connector on the 1-EDIO-5HZGPS-2 is not compatible with the eDAQXR CPU, which has its own GPS connector

Block diagram

NOTE
A double-arrowhead symbol in the diagram represents male and female connectors only, not power polarity or input/output direction.

Detailed Description

The EDIO Digital Input/Output Layer is an extremely versatile layer that supports digital input/output (I/O), pulse counter, vehicle bus and optional GPS channels. The EDIO layer offers 24 channels that can be used as digital inputs and outputs, 12 channels dedicated to wide-range inputs and 18 integrated configurable pulse counters. One layer can also support up to two independent vehicle bus modules (VBM).

The digital I/O channels are grouped into three functionally identical banks (A, B and C). Each bank contains three Somat M8 female bulkhead connectors of four digital I/O channels (i.e., bits). The eight channels on connectors |1-4| and |5-8| are individually configurable to be either inputs or outputs. The four channels on connector |9-12| are dedicated wide-range input channels. Each connector also provides two pulse counter channels for a total of six pulse counter channels per bank. When configured for VBM use, the first two connectors (|1-4| and |5-8|) on bank A become dedicated VBM interfaces.

The pulse counters support pulse time period, pulse on time period, pulse rate counting and quadrature decoder. The pulse rate and quadrature decoder functions count range spans four billion counts for signals of frequencies up to 1 MHz. Pulse width period and pulse on period functions use a 5 MHz (200 nanosecond resolution) clock. The EDIO layer measures frequency inputs as low as 0.001176 Hz.

Use of the GPS connector on the 1-EDIO-5HZGPS-2 is not compatible with the eDAQXR CPU. The GPS features of this EDIO layer are superseded by the GPS port on the eDAQXR CPU.

Ordering Options

Order No.	Description
1-EDIO-B-2	EDIO digital input / output layer – Base Layer, Inputs: (24) digital I/O, (12) wide range (+/- 45V) digital inputs, (18) pulse counters. Includes: (9) 1-SAC-TRAN-MP-2-2 cables.
1-EDIO-5HZGPS-2	eDAQ Digital Input/Output Layer - 5 Hz GPS Installed Option: GPS Communications Port Includes: (9) 1-SAC-TRAN-MP-2-2 Transducer Cables and (1) 1-EGPS-5HZ-2 GPS Receiver

Cables and Accessories (Order Separately)

Order No.	Description	Order No.	Description
1-HDW-0034-00-2	M8 Hex Nut Wrench	1-SAC-EXT-MF-2-2	Extension Cable - Male/Female Connectors - 2 Meters Length
1-SAC-TRAN-MP-2-2	Transducer Cable - Male/Pigtail - 2 Meters Length	1-SAC-EXT-MF-5-2	Extension Cable - Male/Female Connectors - 5 Meters Length
1-SAC-TRAN-MP-10-2	Transducer Cable - Male/Pigtail - 10 Meters Length	1-SAC-EXT-MF-10-2	Extension Cable - Male/Female Connectors - 10 Meters Length
1-EPCM-2	Pulse Conditioning Module Requires: (1) Extension Cable (not included, 1-SAC-EXT-MF-X-2)	1-SAC-EXT-MF-15-2	Extension Cable - Male/Female Connectors - 15 Meters Length
1-EVBM-CAN-2	Vehicle Bus Module - CAN Requires: (1) Extension Cable (not included, 1-SAC-EXT-MF-X-2)	1- EGPS-5HZ-2	GPS receiver, updates at 5Hz

Specifications

Parameter	Unit	Value
Dimensions: width x length x height	cm	23.4 x 25.0 x 3.3
Weight	kg	2.0
Temperature range	°C [°F]	-20 ... +65 [-4 ... +149]
Relative humidity range, non-condensing	%	0 ... 90
Power consumption, no load [1]	W	2.44
Digital Inputs		
Steady-state input voltage (V_{in}) limits	-	-
minimum (channels 1-8)	V	-0.2
minimum (channels 9-12)	V	-45
maximum (channels 1-8 and 9-12)	V	+45
Transient input voltage (V_{in}) limits	-	-
minimum (channels 1-8)	V	-0.3
minimum (channels 9-12)	V	-100
maximum (channels 1-8 and 9-12)	V	+100
Input current	-	-
$V_{in} < 5.5$ V (channels 1-8)	µA	110
$V_{in} < 5.5$ V (channels 9-12)	µA	10
$V_{in} \geq 5.5$ V (channels 1-8)	mA	$(V_{in}-5.5)/10+0.110$
$V_{in} \geq 5.5$ V (channels 9-12)	mA	$(V_{in}-5.5)/10+0.010$
Threshold voltage	-	-
upper threshold ($V_{th,upper}$) range (channels 1-8)	V	0.8 ... 4.8
upper threshold ($V_{th,upper}$) range (channels 9-12)	V	0.001 ... 4.8
lower threshold ($V_{th,lower}$) (channels 1-12)	V	$V_{th,upper}-1$
accuracy (channels 1-12)	V	±0.02
Hysteresis voltage	V	1
Pulse Counters		
Pulse rate mode	-	-
maximum input frequency	MHz	1
maximum counts per sample period	counts	$2^{32} = 4.295E^{+09}$ (Bi-direction counting, $2^{32}/2$)
Quadrature decoder mode	-	-
maximum input frequency	MHz	1
Pulse time period mode	-	-
resolution	nanoseconds	200
accuracy	%	±0.01
minimum input frequency	Hz	0.0012
Pulse on period mode	-	-
resolution	nanoseconds	200
accuracy	%	±0.01
minimum input frequency	Hz	0.0012
Digital Outputs		

Parameter	Unit	Value
Logic 0 provided current to ground (at 100 mA)	-	-
maximum	V	1.1
typical	V	0.9
Maximum allowable output current sink (single output) [2]	mA	400
Logic 1 output voltage (V_{out}) (with no pull-up)	V	5
Maximum allowable pull-up voltage (channels 1-8)	V	45
Output power [3]	-	-
5-V output	A	1
12-V output	A	1
voltage tolerance	%	±10

[1] Power consumption measurements include the efficiency of the power supply.

[2] For multiple outputs, see Allowable Output Sink Current plot below.

[3] On MSDIO.02 (or earlier) board models, the 12 volt option worked correctly only if the input power to the eDAQ was about 14 to 15 volts (or more); otherwise, the DIO output would be something less than 12 volts.

Standards

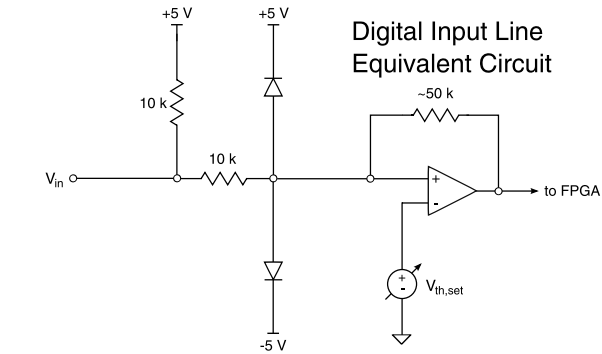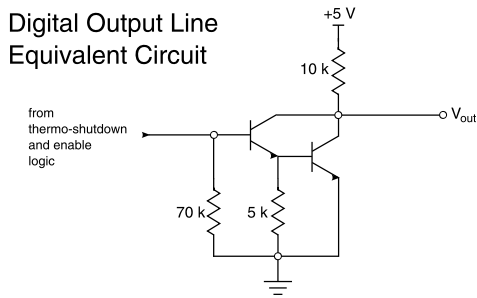| Category	Standard	Description
Shock	MIL-STD-810F	Method 516.5, Section 2.2.2 Functional Shock - ground vehicle
Vibration	MIL-STD-202G	Method 204D, Test condition C (10 *g* swept sine tested from 5 Hz to 2000 Hz)
EMC requirements	EN 61326-1:2006	Before July 2018, CE conformity test per EN 61326-1:2006
-	EN 61326-1:2012	After June 2018, CE conformity test per EN 61326-1:2012

Allowable Output Sink Current

The graph shows the allowable collector current at 50 °C depending on the number of simultaneous outputs. The data applies to the eight output channels on one DIO bank.
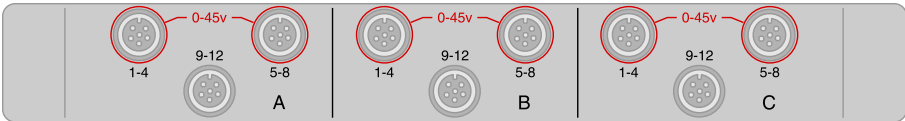
Digital Circuits

The digital input circuitry sets the threshold voltages and determines the input as a logic 1 or 0. The input equivalent circuit is the same for all input channels.

The output circuitry is applicable to the first two connectors (channels 1-8). Note that since the outputs share common I/O lines with the digital inputs, the lines are not allowed a DC voltage level lower than -0.3 volts.

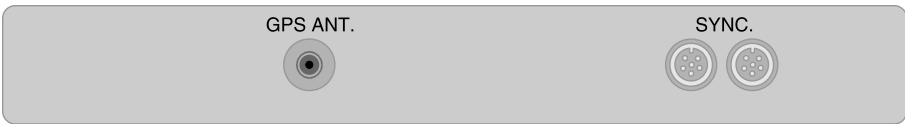Digital Output Line
Equivalent Circuit

Connectors

This diagram shows the M8 connectors on an EDIO layer. The following table lists the pin assignments for the SAC-TRAN-MP cable when used for DIO inputs (i.e., |1-4|, |5-8| or |9-12|). The I/O pin depends on the bank connector (i.e., |1-4|, |5-8| or |9-12|).

Connector	Pin	Function	Wire color	Quad encoder use
	1	I/O 4, 8 or 12	Brown	Encoder 2, output B
	2	I/O 3, 7 or 11	White	Encoder 2, output A
	3	GND/Shield	Bare wire	Return
	4	I/O 1, 5 or 9	Black	Encoder 1, output A
	5	Power	Red	Power
	6	I/O 2, 6 or 10	Green	Encoder 1, output B

This diagram shows the optional GPS antenna and Sync connectors on the 1-EDIO-5HZGPS-2 EDIO layer. The Sync ports are not supported.

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